12-Bit, 1 GSPS JESD204B, Dual Analog-to-Digital Converter

Data Sheet

AD9234

FEATURES

JESD204B (Subclass 1) coded serial digital outputs
1.5 W total power per channel at 1 GSPS (default settings)
SFDR = 79 dBFS at 340 MHz
SNR = 63.4 dBFS at 340 MHz (A_{IN} = −1.0 dBFS)
ENOB = 10.4 bits at 10 MHz
DNL = ±0.16 LSB
INL = ±0.35 LSB
Noise density = −151 dBFS/Hz at 1 GSPS
1.25 V, 2.5 V, and 3.3 V dc supply operation
No missing codes
Internal ADC voltage reference
Flexible termination impedance
400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
2 GHz usable analog input full power bandwidth
95 dB channel isolation/crosstalk
Amplitude detect bits for efficient AGC implementation
Differential clock input
Optional decimate-by-2 DDC per channel
Differential clock input
Integer clock divide by 1, 2, 4, or 8
Flexible JESD204B lane configurations
Small signal dither

APPLICATIONS

Communications
Diversity multiband, multimode digital receivers
3G/4G, TD-SCDMA, W-CDMA, GSM, LTE
Point-to-point radio systems
Digital predistortion observation path
General-purpose software radios
Ultrawideband satellite receiver
Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
Digital oscilloscopes
High speed data acquisition systems
DOCSIS 3.0 CMTS upstream receive paths
HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

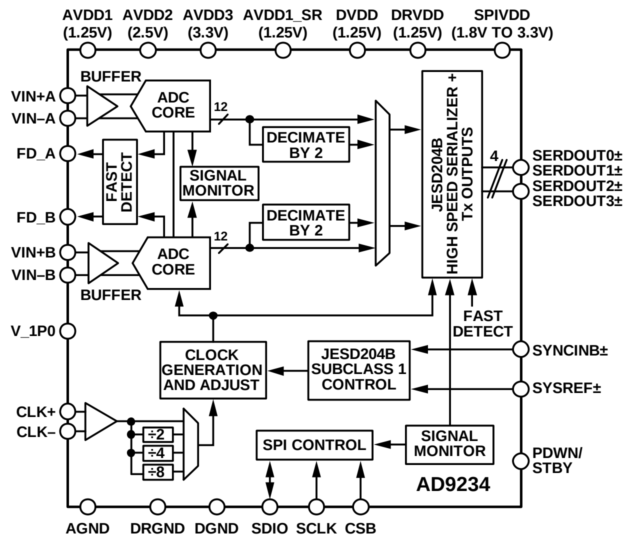

Figure 1.

PRODUCT HIGHLIGHTS

1. Low power consumption analog core, 12-bit, 1.0 GSPS dual analog-to-digital converter (ADC) with 1.5 W per channel.
2. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
3. Buffered inputs with programmable input termination eases filter design and implementation.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 9 mm × 9 mm 64-lead LFCSP.
7. Pin compatible with the AD9680 14-bit, 1 GSPS dual ADC.

Rev. 0

Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

8/14—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9234 is a dual, 12-bit, 1 GSPS ADC. The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed for sampling wide bandwidth analog signals. The AD9234 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth buffered inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. Each ADC data output is internally connected to an optional decimate-by-2 block.

The AD9234 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9234 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the acceptable lane rate of the receiving logic device and the sampling rate of the ADC. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9234 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable 3-wire SPI.

The AD9234 is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1000 MSPS), 1.34 V p-p full-scale differential input, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	12			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.22	0	+0.20	% FSR
Offset Matching	Full		0	+0.19	% FSR
Gain Error	Full		0		% FSR
Gain Matching	Full		1	+4.8	% FSR
Differential Nonlinearity (DNL)	Full	−0.3	±0.16	+0.3	LSB
Integral Nonlinearity (INL)	Full	−1.2	±35	+1.4	LSB
TEMPERATURE DRIFT					
Offset Error	25°C		±6		ppm/°C
Gain Error	25°C		±36		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Voltage	Full		1.0		V
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		1.02		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range	Full		1.34		V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05		V
Differential Input Capacitance[1]	25°C		1.5		pF
Analog Input Full Power Bandwidth	25°C		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	V
I_{AVDD1}	Full		675	740	mA
I_{AVDD2}	Full		525	590	mA
I_{AVDD3}	Full		75	91	mA
I_{AVDD1_SR}	Full		16	18	mA
I_{DVDD}[2]	Full		230	236	mA
I_{DRVDD}[1]	Full		205	225	mA
I_{SPIVDD}	Full		5	6	mA
POWER CONSUMPTION					
Total Power Dissipation (Including Output Drivers)[2]	Full		3.0	3.3	W
Power-Down Dissipation	Full		750		mW
Standby[3]	Full		1.25		W

[1] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[2] Default mode. No DDCs used. L = 4, M = 2, F = 1.
[3] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1000 MSPS), 1.34 V p-p full-scale differential input, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		1.34		V p-p
NOISE DENSITY[2]	Full		−151		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 10 MHz	25°C		64.2		dBFS
f_{IN} = 170 MHz	Full	61.6	63.9		dBFS
f_{IN} = 340 MHz	25°C		63.4		dBFS
f_{IN} = 450 MHz	25°C		63.1		dBFS
f_{IN} = 737 MHz	25°C		61.6		dBFS
f_{IN} = 985 MHz	25°C		60.7		dBFS
f_{IN} = 1410 MHz	25°C		58.8		dBFS
SNR AND DISTORTION RATIO (SINAD)[3]					
f_{IN} = 10 MHz	25°C		64.1		dBFS
f_{IN} = 170 MHz	Full	61.2	63.8		dBFS
f_{IN} = 340 MHz	25°C		63.3		dBFS
f_{IN} = 450 MHz	25°C		63.0		dBFS
f_{IN} = 737 MHz	25°C		61.5		dBFS
f_{IN} = 985 MHz	25°C		60.6		dBFS
f_{IN} = 1410 MHz	25°C		58.7		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C		10.4		Bits
f_{IN} = 170 MHz	Full	9.9	10.3		Bits
f_{IN} = 340 MHz	25°C		10.2		Bits
f_{IN} = 450 MHz	25°C		10.2		Bits
f_{IN} = 737 MHz	25°C		9.9		Bits
f_{IN} = 985 MHz	25°C		9.8		Bits
f_{IN} = 1410 MHz	25°C		9.5		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]					
f_{IN} = 10 MHz	25°C		89		dBFS
f_{IN} = 170 MHz	Full	70	80		dBFS
f_{IN} = 340 MHz	25°C		79		dBFS
f_{IN} = 450 MHz	25°C		80		dBFS
f_{IN} = 737 MHz	25°C		81		dBFS
f_{IN} = 985 MHz	25°C		79		dBFS
f_{IN} = 1410 MHz	25°C		78		dBFS
WORST HARMONIC, SECOND OR THIRD[3]					
f_{IN} = 10 MHz	25°C		−89		dBFS
f_{IN} = 170 MHz	Full		−80	−70	dBFS
f_{IN} = 340 MHz	25°C		−79		dBFS
f_{IN} = 450 MHz	25°C		−80		dBFS
f_{IN} = 737 MHz	25°C		−82		dBFS
f_{IN} = 985 MHz	25°C		−79		dBFS
f_{IN} = 1410 MHz	25°C		−78		dBFS

Parameter[1]	Temperature	Min	Typ	Max	Unit
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]					
f_{IN} = 10 MHz	25°C		−89		dBFS
f_{IN} = 170 MHz	Full		−85	−76	dBFS
f_{IN} = 340 MHz	25°C		−83		dBFS
f_{IN} = 450 MHz	25°C		−82		dBFS
f_{IN} = 737 MHz	25°C		−81		dBFS
f_{IN} = 985 MHz	25°C		−85		dBFS
f_{IN} = 1410 MHz	25°C		−80		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS					
f_{IN1} = 187 MHz, f_{IN2} = 190 MHz	25°C		−81		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−78		dBFS
CROSSTALK[4]	25°C		95		dB
FULL POWER BANDWIDTH[5]	25°C		2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 9 for recommended settings for the buffer current setting optimized for SFDR.
[4] Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[5] Measured with circuit shown in Figure 42.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1000 MSPS), 1.34 V p-p full-scale differential input, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 μA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 μA)	Full	0		0.5	V
SYNC INPUTS (SYNCINB+, SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{Dshort})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.34 V p-p full-scale differential input, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	GHz
Maximum Sample Rate[1]	Full	1000			MSPS
Minimum Sample Rate[2]	Full	300			MSPS
Clock Pulse Width High	Full	500			ps
Clock Pulse Width Low	Full	500			ps
OUTPUT PARAMETERS					
Unit Interval (UI)[3]	Full	80	100		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C	24	32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C	24	32		ps
PLL Lock Time	25°C		2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	10	12.5	Gbps
LATENCY[5]					
Pipeline Latency	Full		55		Clock cycles
Fast Detect Latency	Full			28	Clock cycles
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down	25°C			4	ms
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_j)	Full		55		fs rms
Out-of-Range Recovery Time	Full		1		Clock Cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 4. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 4, M = 2, F = 1.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 2				
t_{SU_SR}	Device clock to SYSREF+ setup time		117		ps
t_{H_SR}	Device clock to SYSREF+ hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

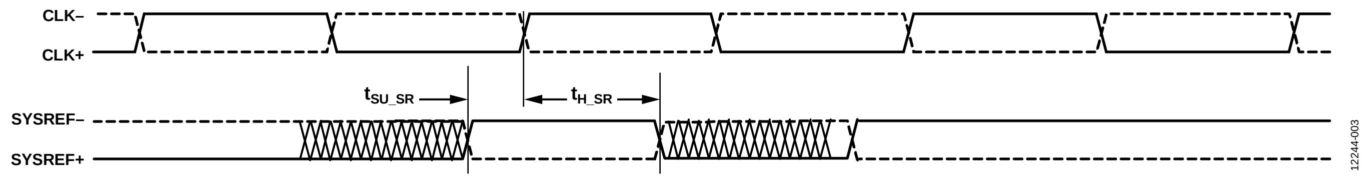


Figure 2. SYSREF± Setup and Hold Timing

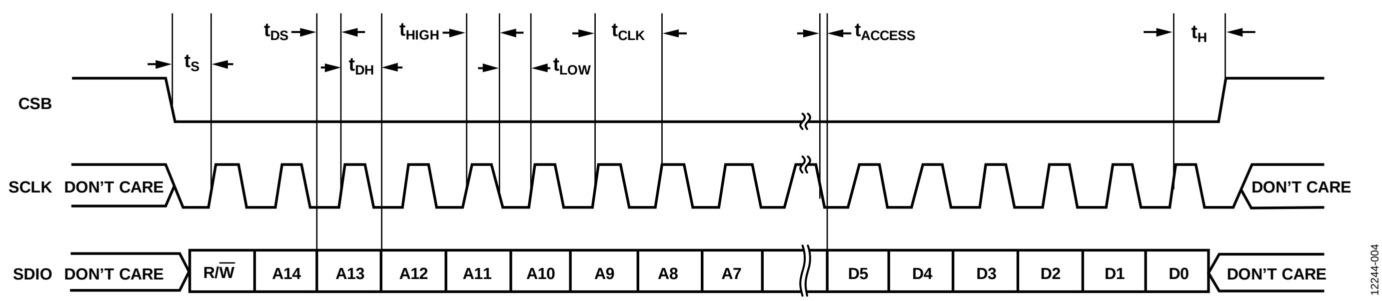


Figure 3. Serial Port Interface Timing Diagram

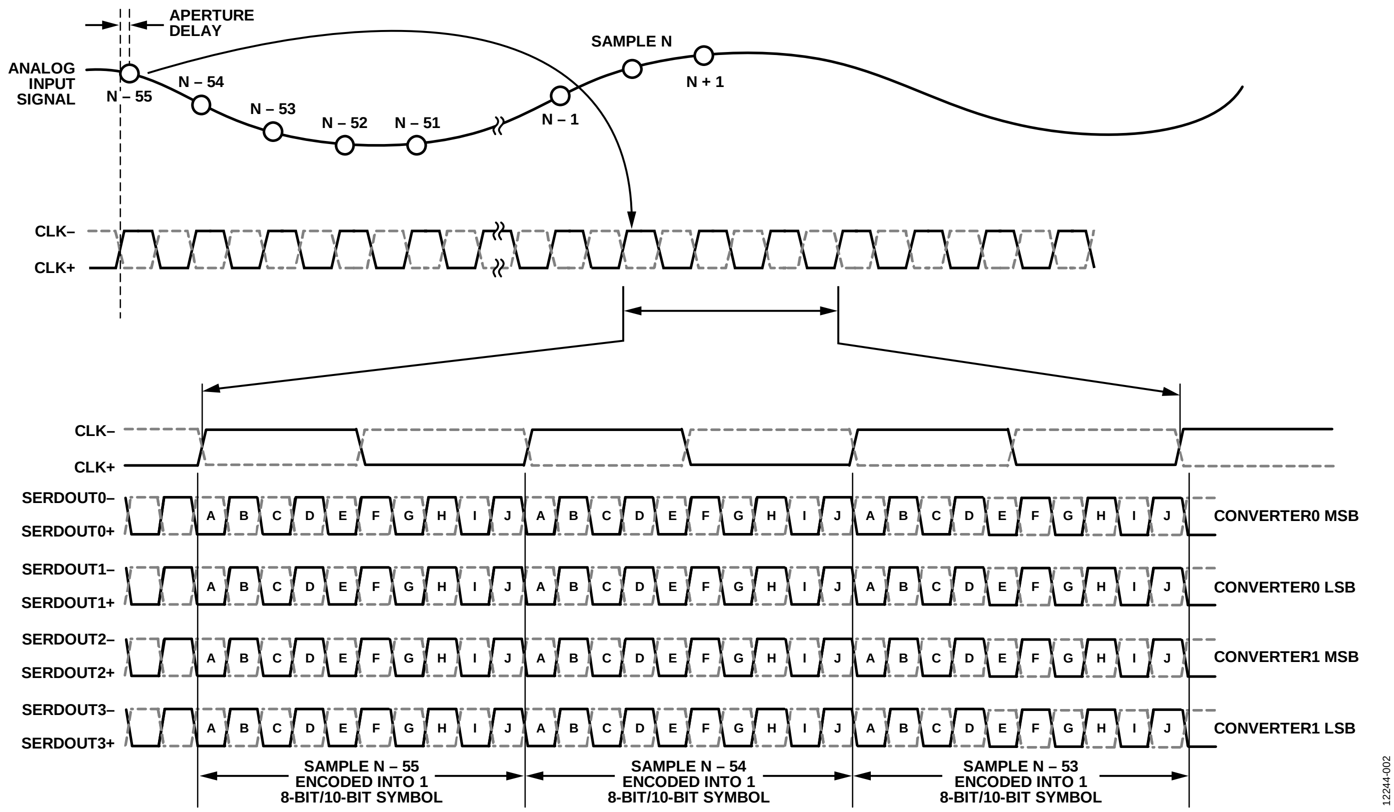


Figure 4. Data Output Timing (Full Bandwidth Mode; L = 4; M = 2; F = 1)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

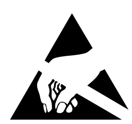
Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 7.

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1, 2]	6.3[1, 3]	4.7[1, 5]	1.2[1, 5]	°C/W
	1.0	15.6[1, 2]	5.9[1, 3]	N/A[4]		°C/W
	2.5	15.0[1, 2]	5.7[1, 3]	N/A[4]		°C/W
10-Layer PCB 81 Vias Under Exposed Pad	0.0	13.8	4.6	4.7	1.2	°C/W
	1.0	12.7	4.6	N/A[4]		°C/W
	2.5	12.0	4.6	N/A[4]		°C/W

1 Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
2 Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
3 Per JEDEC JESD51-8 (still air).
4 N/A = not applicable.
5 Per MIL-STD 883, Method 1012.1.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

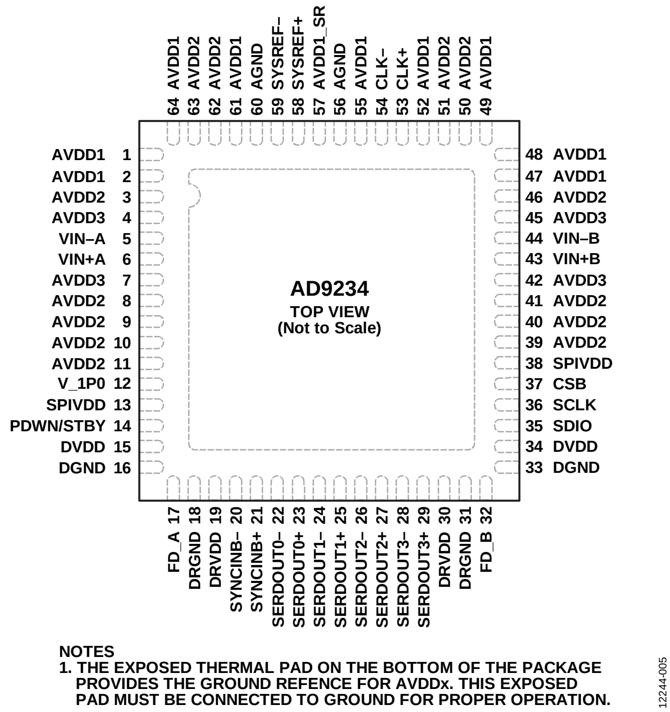


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation.
1, 2, 47, 48, 49, 52, 55, 61, 64	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63	AVDD2	Supply	Analog Power Supply (2.5 V Nominal).
4, 7, 42, 45	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 38	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.3 V).
15, 34	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 33	DGND	Ground	Ground Reference for DVDD.
18, 31	DRGND	Ground	Ground Reference for DRVDD.
19, 30	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
56, 60	AGND[1]	Ground	Ground Reference for SYSREF±.
57	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
43, 44	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
53, 54	CLK+, CLK−	Input	Clock Input True/Complement.
CMOS Outputs			
17, 32	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.

Pin No.	Mnemonic	Type	Description
Digital Inputs			
20, 21	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input Complement/True.
58, 59	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement.
Data Outputs			
22, 23	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
35	SDIO	Input/output	SPI Serial Data Input/Output.
36	SCLK	Input	SPI Serial Clock.
37	CSB	Input	SPI Chip Select (Active Low).

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, refer to the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.34 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted.

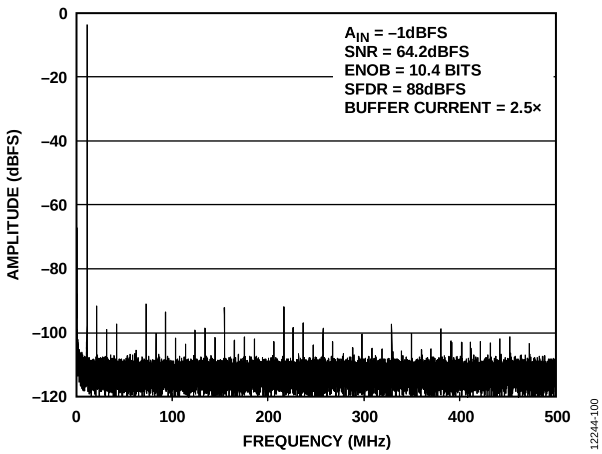


Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

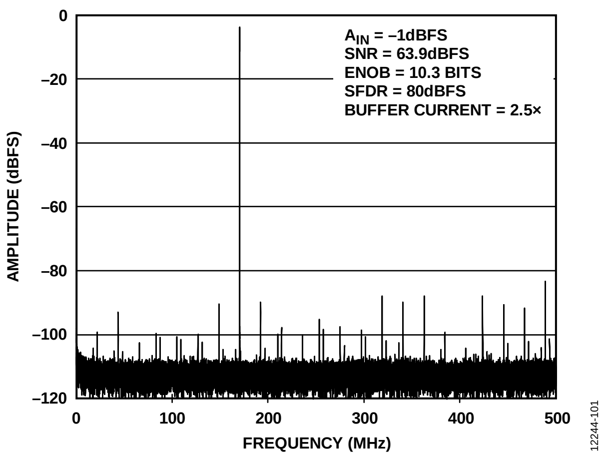


Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz

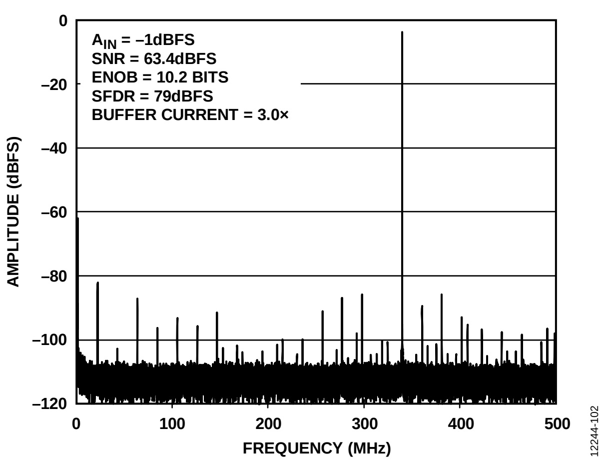


Figure 8. Single-Tone FFT with f_{IN} = 340.3 MHz

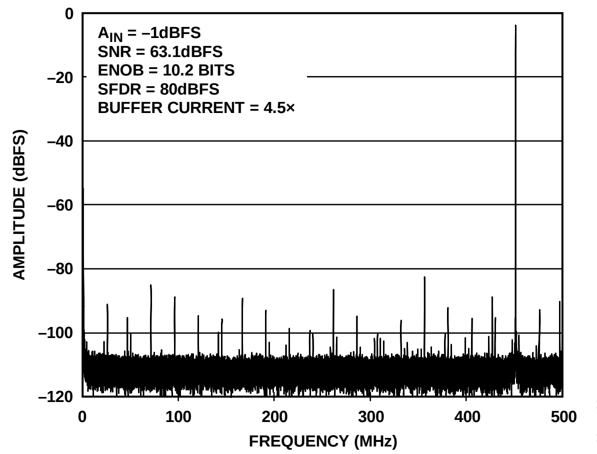


Figure 9. Single-Tone FFT with f_{IN} = 450.3 MHz

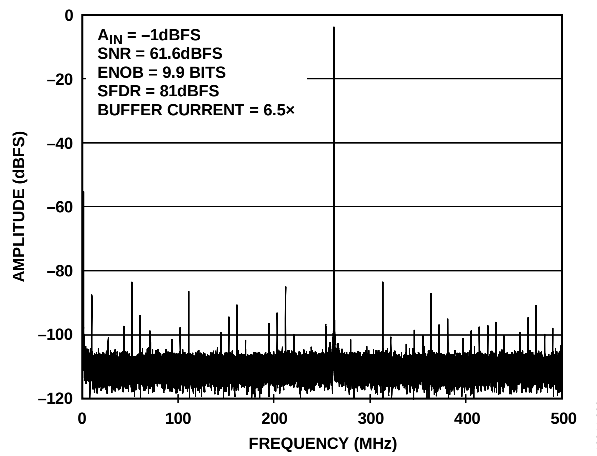


Figure 10. Single-Tone FFT with f_{IN} = 737.3 MHz

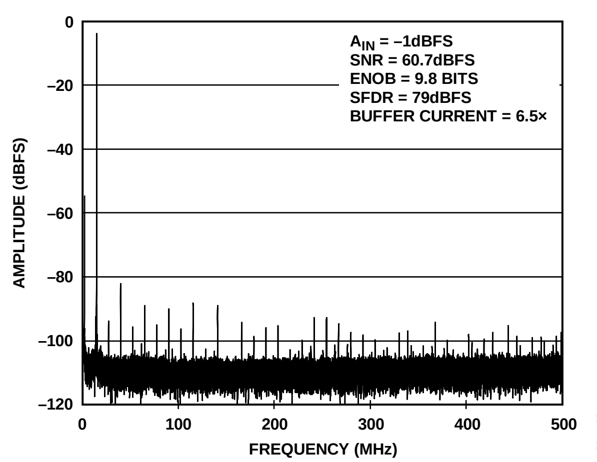


Figure 11. Single-Tone FFT with f_{IN} = 985.3 MHz

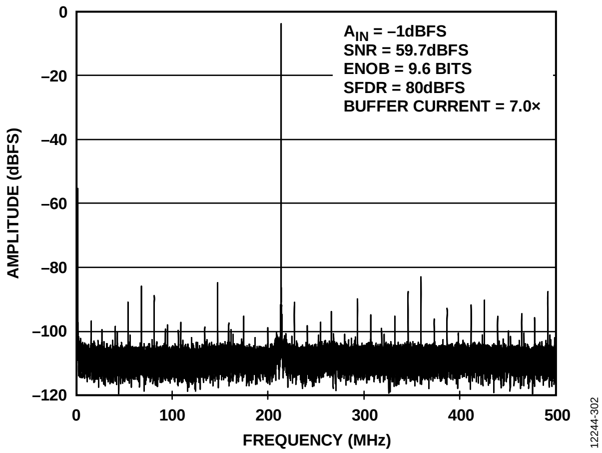


Figure 12. Single-Tone FFT with f_{IN} = 1213.3 MHz

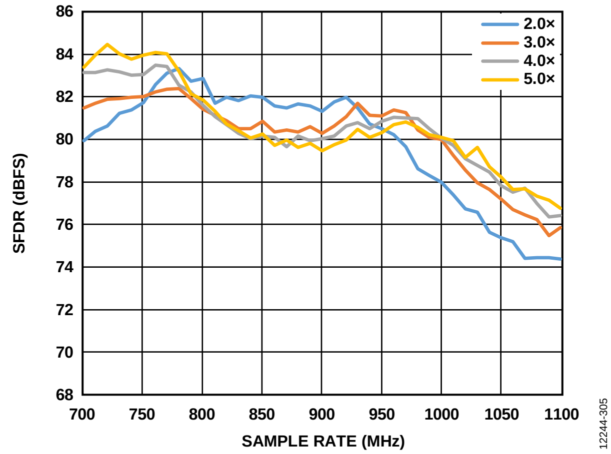


Figure 15. SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz, Buffer Current = 2.0×, 3.0×, 4.0×, and 5.0×

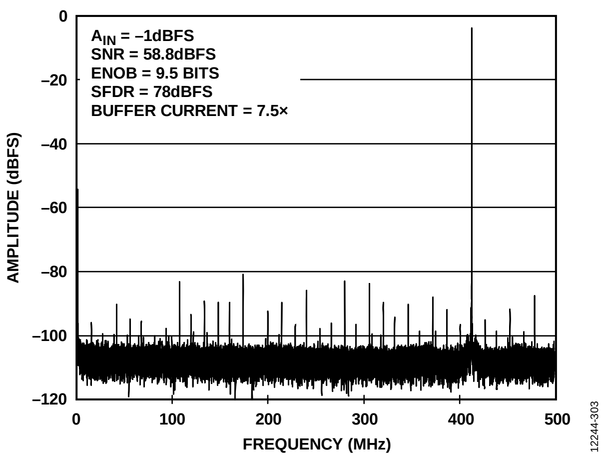


Figure 13. Single-Tone FFT with f_{IN} = 1413.3 MHz

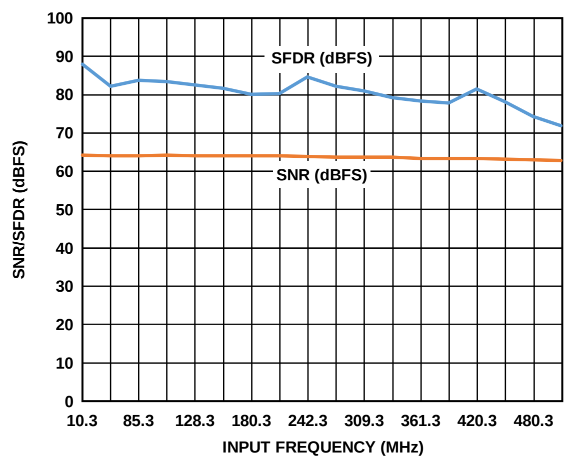


Figure 16. SNR/SFDR vs. Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Current = 3.5× (Uses Circuit Shown in Figure 41)

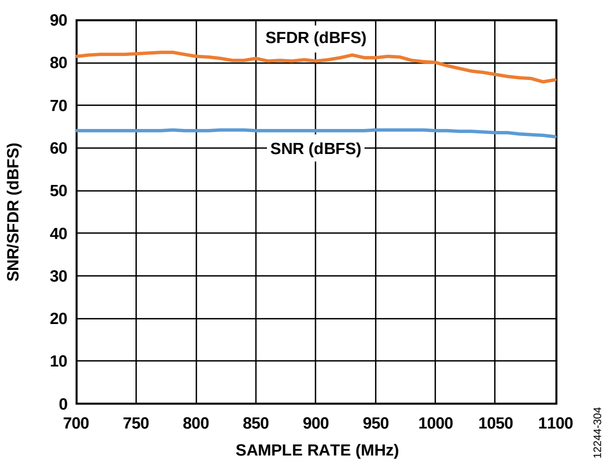


Figure 14. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz; Buffer Current = 3.0×

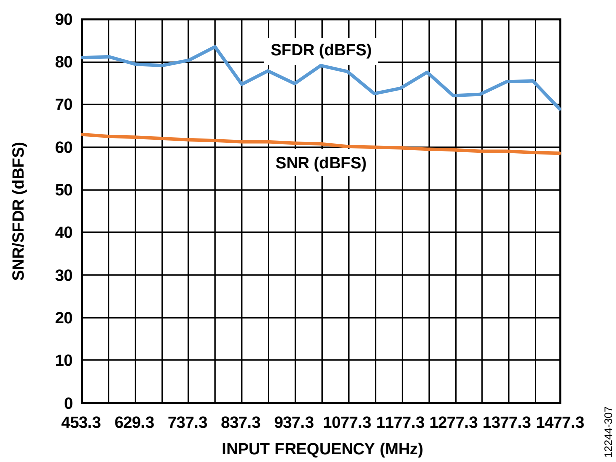


Figure 17. SNR/SFDR vs. Input Frequency (f_{IN}); 450 MHz < f_{IN} < 1500 MHz; Buffer Current = 7.5× (Uses Circuit Shown in Figure 42)

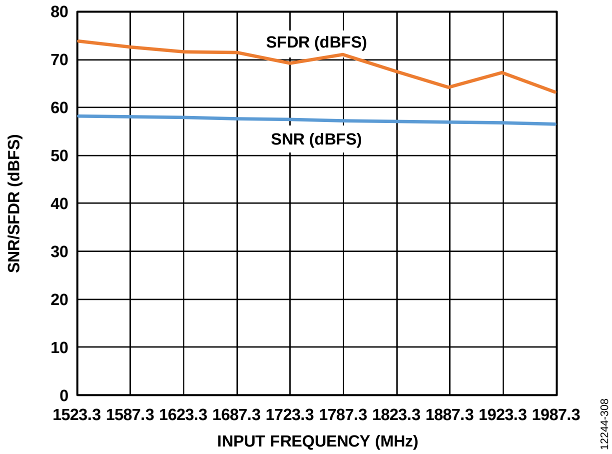


Figure 18. SNR/SFDR vs. Input Frequency (f_{IN}); 1500 MHz < f_{IN} < 2000 MHz ; Buffer Current = 8.5× (Uses Circuit Shown in Figure 42)

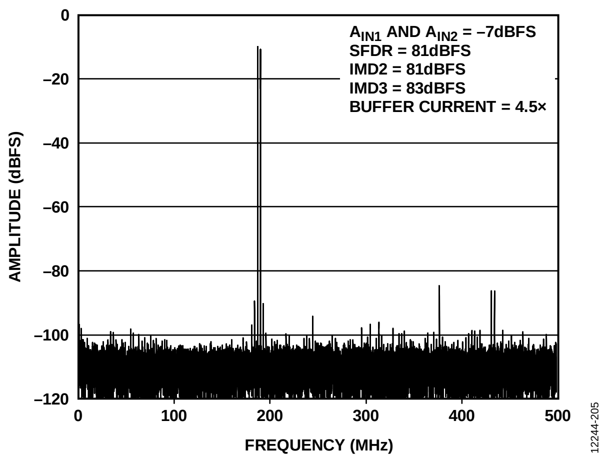


Figure 19. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

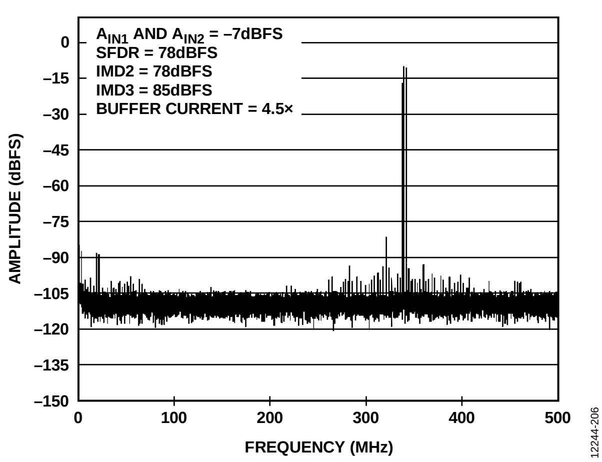


Figure 20. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

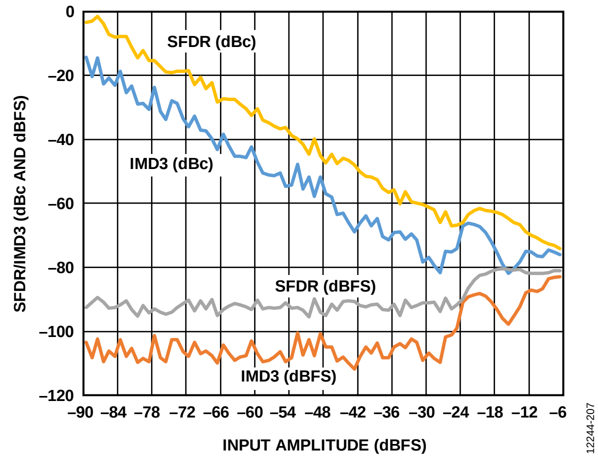


Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

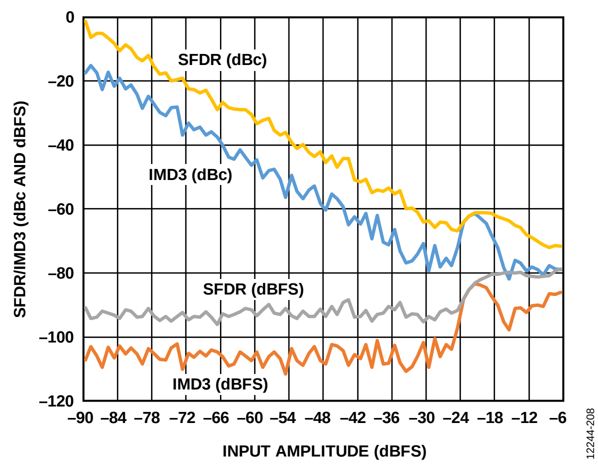


Figure 22. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

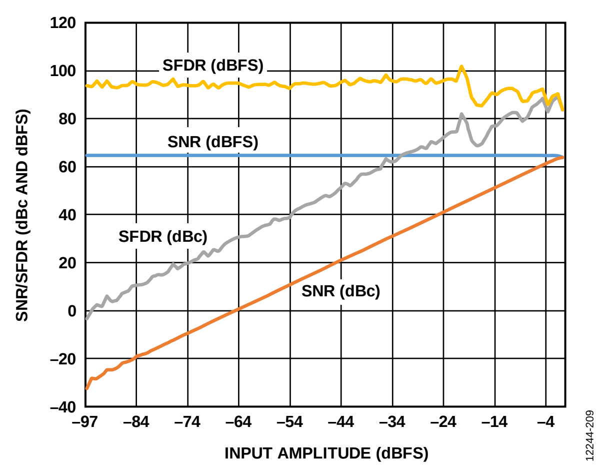


Figure 23. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz; Buffer Current = 2.0×

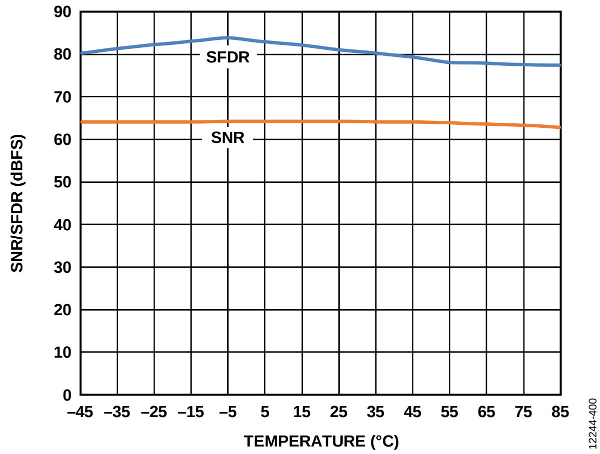


Figure 24. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

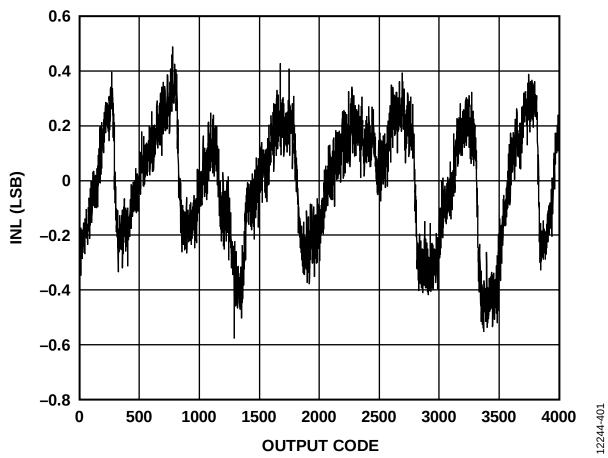


Figure 25. INL, f_{IN} = 10.3 MHz

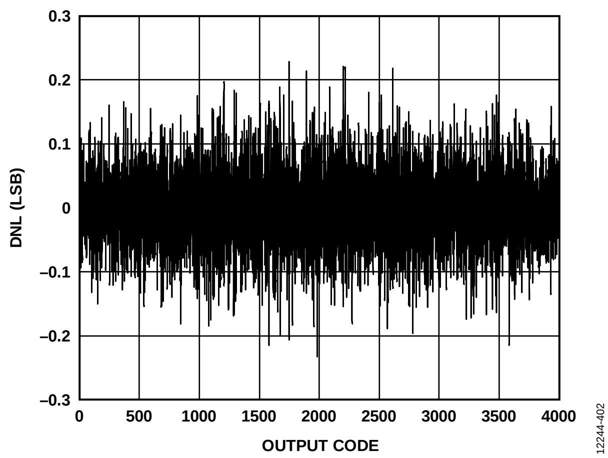


Figure 26. DNL, f_{IN} = 10 MHz

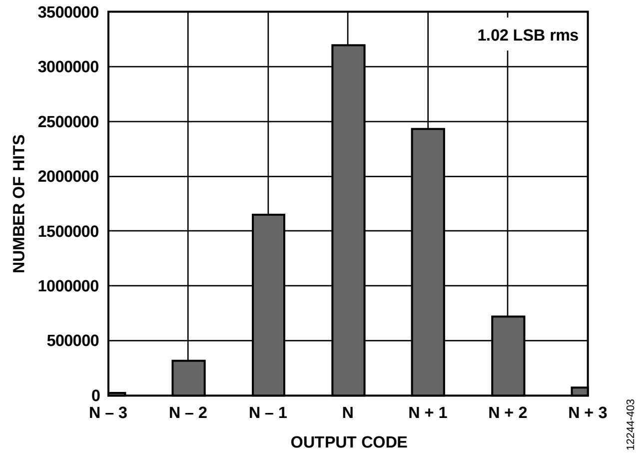


Figure 27. Input-Referred Noise Histogram

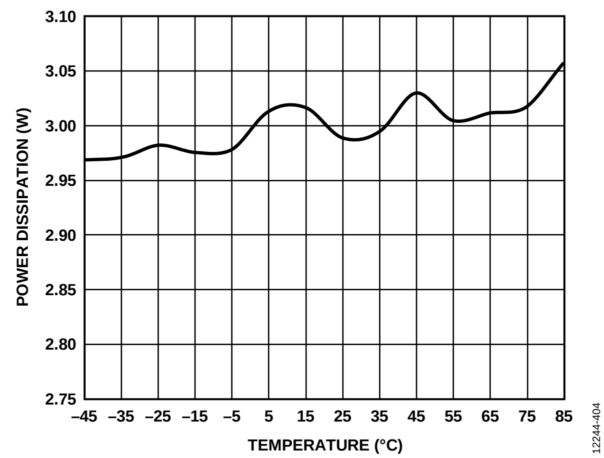


Figure 28. Power Dissipation vs. Temperature

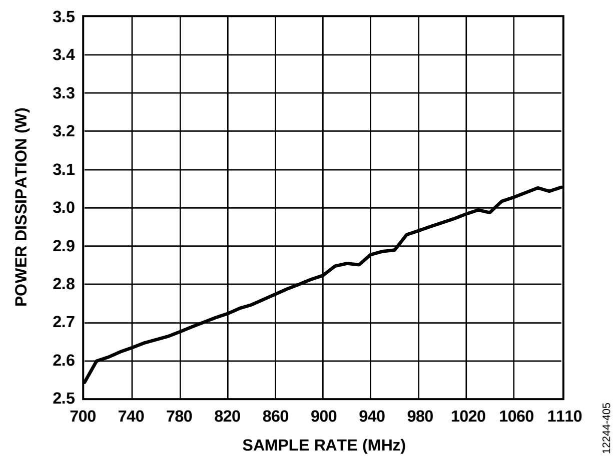


Figure 29. Power Dissipation vs. Sample Rate (f_S)

EQUIVALENT CIRCUITS

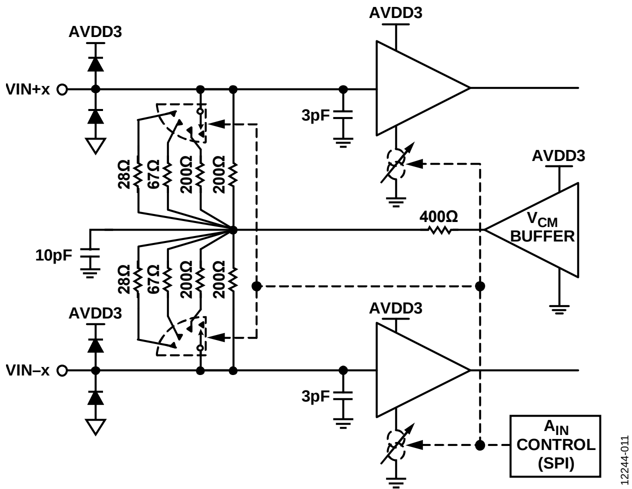


Figure 30. Analog Inputs

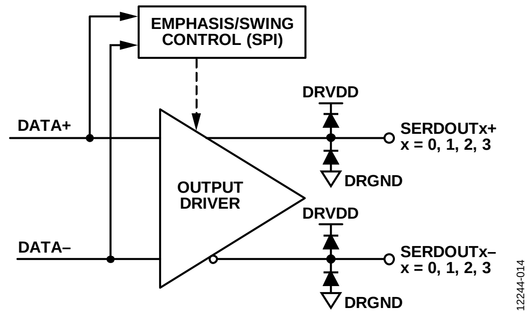


Figure 33. Digital Outputs

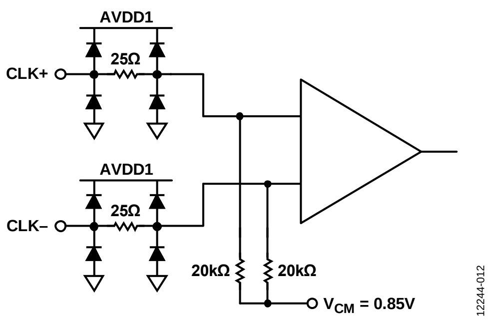


Figure 31. Clock Inputs

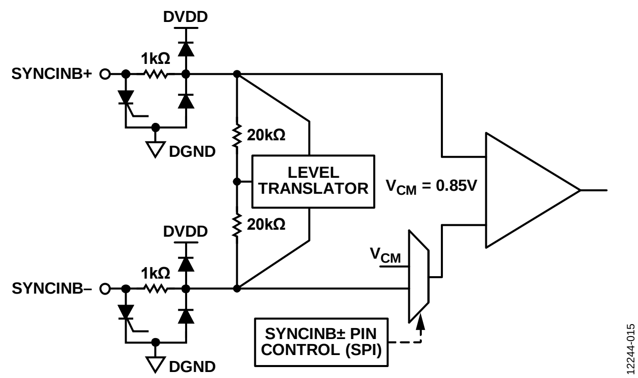


Figure 34. SYNCINB± Inputs

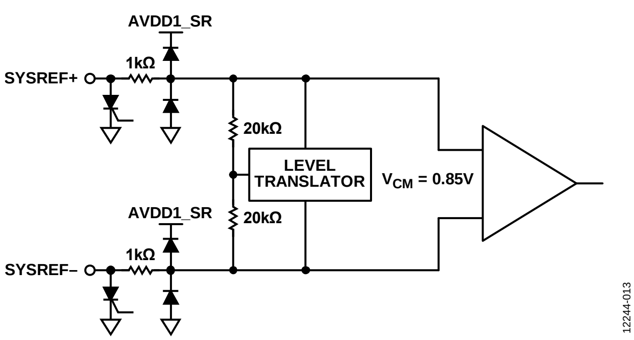


Figure 32. SYSREF± Inputs

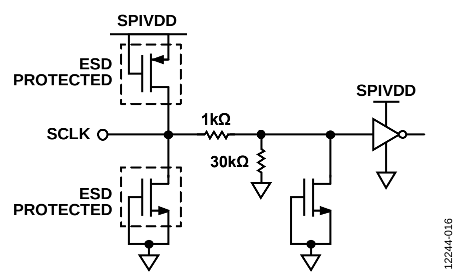


Figure 35. SCLK Input

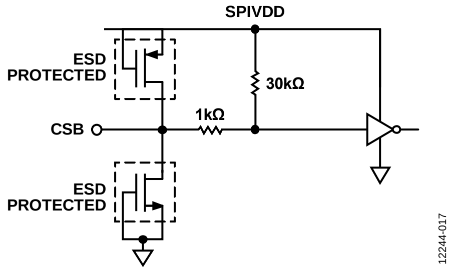


Figure 36. CSB Input

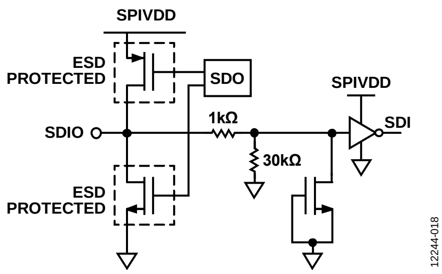


Figure 37. SDIO Input

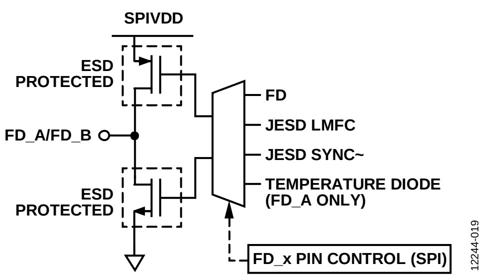


Figure 38. FD_A/FD_B Outputs

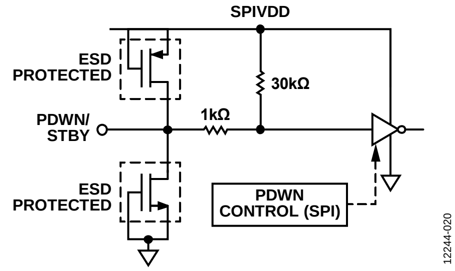


Figure 39. PDWN/STBY Input

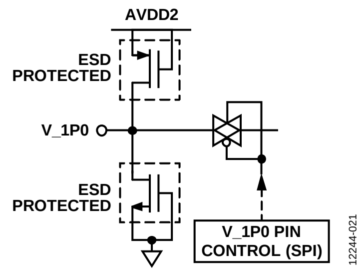


Figure 40. V_1P0 Input

THEORY OF OPERATION

The AD9234 has two analog input channels and four JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD9234 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD9234 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data rate can be configured in one-lane (L = 1), two-lane (L = 2), and four-lane (L = 4) configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

ADC ARCHITECTURE

The architecture of the AD9234 consists of an input buffered pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 30. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9234 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, refer to the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9234, the available span is 1.34 V p-p differential.

Differential Input Configurations

There are several ways to drive the AD9234, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 41 and Figure 42) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9234.

For low to midrange frequencies, a double balun or double transformer network (see Figure 41) is recommended for optimum performance of the AD9234. For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 42).

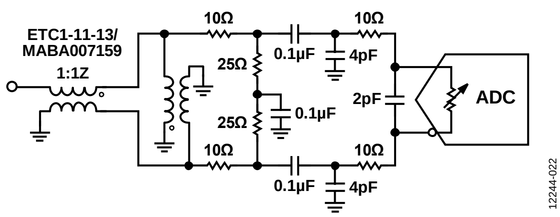


Figure 41. Differential Transformer-Coupled Configuration for First and Second Nyquist Frequencies

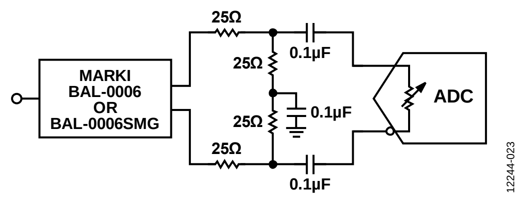


Figure 42. Differential Transformer-Coupled Configuration for Second and Third Nyquist Frequencies

Input Common Mode

The analog inputs of the AD9234 are internally biased to the common mode as shown in Figure 43. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V, ±100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD9234 offers flexible controls for the analog inputs, such as input termination and buffer current. All of the available controls are shown in Figure 43.

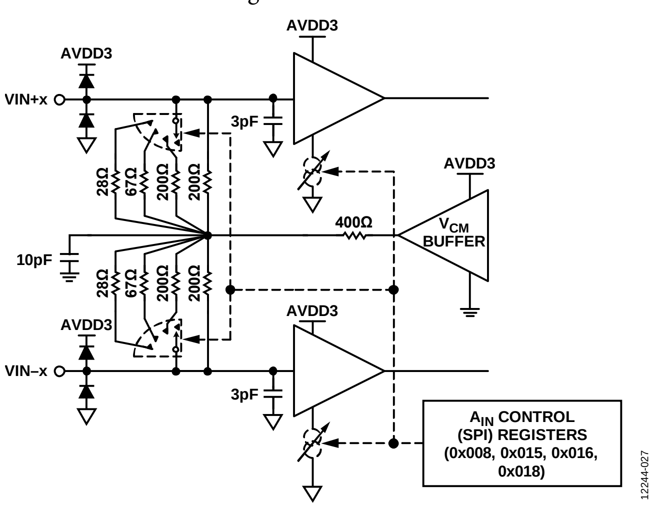


Figure 43. Analog Input Controls

Using Register 0x018, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 44. For a complete list of buffer current settings, see Table 17.

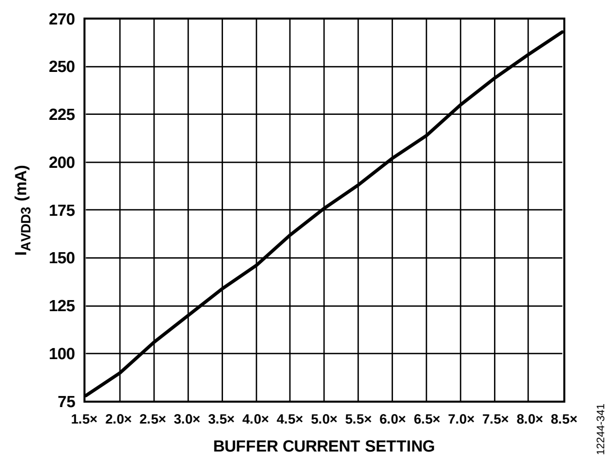


Figure 44. AVDD3 Power (I_{AVDD3}) vs. Buffer Current Setting

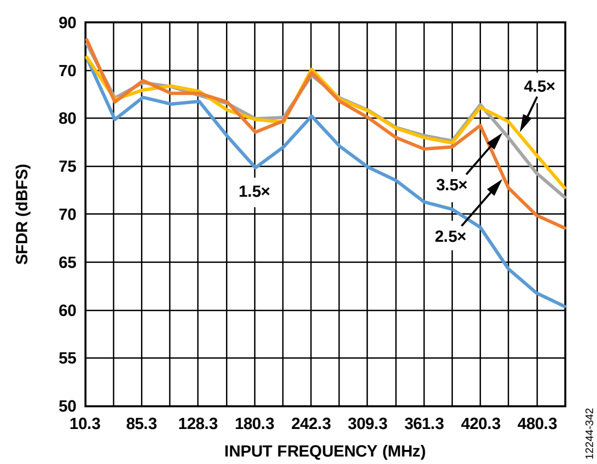


Figure 45. Buffer Current Sweeps, SFDR vs. Input Frequency (I_{BUFF}); f_{IN} < 500 MHz

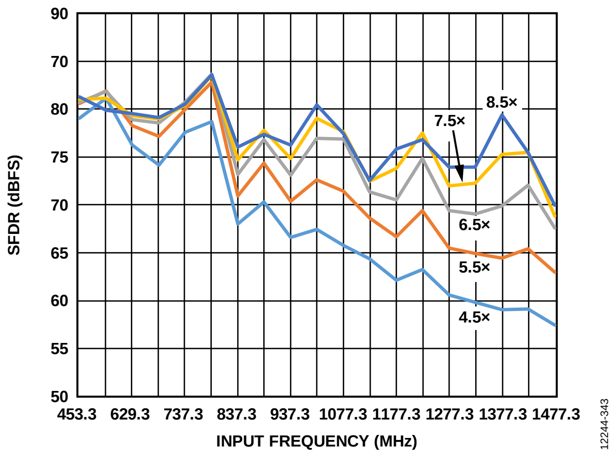


Figure 46. Buffer Current Sweeps, SFDR vs. Input Frequency (I_{BUFF}); 500 MHz < f_{IN} < 1500 MHz

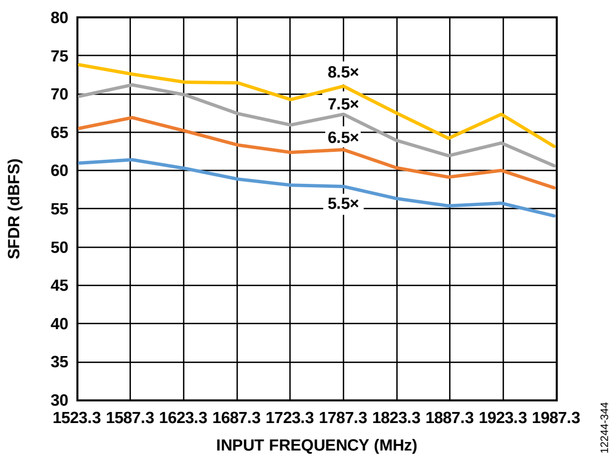


Figure 47. Buffer Current Sweeps, SFDR vs. Input Frequency (I_{BUFF}); 1500 MHz < f_{IN} < 2000 MHz

Figure 45, Figure 46, and Figure 47 show how the SFDR can be optimized using the buffer current setting in Register 0x018 for different Nyquist zones. At frequencies greater than 1 GHz, it is better to run the ADC at input amplitudes less than −1 dBFS (−3 dBFS, for example). This greatly improves the linearity of the converted signal without sacrificing SNR performance.

Table 9 shows the recommended buffer current and full-scale voltage settings for the different analog input frequency ranges.

Table 9. SFDR Optimization for Input Frequencies

Input Frequency	Input Buffer Current Control Setting, Register 0x018
<400 MHz	2.5× or 3.0×
400 MHz to 1 GHz	4.5× or 6.5×
>1 GHz	6.5× or higher

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9234 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9234. This internal 1.0 V reference is used to set the full-scale input range of the ADC. For more information on adjusting the input swing, see Table 17. Figure 48 shows the block diagram of the internal 1.0 V reference controls.

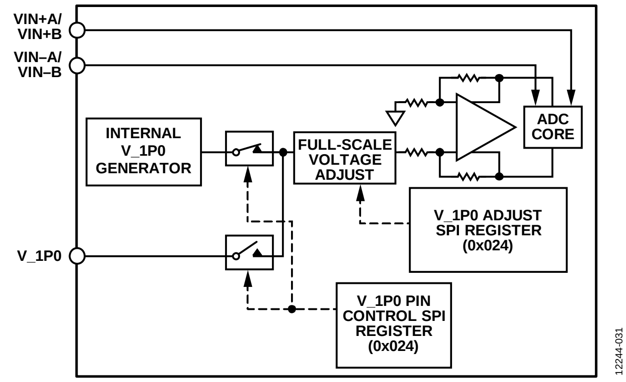


Figure 48. Internal Reference Configuration and Controls

The SPI Register 0x024 enables the user to either use this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9234, refer to the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 49 shows the typical drift characteristics of the internal 1.0 V reference.

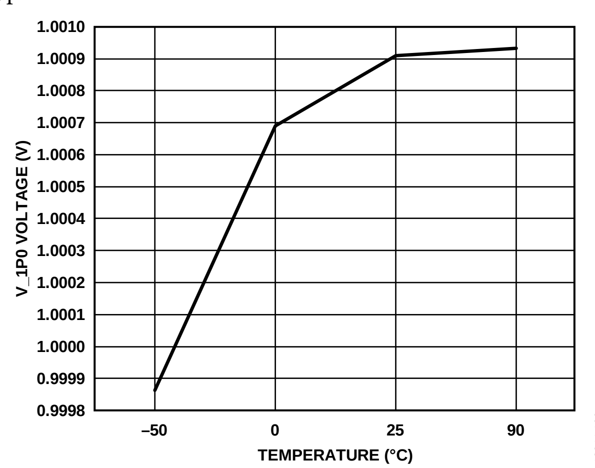


Figure 49. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 50 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD9234. The grayed out areas show unused blocks within the AD9234 while using the ADR130 to provide the external reference.

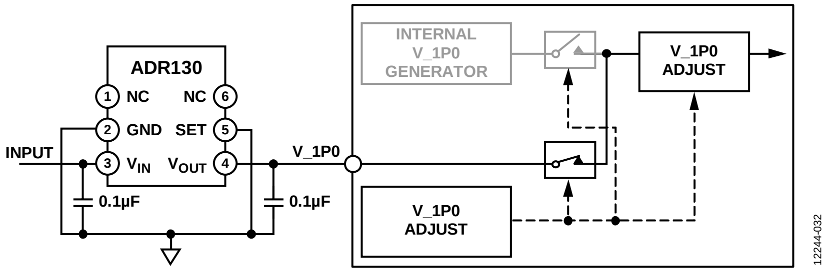


Figure 50. External Reference Using ADR130

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9234 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 51 shows a preferred method for clocking the AD9234. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

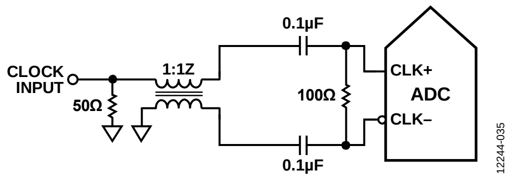


Figure 51. Transformer-Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 52 and Figure 53.

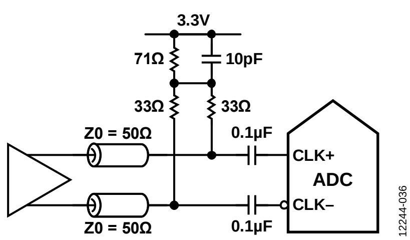


Figure 52. Differential CML Sample Clock

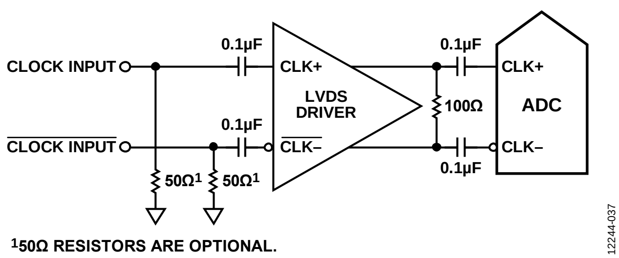


Figure 53. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the device. The AD9234 can be clocked at 2 GHz with the internal clock divider set to 2. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider

The AD9234 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, and 8. The divider ratios can be selected using Register 0x10B. This is shown in Figure 54.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, care must be taken to program the appropriate divider ratio into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

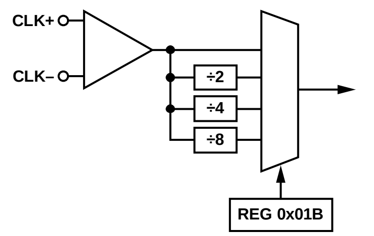


Figure 54. Clock Divider Circuit

The AD9234 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This feature is enabled by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. See the Multichip Synchronization section for more information

Input Clock Divider ½ Period Delay Adjust

The input clock divider inside the AD9234 provides phase delay in increments of ½ the input clock cycle. Register 0x10C can be programmed to enable this delay independently for each channel. Changing this register does not affect the stability of the JESD204B link.

Clock Fine Delay Adjust

The AD9234 sampling edge instant can be adjusted by writing to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the feature, and Register 0x118, Bits[7:0] set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in ~1.7 ps increments. The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x117 causes a datapath reset. However, the contents of Register 0x118 can be changed without affecting the stability of the JESD204B link.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20 \times \log 10\ (2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 55).

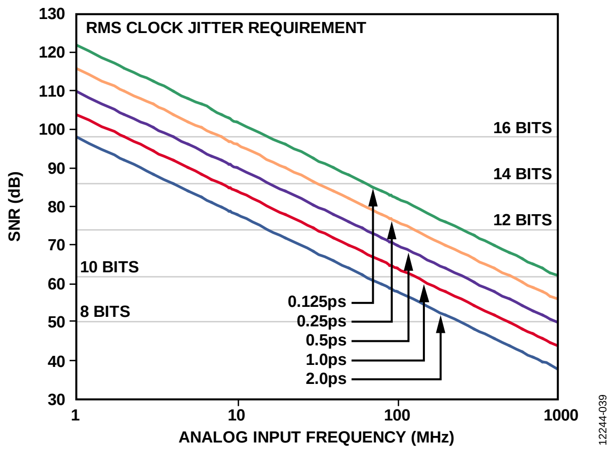


Figure 55. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9234. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

POWER-DOWN/STANDBY MODE

The AD9234 has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode. The default operation is the PDWN function. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not disrupted and transmits zeroes for all converter samples. This can be changed using Register 0x571, Bit 7 to select /K/ characters.

TEMPERATURE DIODE

The AD9234 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028, Bit 0 to enable or disable the diode. Register 0x028 is a local register. Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040[2:0]. See Table 17 for more information.

The voltage response of the temperature diode (SPIVDD = 1.8 V) is shown in Figure 56.

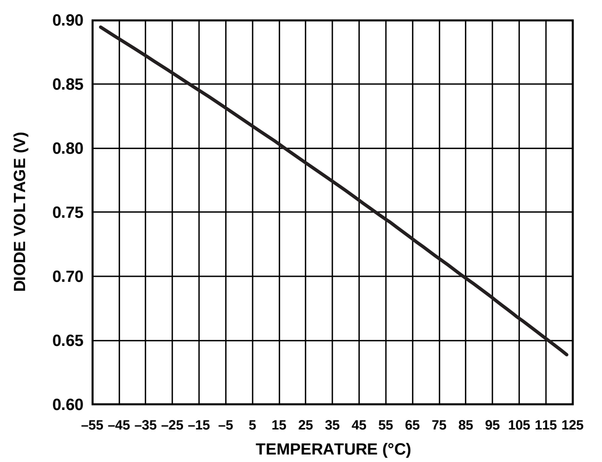


Figure 56. Diode Voltage vs. Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9234 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD9234 also records any overrange condition in any of the four virtual converters. For more information on the virtual converters, refer to Figure 62. The overrange status of each virtual converter is registered as a sticky bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562, by toggling the bits corresponding to the virtual converter to set and reset position.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The FD bit (enabled via the control bits in Register 0x559 and Register 0x55A) is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 57.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\text{Upper Threshold Magnitude (dBFS)} = 20 \log (\text{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\text{Lower Threshold Magnitude (dBFS)} = 20 \log (\text{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x247 and Register 0x248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x249 and Register 0x24A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x040, and Register 0x245 to Register 0x24C in Table 17) for more details.

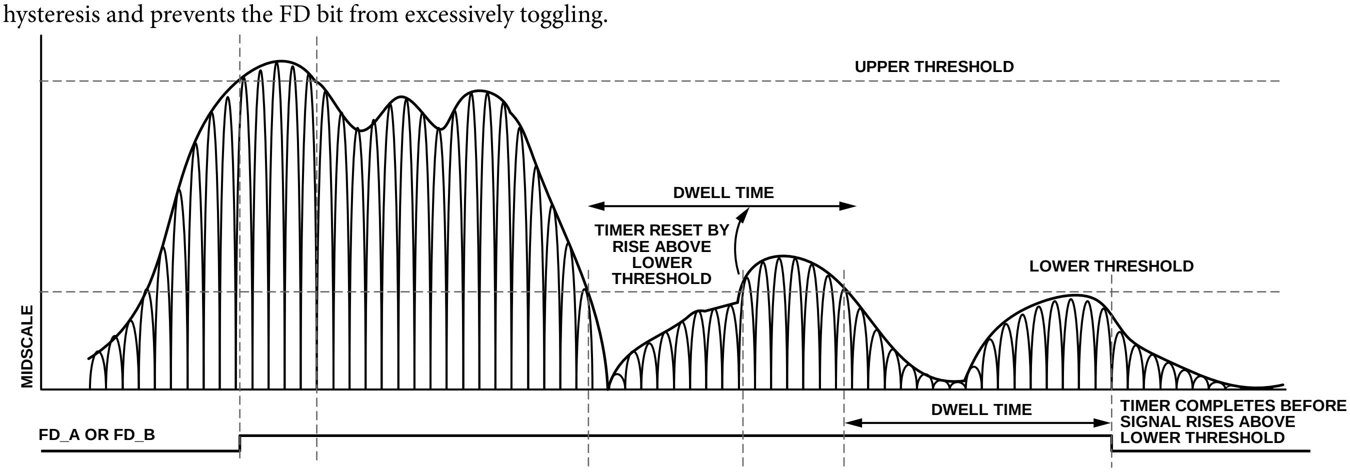


Figure 57. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 58 shows the simplified block diagram of the signal monitor block.

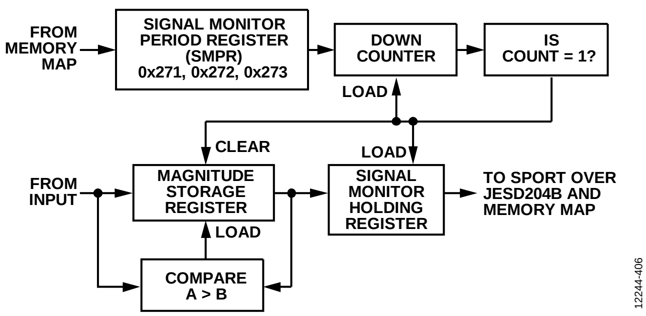


Figure 58. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$\textit{Peak Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Peak Detector Value}/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure, as explained previously, continues.

SPORT Over JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. This function is enabled by setting Bit 1 and Bit 0 of Register 0x279 and Bit 1 of Register 0x27A. Figure 59 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. There are a maximum of three control bits that can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), then only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 59). To select the SPORT over JESD204B option, program Register 0x559, Register 0x55A, and Register 0x58F. See Table 17 for more information on setting these bits.

Figure 60 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 61 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

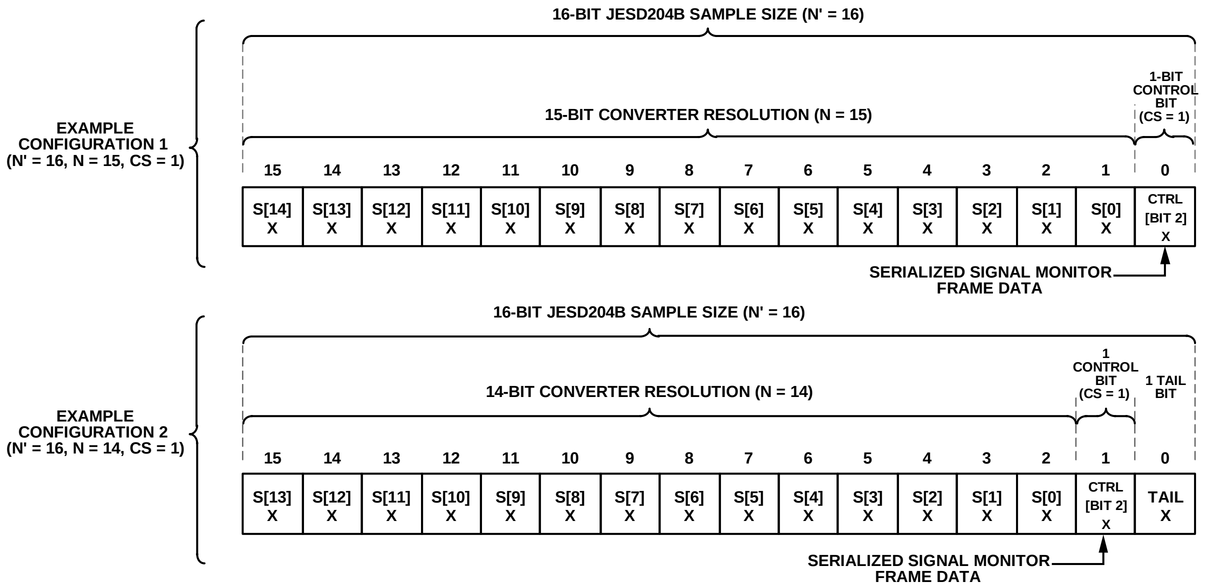


Figure 59. Signal Monitor Control Bit Locations

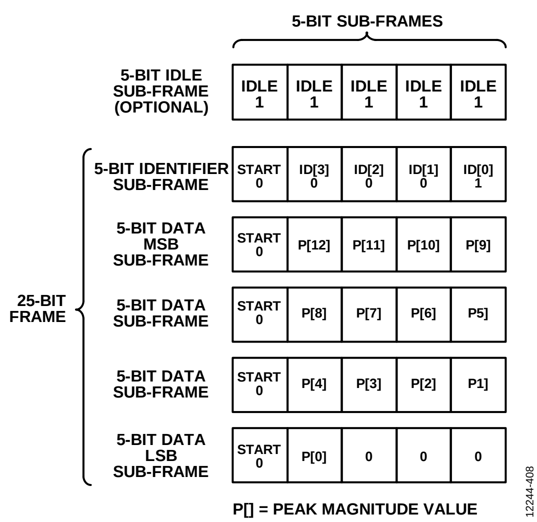


Figure 60. SPORT over JESD204B Signal Monitor Frame Data

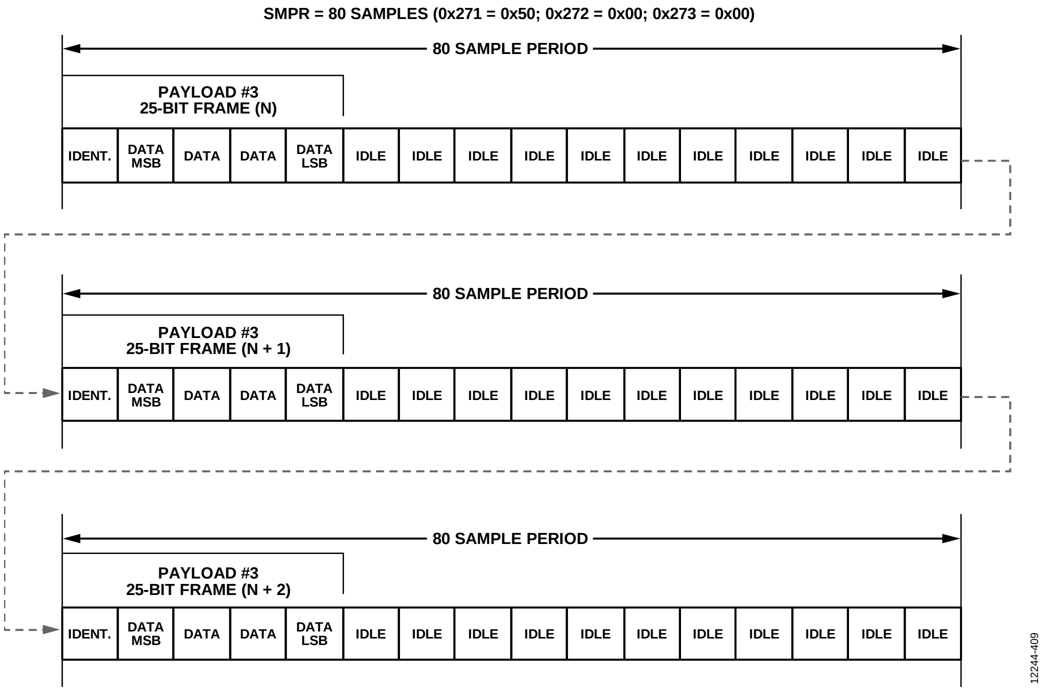


Figure 61. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

DIGITAL DOWNCONVERTER (DDC)

The AD9234 includes two digital downconverters (DDC 0 and DDC 1) that provide filtering and reduce the output data rate. This digital processing section includes a half-band decimating filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverter can be configured to output either real data or complex output data.

DDC GENERAL DESCRIPTION

The two DDC blocks are used to extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains a decimate-by-2 digital processing block, as shown in Figure 62.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio of all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

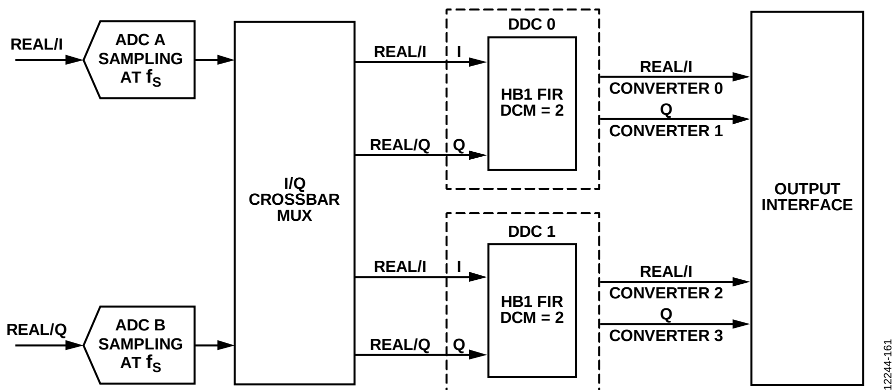


Figure 62. DDC Detailed Block Diagram

HALF-BAND FILTER

The AD9234 offers one half-band filter per DDC to enable digital signal processing of the ADC converted data.

The decimate-by-2, half-band (HB), low-pass FIR filter uses a 55-tap, symmetrical, fixed coefficient filter implementation, optimized for low power consumption. The HB filter is enabled when the DDC is selected. Table 10 and Figure 63 show the coefficients and response of the HB1 filter.

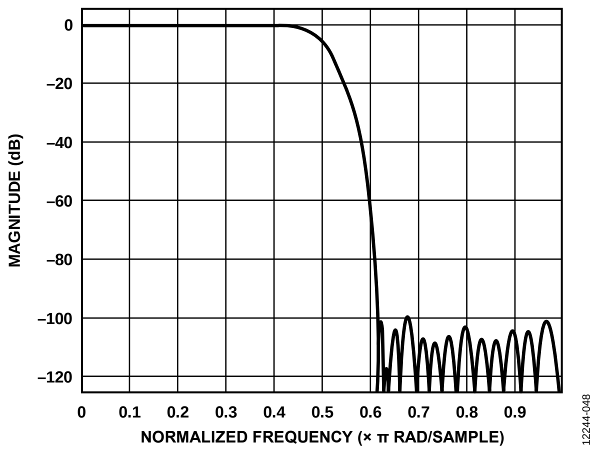


Figure 63. HB1 Filter Response

Table 10. Half-Band Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C1, C55	−0.000023	−24
C2, C54	0	0
C3, C53	0.000097	102
C4, C52	0	0
C5, C51	−0.000288	−302
C6, C50	0	0
C7, C49	0.000696	730
C8, C48	0	0
C9, C47	−0.0014725	−1544
C10, C46	0	0
C11, C45	0.002827	2964
C12, C44	0	0
C13, C43	−0.005039	−5284
C14, C42	0	0
C15, C41	0.008491	8903
C16, C40	0	0
C17, C39	−0.013717	−14,383
C18, C38	0	0
C19, C37	0.021591	22640
C20, C36	0	0
C21, C35	−0.033833	−35476
C22, C34	0	0
C23, C33	0.054806	57468
C24, C32	0	0
C25, C31	−0. .100557	−105442
C26, C30	0	0
C27, C29	0.316421	331,792
C28	0.500000	524,288

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits and no additional gain is necessary. However, the optional 6 dB gain can be used to compensate for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage (see Figure 64).

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage, along with an $f_S/4$ complex mixer, to upconvert the signal.

After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 64 shows a simplified block diagram of the complex to real conversion.

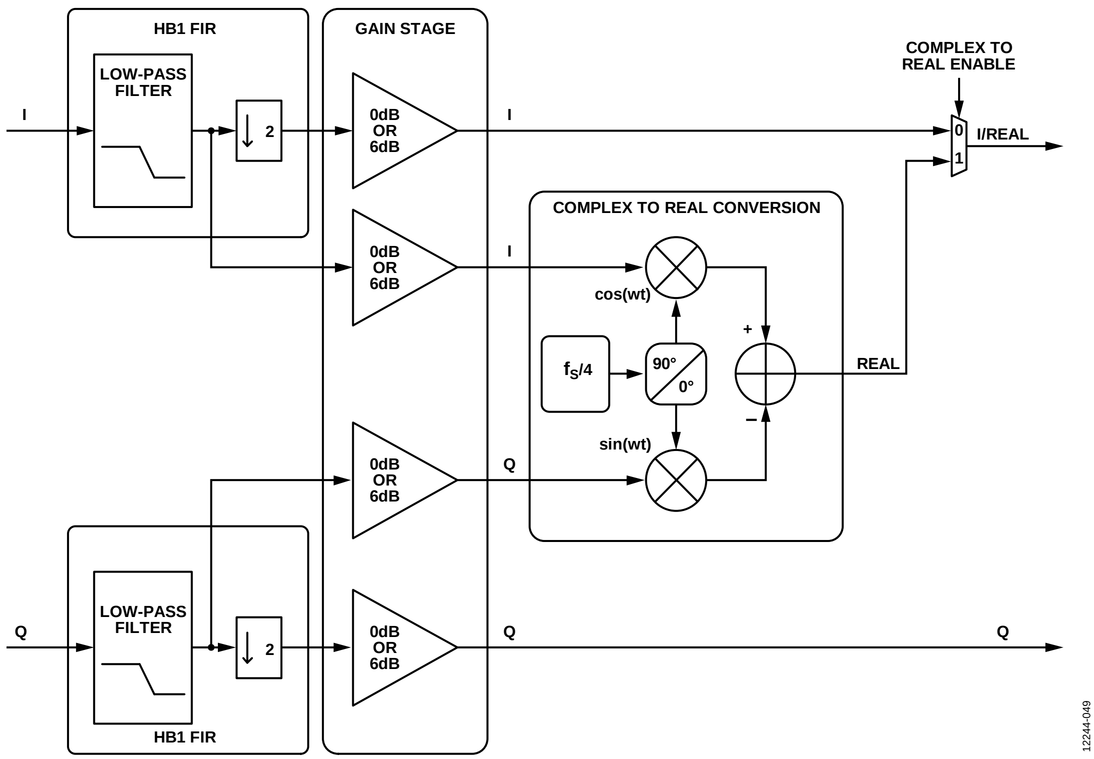


Figure 64. Complex to Real Conversion Block

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9234 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9234 to a digital processing device over a serial interface with lane rates of up to 10 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8B/10B encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, users are encouraged to refer to the JESD204B standard.

The AD9234 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9234 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L = number of lanes/converter device (lanes/link) (AD9234 value = 1, 2, or 4)
- M = number of converters/converter device (virtual converters/link) (AD9234 value = 1, 2, 4, or 8)
- F = octets/frame (AD9234 value = 1, 2, 4, 8, or 16)
- N′ = number of bits per sample (JESD204B word size) (AD9234 value = 8 or 16)
- N = converter resolution (AD9234 value = 7 to 16)
- CS = number of control bits/sample (AD9234 value = 0, 1, 2, or 3)
- K = number of frames per multiframe (AD9234 value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S = samples transmitted/single converter/frame cycle (AD9234 value = set automatically based on L, M, F, and N′)
- HD = high density mode (AD9234 = set automatically based on L, M, F, and N′)
- CF = number of control words/frame clock cycle/converter device (AD9234 value = 0)

Figure 65 shows a simplified block diagram of the AD9234 JESD204B link. By default, the AD9234 is configured to use two converters and four lanes. Converter A data is output to SERDOUT0± and/or SERDOUT1± , and Converter B is output to SERDOUT2± and/or SERDOUT3±. The AD9234 allows other configurations such as combining the outputs of both converters onto a single lane, or changing the mapping of the A and B digital output paths. These modes are set up via a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9234, the 12-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, signal monitor, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8B/10B encoder. The 8B/10B encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 66 shows how the 12-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 66 illustrates the default data format.

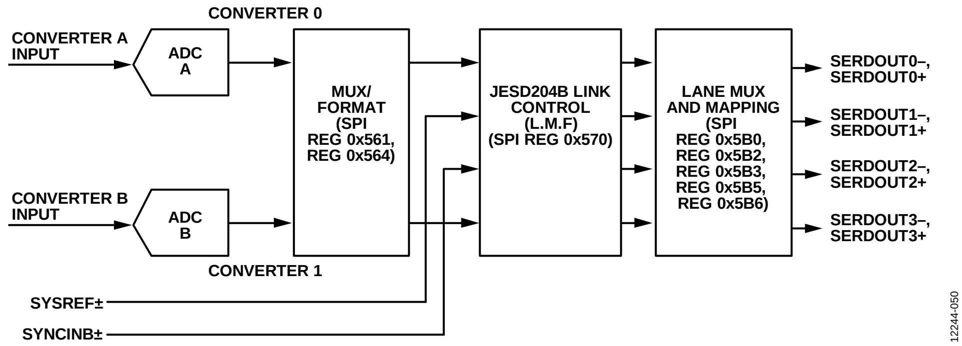


Figure 65. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x200 = 0x00)

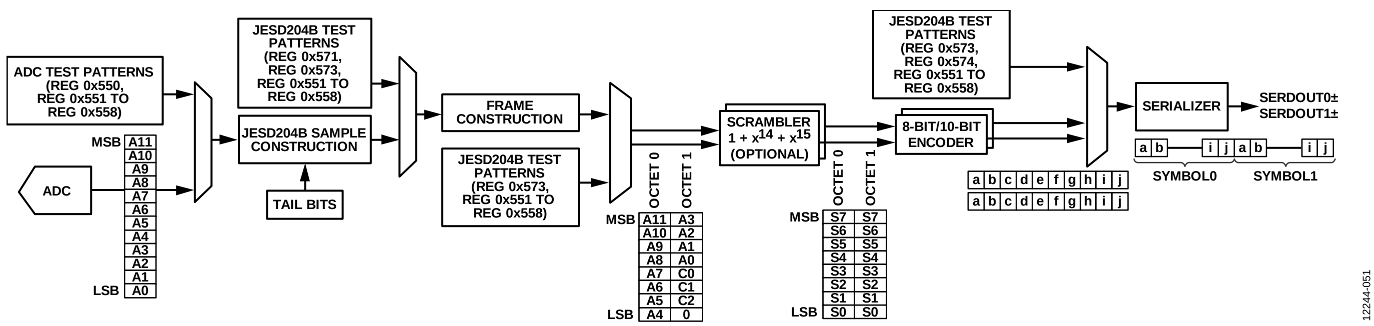


Figure 66. ADC Output Datapath Showing Data Framing

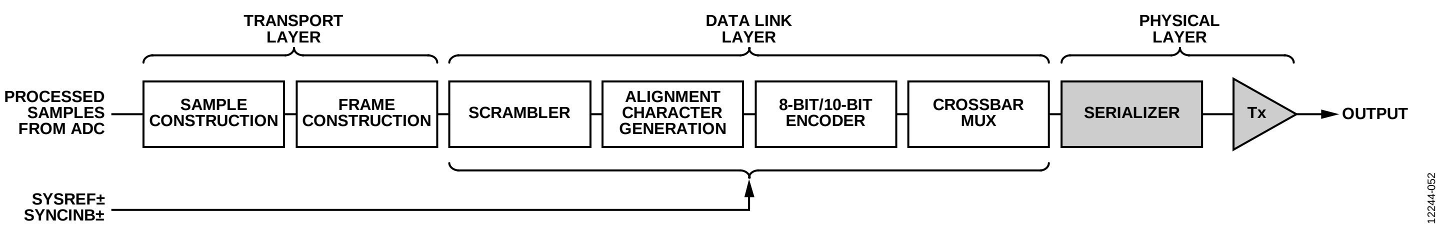


Figure 67. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 67 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open-source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9234 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard JESD204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB±

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD9234 low. The JESD204B Tx then begins sending /K/ characters. After the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD9234 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation, refer to Register 0x572.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 68. The four multiframes include the following:

- Multiframe 1. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2. Begins with an /R/ character followed by a /Q/ (/K28.4/) character, followed by link configuration parameters over 14 configuration octets (see Table 11) and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

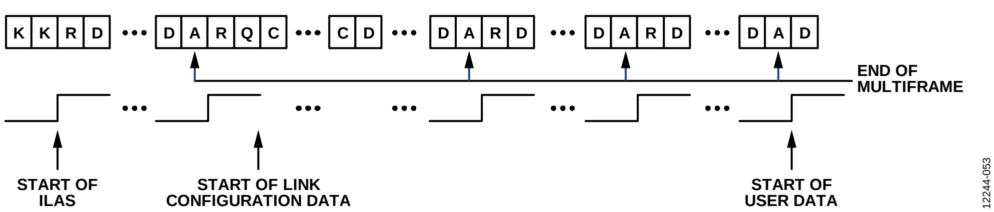


Figure 68. Initial Lane Alignment Sequence

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames is equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x571.

8B/10B Encoder

The 8B/10B encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 11. The 8B/10B encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8B/10B interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are intended to be troubleshooting tools for the verification of the digital front end (DFE). Refer to the Memory Map section, Register 0x572[2:1] for information on configuring the 8B/10B encoder.

Table 11. AD9234 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0010	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9234 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver, which results in a nominal 300 mV p-p swing at the receiver (see Figure 69). It is recommended to use ac coupling to connect the AD9234 SERDES outputs to the receiver.

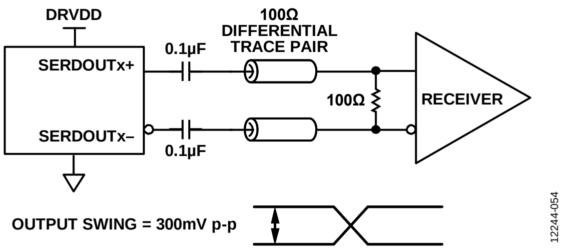


Figure 69. AC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

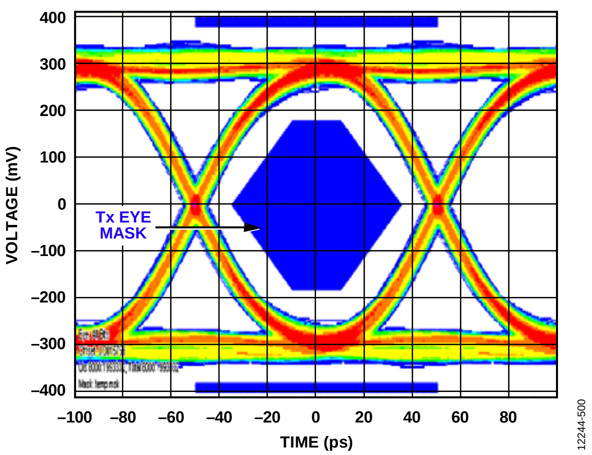


Figure 70. Digital Outputs Data Eye, External 100 Ω Terminations at 10 Gbps

Figure 70 to Figure 75 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one AD9234 lane running at 10 Gbps and 6 Gbps, respectively. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x561 in Table 17).

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link may cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it may increase electromagnetic interference (EMI). See the Memory Map section (Register 0x5C1 to Register 0x5C5 in Table 17) for more details.

Phase-Locked Loop

The PLL is used to generate the serializer clock, which will operate at the JESD204B lane rate. The JESD204B lane rate Register 0x056E[4:3] must be set to correspond with the lane rate.

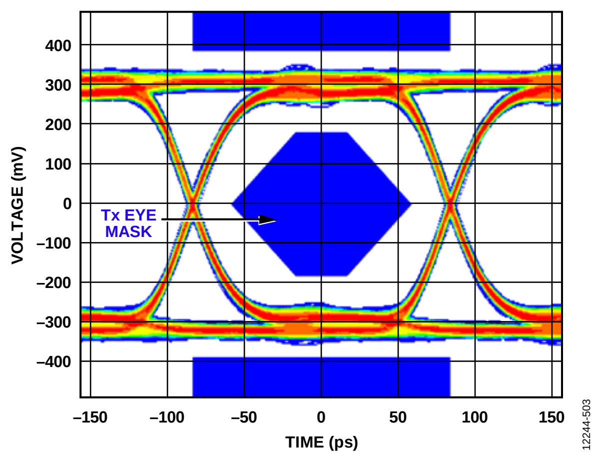


Figure 71. Digital Outputs Data Eye, External 100 Ω Terminations at 6 Gbps

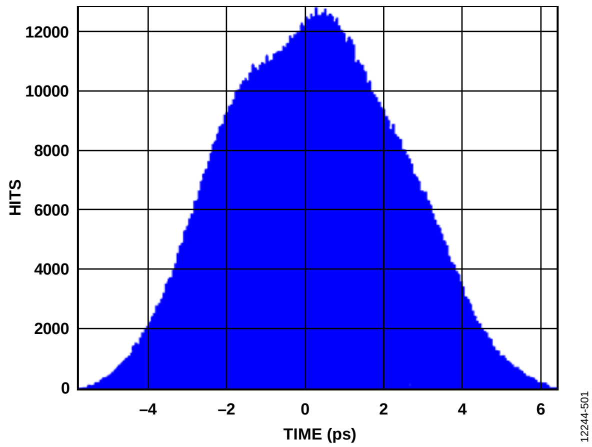


Figure 72. Digital Outputs Histogram, External 100 Ω Terminations at 10 Gbps

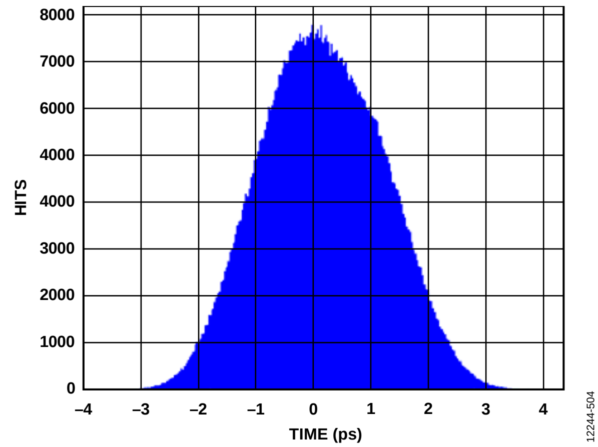


Figure 74. Digital Outputs Histogram, External 100 Ω Terminations at 6 Gbps

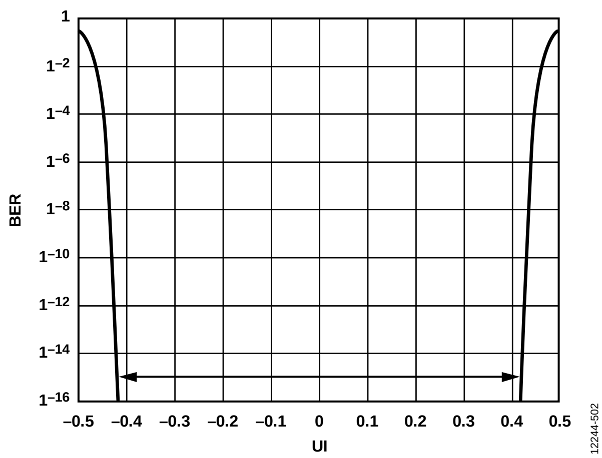


Figure 73. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 10 Gbps

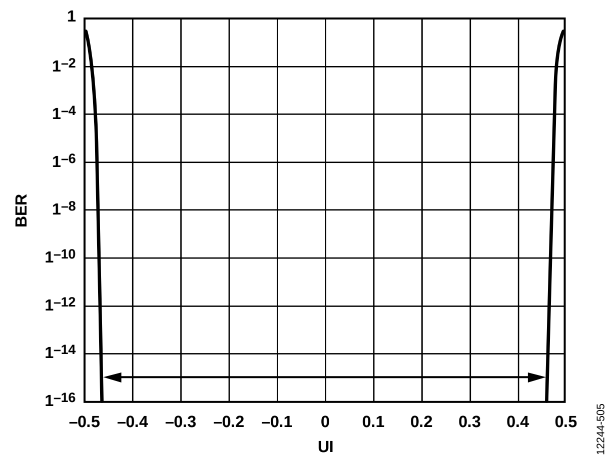


Figure 75. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 6 Gbps

CONFIGURING THE JESD204B LINK

The AD9234 has one JESD204B link. The device offers an easy way to set up the JESD204B link through the quick configuration register (Register 0x570). The serial outputs (SERDOUT0± to SERDOUT3±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

The maximum lane rate allowed by the JESD204B specification is 12.5 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$Lane\ Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where $f_{OUT} = f_{ADC\_CLOCK}/decimation\ ratio.$

The following steps can be used to configure the output:

1. Power down the link.
2. Select quick configuration options.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.25 Gbps, select the low line rate option. This is done by programming a value of 0x10 to Register 0x56E.

Table 12 and Table 13 show the JESD204B output configurations supported for both N′ = 16 and N′ = 8 for a given number of virtual converters. Care must be taken to ensure that the serial line rate for a given configuration is within the supported range of 3.125 Gbps to 12.5 Gbps.

Table 12. JESD204B Output Configurations for N′ = 16

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (0x570)	JESD204B Serial Line Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x01	20 × f_{OUT}	1	1	2	1	0	8 to 16	16	0 to 3	Only valid K values that are divisible by 4 are supported
	0x40	10 × f_{OUT}	2	1	1	1	1	8 to 16	16	0 to 3	
	0x41	10 × f_{OUT}	2	1	2	2	0	8 to 16	16	0 to 3	
	0x80	5 × f_{OUT}	4	1	1	2	1	8 to 16	16	0 to 3	
	0x81	5 × f_{OUT}	4	1	2	4	0	8 to 16	16	0 to 3	
2	0x0A	40 × f_{OUT}	1	2	4	1	0	8 to 16	16	0 to 3	
	0x49	20 × f_{OUT}	2	2	2	1	0	8 to 16	16	0 to 3	
	0x88	10 × f_{OUT}	4	2	1	1	1	8 to 16	16	0 to 3	
	0x89	10 × f_{OUT}	4	2	2	2	0	8 to 16	16	0 to 3	
4	0x13	80 × f_{OUT}	1	4	8	1	0	8 to 16	16	0 to 3	
	0x52	40 × f_{OUT}	2	4	4	1	0	8 to 16	16	0 to 3	
	0x91	20 × f_{OUT}	4	4	2	1	0	8 to 16	16	0 to 3	

[1] f_{OUT} = output sample rate = ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥3.125 Gbps and ≤12.5 Gbps; when the serial line rate is ≤12.5 Gbps and ≥6.25 Gbps, the low line rate mode must be disabled (set Bit 4 to 0x0 in 0x56E). When the serial line rate is <6.25 Gbps and ≥3.125 Gbps, the low line rate mode must be enabled (set Bit 4 to 0x1 in 0x56E).
[2] JESD204B transport layer descriptions are as described in the JESD204B Overview section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Table 13. JESD204B Output Configurations for N′ = 8

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (0x570)	Serial Line Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x00	10 × f_{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values which are divisible by 4 are supported
	0x01	10 × f_{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f_{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f_{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f_{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
	0x80	2.5 × f_{OUT}	4	1	1	4	0	7 to 8	8	0 to 1	
	0x81	2.5 × f_{OUT}	4	1	2	8	0	7 to 8	8	0 to 1	

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (0x570)	Serial Line Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
2	0x09	$20 \times f_{OUT}$	1	2	2	1	0	7 to 8	8	0 to 1	
	0x48	$10 \times f_{OUT}$	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	$10 \times f_{OUT}$	2	2	2	2	0	7 to 8	8	0 to 1	
	0x88	$5 \times f_{OUT}$	4	2	1	2	0	7 to 8	8	0 to 1	
	0x89	$5 \times f_{OUT}$	4	2	2	4	0	7 to 8	8	0 to 1	
	0x8A	$5 \times f_{OUT}$	4	2	4	8	0	7 to 8	8	0 to 1	

[1] f_{OUT} = output sample rate = ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥3125 Mbps and ≤12,500 Mbps; when the serial line rate is ≤12.5 Gbps and ≥6.25 Gbps, the low line rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial line rate is <6.25 Gbps and ≥3.125 Gbps, the low line rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).
[2] JESD204B transport layer descriptions are as described in the JESD204B Overview section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

See the Example 1: Full Bandwidth Mode section and the Example 2: ADC with DDC Option (Two ADCs Plus Two DDCs) section for two examples describing which JESD204B transport layer settings are valid for a given chip mode.

Example 1: Full Bandwidth Mode

Chip application mode is full bandwidth mode (see Figure 76).

- Two 12-bit converters at 1000 MSPS
- Full bandwidth application layer mode
- No decimation

JESD204B output configuration includes the following:

- Two virtual converters required (see Table 12)
- Output sample rate (f_{OUT}) = 1000/1 = 1000 MSPS

JESD204B supported output configurations (see Table 12) include

- N′ = 16 bits
- N = 12 bits
- L = 4, M = 2, and F = 1, or L = 4, M = 2, and F = 2 (quick configuration = 0x88 or 0x89)
- CS = 0 to 2
- K = 32
- Output serial line rate = 10 Gbps per lane, low line rate mode disabled

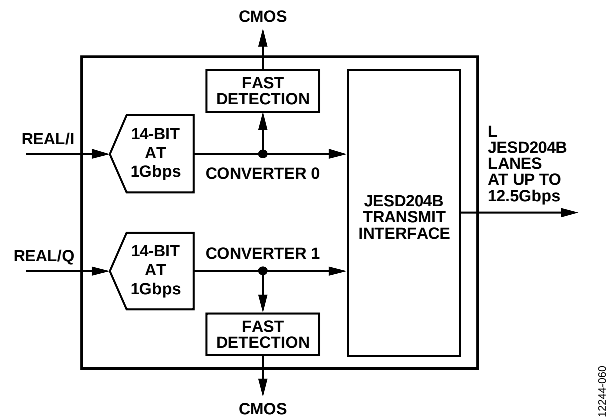


Figure 76. Full Bandwidth Mode

Example 2: ADC with DDC Option (Two ADCs Plus Two DDCs)

Chip application mode is two-DDC mode. (see Figure 77).

- Two 12-bit converters at 1 MSPS
- Two DDC application layer mode with complex outputs (I/Q)
- Chip decimation ratio = 2
- DDC decimation ratio = 2 (see Table 17)

JESD204B output configuration includes the following:

- Virtual converters required = 4 (see Table 12)
- Output sample rate (f_{OUT}) = 1000/2 = 500 MSPS

JESD204B supported output configurations include (see Table 12)

- N′ = 16 bits
- N = 12 bits
- L = 4, M = 4, and F = 2 (quick configuration = 0x91)
- CS = 0 to 1
- K = 32
- Output serial line rate = 10 Gbps per lane (L = 4)
- Low line rate mode is disabled (0x56E = 0x00).

Example 2 shows the flexibility in the digital and lane configurations for the AD9234. The sample rate is 1 GSPS, but the outputs are all combined in either one or two lanes, depending on the I/O speed capability of the receiving device.

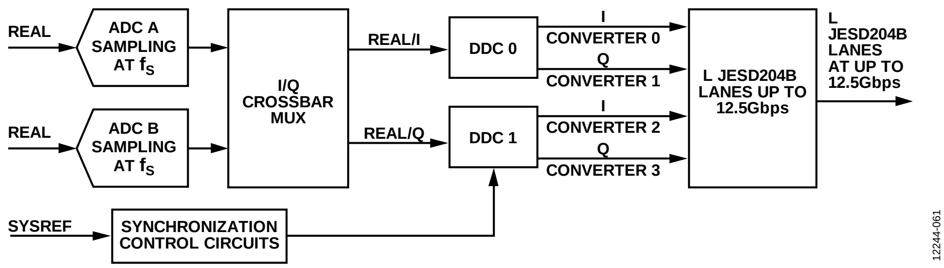


Figure 77. Two-ADC Plus Two-DDC Mode

MULTICHIP SYNCHRONIZATION

The AD9234 has a SYSREF± input that allows the user flexible options for synchronizing the internal blocks. The SYSREF± input is a source synchronous system reference signal that enables multichip synchronization. The input clock divider, DDCs, signal monitor block, and JESD204B link can be synchronized using the SYSREF± input. For the highest level of timing accuracy, SYSREF± must meet setup and hold requirements relative to the CLK± input.

The flowchart in Figure 78 describes the internal mechanism by which multichip synchronization can be achieved in the AD9234. The AD9234 supports several features which aid users in meeting the requirements set out for capturing a SYSREF± signal. The SYSREF sample event can be defined as either a synchronous low to high transition, or synchronous high to low transition. Additionally, the AD9234 allows the SYSREF signal to be sampled using either the rising edge or falling edge of the CLK± input. The AD9234 also has the ability to ignore a programmable number (up to 16) of SYSREF± events. The SYSREF± control options can be selected using Register 0x120 and Register 0x121.

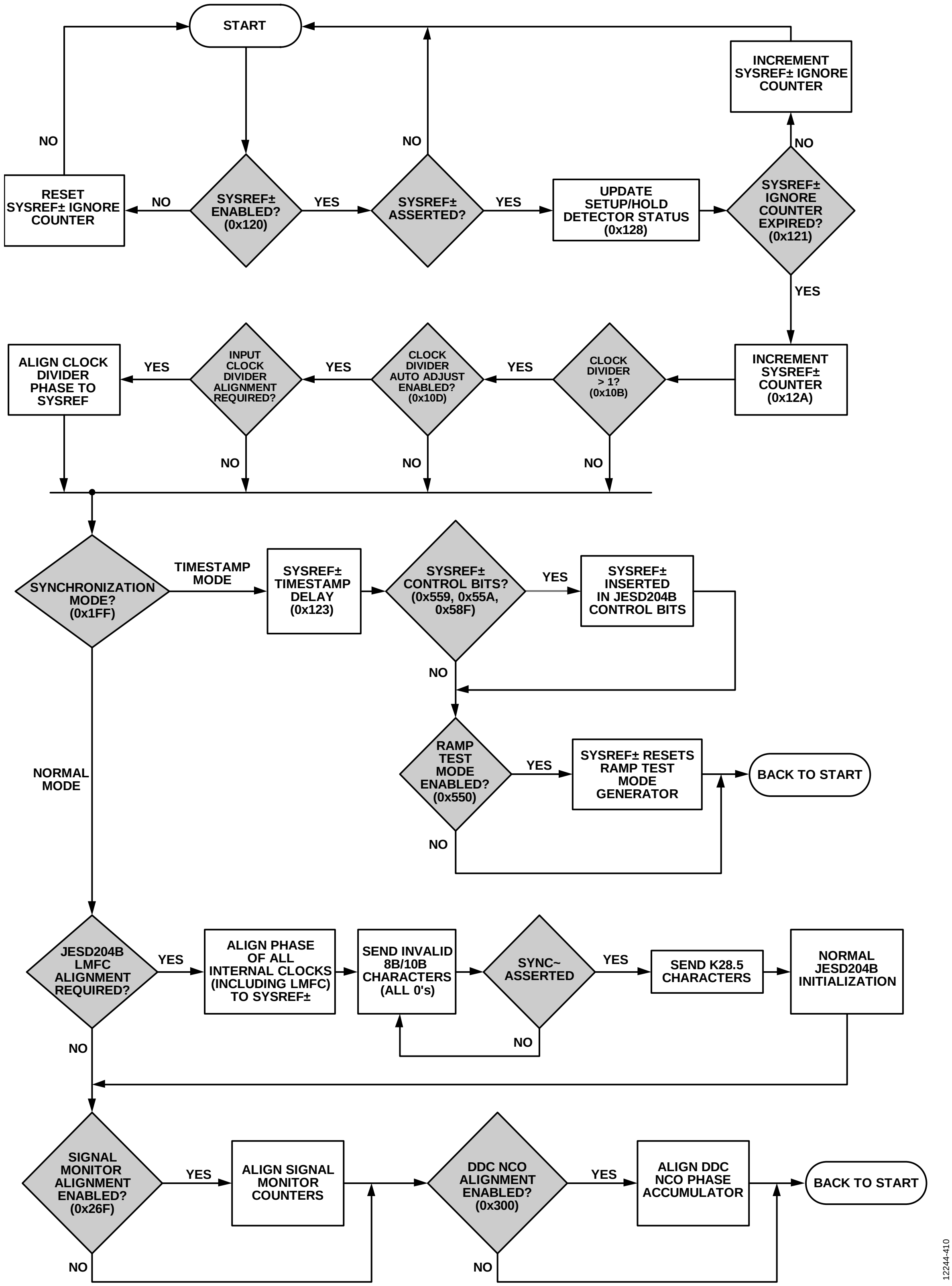


Figure 78. Multichip Synchronization

SYSREF± SETUP/HOLD WINDOW MONITOR

To assist in ensuring a valid SYSREF signal capture, the AD9234 has a SYSREF± setup/hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map. Figure 79 and Figure 80 show the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF±signal before the CLK± edge and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x128 stores the status of SYSREF± and lets the user know if the SYSREF± signal is successfully captured by the ADC.

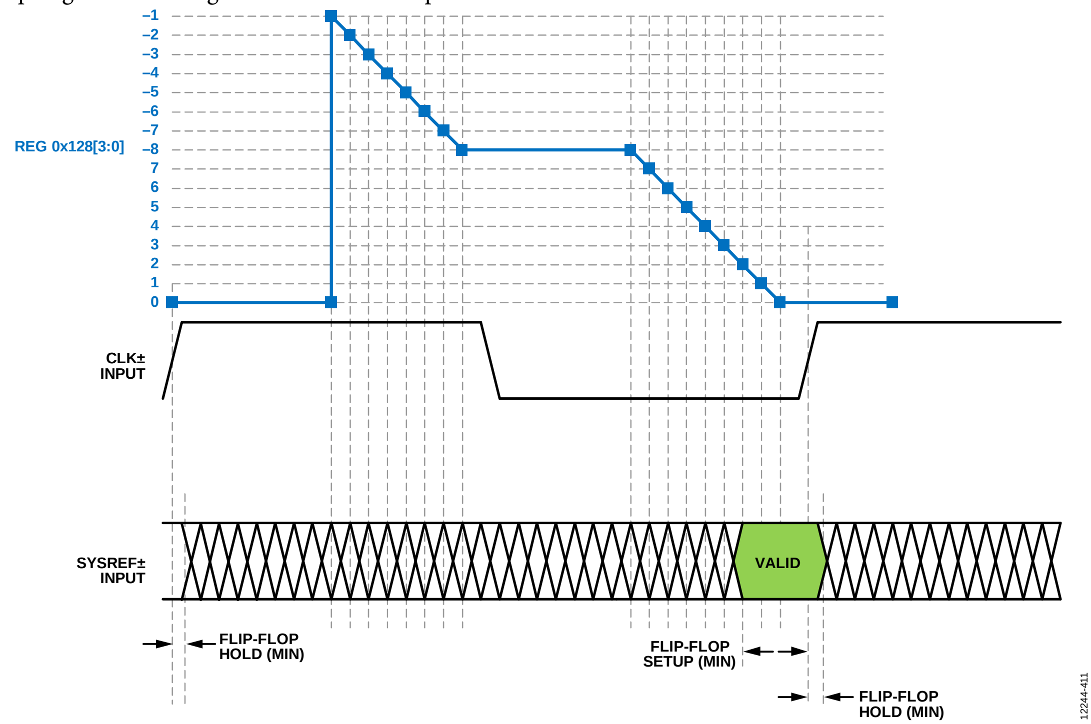


Figure 79. SYSREF± Setup Detector

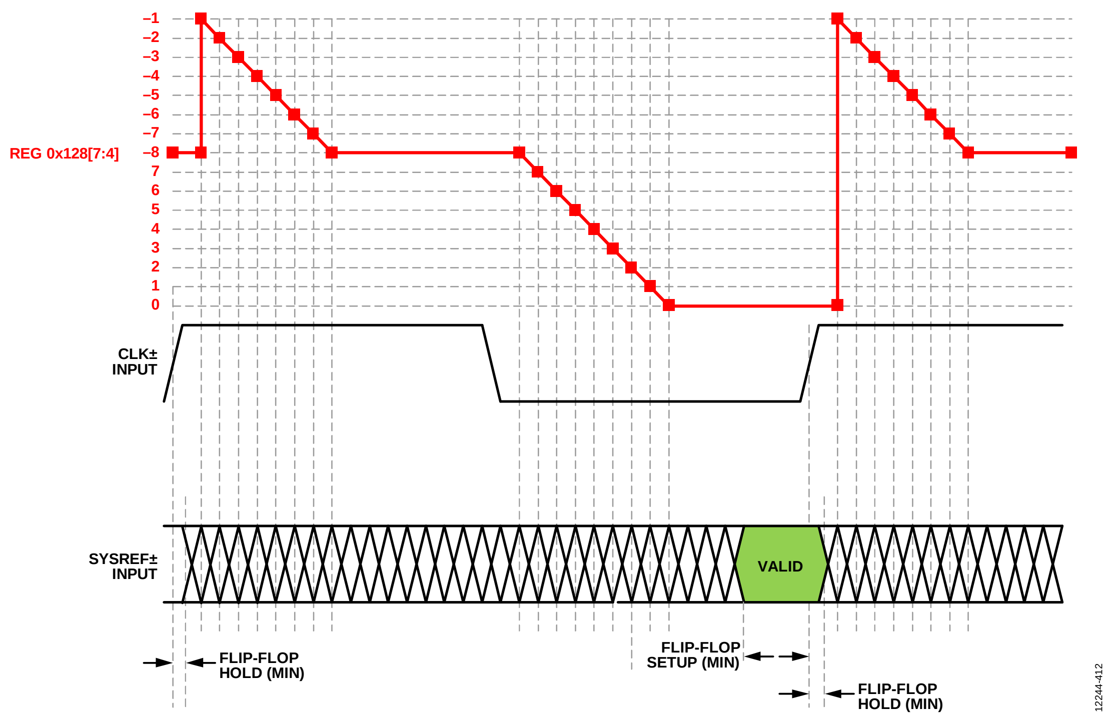


Figure 80. SYSREF± Hold Detector

Table 14 shows the description of the contents of Register 0x128 and how to interpret them.

Table 14. SYSREF± Setup/Hold Monitor, Register 0x128

Register 0x128[7:4] Hold Status	Register 0x128[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

SERIAL PORT INTERFACE

The AD9234 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 15). The SCLK (serial clock) pin synchronizes the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 15. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 3 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the AD9234. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9234 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD9234 device specific features are described in the Memory Map section.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x000 to Register 0x00D), the ADC function registers (Register 0x015 to Register 0x27A), The DDC function registers (Register 0x300 to Register 0x347), and the digital outputs and test modes registers (Register 0x550 to Register 0x5C5).

Table 17 (see the Memory Map section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the Table 17.

Open and Reserved Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x561). If the entire address location is open (for example, Address 0x013), do not write to this address location.

Default Values

After the AD9234 is reset, critical registers are loaded with default values. The default values for the registers are given in Table 17.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

Channel-Specific Registers

Some channel setup functions, such as the input termination (Register 0x016), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 17 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 17 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x005 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the AD9234 requires 5 ms to recover. When programming the AD9234 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTER TABLE

All address locations that are not included in Table 17 are not currently supported for this device and must not be written.

Table 17. Memory Map Registers

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Analog Devices SPI Registers											
0x000	INTERFACE_ CONFIG_A	Soft reset (self clearing)	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing)	0x00	
0x001	INTERFACE_ CONFIG_B	Single instruction	0	0	0	0	0	Datapath soft reset (self clearing)	0	0x00	
0x002	DEVICE_ CONFIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE					011 = high speed ADC				0x03	Read only
0x004	CHIP_ID (low byte)	1	1	0	0	1	1	1	0	0xCE	Read only
0x005	CHIP_ID (high byte)	0	0	0	0	0	0	0	0	0x00	Read only
0x006	CHIP_GRADE	1	0	1	0	X	X	X	X	0xAX	Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x03	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
ADC Function Registers											
0x015	Analog Input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	
0x016	Input termination (local)	Analog input differential termination 0000 = 400 Ω 0001 = 200 Ω 0010 = 100 Ω 0110 = 50 Ω				0	0	1	1	0x03	
0x018	Input buffer current control (local)	0000 = 1.0× buffer current 0001 = 1.5× buffer current 0010 = 2.0× buffer current 0011 = 2.5× buffer current (default) 0100 = 3.0× buffer current 0101 = 3.5× buffer current … 1111 = 8.5× buffer current				0	0	0	0	0x30	
0x024	V_1P0 control	0	0	0	0	0	0	0	1.0 V reference select 0 = internal 1 = external	0x00	
0x028	Temperature diode (local)	0	0	0	0	0	0	0	Diode selection 0 = no diode selected 1 = temperature diode selected	0x00	Used in conjunction with Reg. 0x040

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x03F	PDWN/ STBY pin control (local)	0 = PDWN/ STBY enabled 1 = disabled	0	0	0	0	0	0	0	0x00	Used in conjunc-tion with Reg. 0x040
0x040	Chip pin control	PDWN/STBY function 00 = power down 01 = standby 10 = disabled		Fast Detect B (FD_B) 000 = Fast Detect B output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 111 = disabled			Fast Detect A (FD_A) 000 = Fast Detect A output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 011 = temperature diode 111 = disabled			0x3F	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1 001 = divide by 2 011 = divide by 4 111 = divide by 8			0x00	
0x10C	Clock divider phase (local)	0	0	0	0	Independently controls Channel A and Channel B clock divider phase offset 0000 = 0 input clock cycles delayed 0001 = ½ input clock cycles delayed 0010 = 1 input clock cycles delayed 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				0x00	
0x10D	Clock divider and SYSREF control	Clock divider auto phase adjust 0 = disabled 1 = enabled	0	0	0	Clock divider negative skew window 00 = no negative skew 01 = 1 device clock of negative skew 10 = 2 device clocks of negative skew 11 = 3 device clocks of negative skew		Clock divider positive skew window 00 = no positive skew 01 = 1 device clock of positive skew 10 = 2 device clocks of positive skew 11 = 3 device clocks of positive skew		0x00	Clock divider must be >1
0x117	Clock delay control	0	0	0	0	0	0	0	Clock fine delay adjust enable 0 = disabled 1 = enabled	0x00	Enabling the clock fine delay adjust causes a datapath reset
0x118	Clock fine delay (local)	Clock fine delay adjust[7:0], twos complement coded control to adjust the fine sample clock skew in ~1.7 ps steps ≤ −88 = −151.7 ps skew −87 = −150 ps skew … 0 = 0 ps skew … ≥ +87 = +150 ps skew								0x00	Used in con-junction with Reg. 0x0117
0x11C	Clock status	0	0	0	0	0	0	0	0 = no input clock detected 1 = input clock det-ected	Read only	
0x120	SYSREF± Control 1	0	SYSREF± flag reset 0 = normal operation 1 = flags held in reset	0	SYSREF± transition select 0 = low to high 1 = high to low	CLK± edge select 0 = rising 1 = falling	SYSREF± mode select 00 = disabled 01 = continuous 10 = N shot		0	0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x121	SYSREF± Control 2	0	0	0	0	SYSREF± N-shot ignore counter select 0000 = next SYSREF± Only 0001 = ignore the first SYSREF± transitions 0010 = ignore the first two SYSREF± transitions … 1111 = ignore the first 16 SYSREF± transitions				0x00	Mode select, Reg. 0x120, Bits[2:1], must be N shot
0x123	SYSREF± timestamp delay control		SYSREF± timestamp delay, Bits[6:0] 0x00 = no delay 0x01 = 1 clock delay … 0x7F = 127 clocks delay							0x00	Ignored when Reg. 0x01FF = 0x00
0x128	SYSREF± Status 1	SYSREF± hold status, Register 0x128[7:4], refer to Table 14				SYSREF± setup status, Register 0x128[3:0], refer to Table 14				Read only	
0x129	SYSREF± and clock divider status	0	0	0	0	Clock divider phase when SYSREF± was captured 0000 = in-phase 0001 = SYSREF± is ½ cycle delayed from clock 0010 = SYSREF± is 1 cycle delayed from clock 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				Read only	
0x12A	SYSREF± counter	SYSREF± counter, Bits[7:0] increments when a SYSREF± signal is captured								Read only	
0x1FF	Chip sync mode							Synchronization mode 00 = normal 01 = timestamp		0x00	
0x200	Chip application mode	0	0	Chip Q ignore 0 = normal (I/Q) 1 = ignore (I– only)	0	0	0	Chip operating mode 00 = full bandwidth mode 01 = DDC 0 on 10 = DDC 0 and DDC 1		0x00	
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select 000 = full sample rate (decimate = 1) 001 = decimate by 2			0x00	
0x228	Customer offset	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x245	Fast detect (FD) control (local)	0	0	0	0	Force FD_A/ FD_B pins; 0 = normal function; 1 = force to value	Force value of FD_A/ FD_B pins if force pins is true, this value is output on FD pins	0	Enable fast detect output	0x00	
0x247	FD upper threshold LSB (local)	Fast detect upper threshold, Bits[7:0]								0x00	
0x248	FD upper threshold MSB (local)	0	0	0	Fast detect upper threshold, Bits[12:8]					0x00	
0x249	FD lower threshold LSB (local)	Fast detect lower threshold, Bits[7:0]								0x00	
0x24A	FD lower threshold MSB (local)	0	0	0	Fast detect lower threshold, Bits[12:8]					0x00	
0x24B	FD dwell time LSB (local)	Fast detect dwell time, Bits[7:0]								0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x24C	FD dwell time MSB (local)	Fast detect dwell time, Bits[15:8]								0x00	
0x26F	Signal ,onitor synchronizatio n control	0	0	0	0	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one shot		0x00	Refer to the Signal Monitor section
0x270	Signal monitor control (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
0x271	Signal Monitor Period Register 0 (local)	Signal monitor period, Bits[7:0]								0x80	In decimated output clock cycles
0x272	Signal Monitor Period Register 1 (local)	Signal monitor period, Bits[15:8]								0x00	In decimated output clock cycles
0x273	Signal Monitor PeriodRegister 2 (local)	Signal monitor period, Bits[23:16]								0x00	In decimated output clock cycles
0x274	Signal monitor result control (local)	0	0	0	Result update 1 = update results (self clear)	0	0	0	Result selection 0 = reserved 1 = peak detector	0x01	
0x275	Signal Monitor Result Register 0 (local)	Signal monitor result, Bits[7:0] When Register 0x0274[0] = 1, result bits [19:7] = peak detector absolute value [12:0]; result bits [6:0] = 0								Read only	Updated based on Reg. 0x274[4]
0x276	Signal Monitor Result Register 1 (local)	Signal monitor result, Bits[15:8]								Read only	Updated based on Reg. 0x274[4]
0x277	Signal Monitor Result Register 1 (local)	0	0	0	0	Signal monitor result, Bits[19:16]				Read only	Updated based on Reg. 0x274[4]
0x278	Signal monitor period counter result (local)	Period count result, Bits[7:0]								Read only	Updated based on Reg. 0x274[4]
0x279	Signal monitor SPORT over JESD204B control (local)	0	0	0	0	0	0	00 = reserved 11 = enable		0x00	
0x27A	SPORT over JESD204B input selection (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
DDC Function Registers (See the Digital Downconverter (DDC) Section)											
0x300	DDC synch control	0	0	0	DDC NCO soft reset 0 = normal operation 1 = reset	0	0	Synchronization mode (triggered by SYSREF±) 00 = disabled 01 = continuous 11 = 1-shot			
0x310	DDC 0 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 (complex to real enabled) 11 = decimate by 1		0x00	
0x311	DDC 0 input selection	0	0	0	0	0	Q input select 0 = Ch A 1 = Ch B	0	I input select 0 = Ch A 1 = Ch B	0x00	
0x314	DDC 0 frequency LSB	DDC 0 NCO frequency value, Bits[7:0], twos complement								0x00	
0x315	DDC0 frequency MSB	X	X	X	X	DDC 0 NCO frequency value, Bits[11:8], twos complement				0x00	
0x320	DDC 0 phase LSB	DDC 0 NCO phase value, Bits[7:0], twos complement								0x00	
0x321	DDC 0 phase MSB	X	X	X	X	DDC 0 NCO phase value, Bits[11:8], twos complement				0x00	
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch B	0	I output test mode enable 0 = disabled 1 = enabled from Ch A	0x00	
0x330	DDC 1 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 (complex to real enabled) 11 = decimate by 1		0x00	
0x331	DDC 1 input selection	0	0	0	0	0	Q input select 0 = Ch A 1 = Ch B	0	I input select 0 = Ch A 1 = Ch B	0x00	
0x334	DDC 1 frequency LSB	DDC 1 NCO frequency value, Bits[7:0], twos complement								0x00	
0x335	DDC 1 frequency MSB	X	X	X	X	DDC 1 NCO frequency value, Bits[11:8], twos complement				0x00	
0x340	DDC 1 phase LSB	DDC 1 NCO phase value, Bits[7:0], twos complement								0x00	
0x341	DDC 1 phase MSB	X	X	X	X	DDC 1 NCO phase value, Bits[11:8], twos complement				0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch B	0	I output test mode enable 0 = disabled 1 = enabled from Ch A	0x00	
Digital Outputs and Test Modes											
0x550	ADC test modes (local)	User pattern selection 0 = continuous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off, normal operation 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checker board 0101 = PN sequence, long 0110 = PN sequence, short 0111 = 1/0 word toggle 1000 = the user pattern test mode (used with Register 0x550, Bit 7 and user pattern (1, 2, 3, 4) registers), 1111 = ramp output				0x00	
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x559	Output Mode Control 1	0	Converter control Bit 1 selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 101 = SYSREF± Only used when CS (Register 0x58F) = 2 or 3			0	Converter control Bit 0 selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 101 = SYSREF± Only used when CS (Register 0x58F) = 3			0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x55A	Output Mode Control 2	0	0	0	0	0	Converter control Bit 2 selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 101 = SYSREF Used when CS (Register 0x58F) = 1, 2, or 3			0x00	
0x561	Output mode	0	0	0	0	0	Sample invert 0 = normal 1 = sample invert	Data format select 00 = offset binary 01 = twos complement		0x01	
0x562	Output overrange (OR) clear	Virtual Converter 7 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 6 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Con-verter 5 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Con-verter 4 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Con-verter 3 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Con-verter 2 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Con-verter 1 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Con-verter 0 OR 0 = OR bit enabled 1 = OR bit cleared	0x00	
0x563	Output OR status	Virtual Con-verter 7 OR 0 = no OR 1 = OR occured	Virtual Con-verter 6 OR 0 = no OR 1 = OR occured	Virtual Con-verter 5 OR 0 = no OR 1 = OR occured	Virtual Converter 4 OR 0 = no OR 1 = OR occured	Virtual Converter 3 OR 0 = no OR 1 = OR occured	Virtual Con-verter 2 OR 0 = no OR 1 = OR occured	Virtual Con-verter 1 OR 0 = no OR 1 = OR occured	Virtual Con-verter 0 OR 0 = no OR 1 = OR occured	0x00	Read only
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	
0x56E	JESD204B lane rate control	0	0	0	0 = serial lane rate ≥ 6.25 Gbps and ≤12.5 Gbps 1 = serial lane rate must be ≥ 3.125 Gbps and ≤ 6.25 Gbps	0	0	0	0	0x00	
0x570	JESD204B quick config-uration	JESD204B quick configuration L = number of lanes = $2^{\text{Register 0x570, Bits[7:6]}}$ M = number of converters = $2^{\text{Register 0x570, Bits[5:3]}}$ F = number of octets/frame = $2^{\text{Register 0x570, Bits[2:0]}}$								0x88	Refer to Table 12 and Table 13
0x571	JESD204B Link Mode Control 1	Standby mode 0 = all converter outputs 0 1 = CGS (/K28.5/)	Tail bit (t) PN 0 = disable 1 = enable T = N′ – N – CS	Long transport layer test 0 = disable 1 = enable	Lane synchron-ization 0 = disable FACI uses /K28.7/ 1 = enable FACI uses /K28.3/ and /K28.7/	ILAS sequence mode 00 = ILAS disabled 01 = ILAS enabled 11 = ILAS always on test mode		FACI 0 = enabled 1 = disabled	Link control 0 = active 1 = power down	0x14	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x572	JESD204B Link Mode Control 2	SYNCINB± pin control 00 = normal 10 = ignore SYNCINB± (force CGS) 11 = ignore SYNCINB± (force ILAS/user data)		SYNC-INB± pin invert 0 = active low 1 = active high	SYNCINB± pin type 0 = differential 1 = cmos	0	8B/10B bypass 0 = normal 1 = bypass	8B/10B bit invert 0 = normal 1 = invert the a…j symbols	0	0x00	
0x573	JESD204B Link Mode Control 3	CHKSUM mode 00 = sum of all 8-bit link config registers 01 = sum of individual link config fields 10 = checksum set to zero		Test injection point 00 = N′ sample input 01 = 10-bit data at 8B/10B output (for PHY testing) 10 = 8-bit data at scrambler input		JESD204B test mode patterns 0000 = normal operation (test mode disabled) 0001 = alternating checker board 0010 = 1/0 word toggle 0011 = 31-bit PN sequence—$X^{31} + X^{28} + 1$ 0100 = 23-bit PN sequence—$X^{23} + X^{18} + 1$ 0101 = 15-bit PN sequence—$X^{15} + X^{14} + 1$ 0110 = 9-bit PN sequence—$X^{9} + X^{5} + 1$ 0111 = 7-bit PN sequence—$X^{7} + X^{6} + 1$ 1000 = ramp output 1110 = continuous/repeat user test 1111 = single user test				0x00	
0x574	JESD204B Link Mode Control 4	ILAS delay 0000 = transmit ILAS on first LMFC after SYNCINB± deasserted 0001 = transmit ILAS on second LMFC after SYNCINB± deasserted … 1111 = transmit ILAS on 16th LMFC after SYNCINB± deasserted				0	Link layer test mode 000 = normal operation (link layer test mode disabled) 001 = continuous sequence of /D21.5/ characters 100 = modified RPAT test sequence 101 = JSPAT test sequence 110 = JTSPAT test sequence			0x00	
0x578	JESD204B LMFC offset	0	0	0	LMFC phase offset value, Bits[4:0]					0x00	
0x580	JESD204B DID config	JESD204B Tx DID value, Bits[7:0]								0x00	
0x581	JESD204B BID config	0	0	0	0	JESD204B Tx BID value, Bits[7:0]				0x00	
0x583	JESD204B LID Config 1	0	0	0	Lane 0 LID value, Bits[4:0]					0x00	
0x585	JESD204B LID Config 2	0	0	0	Lane 1 LID value, Bits[4:0]					0x02	
0x587	JESD204B LID Config 3	0	0	0	Lane 2 LID value, Bits[4:0]					0x04	
0x589	JESD204B LID Config 4	0	0	0	Lane 3 LID value, Bits[4:0]					0x06	
0x58B	JESD204B parameters SCR/L	JESD204B scrambling (SCR) 0 = disabled 1 = enabled	0	0	0	0	0	JESD204B lanes (L) 00 = 1 lane 01 = 2 lanes 11 = 4 lanes Read only, see Register 0x570		0x8X	
0x58C	JESD204B F config	Number of octets per frame, F = Register 0x58C, Bits[7:0] + 1								0x88	Read only, see Reg. 0x570
0x58D	JESD204B K config	0	0	0	Number of frames per multiframe, K = Register 0x58D, Bits[4:0] + 1 Only values where (F × K) mod 4 = 0 are supported					0x1F	See Reg. 0x570
0x58E	JESD204B M config	Number of converters per link, Bits[7:0] 0x00 = link connected to one virtual converter (M = 1) 0x01 = link connected to two virtual converters (M = 2) 0x03 = link connected to four virtual converters (M = 4) 0x07 = link connected to eight virtual converters (M = 8)									Read only

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x58F	JESD204B CS/N config	Number of control bits (CS) per sample 00 = no control bits (CS = 0) 01 = 1 control bit (CS = 1); Control Bit 2 only 10 = 2 control bits (CS = 2); Control Bit 2 and Control Bit 1 only 11 = 3 control bits (CS = 3); all control bits (2, 1, 0)		0	ADC converter resolution (N) 0x06 = 7-bit resolution 0x07 = 8-bit resolution 0x08 = 9-bit resolution 0x09 = 10-bit resolution 0x0A = 11-bit resolution 0x0B = 12-bit resolution (default) 0x0C = 13-bit resolution 0x0D = 14-bit resolution 0x0E = 15-bit resolution 0x0F = 16-bit resolution						
0x0590	JESD204B N′ config	Subclass support (Subclass version) 000 = Subclass 0 (no deterministic latency) 001 = Subclass 1			ADC number of bits per sample (N′) 0x7 = 8 bits 0xF = 16 bits					0x2F	
0x591	JESD204B S config	0	0	1	Samples per converter frame cycle (S) S value = Register 0x591[4:0] +1						Read only
0x592	JESD204B HD and CF configuration	HD value 0 = disabled 1 = enabled	0	0	Control words per frame clock cycle per link (CF) CF value = Register 0x592, Bits[4:0]					0x80	Read only
0x5A0	JESD204B CHKSUM 0	CHKSUM value for SERDOUT0±, Bits[7:0]								0xC3	Read only
0x5A2	JESD204B CHKSUM 1	CHKSUM value for SERDOUT1±, Bits[7:0]								0xC5	Read only
0x5A4	JESD204B CHKSUM 2	CHKSUM value for SERDOUT2±, Bits[7:0]								0xC7	Read only
0x5A6	JESD204B CHKSUM 3	CHKSUM value for SERDOUT3±, Bits[7:0]								0xC9	Read only
0x5B0	JESD204B lane power-down	1	SERD-OUT3± 0 = on 1 = off	1	SERD-OUT2± 0 = on 1 = off	1	SERD-OUT1± 0 = on 1 = off	1	SERDOUT0± 0 = on 1 = off	0xAA	
0x5B2	JESD204B lane SERDOUT0± assign	X	X	X	X	0	SERDOUT0± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x00	
0x5B3	JESD204B lane SERDOUT1± assign	X	X	X	X	0	SERDOUT1± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x11	
0x5B5	JESD204B lane SERDOUT2± assign	X	X	X	X	0	SERDOUT2± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x22	
0x5B6	JESD204B lane SERDOUT3± assign	X	X	X	X	0	SERDOUT3± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x33	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x5BF	JESD serializer drive adjust	0	0	0	0	Swing voltage 0000 = 237.5 mV 0001 = 250 mV 0010 = 262.5 mV 0011 = 275 mV 0100 = 287.5 mV 0101 = 300 mV (default) 0110 = 312.5 mV 0111 = 325 mV 1000 = 337.5 mV 1001 = 350 mV 1010 = 362.5 mV 1011 = 375 mV 1100 = 387.5 mV 1101 = 400 mV 1110 = 412.5 mV 1111 = 425 mV				0x05	
0x5C1	De-emphasis select	0	SERD-OUT3± 0 = disable 1 = enable	0	SERD-OUT2± 0 = disable 1 = enable	0	SERD-OUT1± 0 = disable 1 = enable	0	SERDOUT0± 0 = disable 1 = enable	0x00	
0x5C2	De-emphasis setting for SERDOUT0±	0	0	0	0	SERDOUT0± de-emphasis settings: 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C3	De-emphasis setting for SERDOUT1±	0	0	0	0	SERDOUT1± de-emphasis settings: 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C4	De-emphasis setting for SERDOUT2±	0	0	0	0	SERDOUT2± de-emphasis settings: 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C5	De-emphasis setting for SERDOUT3±	0	0	0	0	SERDOUT3± de-emphasis settings: 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD9234 must be powered by the following seven supplies: AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, and SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP2164 and ADP2370 switching regulators be used to convert the 3.3 V, 5.0 V, or 12 V input rails to an intermediate rail (1.8 V and 3.8 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1741, ADP170, and ADP125). Figure 81 shows the recommended power supply scheme for AD9234.

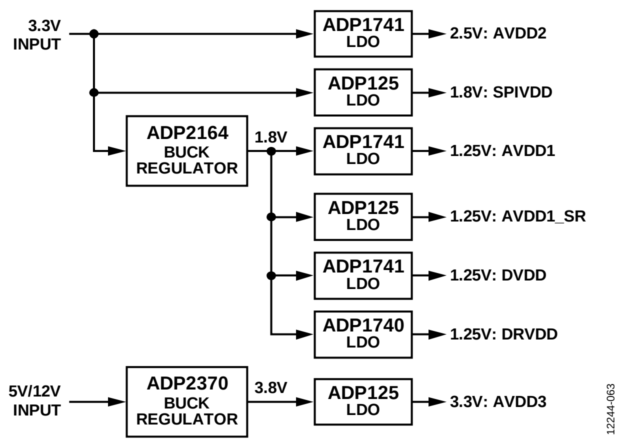


Figure 81. High Efficiency, Low Noise Power Solution for the AD9234

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 81 provides the lowest noise, highest efficiency power delivery system for the AD9234. If only one 1.25 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1_SR, SPIVDD, DVDD, and DRVDD, in that order. The user can employ several different decoupling capacitors to cover both high and low frequencies. These must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to ground to achieve the best electrical and thermal performance of the AD9234. Connect an exposed continuous copper plane on the PCB to the AD9234 exposed pad, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias must be solder filled or plugged. The number of vias and the fill determine the resultant θ_{JA} measured on the board. This is shown in Table 7.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 82 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

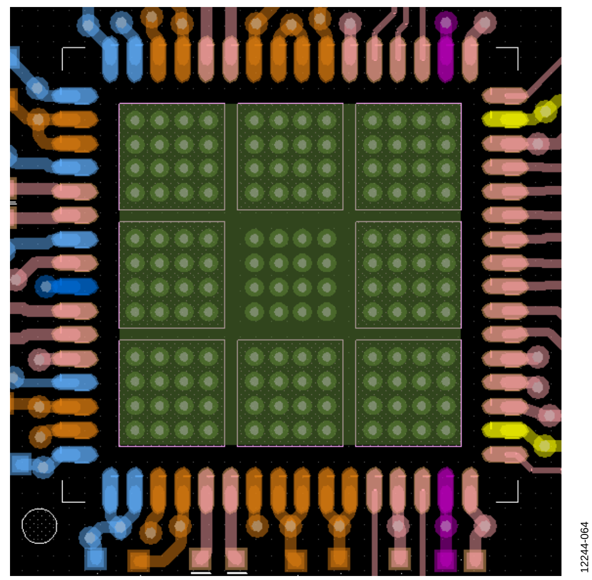


Figure 82. Recommended PCB Layout of Exposed Pad for the AD9234

AVDD1_SR (PIN 57) AND AGND (PIN 56 AND PIN 60)

AVDD1_SR (Pin 57) and AGND (Pin 56 and Pin 60) can be used to provide a separate power supply node to the SYSREF± circuits of AD9234. If running in Subclass 1, the AD9234 can support periodic one-shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is needed.

OUTLINE DIMENSIONS

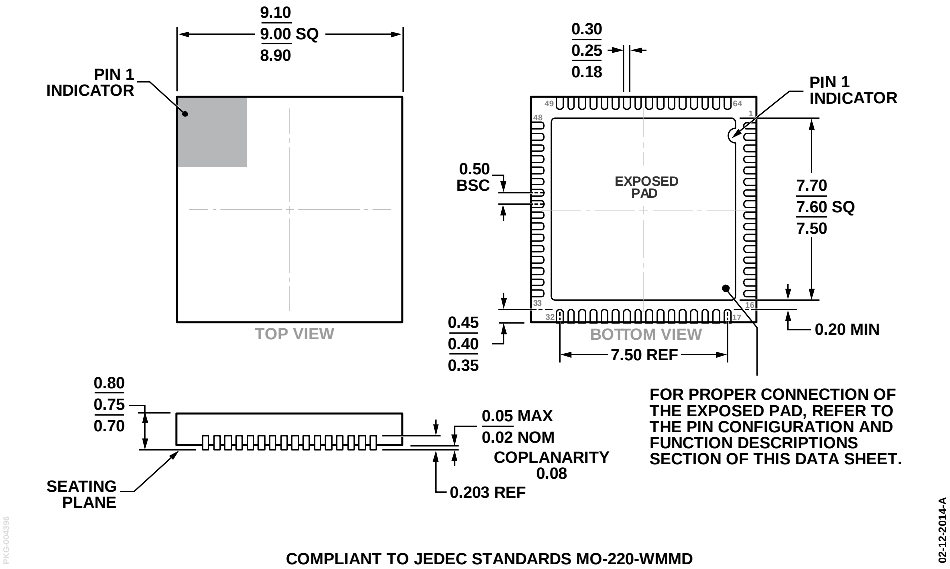


Figure 83. 64-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9234BCPZ-1000	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-64-15
AD9234BCPZRL7-1000	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-64-15
AD9234-1000EBZ		Evaluation Board for AD9234-1000	

[1] Z = RoHS Compliant Part.