ANALOG DEVICES

Quad, 16-Bit, 2.8 GSPS, TxDAC+® Digital-to-Analog Converter

Data Sheet **AD9144**

FEATURES

Supports input data rate >1 GSPS
Proprietary low spurious and distortion design
- **6-carrier GSM IMD = 77 dBc at 75 MHz IF**
- **SFDR = 82 dBc at dc IF, −9 dBFS**
- **Flexible 8-lane JESD204B interface**
- **Support quad or dual DAC mode at 2.8 GSPS**

Multiple chip synchronization
- **Fixed latency**
- **Data generator latency compensation**

Selectable 1×, 2×, 4×, 8× interpolation filter
- **Low power architecture**

Input signal power detection
- **Emergency stop for downstream analog circuitry protection**

Transmit enable function allows extra power saving
High performance, low noise phase-locked loop (PLL) clock multiplier
Digital inverse sinc filter
Low power: 1.6 W at 1.6 GSPS, 1.7 W at 2.0 GSPS, full operating conditions
88-lead LFCSP with exposed pad

APPLICATIONS

Wireless communications
- **3G/4G W-CDMA base stations**
- **Wideband repeaters**
- **Software defined radios**

Wideband communications
- **Point-to-point**
- **Local multipoint distribution service (LMDS) and multichannel multipoint distribution service (MMDS)**

Transmit diversity, multiple input/multiple output (MIMO)
Instrumentation
Automated test equipment

GENERAL DESCRIPTION

The AD9144 is a quad, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a maximum sample rate of 2.8 GSPS, permitting a multicarrier generation up to the Nyquist frequency. The DAC outputs are optimized to interface seamlessly with the ADRF672x analog quadrature modulators (AQMs) from Analog Devices, Inc. An optional 3-wire or 4-wire serial port interface (SPI) provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a typical range of 13.9 mA to 27.0 mA. The AD9144 is available in an 88-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

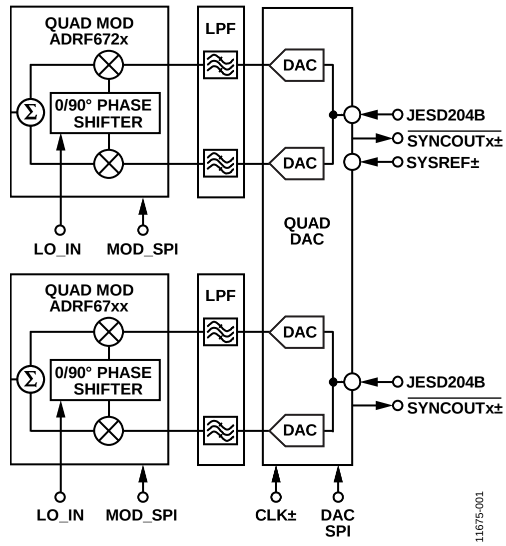


Figure 1.

PRODUCT HIGHLIGHTS

1. Greater than 1 GHz, ultrawide complex signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization in software and hardware design.
4. Fewer pins for data interface width with a serializer/deserializer (SERDES) JESD204B eight-lane interface.
5. Programmable transmit enable function allows easy design balance between power consumption and wake-up time.
6. Small package size with 12 mm × 12 mm footprint.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

7/14—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

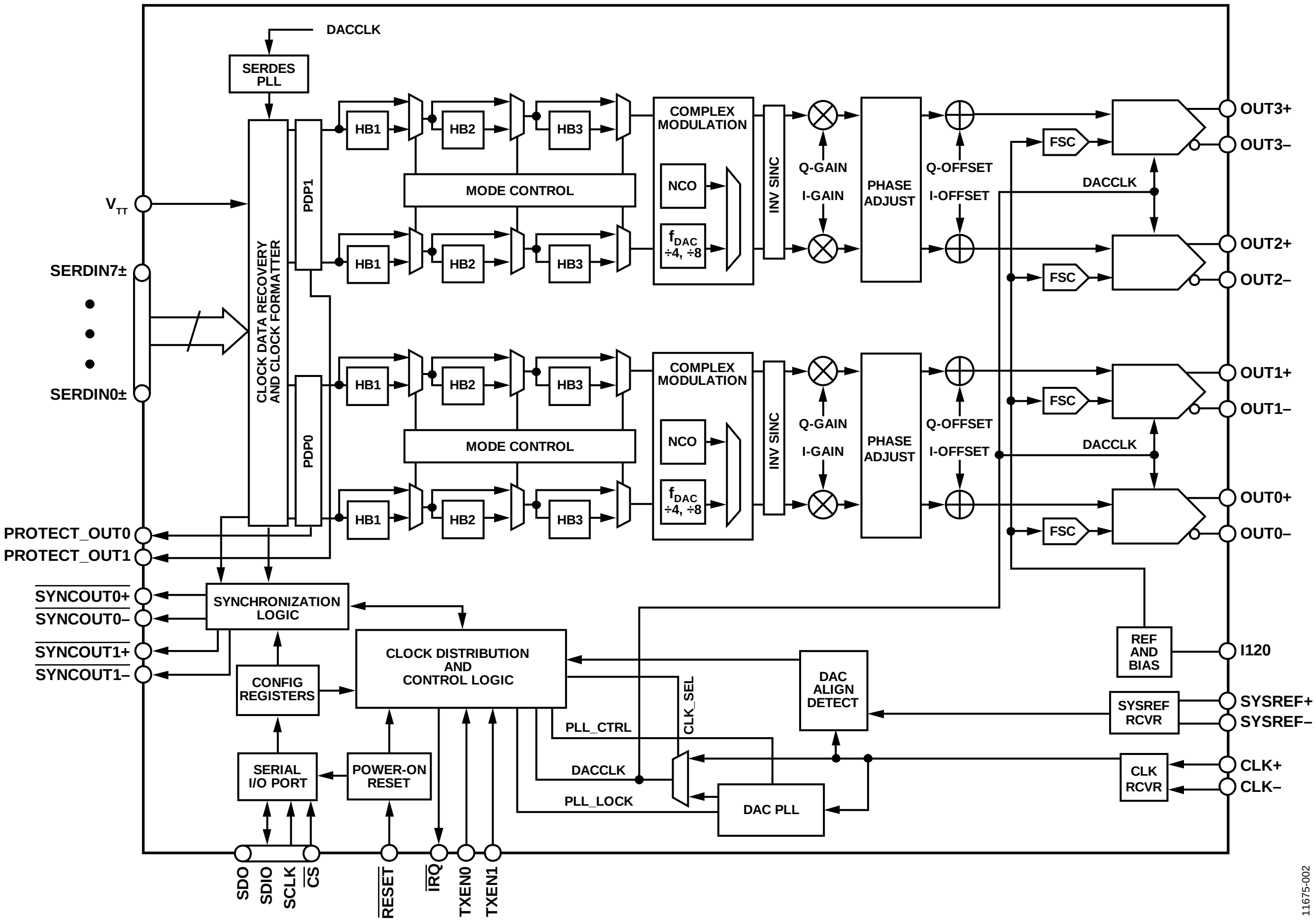


Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY	With calibration				
Differential Nonlinearity (DNL)			±1.0		LSB
Integral Nonlinearity (INL)			±2.0		LSB
MAIN DAC OUTPUTS					
Gain Error	With internal reference	−2.5	+2	+5.5	% FSR
I/Q Gain Mismatch		−0.6		+0.6	% FSR
Full-Scale Output Current	Based on a 4 kΩ external resistor between I120 and GND				
Maximum Setting		25.5	27.0	28.6	mA
Minimum Setting		13.1	13.9	14.8	mA
Output Compliance Range		−250		+750	mV
Output Resistance			0.2		MΩ
Output Capacitance			3.0		pF
Gain DAC Monotonicity			Guaranteed		
Settling Time	To within ±0.5 LSB		20		ns
MAIN DAC TEMPERATURE DRIFT					
Offset			0.04		ppm/°C
Gain			32		ppm/°C
Reference Voltage			16		ppm/°C
REFERENCE					
Internal Reference Voltage			1.2		V
ANALOG SUPPLY VOLTAGES					
AVDD33		3.13	3.3	3.47	V
PVDD12		1.14	1.2	1.26	V
CVDD12		1.14	1.2	1.26	V
DIGITAL SUPPLY VOLTAGES					
SIOVDD33		3.13	3.3	3.47	V
V_{TT}		1.1	1.2	1.37	V
DVDD12					
		1.14	1.2	1.26	V
		1.274	1.3	1.326	V
SVDD12					
		1.14	1.2	1.26	V
		1.274	1.3	1.326	V
IOVDD		1.71	1.8	3.47	V
POWER CONSUMPTION					
4× Interpolation Mode, JESD Mode 4, 8 SERDES Lanes	f_{DAC} = 1.6 GSPS, IF = 40 MHz, NCO off, PLL on, digital gain on, inverse sinc on, DAC FSC = 20 mA		1.59	1.84	W
AVDD33			126	134	mA
PVDD12			95.3	112.4	mA
CVDD12			101	111	mA
SVDD12	Includes V_{TT}		518.2	654	mA
DVDD12			234	255	mA
SIOVDD33			11	12	mA
IOVDD			36	50	µA

DIGITAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input Voltage (V_{IN}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
CMOS OUTPUT LOGIC LEVEL						
Output Voltage (V_{OUT}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
MAXIMUM DAC UPDATE RATE[1]						
		1× interpolation[2] (see Table 4)	1060			MSPS
		2× interpolation[3]	2120			MSPS
		4× interpolation	2800			MSPS
		8× interpolation	2800			MSPS
ADJUSTED DAC UPDATE RATE						
		1× interpolation	1060			MSPS
		2× interpolation	1060			MSPS
		4× interpolation	700			MSPS
		8× interpolation	350			MSPS
INTERFACE[4]						
Number of JESD204B Lanes				8		Lanes
JESD204B Serial Interface Speed						
Minimum		Per lane			1.42	Gbps
Maximum		Per lane, SVDD12 = 1.3 V ± 2%	10.6			Gbps
DAC CLOCK INPUT (CLK+, CLK−)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Maximum Clock Rate			2800			MHz
REFCLK Frequency (PLL Mode)		6.0 GHz ≤ f_{VCO} ≤ 12.0 GHz	35		1000	MHz
SYSTEM REFERENCE INPUT (SYSREF+, SYSREF−)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage			0		2000	mV
SYSREF± Frequency[5]					f_{DATA}/(K × (F/S))	Hz
SYSREF TO DAC CLOCK[6]		SYSREF differential swing = 0.4 V, slew rate = 1.3 V/ns, common modes tested: ac-coupled, 0 V, 0.6 V, 1.25 V, 2.0 V				
Setup Time	t_{SSD}		131			ps
Hold Time	t_{HSD}		119			ps
Keep Out Window	KOW			20		ps
SPI						
Maximum Clock Rate	SCLK	IOVDD = 1.8 V	10			MHz
Minimum SCLK Pulse Width						
High	t_{PWH}				8	ns
Low	t_{PWL}				12	ns
SDIO to SCLK						
Setup Time	t_{DS}		5			ns
Hold Time	t_{DH}		2			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SDO to SCLK						
Data Valid Window	t_{DV}		25			ns
$\overline{CS}$ to SCLK						
Setup Time	t_{SCSB}		5			ns
Hold Time	t_{HCSB}		2			ns

[1] See Table 3 for detailed specifications for DAC update rate conditions.
[2] Maximum speed for 1× interpolation is limited by the JESD interface. See Table 4 for details.
[3] Maximum speed for 2× interpolation is limited by the JESD interface. See Table 4 for details.
[4] See Table 4 for detailed specifications for JESD speed conditions.
[5] K, F, and S are JESD204B transport layer parameters. See Table 42 for the full definitions.
[6] See Table 5 for detailed specifications for SYSREF to DAC clock timing conditions.

MAXIMUM DAC UPDATE RATE SPEED SPECIFICATIONS BY SUPPLY

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE	DVDD12, CVDD12 = 1.2 V ± 5%	2.23			GSPS
	DVDD12, CVDD12 = 1.2 V ± 2%	2.41			GSPS
	DVDD12, CVDD12 = 1.3 V ± 2%	2.80			GSPS

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HALF RATE	SVDD12 = 1.2 V ± 5%	5.65		8.92	Gbps
	SVDD12 = 1.2 V ±2%	5.65		9.42	Gbps
	SVDD12 = 1.3 V ± 2%	5.65		10.64	Gbps
FULL RATE	SVDD12 = 1.2 V ± 5%	2.83		4.63	Gbps
	SVDD12 = 1.2 V ±2%	2.83		4.93	Gbps
	SVDD12 = 1.3 V ± 2%	2.83		5.52	Gbps
OVERSAMPLING	SVDD12 = 1.2 V ± 5%	1.42		2.31	Gbps
	SVDD12 = 1.2 V ±2%	1.42		2.46	Gbps
	SVDD12 = 1.3 V ± 2%	1.42		2.76	Gbps

SYSREF TO DAC CLOCK TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, SYSREF± common-mode voltages = 0.0 V, 0.6 V, 1.25 V, and 2.0 V, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Unit
SYSREF DIFFERENTIAL SWING = 0.4 V, SLEW RATE = 1.3 V/ns			
Setup Time	AC-coupled	126	ps
	DC-coupled	131	ps
Hold Time	AC-coupled	92	ps
	DC-coupled	119	ps
SYSREF DIFFERENTIAL SWING = 0.7 V, SLEW RATE = 2.28 V/ns			
Setup Time	AC-coupled	96	ps
	DC-coupled	104	ps
Hold Time	AC-coupled	77	ps
	DC-coupled	95	ps

Parameter	Test Conditions/Comments	Min	Unit
SYSREF SWING = 1.0 V, SLEW RATE = 3.26 V/ns			
Setup Time	AC-coupled	83	ps
	DC-coupled	90	ps
Hold Time	AC-coupled	68	ps
	DC-coupled	84	ps

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY					
Interface			17		PClock[1] cycles
Interpolation	With or without modulation				
1×			58		DAC clock cycles
2×			137		DAC clock cycles
4×			251		DAC clock cycles
8×			484		DAC clock cycles
Inverse Sinc			17		DAC clock cycles
Fine Modulation			20		DAC clock cycles
Coarse Modulation					
$f_S/8$			8		DAC clock cycles
$f_S/4$			4		DAC clock cycles
Digital Phase Adjust			12		DAC clock cycles
Digital Gain Adjust			12		DAC clock cycles
Power-Up Time					
Dual A Only	Register 0x011 from 0x60 to 0x00		60		µs
Dual B Only	Register 0x011 from 0x18 to 0x00		60		µs
All DACs	Register 0x011 from 0x7C to 0x00		60		µs

[1] PClock is the AD9144 internal processing clock and equals the lane rate ÷ 40.

LATENCY VARIATION SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC LATENCY VARIATION					
SYNC Off					
Subclass 0 Mode	−4		+4	DACCLK cycles	Given proper calibration of local multiframe clock (LMFC) delay
SYNC On					
PLL Off		0	1	DACCLK cycles	
PLL On	−1		+1	DACCLK cycles	

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		94		714	ps
Common-Mode Voltage	V_{RCM}	AC-coupled	−0.05		+1.85	V
		V_{TT} = SVDD12[1]				
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
DIFFERENTIAL OUTPUTS ($\overline{\text{SYNCOUT}}$±)[2]						
Output Differential Voltage	V_{OD}	Normal swing mode: Register 0x2A5[0] = 0	192		235	mV
Output Offset Voltage	V_{OS}		1.19		1.27	V
Output Differential Voltage	V_{OD}	High swing mode: Register 0x2A5[0] = 1	341		394	mV
DETERMINISTIC LATENCY						
Fixed					17	PClock[3] cycles
Variable					2	PClock[3] cycles
SYSREF±-to-LMFC DELAY				4		DAC clock cycles

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.
[3] PClock is the AD9144 internal processing clock and equals the lane rate ÷ 40.

AC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V,[1] V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−9 dBFS single tone				
f_{DAC} = 983.04 MSPS	f_{OUT} = 20 MHz		82		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		76		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		81		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 170 MHz		69		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	−9 dBFS				
f_{DAC} =983.04 MSPS	f_{OUT} = 20 MHz		90		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		82		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		90		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 170 MHz		81		dBc
NOISE SPECTRAL DENSITY (NSD), SINGLE TONE	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		−162		dBm/Hz
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		−163		dBm/Hz
W-CDMA FIRST ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		82		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		80		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		80		dBc
W-CDMA SECOND ACLR, SINGLE CARRIER	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		84		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		85		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		85		dBc

[1] SVDD12 = 1.3 V for all f_{DAC} = 1966.08 MSPS conditions in Table 9.

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
I120 to Ground	−0.3 V to AVDD33 + 0.3 V
SERDINx±, V_{TT}, $\overline{\text{SYNCOUT1}}$±/ $\overline{\text{SYNCOUT0}}$±, TXENx	−0.3 V to SIOVDD33 + 0.3 V
OUTx±	−0.3 V to AVDD33 + 0.3 V
SYSREF±	GND − 0.5 V to +2.5 V
CLK± to Ground	−0.3 V to PVDD12 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO, PROTECT_OUTx to Ground	−0.3 V to IOVDD + 0.3 V
LDO_BYP1	−0.3 V to SVDD12 + 0.3 V
LDO_BYP2	−0.3 V to PVDD12 + 0.3 V
LDO24	−0.3 V to AVDD33 + 0.3 V
Ambient Operating Temperature (T_A)	−40°C to +85°C
Junction Temperature	125°C
Storage Temperature	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane for the 88-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JB} is obtained following double-ring cold plate test conditions (JESD51-8). θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P), \text{ or}$$

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.

Table 11. Thermal Resistance

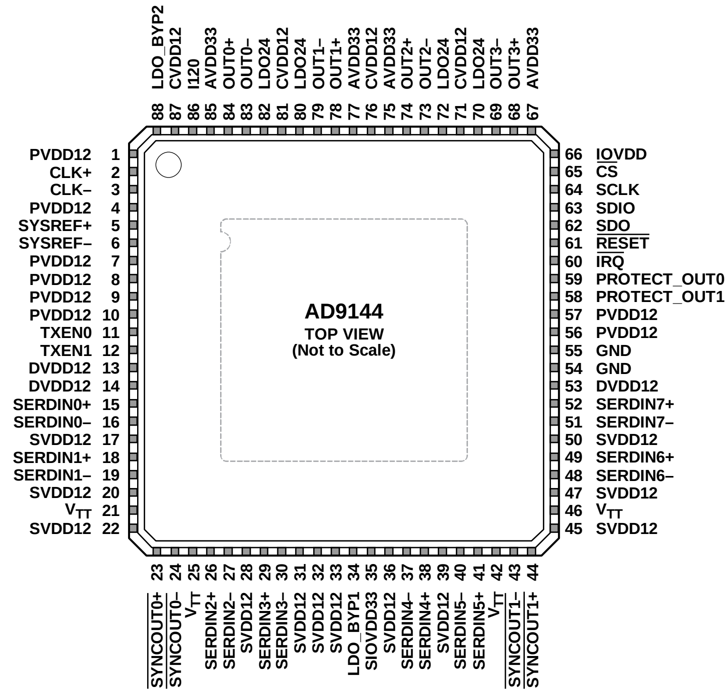
Package	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
88-Lead LFCSP[1]	22.6	5.59	1.17	0.1	5.22	°C/W

[1] The exposed pad must be securely connected to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE SECURELY CONNECTED TO THE GROUND PLANE.

Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
2	CLK+	PLL Reference/Clock Input, Positive. When the PLL is used, this is the positive reference clock input. When the PLL is not used, this is the positive device clock input. This pin is self biased and must be ac-coupled.
3	CLK–	PLL Reference/Clock Input, Negative. When the PLL is used, this is the negative reference clock input. When the PLL is not used, this is the negative device clock input. This pin is self biased and must be ac-coupled.
4	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
5	SYSREF+	Positive Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. It may be ac-coupled or dc-coupled.
6	SYSREF–	Negative Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. It may be ac-coupled or dc-coupled.
7	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
8	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
9	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
10	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
11	TXEN0	Transmit Enable for DAC0 and DAC1. The CMOS levels are determined with respect to IOVDD.
12	TXEN1	Transmit Enable for DAC2 and DAC3. The CMOS levels are determined with respect to IOVDD.
13	DVDD12	1.2 V Digital Supply.
14	DVDD12	1.2 V Digital Supply.
15	SERDIN0+	Serial Channel Input 0, Positive. CML compliant. SERDIN0+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
16	SERDIN0–	Serial Channel Input 0, Negative. CML compliant. SERDIN0– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
17	SVDD12	1.2 V JESD204B Receiver Supply.
18	SERDIN1+	Serial Channel Input 1, Positive. CML compliant. SERDIN1+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
19	SERDIN1–	Serial Channel Input 1, Negative. CML compliant. SERDIN1– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.

Pin No.	Mnemonic	Description
20	SVDD12	1.2 V JESD204B Receiver Supply.
21	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
22	SVDD12	1.2 V JESD204B Receiver Supply.
23	$\overline{\text{SYNCOUT0+}}$	Positive LVDS Sync (Active Low) Output Signal Channel Link 0.
24	$\overline{\text{SYNCOUT0−}}$	Negative LVDS Sync (Active Low) Output Signal Channel Link 0.
25	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
26	SERDIN2+	Serial Channel Input 2, Positive. CML compliant. SERDIN2+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
27	SERDIN2−	Serial Channel Input 2, Negative. CML compliant. SERDIN2− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
28	SVDD12	1.2 V JESD204B Receiver Supply.
29	SERDIN3+	Serial Channel Input 3, Positive. CML compliant. SERDIN3+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
30	SERDIN3−	Serial Channel Input 3, Negative. CML compliant. SERDIN3− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
31	SVDD12	1.2 V JESD204B Receiver Supply.
32	SVDD12	1.2 V JESD204B Receiver Supply.
33	SVDD12	1.2 V JESD204B Receiver Supply.
34	LDO_BYP1	LDO SERDES Bypass. This pin requires a 1 Ω resistor in series with a 1 μF capacitor to ground.
35	SIOVDD33	3.3 V Supply for SERDES.
36	SVDD12	1.2 V JESD204B Receiver Supply.
37	SERDIN4−	Serial Channel Input 4, Negative. CML compliant. SERDIN4− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
38	SERDIN4+	Serial Channel Input 4, Positive. CML compliant. SERDIN4+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
39	SVDD12	1.2 V JESD204B Receiver Supply.
40	SERDIN5−	Serial Channel Input 5, Negative. CML compliant. SERDIN5− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
41	SERDIN5+	Serial Channel Input 5, Positive. CML compliant. SERDIN5+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
42	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
43	$\overline{\text{SYNCOUT1−}}$	Negative LVDS Sync (Active Low) Output Signal Channel Link 1.
44	$\overline{\text{SYNCOUT1+}}$	Positive LVDS Sync (Active Low) Output Signal Channel Link 1.
45	SVDD12	1.2 V JESD204B Receiver Supply.
46	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
47	SVDD12	1.2 V JESD204B Receiver Supply.
48	SERDIN6−	Serial Channel Input 6, Negative. CML compliant. SERDIN6− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
49	SERDIN6+	Serial Channel Input 6, Positive. CML compliant. SERDIN6+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
50	SVDD12	1.2 V JESD204B Receiver Supply.
51	SERDIN7−	Serial Channel Input 7, Negative. CML compliant. SERDIN7− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
52	SERDIN7+	Serial Channel Input 7, Positive. CML compliant. SERDIN7+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
53	DVDD12	1.2 V Digital Supply.
54	GND	Ground. Connect GND to the ground plane.
55	GND	Ground. Connect GND to the ground plane.
56	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
57	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
58	PROTECT_OUT1	Power Detection Protection Pin Output for DAC2 and DAC3. Pin 58 is high when power protection is in process.
59	PROTECT_OUT0	Power Detection Protection Pin Output for DAC0 and DAC1. Pin 59 is high when power protection is in process.
60	$\overline{\text{IRQ}}$	Interrupt Request (Active Low, Open Drain).

Pin No.	Mnemonic	Description
61	$\overline{\text{RESET}}$	Reset. This pin is active low. CMOS levels are determined with respect to IOVDD.
62	SDO	Serial Port Data Output. CMOS levels are determined with respect to IOVDD.
63	SDIO	Serial Port Data Input/Output. CMOS levels are determined with respect to IOVDD.
64	SCLK	Serial Port Clock Input. CMOS levels are determined with respect to IOVDD.
65	$\overline{\text{CS}}$	Serial Port Chip Select. This pin is active low; CMOS levels are determined with respect to IOVDD.
66	IOVDD	IOVDD Supply for CMOS Input/Output and SPI. Operational for 1.8 V ≤ IOVDD ≤ 3.3 V.
67	AVDD33	3.3 V Analog Supply for DAC Cores.
68	OUT3+	DAC3 Positive Current Output.
69	OUT3−	DAC3 Negative Current Output.
70	LDO24	2.4 V LDO. Requires a 1 μF capacitor to ground.
71	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 71.
72	LDO24	2.4 V LDO. Requires a 1 μF capacitor to ground.
73	OUT2−	DAC2 Negative Current Output.
74	OUT2+	DAC2 Positive Current Output.
75	AVDD33	3.3 V Analog Supply for DAC Cores.
76	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 76.
77	AVDD33	3.3 V Analog Supply for DAC Cores.
78	OUT1+	DAC1 Positive Current Output.
79	OUT1−	DAC1 Negative Current Output.
80	LDO24	2.4 V LDO. Requires a 1 μF capacitor to ground.
81	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 81.
82	LDO24	2.4 V LDO. Requires a 1 μF capacitor to ground.
83	OUT0−	DAC0 Negative Current Output.
84	OUT0+	DAC0 Positive Current Output.
85	AVDD33	3.3 V Analog Supply for DAC Cores.
86	I120	Output Current Generation Pin for DAC Full-Scale Current. Tie a 4 kΩ resistor from the I120 pin to ground.
87	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 87.
88	LDO_BYP2	LDO Clock Bypass for DAC PLL. This pin requires a 1 Ω resistor in series with a 1 μF capacitor to ground.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

TERMINOLOGY

Integral Nonlinearity (INL)

INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error

Offset error is the deviation of the output current from the ideal of 0 mA. For OUTx+, 0 mA output is expected when all inputs are set to 0. For OUTx−, 0 mA output is expected when all inputs are set to 1.

Gain Error

Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range

The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)

PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter

If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)

ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection

In a traditional two part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Adjusted DAC Update Rate

The adjusted DAC update rate is defined as the DAC update rate divided by the smallest interpolating factor. For clarity on DACs with multiple interpolating factors, the adjusted DAC update rate for each interpolating factor may be given.

Physical Lane

Physical Lane x refers to SERDINx±.

Logical Lane

Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane

Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300[2] = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300[2] = 1, dual link only), Link Lane x = Logical Lane x + 4.

TYPICAL PERFORMANCE CHARACTERISTICS

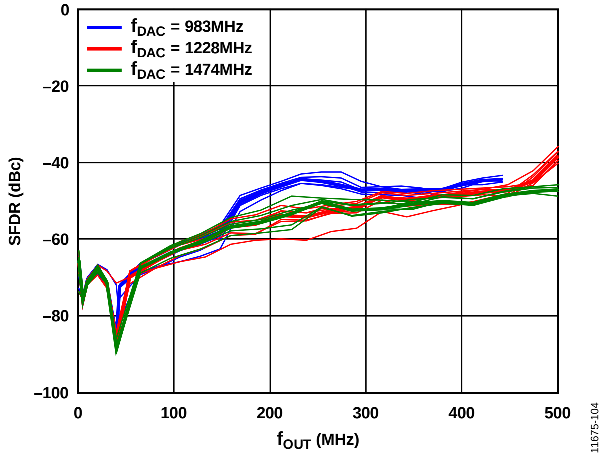


Figure 4. Single Tone SFDR vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

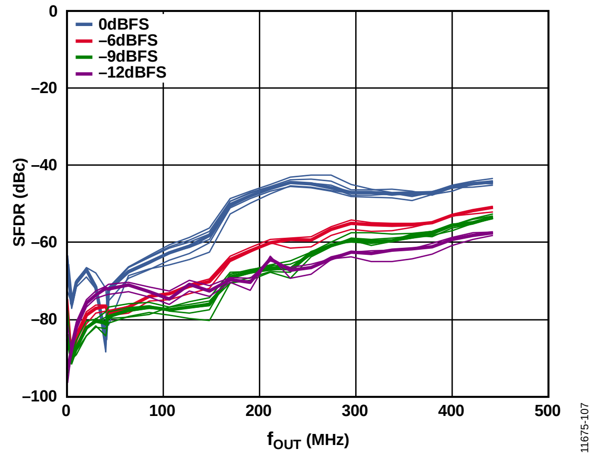


Figure 7. Single Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 983 MHz

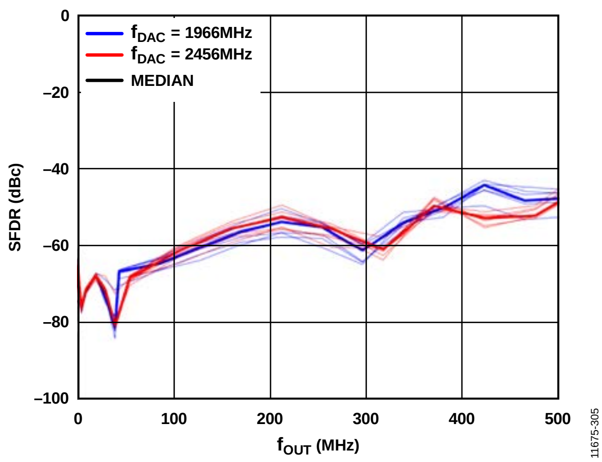


Figure 5. Single Tone SFDR vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 1966 MHz and 2456 MHz

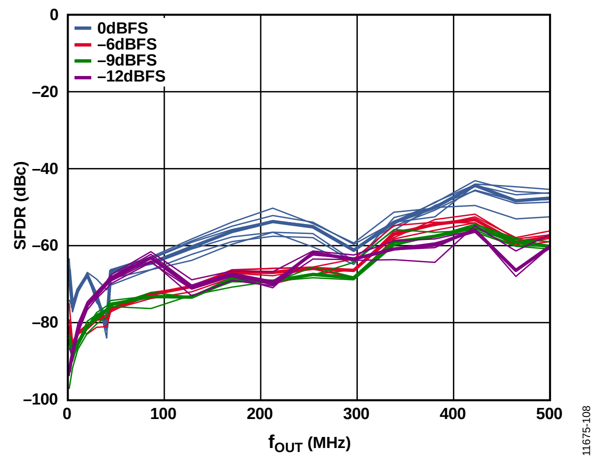


Figure 8. Single Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966 MHz

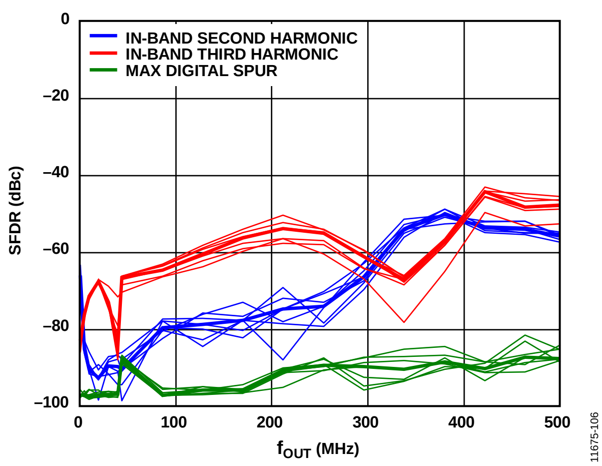


Figure 6. Single Tone Second and Third Harmonics and Maximum Digital Spur in the First Nyquist Zone, f_{DAC} = 1966 MHz, 0 dB Back Off

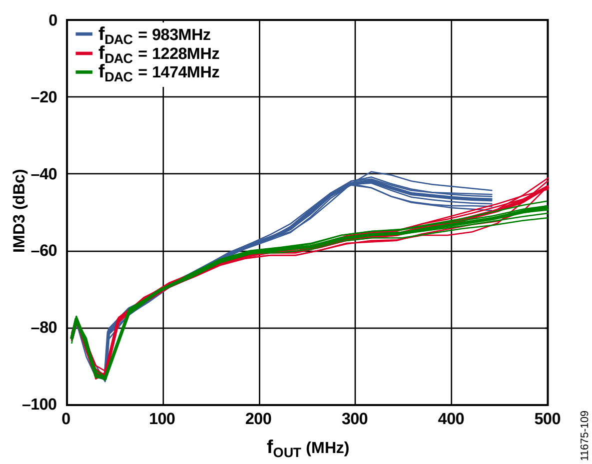


Figure 9. Two Tone Third IMD (IMD3) vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

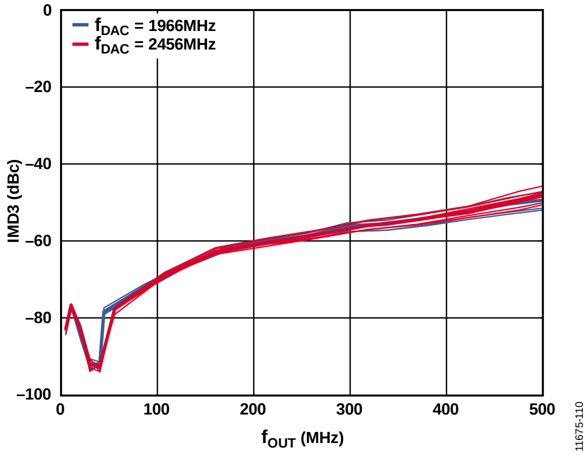


Figure 10. Two Tone Third IMD (IMD3) vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

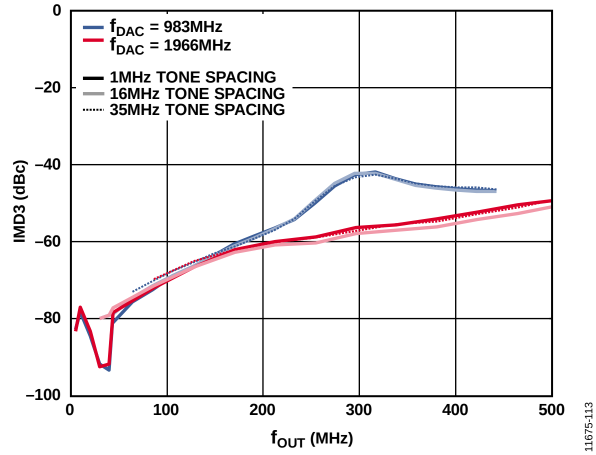


Figure 13. Two Tone Third IMD (IMD3) vs. f_{OUT} over Tone Spacing at 0 dB Back Off, f_{DAC} = 983 MHz and 1966 MHz

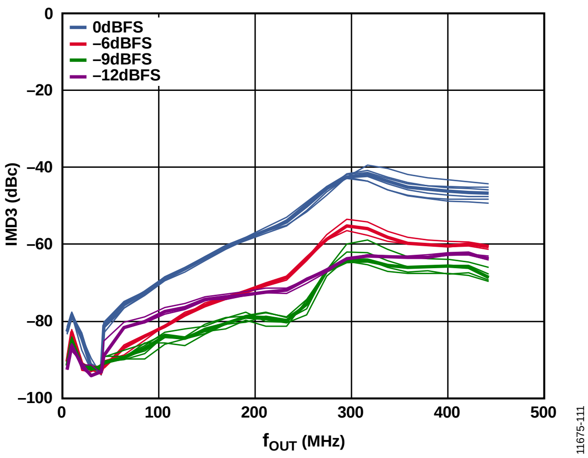


Figure 11. Two Tone Third IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz, Each Tone Is at −6 dBFS

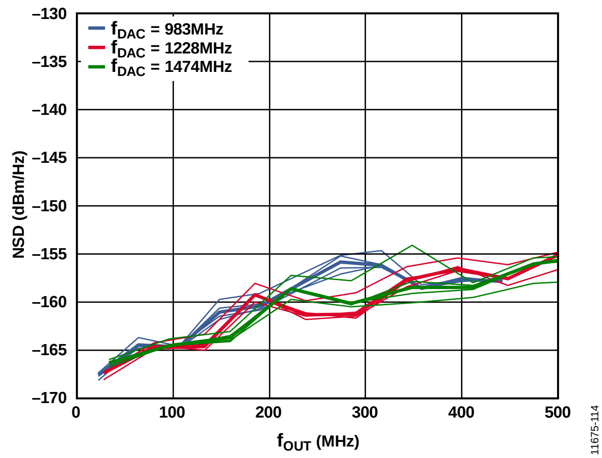


Figure 14. Single Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

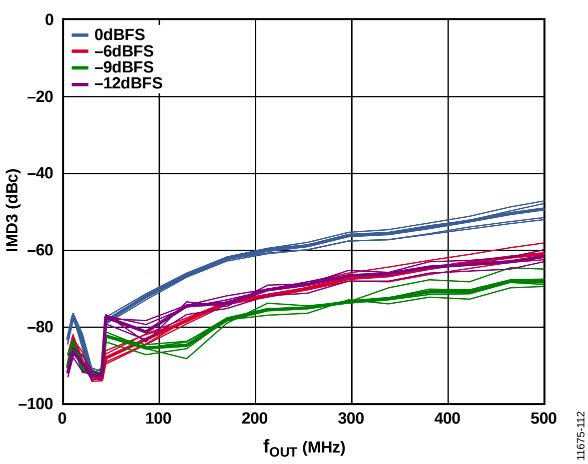


Figure 12. Two Tone Third IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz, Each Tone Is at −6 dBFS

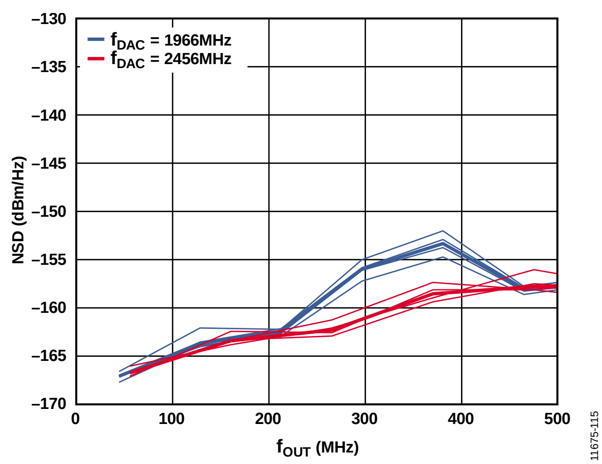


Figure 15. Single Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

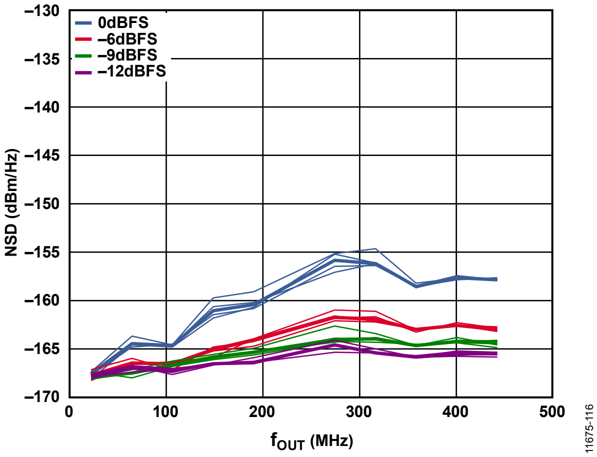


Figure 16. Single Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz

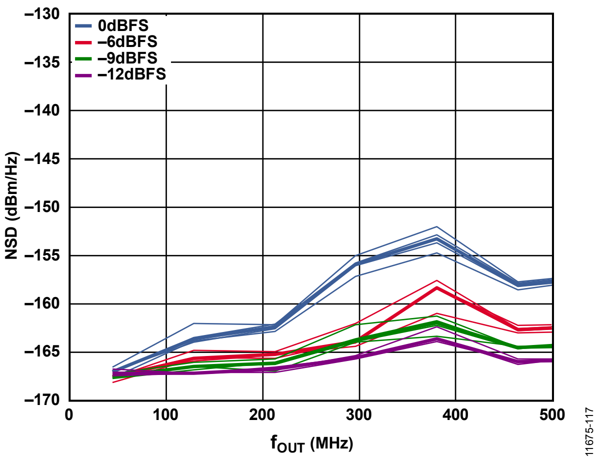


Figure 17. Single Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz

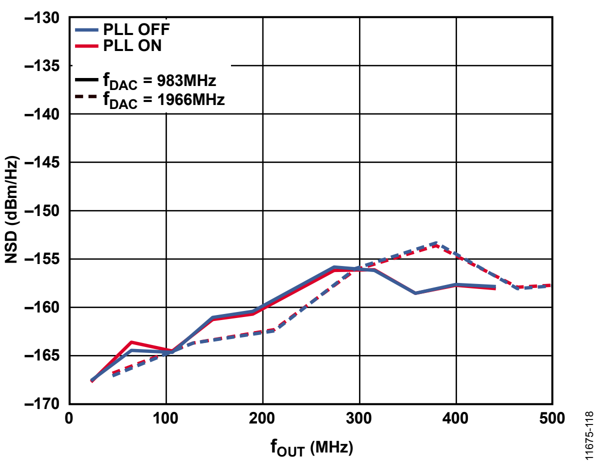


Figure 18. Single Tone NSD (0 dBFS) vs. f_{OUT}, f_{DAC} = 983 MHz and 1966 MHz, PLL On and Off

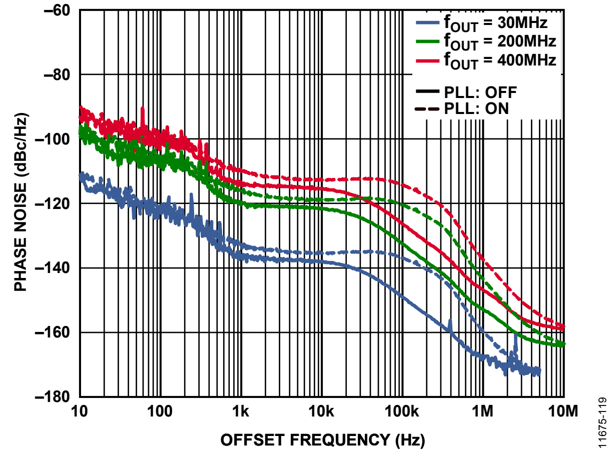


Figure 19. Single Tone Phase Noise vs. Offset Frequency over f_{OUT}, f_{DAC} = 2.0 GHz, PLL On and Off

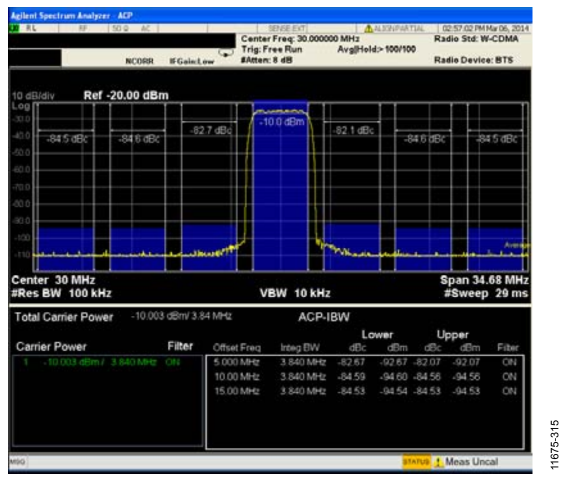


Figure 20. 1C WCDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

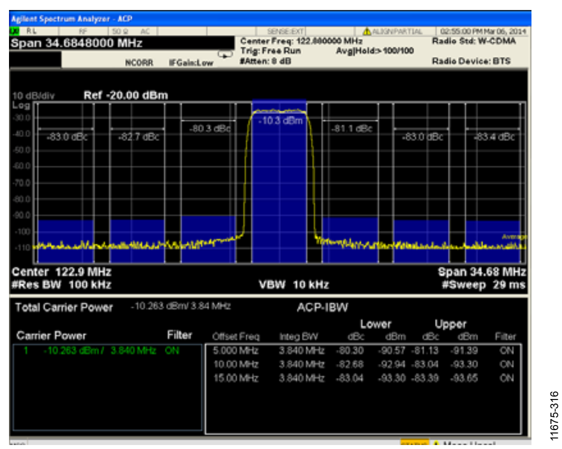
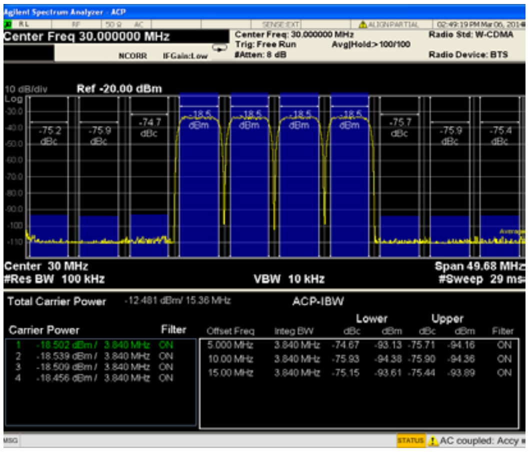
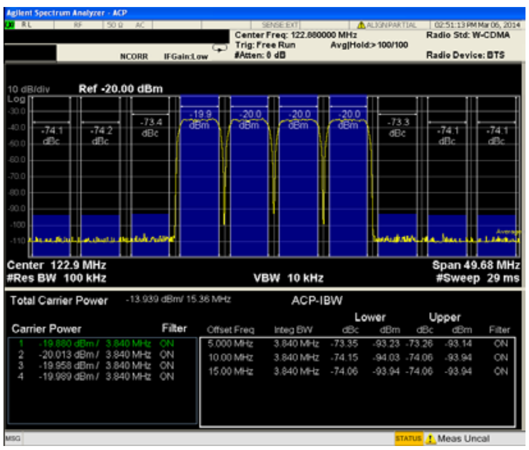


Figure 21. 1C WCDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz



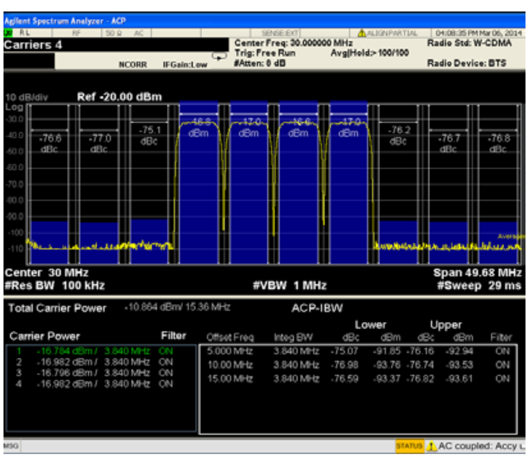
11675-317

Figure 22. 4C WCDMA ACLR, f_{OUT} = 30 MHz,
f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz



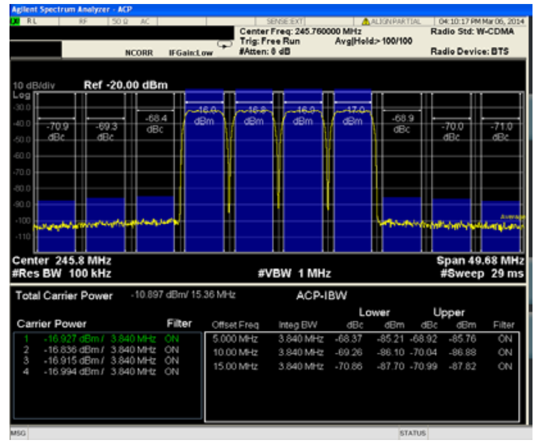
11675-318

Figure 23. 4C WCDMA ACLR, f_{OUT} = 122 MHz,
f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz



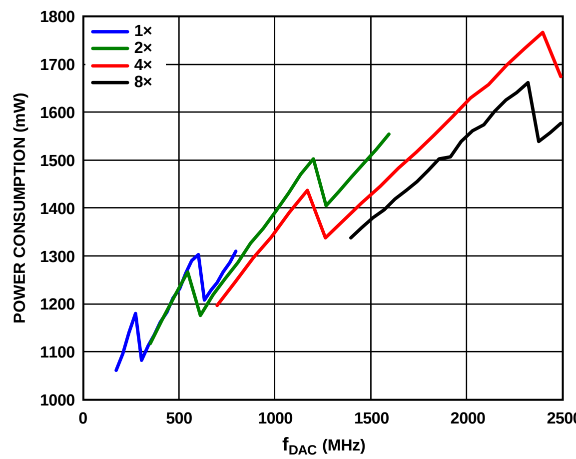
11675-319

Figure 24. 4C WCDMA ACLR, f_{OUT} = 30 MHz,
f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 245 MHz



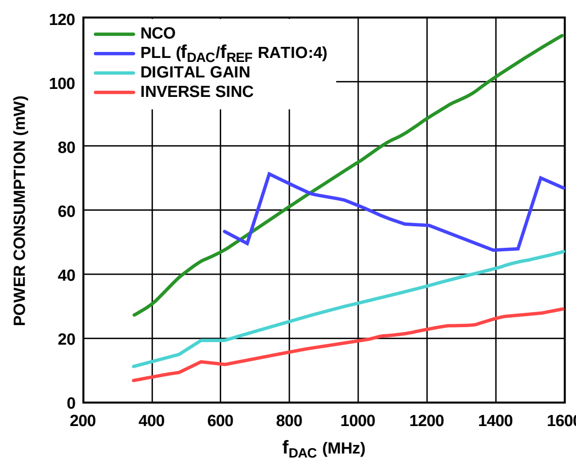
11675-320

Figure 25. 4C WCDMA ACLR, f_{OUT} = 245 MHz,
f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 245 MHz



11675-326

Figure 26. Total Power Consumption vs. f_{DAC} over Interpolation, 8 SERDES Lanes Enabled, NCO, Digital Gain, Inverse Sinc and DAC PLL Disabled



11675-327

Figure 27. Power Consumption vs. f_{DAC} over Digital Functions

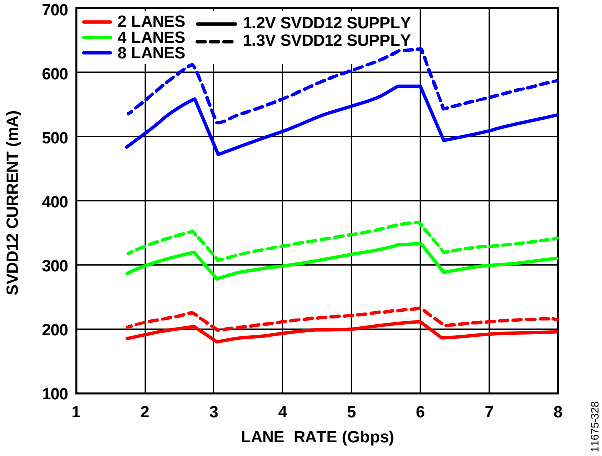


Figure 28. SVDD12 Current vs. Lane Rate over Number of SERDES Lanes and Supply Voltage Setting

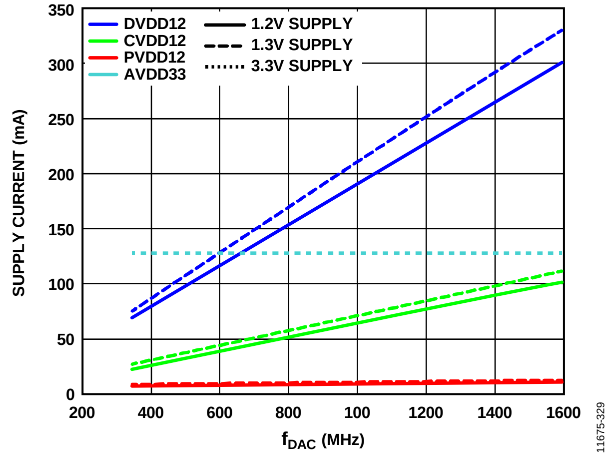


Figure 29. DVDD12, CVDD12, PVDD12, and AVDD33 Supply Current vs. f_{DAC} over Supply Voltage Setting

THEORY OF OPERATION

The AD9144 is a 16-bit, quad DAC with a SERDES interface. Figure 2 shows a detailed functional block diagram of the AD9144. Eight high speed serial lanes carry data at a maximum speed of 10.6 Gbps, and a 1.06 GSPS input data rate to the DACs. Compared to either LVDS or CMOS interfaces, the SERDES interface simplifies pin count, board layout, and input clock requirements to the device.

The clock for the input data is derived from the device clock (required by the JESD204B specification). This device clock can be sourced with a PLL reference clock used by the on-chip PLL to generate a DAC clock or a high fidelity direct external DAC sampling clock. The device can be configured to operate in one-, two-, four-, or eight-lane modes, depending on the required input data rate. To add application flexibility, the quad DAC can be configured as a dual link device with each JESD204B link providing data for a dual DAC pair.

The digital datapath of the AD9144 offers four interpolation modes (1×, 2×, 4×, and 8×) through three half-band filters with a maximum DAC sample rate of 2.8 GSPS. An inverse sinc filter is provided to compensate for sinc related roll-off.

The AD9144 DAC cores provide a fully differential current output with a nominal full-scale current of 20 mA. The full-scale current, I_{OUTFS}, is user adjustable to between 13.9 mA and 27.0 mA, typically. The differential current outputs are complementary and are optimized for easy integration with the Analog Devices ADRF672x AQMs. The AD9144 is capable of multichip synchronization that can both synchronize multiple DACs and establish a constant and deterministic latency (latency locking) path for the DACs. The latency for each of the DACs remains constant from link establishment to link establishment. An external alignment (SYSREF±) signal makes the AD9144 Subclass 1 compliant. Several modes of SYSREF± signal handling are available for use in the system.

An SPI configures the various functional blocks and monitors their statuses. The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Device Setup Guide section). Simple SPI initialization routines set up the JESD204B link and are included in the evaluation board package. The following sections describe the various blocks of the AD9144 in greater detail. Descriptions of the JESD204B interface, control parameters, and various registers to set up and monitor the device are provided. The recommended start-up routine reliably sets up the data link.

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The serial input/output (I/O) is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9144. MSB first or LSB first transfer formats are supported. The serial port interface can be configured as a 4-wire interface or a 3-wire interface in which the input and output share a single-pin I/O (SDIO).

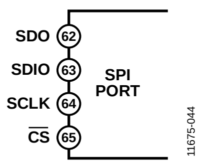


Figure 30. Serial Port Interface Pins

There are two phases to a communication cycle with the AD9144. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are needed to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word (FTW) and numerically controlled oscillator (NCO) phase offsets, which change only when the frequency tuning word FTW_UPDATE_REQ bit is set.

DATA FORMAT

The instruction byte contains the information shown in Table 13.

Table 13. Serial Port Instruction Word

I15 (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit 14 to Bit 0 of the instruction word, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The remaining register addresses are generated by the device based on the ADDRINC bit. If ADDRINC is set high (Register 0x000, Bit 5 and Bit 2), multibyte SPI writes start on A[14:0] and increment by 1 every 8 bits sent/received. If ADDRINC is set to 0, the address decrements by 1 every 8 bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 10 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, chip select must stay low.

Serial Data I/O (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSBFIRST bit (Register 0x000, Bit 6 and Bit 1). The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When LSBFIRST = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When SDOACTIVE = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When SDOACTIVE = 0, the SDO pin is unused and the SDIO pin is used for both input and output.

Multibyte data transfers can be performed as well. This is done by holding the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. The direction of the address can be set using ADDRINC (Register 0x000, Bit 5 and Bit 2). When ADDRINC is 1, the multicycle addresses are incremented. When ADDRINC is 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

To prevent confusion and to ensure consistency between devices, the chip tests the first nibble following the address phase, ignoring the second nibble. This is completed independently from the LSB first bit and ensures that there are extra clock cycles following the soft reset bits (Register 0x000, Bit 0 and Bit 7) This only applies when writing to Register 0x000.

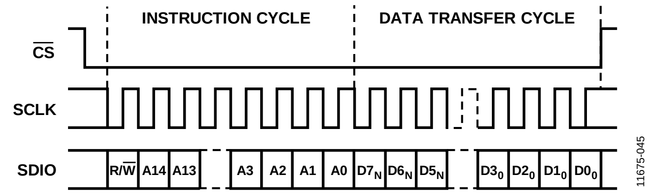


Figure 31. Serial Register Interface Timing, MSB First, ADDRINC = 0

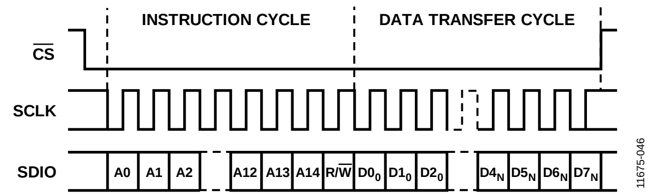


Figure 32. Serial Register Interface Timing, LSB First, ADDRINC = 1

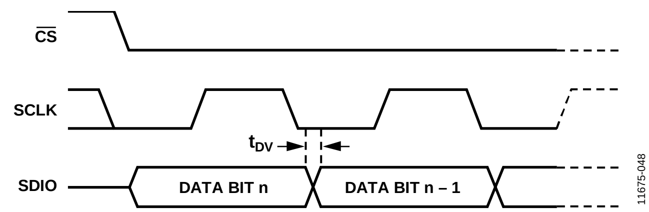


Figure 33. Timing Diagram for Serial Port Register Read

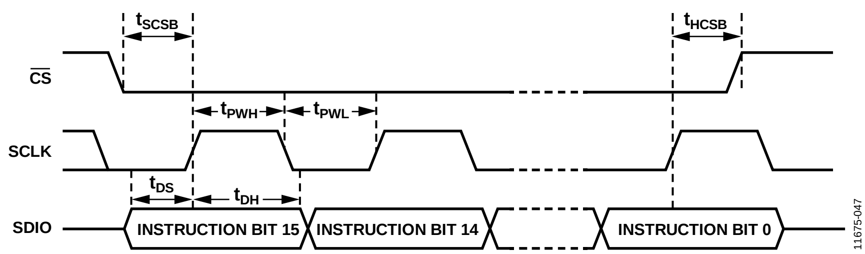


Figure 34. Timing Diagram for Serial Port Register Write

CHIP INFORMATION

Register 0x003 to Register 0x006 contain chip information, as shown in Table 14.

Table 14. Chip Information

Information	Description
Chip Type	The product type is high speed DAC, which is represented by a code of 0x04 in Register 0x003.
Product ID	8 MSBs in Register 0x005 and 8 LSBs in Register 0x004. The product ID is 0x9144.
Product Grade	Register 0x006[7:4]. The product grade is 0x00.
Device Revision	Register 0x006[3:0]. The device revision is 0x02.

DEVICE SETUP GUIDE

OVERVIEW

The sequence of steps to properly set up the AD9144 is as follows:

1. Set up the SPI interface, power up necessary circuit blocks, make required writes to the configuration registers, and set up the DAC clocks (see Step 1: Start Up the DAC).
2. Set the digital features of the AD9144 (see Step 2: Digital Datapath).
3. Set up the JESD204B links (see Step 3: Transport Layer).
4. Set up the physical layer of the SERDES interface (see Step 4: Physical Layer).
5. Set up the data link layer of the SERDES interface (see Step 5: Data Link Layer).
6. Check for errors (see Step 6: Optional Error Monitoring).
7. Optionally, enable any needed features as described in Step 7: Optional Features.

The register writes listed in Table 15 to Table 21 give the register writes necessary to set up the AD9144. Consider printing out this two page setup guide and filling in the Value column with appropriate variable values for the conditions of the desired application.

The notation 0x, shaded in gray, indicates register settings that must be filled in by the user. To fill in the unknown register values, select the correct settings for each variable listed in the Variable column of Table 15 to Table 21. The Description column describes how to set variables or provides a link to a section where this is described.

STEP 1: START UP THE DAC

This section describes how to set up the SPI interface, powers up necessary circuit blocks, writes required configuration registers, and sets up the DAC clocks.

Table 15. Power-Up and DAC Initialization Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x000		0xBD		Soft reset.
0x000		0x3C		Deassert reset, set 4-wire SPI.
0x011		0x		
	7	0		Power up band gap.
	[6:3]		PdDACs	PdDACs = 0 if all 4 DACs are being used. If not, see the DAC Power-Down Setup section.
	2	0		Power up master DAC.
0x080		0x	PdClocks	PdClocks = 0 if all 4 DACs are being used. If not, see the DAC Power-Down Setup section.
0x081		0x	PdSysref	PdSysref = 0x00 for Subclass 1. PdSysref = 0x10 for Subclass 0. See the Subclass Setup section for details on subclass.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

The following registers must be written to and values changed from default for the device to work correctly and must be written after any soft reset, hard reset, or power-up occurs.

Table 16. Required Device Configurations

Addr.	Value	Description
0x12D	0x8B	Digital datapath configuration
0x146	0x01	Digital datapath configuration
0x2A4	0xFF	Clock configuration
0x1C4	0x73	DAC PLL configuration
0x291	0x49	SERDES PLL configuration
0x29C	0x24	SERDES PLL configuration
0x29F	0x73	SERDES PLL configuration
0x232	0xFF	JESD interface configuration
0x333	0x01	JESD interface configuration

If using the optional DAC PLL, also set the registers in Table 17.

Table 17. Optional DAC PLL Configuration Procedure

Addr.	Value[1]	Variable	Description
0x08B	0x	LODivMode	See the DAC PLL Setup section
0x08C	0x	RefDivMode	See the DAC PLL Setup section
0x085	0x	BCount	See the DAC PLL Setup section
Various	0x	LookUpVals	See the DAC PLL Setup section
0x083	0x10		Enable DAC PLL[2]

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

[2] Verify that Register 0x084[1] reads back 1 after enabling the DAC PLL to indicate that the DAC PLL has locked.

STEP 2: DIGITAL DATAPATH

This section describes which interpolation filters to use and sets the data format being used. Additional digital features are available including fine and coarse modulation, digital gain scaling, and an inverse sinc filter used to improve pass-band flatness. Table 22 provides further details on the feature blocks available.

Table 18. Digital Datapath Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x112		0x	InterpMode	Select interpolation mode; see the Interpolation section.
0x110		0x		
	7		DataFmt	DataFmt = 0 if twos complement; DataFmt = 1 if unsigned binary.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

STEP 3: TRANSPORT LAYER

This section describes how to set up the JESD204B links. The parameters are determined by the desired JESD204B operating mode. See the JESD204B Setup section for details.

Table 19. Transport Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x200		0x00		Power up the interface.
0x201		0x	UnusedLanes	See the JESD204B Setup section.
0x300		0x		
	6		CheckSumMode	See the JESD204B Setup section.
	3		DualLink	See the JESD204B Setup section.
	2		CurrentLink	See the JESD204B Setup section.
0x450		0x	DID	Set DID to match the Device ID sent by the transmitter.
0x451		0x	BID	Set BID to match the Bank ID sent by the transmitter.
0x452		0x	LID	Set LID to match the Lane ID sent by the transmitter.
0x453		0x		
	7		Scrambling	See the JESD204B Setup section.
	[4:0]		L − 1[2]	See the JESD204B Setup section.
0x454		0x	F − 1[2]	See the JESD204B Setup section.
0x455		0x	K − 1[2]	See the JESD204B Setup section.
0x456		0x	M − 1[2]	See the JESD204B Setup section.
0x457		0x	N − 1[2]	N = 16.
0x458		0x		
	5		Subclass	See the JESD204B Setup section.
	[4:0]		Np − 1[2]	Np = 16.
0x459		0x		
	5		JESDVer	JESDVer = 1 for JESD204B, JESDVer = 0 for JESD204A.
	[4:0]		S − 1[2]	See the JESD204B Setup section.
0x45A	5	0x	HD	See the JESD204B Setup section.
0x45D		0x	Lane0Checksum	See the JESD204B Setup section.
0x46C		0x	Lanes	Deskew lanes.
0x476		0x	F	See the JESD204B Setup section.
0x47D		0x	Lanes	Enable lanes. See the JESD204B Setup section.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] This JESD204B link parameter is programmed in n − 1 notation as noted. For example, if the setup requires L = 8 (8 lanes per link), program L − 1 or 7 into Register 0x453[4:0].

If using dual link, perform writes from Register 0x300 to Register 0x47D with CurrentLink = 0 and then repeat the same set of register writes with CurrentLink = 1 (Register 0x200 and Register 0x201 need only be written once).

STEP 4: PHYSICAL LAYER

This section describes how to set up the physical layer of the SERDES interface. In this section the input termination settings are configured along with the CDR sampling and SERDES PLL.

Table 20. Device Configurations and Physical Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x2AA		0xB7		JESD interface termination setting
0x2AB		0x87		JESD interface termination setting
0x2B1		0xB7		JESD interface termination setting
0x2B2		0x87		JESD interface termination setting
0x2A7		0x01		Autotune PHY setting
0x2AE		0x01		Autotune PHY setting
0x314		0x01		SERDES SPI configuration
0x230		0x		
	5		Halfrate	Set up CDR; see the SERDES Clocks Setup section
	[2:1]		OvSmp	Set up CDR; see the SERDES Clocks Setup section
0x206		0x00		Reset CDR
0x206		0x01		Release CDR reset
0x289		0x		
	2	1		SERDES PLL configuration
	[1:0]		PLLDiv	Set CDR oversampling for PLL; see the SERDES Clocks Setup section
0x280		0x01		Enable SERDES PLL[2]
0x268		0x		
	[7:6]		EqMode	See the Equalization Mode Setup section
	[5:0]	0x22		Required value (default)

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] Verify that Register 0x281[0] reads back 1 after enabling the SERDES PLL to indicate that the SERDES PLL has locked.

STEP 5: DATA LINK LAYER

This section describes how to set up the data link layer of the SERDES interface. This section deals with SYSREF processing, setting deterministic latency, and establishing the link.

Table 21. Data Link Layer Settings

Address	Bit No.	Value[1]	Variable	Description
0x301		0x	Subclass	See the JESD204B Setup section.
0x304		0x	LMFCDel	See the Link Latency Setup section.
0x305		0x	LMFCDel	See the Link Latency section.
0x306		0x	LMFCVar	See the Link Latency Setup section.
0x307		0x	LMFCVar	See the Link Latency Setup section.
0x03A		0x01		Set sync mode = one shot sync; see the Syncing LMFC Signals section for other sync options.
0x03A		0x81		Enable the sync machine.
0x03A		0xC1		Arm the sync machine.
SYSREF±				If Subclass = 1, ensure that at least one SYSREF± edge is sent to the device.[2]
0x308 to 0x30B		0x	XBarVals	If remapping lanes, set up crossbar; see the Crossbar Setup section.
0x334		0x	InvLanes	Invert polarity of desired logical lanes. Bit x of InvLanes must be a 1 for each Logical Lane x to invert.
0x300		0x		Enable the links.
	6		ChkSmMd	See the JESD204B Setup section.
	3		Subclass	See the JESD204B Setup section.
	[1:0]		EnLinks	EnLinks = 3 if DualLink = 1 (enables Link 0 and Link 1); EnLinks = 1 if DualLink = 0 (enables Link 0 only).

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] Verify that Register 0x03B[3] reads back 1 after sending at least one SYSREF± edge to the device to indicate that the LMFC sync machine has properly locked.

STEP 6: OPTIONAL ERROR MONITORING

For JESD204B error monitoring, see the JESD204B Error Monitoring section. For other error checks, see the Interrupt Request Operation section.

STEP 7: OPTIONAL FEATURES

There are a number of optional features that can be enabled. Table 22 provides links to the sections describing each feature. Unless otherwise noted, these features are paged as described in the Dual Paging section. Paging is particularly important for dual specific settings like digital gain, phase adjust, and dc offset.

Table 22. Optional Features

Feature	Default	Description
Digital Modulation	Off	Modulates the data with a desired carrier. See the Digital Modulation section.
Inverse Sinc	On	Improves pass-band flatness. See the Inverse Sinc section.
Digital Gain	2.7 dB	Multiplies data by a factor. Can compensate inverse sinc usage or balance I/Q amplitude. See the Digital Gain section.
Phase Adjust	Off	Used to balance I/Q phase. See the Phase Adjust section.
DC Offset	Off	Used to cancel LO leakage. See the DC Offset section.
Group Delay	0	Used to control overall latency. See the Group Delay section.
Downstream Protection	Off	Used to protect downstream components. See the Downstream Protection section.
Self Calibration	Off	Used to improve DAC linearity. Not paged by the dual paging register. See the Self Calibration section.

DAC PLL SETUP

This section explains how to select appropriate LODivMode, RefDivMode, and BCount in the Step 1: Start Up the DAC section. These parameters depend on the desired DAC clock frequency (f_{DACCLK}) and DAC reference clock frequency (f_{REF}). When using the DAC PLL, the reference clock signal is applied to the CLK± differential pins (Pin 2 and Pin 3).

Table 23. DAC PLL LODivMode Settings

DAC Frequency Range (MHz)	LODivMode, Register 0x08B[1:0]
1500 to 2800	1
750 to 1500	2
420 to 750	3

Table 24. DAC PLL RefDivMode Settings

DAC PLL Reference Frequency (f_{REF}) (MHz)	Divide by (RefDivFactor)	RefDivMode, Register 0x08C[2:0]
35 to 80	1	0
80 to 160	2	1
160 to 320	4	2
320 to 640	8	3
640 to 1000	16	4

The VCO frequency (f_{VCO}) is related to the DAC clock frequency according to the following equation:

$$f_{VCO} = f_{DACCLK} \times 2^{LODivMode + 1}$$

where 6 GHz ≤ f_{VCO} ≤ 12 GHz.

BCount must be between 6 and 127 and is calculated based on f_{DACCLK} and f_{REF} as follows:

$$BCount = \text{floor}((f_{DACCLK})/(2 \times f_{REF}/RefDivFactor))$$

where $RefDivFactor = 2^{RefDivMode}$ (see Table 24).

Finally, set a number of registers to configure the PLL loop. These are based on PLL reference frequency and VCO frequency. Table 96 through Table 98 show how to set these values. Each table is optimized for a particular PLL reference frequency (40 MHz, 60 MHz, or 80 MHz); use the closest frequency to the actual PLL reference frequency. After a table is chosen, select the parameters from the row containing the VCO frequency (f_{VCO}) being used or the next lowest f_{VCO} if the value falls between table values listed. Write the registers listed in the table with the corresponding LookUpVals.

For more information on the DAC PLL, see the DAC Input Clock Configurations section.

INTERPOLATION

The transmit path can use zero to three cascaded interpolation filters, which each provide a 2× increase in output data rate and a low-pass function. Table 25 shows the different interpolation modes and the respective usable bandwidth along with the maximum f_{DATA} rate attainable.

Table 25. Interpolation Modes and Their Usable Bandwidth

Interpolation Mode	InterpMode	Usable Bandwidth	Max f_{DATA} (MHz)
1× (bypass)	0x00	f_{DATA}	1060 (JESD limited)
2×	0x01	$0.4 \times f_{DATA}$	1060 (JESD limited)
4×	0x03	$0.4 \times f_{DATA}$	700
8×	0x04	$0.4 \times f_{DATA}$	350

The usable bandwidth is defined for 1×, 2×, 4×, and 8× modes as the frequency band over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 85 dB. For more information, see the Interpolation Filters section.

JESD204B SETUP

This section explains how to select a JESD204B operating mode for a desired application. This in turn defines appropriate values for CheckSumMode, UnusedLanes, DualLink, CurrentLink, Scrambling, L, F, K, M, N, Np, Subclass, S, HD, Lane0Checksum, and Lanes needed for the Step 3: Transport Layer section.

Note that DualLink, Scrambling, L, F, K, M, N, Np, S, HD, and Subclass must be set the same on the transmit side.

For a summary of how a JESD204B system works and what each parameters mean, see the JESD204B Serial Data Interface section.

Available Operating Modes

Table 26. JESD204B Operating Modes (Single Link Only)

Parameter	Mode			
	0	1	2	3
M (Converter Count)	4	4	4	4
L (Lane Count)	8	8	4	2
S ((Samples per Converter) per Frame)	1	2	1	1
F ((Octets per Frame) per Lane)	1	2	2	4

Table 27. JESD204B Operating Modes (Single or Dual Link)

Parameter	Mode					
	4	5	6	7	9	10
M (Converter Count)	2	2	2	2	1	1
L (Lane Count)	4	4	2	1	2	1
S ((Samples per Converter) per Frame)	1	2	1	1	1	1
F ((Octets per Frame) per Lane)	1	2	2	4	1	2

For a particular application, the number of converters to use (M) and the f_{DATA} (DataRate) are known. The LaneRate and number of lanes (L) can be traded off as follows:

$$DataRate = (DACRate)/(InterpolationFactor)$$
$$LaneRate = (20 \times DataRate \times M)/L$$

where *LaneRate* is between 1.42 Gbps and 10.64 Gbps.

Octets per frame per lane (F) and samples per convertor per frame (S) define how the data is packed. If F = 1, the high density setting must be set to one (HD = 1). Otherwise, set HD = 0.

Converter resolution and bits per sample (N and Np) must both be set to 16. Frames per multiframe (K) must be set to 32 for Mode 0, Mode 4 and Mode 9. Other modes may use either K = 16 or K = 32.

DualLink

DualLink sets up two independent JESD204B links, which allows each link to be reset independently. If this functionality is desired, set DualLink to 1; if a single link is desired, set DualLink to 0. Note that Link 0 and Link 1 must have identical parameters. The operating modes available when using dual link mode are shown in Table 26. In addition to these operating modes, the modes in Table 27 may also be used when using single link mode.

Scrambling

Scrambling is a feature that makes the spectrum of the link data independent. This avoids spectral peaking and provides some protection against data dependent errors caused by frequency selective effects in the electrical interface. Set to 1 if scrambling is being used, or to 0 if it is not.

Subclass

Subclass determines whether the latency of the device is deterministic, meaning it requires an external synchronization signal. See the Subclass Setup section for more information.

CurrentLink

Set CurrentLink to either 0 or 1 depending on if you wish to configure Link 0 or Link 1, respectively.

Lanes

Lanes is used to enable and deskew particular lanes in two thermometer coded registers.

$$Lanes = (2^{L}) - 1.$$

UnusedLanes

UnusedLanes is used to turn off unused circuit blocks to save power. Each physical lane that is not being used (SERDINx±) must be powered off by writing a 1 to the corresponding bit of Register 0x201.

For example, if using Mode 6 in dual link mode and sending data on SERDIN0±, SERDIN1±, SERDIN4±, and SERDIN5±, set UnusedLanes = 0xCC to power off Physical Lane 2, Lane 3, Lane 6, and Lane 7.

CheckSumMode

CheckSumMode must match the checksum mode used on the transmit side. If the checksum used is the sum of fields in the link configuration table, CheckSumMode = 0. If summing the registers containing the packed link configuration fields, CheckSumMode = 1. For more information on the how to calculate the two checksum modes, see the Lane0Checksum section.

Lane0Checksum

Lane0Checksum may be used for error checking purposes to ensure that the transmitter is set up as expected.

If CheckSumMode = 0, the checksum is the lower 8 bits of the sum of the L − 1, M − 1, K − 1, N − 1, Np − 1, S − 1, Scrambling, HD, Subclass, and JESDVer variables.

If CheckSumMode = 1, Lane0Checksum is the lower 8 bits of the sum of Register 0x450 to Register 0x45A. Select whether to sum by fields or by registers, matching the setting on the transmitter.

DAC Power-Down Setup

As described in the Step 1: Start Up the DAC section, PdDACs must be set to 0 if all 4 converters are being used. If fewer than four converters are being used, the unused converters must be powered down. Table 28 can be used to determine which DACs are powered down based on the number of converters per link (M) and whether the device is in DualLink mode.

Table 28. DAC Power-Down Configuration Settings

M (Converters per link)	DualLink	DACs to Power Down				PdDAC
		0	1	2	3	
1	0	0	1	1	1	0b0111
1	1	0	1	0	1	0b0101
2	0	0	0	1	1	0b0011
2	1	0	0	0	0	0b0000
4	0	0	0	0	0	0b0000

PdClocks

If both DACs in DAC Dual B (DAC2 and DAC3) are powered down, the clock for DAC Dual B can be powered down. In this case, PdClocks = 0x40; if not, PdClocks = 0x00.

SERDES CLOCKS SETUP

This section describes how to select the appropriate Halfrate, OvSmp, and PLLDiv settings in the Step 4: Physical Layer section. These parameters depend solely on the lane rate (the lane rate is established in the JESD204B Setup section).

Table 29. SERDES Lane Rate Configuration Settings

Lane Rate (Gbps)	Halfrate	OvSmp	PLLDiv
1.42 to 2.76	0	1	2
2.83 to 5.52	0	0	1
5.65 to 10.64	1	0	0

Halfrate and OvSmp set how the Clock Detect and Recover (CDR) circuit sample. See the SERDES PLL section for an explanation of how that circuit blocks works and the role of PLLDiv in the block.

EQUALIZATION MODE SETUP

Set EqMode = 1 for a low power setting. Select this mode if the insertion loss in your printed circuit board (PCB) is less than 12 dB. For insertion losses greater than 12 dB, but less than 17.5 dB, set EqMode = 0. More details can be found in the Equalization section.

LINK LATENCY SETUP

This section describes the steps necessary to guarantee multichip deterministic latency in Subclass 1 and guarantee synchronization of links within a device in Subclass 0. Use this section to fill in LMFCDel, LMFCVar, and Subclass in the Step 5: Data Link Layer section. For more information, see the Syncing LMFC Signals section.

Subclass Setup

The AD9144 supports JESD204B Subclass 0 and Subclass 1 operation.

Subclass 1

This mode gives deterministic latency and allows links to be synced to within ½ DAC clock periods. It requires an external SYSREF± signal that is accurately phase aligned to the DAC clock.

Subclass 0

This mode gives deterministic latency to within 4 DAC clock periods. It does not require any signal on the SYSREF± pins (the pins can be left disconnected).

Subclass 0 still requires that all lanes arrive within the same LMFC cycle and the dual DACs must be synchronized to each other (they are synchronized to an internal clock instead of the SYSREF± signal).

Set Subclass to 0 or 1 as desired.

Link Delay Setup

LMFCVar and LMFCDel are used to impose delays such that all lanes in a system arrive in the same LMFC cycle.

The unit used internally for delays is the period of the internal processing clock (PClock), whose rate is 1/40th the lane rate.

Delays that are not in PClock cycles must be converted before they are used.

Some useful internal relationships are defined below:

PClockPeriod = *40/LaneRate*

The PClockPeriod can be used to convert from time to PClock cycles when needed.

PClockFactor = 4/F (Frames per PClock)

The PClockFactor is used to convert from units of PClock cycles to FrameClock cycles, which is needed to set LMFCDel in Subclass 1.

PClocksPerMF= K/PClockFactor (PClocks per LMFC cycle)

where *PClocksPerMF* is the number or PClock cycles in a multiframe cycle.

The values for PClockFactor and PClockPerMF are given per JESD mode in Table 30 and Table 31.

Table 30. PClockFactor and PClockPerMF Per LMFC

JESD Mode ID	0	1	2	3
PClockFactor	4	2	2	1
PClockPerMF (K = 32)	8	16	16	32
PClockPerMF (K = 16)	N/A	8	8	16

Table 31. PClockFactor and PClockPerMF Per LMFC

JESD Mode ID	4	5	6	7	9	10
PClockFactor	4	2	2	1	4	2
PClockPerMF (K = 32)	8	16	16	32	8	16
PClockPerMF (K = 16)	N/A[1]	8	8	16	N/A[1]	8

[1] N/A means not applicable.

With Known Delays

With information about all the system delays, LMFCVar and LMFCDel can be calculated directly.

RxFixed (the fixed receiver delay in PClock cycles) and RxVar (the variable receiver delay in PClock cycles) can be found in Table 8. TxFixed (the fixed transmitter delay in PClock cycles) and TxVar (the variable receiver delay in PClock cycles) can be found in the data sheet of the transmitter used. PCBFixed (the fixed PCB trace delay in PClock cycles) can be extracted from software; because this is generally much smaller than a PClock cycle, it can also be omitted. For both the PCB and transmitter delays, convert the delays into PClock cycles.

For each lane

$MinDelayLane = \text{floor}(RxFixed + TxFixed + PCBFixed)$
$MaxDelayLane = \text{ceiling}(RxFixed + RxVar + TxFixed + TxVar + PCBFixed))$

Across lanes, links, and devices:
MinDelay is the minimum of all *MinDelayLane* values.
MaxDelay is the maximum of all *MaxDelayLane* values.

For safety, add a guard band of 1 PClock cycle to each end of the link delay as in the following equations:

$$LMFCVar = (MaxDelay + 1) - (MinDelay - 1)$$

Note that if LMFCVar must be more than 10, the AD9144 is unable to tolerate the variable delay in the system.

For Subclass 1

$$LMFCDel = ((MinDelay - 1) \times PClockFactor)\ \%\ K$$

For Subclass 0

$$LMFCDel = (MinDelay - 1)\ \%\ PClockPerMF$$

Program the same LMFCDel and LMFCVar across all links and devices.

See the Link Delay Setup Example, With Known Delays section for an example calculation.

Without Known Delays

If comprehensive delay information is not available or known, the AD9144 can read back the link latency between the $LMFC_{RX}$ and the last arriving LMFC boundary in PClock cycles. This information is then used to calculate LMFCVar and LMFCDel.

For each link (on each device)

1. Power up the board.
2. Follow the steps in Table 15 through Table 21 of the Device Setup Guide.
3. Set the subclass and perform a sync. For one shot sync, perform the writes in Table 32. See the Syncing LMFC Signals section for alternate sync modes.
4. Record DYN_LINK_LATENCY_0 (Register 0x302) as a value of Delay for that link and power cycle.
5. Record DYN_LINK_LATENCY_1 (Register 0x303) as a value of Delay for that link and power cycle.

Repeat Steps 1 to Step 5 twenty times for each device in the system. Keep a single list of the Delay values across all runs and devices.

Table 32. Register Configuration and Procedure for One Shot Sync

Addr.	Bit. No.	Value[1]	Variable	Description
0x301		0x	Subclass	Set subclass
0x03A		0x01		Set sync mode = one shot sync
0x03A		0x81		Enable the sync machine
0x03A		0xC1		Arm the sync machine
SYSREF±				If Subclass = 1, ensure that at least one SYSREF± edge is sent to the device
0x300		0x		Enable the links
	6		ChkSmMd	See the JESD204B Setup section
	3		Subclass	See the JESD204B Setup section
	[1:0]		EnLinks	EnLinks = 3 if in DualLink mode to enable Link 0 and Link 1; EnLinks = 1 if not in DualLink mode to enable Link 0

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

The list of delay values is used to calculate LMFCDel and LMFCVar, but first some of the delay values may need to be remapped.

The maximum possible value for DYN_LINK_LATENCY_x is one less than the number of PClocks in a multiframe (PClocksPerMF). It is possible that a roll-over condition may be encountered, meaning the set of recorded Delay values might roll over the edge of a multiframe. If so, Delay values may be near both 0 and PClocksPerMF. If this occurs, add PClocksPerMF to the set of values near 0.

For example, for Delay value readbacks of 6, 7, 0, and 1, the 0 and 1 Delay values must be remapped to 8 and 9, making the new set of Delay values 6, 7, 8, and 9.

Across power cycles, links, and devices

- MinDelay is the minimum of all Delay measurements
- MaxDelay is the maximum of all Delay measurements

For safety, a guard band of 1 PClock cycle is added to each end of the link delay and calculate LMFCVar and LMFCDel with the following equation:

$$LMFCVar = (MaxDelay + 1) - (MinDelay - 1)$$

Note that if LMFCVar must be more than 10, the AD9144 is unable to tolerate the variable delay in the system.

For Subclass 1

$$LMFCDel = ((MinDelay - 1) \times PClockFactor) \% K$$

For Subclass 0

$$LMFCDel = (MinDelay - 1) \% PClockPerMF$$

Program the same LMFCDel and LMFCVar across all links and devices.

See the Link Delay Setup Example, Without Known Delay section for an example calculation.

CROSSBAR SETUP

Registers 0x308 to Register 0x30B allow arbitrary mapping of physical lanes (SERDINx±) to logical lanes used by the SERDES deframers.

Table 33. Crossbar Registers

Address	Bits	Logical Lane
0x308	[2:0]	LOGICAL_LANE0_SRC
0x308	[5:3]	LOGICAL_LANE1_SRC
0x309	[2:0]	LOGICAL_LANE2_SRC
0x309	[5:3]	LOGICAL_LANE3_SRC
0x30A	[2:0]	LOGICAL_LANE4_SRC
0x30A	[5:3]	LOGICAL_LANE5_SRC
0x30B	[2:0]	LOGICAL_LANE6_SRC
0x30B	[5:3]	LOGICAL_LANE7_SRC

Write each LOGICAL_LANEy_SRC with the number (x) of the desired physical lane (SERDINx±) from which to get data. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default LOGICAL_LANE0_SRC = 0, meaning Logical Lane 0 receives data from Physical Lane 0 (SERDIN0±). If instead the user wants to use SERDIN4± as the source for Logical Lane 0, the user must write LOGICAL_LANE0_SRC = 4.

JESD204B SERIAL DATA INTERFACE

JESD204B OVERVIEW

The AD9144 has eight JESD204B data ports that receive data. The eight JESD204B ports can be configured as part of a single JESD204B link or as part of two separate JESD204B links (dual link mode) that share a single system reference (SYSREF±) and device clock (CLK±).

The JESD204B serial interface hardware consists of three layers: the physical layer, the data link layer, and the transport layer. These sections of the hardware are described in subsequent sections, including information for configuring every aspect of the interface. Figure 35 shows the communication layers implemented in the AD9144 serial data interface to recover the clock and deserialize, descramble, and deframe the data before it is sent to the digital signal processing section of the device.

The physical layer is responsible for establishing a reliable channel between the transmitter and the receiver, the data link layer is responsible for unpacking the data into octets and descrambling the data, and the transport layer receives the descrambled JESD204B frames and converts them to DAC samples.

There are a number of JESD204B parameters (L, F, K, M, N, Np, S, HD, and Scrambling) that define how the data is packed and tell the device how to turn the serial data into samples. These parameters are defined in detail in the Transport Layer section.

Only certain combinations of parameters are supported. Each supported combination is called a mode. In total, there are 10 single link modes supported by the AD9144, as described in Table 34. In dual link mode, there are six supported modes, as described in Table 35. Each of these tables shows the associated clock rates when the lane rate is 10 Gbps.

For a particular application, the number of converters to use (M) and the DataRate are known. The LaneRate and number of lanes (L) can be traded off as follows:

$$DataRate = (DACRate)/(InterpolationFactor)$$
$$LaneRate = (20 \times DataRate \times M)/L$$

where *LaneRate* must be between 1.42 Gbps and 10.64 Gbps.

Achieving and recovering synchronization of the lanes is very important. To simplify the interface to the transmitter, the AD9144 designates a master synchronization signal for each JESD204B link. In single link mode, $\overline{\text{SYNCOUT0±}}$ is used as the master signal for all lanes; in dual link mode, $\overline{\text{SYNCOUT0±}}$ is used as the master signal for Link 0 and $\overline{\text{SYNCOUT1±}}$ is used as the master signal for Link 1. If any lane in a link loses synchronization, a resynchronization request is sent to the transmitter via the synchronization signal of the link. The transmitter stops sending data and instead sends synchronization characters to all lanes in that link until resynchronization is achieved.

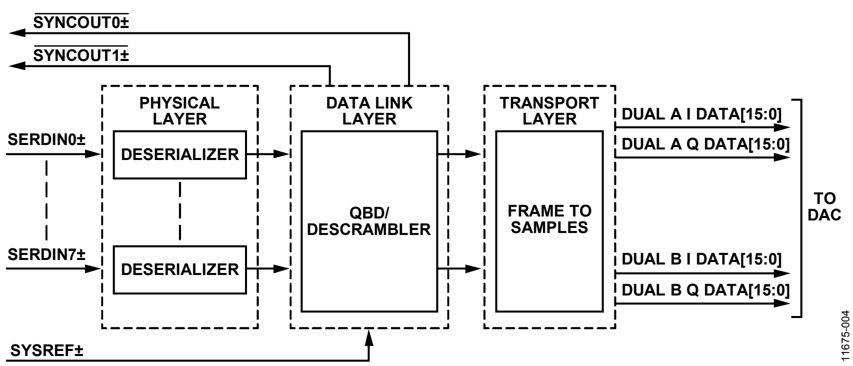


Figure 35. Functional Block Diagram of Serial Link Receiver

Table 34. Single Link JESD204B Operating Modes

Parameter	Mode 0	1	2	3	4	5	6	7	9	10
M (Converter Counts)	4	4	4	4	2	2	2	2	1	1
L (Lane Counts)	8	8	4	2	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	2	1	1	1	1
F (Octets per Frame per Lane)	1	2	2	4	1	2	2	4	1	2
Example Clocks for 10 Gbps Lane Rate										
PClock (MHz)	250	250	250	250	250	250	250	250	250	250
Frame Clock (MHz)	1000	500	500	250	1000	500	500	250	1000	500
Sample Clock (MHz)	1000	1000	500	250	1000	1000	500	250	1000	500

Table 35. Dual Link JESD204B Operating Modes for Link 0 and Link 1

	Mode					
Parameter	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Counts)	2	2	2	2	1	1
L (Lane Counts)	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	1
F (Octets/Frame per Lane)	1	2	2	4	1	2
Example Clock for 10 Gbps Lane Rate						
PClock (MHz)	250	250	250	250	250	250
Frame Clock (MHz)	1000	500	500	250	1000	500
Sample Clock (MHz)	1000	1000	500	250	1000	500

PHYSICAL LAYER

The physical layer of the JESD204B interface, hereafter referred to as the deserializer, has eight identical channels. Each channel consists of the terminators, an equalizer, a clock and data recovery (CDR) circuit, and the 1:40 demux function (see Figure 36).

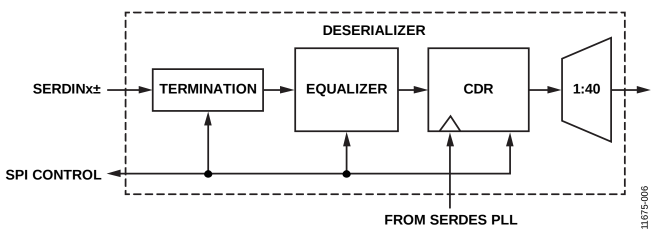


Figure 36. Deserializer Block Diagram

JESD204B data is input to the AD9144 via the SERDINx± 1.2 V differential input pins as per the JESD204B specification.

Interface Power-Up and Input Termination

Before using the JESD204B interface, it must be powered up by setting Register 0x200[0] = 0. In addition, each physical lane that is not being used (SERDINx±) must be powered down. To do so, set the corresponding Bit x for Physical Lane x in Register 0x201 to 0 if the physical lane is being used, and to 1 if it is not being used.

The AD9144 autocalibrates the input termination to 50 Ω. Before running the termination calibration, Register 0x2AA, Register 0x2AB, Register 0x2B1, and Register 0x2B2 must be written as described in Table 36 to guarantee proper calibration. The termination calibration begins when Register 0x2A7[0] and Register 0x2AE[0] transition from low to high. Register 0x2A7 controls autocalibration for PHY 0, PHY 1, PHY 6, and PHY 7. Register 0x2AE controls autocalibration for PHY 2, PHY 3, PHY 4, and PHY 5.

The PHY termination autocalibration routine is as shown in Table 36.

Table 36. PHY Termination Autocalibration Routine

Address	Value	Description
0x2AA	0xB7	JESD interface termination configuration
0x2AB	0x87	JESD interface termination configuration
0x2B1	0xB7	JESD interface termination configuration
0x2B2	0x87	JESD interface termination configuration
0x2A7	0x01	Autotune PHY terminations
0x2AE	0x01	Autotune PHY terminations

The input termination voltage of the DAC is sourced externally via the V_{TT} pins (Pin 21, Pin 23, Pin 40, and Pin 43). Set V_{TT} by connecting it to SVDD12. It is recommended that the JESD204B inputs be ac-coupled to the JESD204B transmit device using 100 nF capacitors.

Receiver Eye Mask

The AD9144 complies with the JESD204B specification regarding the receiver eye mask and is capable of capturing data that complies with this mask. Figure 37 shows the receiver eye mask normalized to the data rate interval with a 600 mV V_{TT} swing. See the JESD204B specification for more information regarding the eye mask and permitted receiver eye opening.

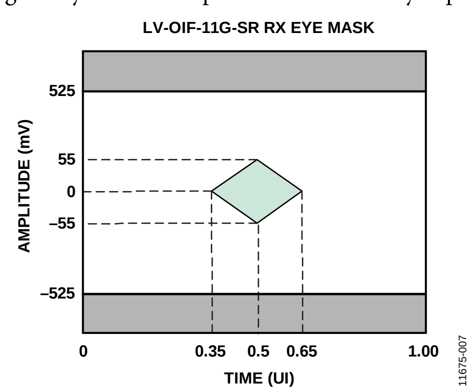


Figure 37. Receiver Eye Mask

Clock Relationships

The following clocks rates are used throughout the rest of the JESD204B section. The relationship between any of the clocks can be derived from the following equations:

$$DataRate = (DACRate)/(InterpolationFactor)$$

$$LaneRate = (20 \times DataRate \times M)/L$$

$$ByteRate = LaneRate/10$$

This comes from 8-bit/10-bit encoding, where each byte is represented by 10 bits.

$$PClockRate = ByteRate/4$$

The processing clock is used for a quad-byte decoder.

$$FrameRate = ByteRate/F$$

where F is defined as (bytes per frame) per lane.

$$PClockFactor = FrameRate/PClockRate = 4/F$$

where:
M is the JESD204B parameter for converters per link.
L is the JESD204B parameter for lanes per link.
F is the JESD204B parameter for octets per frame per lane.

SERDES PLL

Functional Overview of the SERDES PLL

The independent SERDES PLL uses integer-N techniques to achieve clock synthesis. The entire SERDES PLL is integrated on chip, including the VCO and the loop filter. The SERDES PLL VCO operates over the range of 5.65 GHz to 12 GHz.

In the SERDES PLL, a VCO divider block divides the VCO clock by 2 to generate a 2.825 GHz to 6 GHz quadrature clock for the deserializer cores. This clock is the input to the clock and data recovery block that is described in the Clock and Data Recovery section.

The reference clock to the SERDES PLL is always running at a frequency, f_{REF} = 1/40 of the lane rate = PClockRate. This clock is divided by a DivFactor to deliver a clock to the PFD block that is between 35 MHz and 80 MHz. Table 37 includes the respective SERDES_PLL_DIV_MODE register settings for each of the desired DivFactor options available.

Table 37. SERDES PLL Divider Settings

LaneRate (Gbps)	Divide by (DivFactor)	SERDES_PLL_DIV_MODE Register 0x289[1:0]
1.42 to 2.76	1	2
2.83 to 5.52	2	1
5.65 to 10.64	4	0

Register 0x280 controls the synthesizer enable and recalibration.

To enable the SERDES PLL, first set the PLL divider register according to Table 37, then enable the SERDES PLL by writing Register 0x280[0] to 1.

Confirm that the SERDES PLL is working by reading Register 0x281. If Register 0x281[0] = 1, the SERDES PLL has locked. If Register 0x281[3] = 1, the SERDES PLL was successfully calibrated. If Register 0x281[4] or Register 0x281[5] are high, the PLL hit the upper or lower end of its calibration band and must be recalibrated by writing 0 and then 1 to Register 0x280[2].

SERDES PLL IRQ

SERDES PLL lock and lost signals are available as IRQ events. Use Register 0x01F[3:2] to enable these signals, and then use Register 0x023[3:2] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

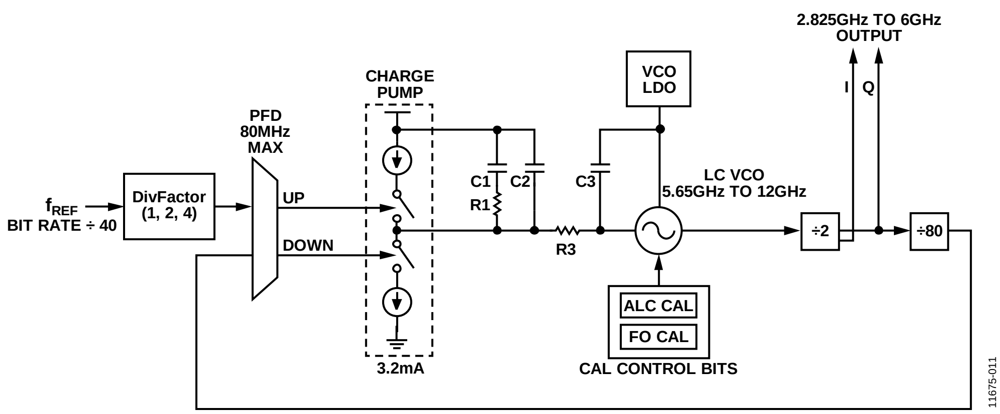


Figure 38. SERDES PLL Synthesizer Block Diagram Including VCO Divider Block

Clock and Data Recovery

The deserializer is equipped with a CDR circuit. Instead of recovering the clock from the JESD204B serial lanes, the CDR recovers the clocks from the SERDES PLL. The 2.825 GHz to 6 GHz output from the SERDES PLL, shown in Figure 38, is the input to the CDR.

A CDR sampling mode must be selected to generate the lane rate clock inside the device. If the desired lane rate is greater than 5.65 GHz, half rate CDR operation must be used. If the desired lane rate is less than 5.65 GHz, disable half rate operation. If the lane rate is less than 2.825 GHz, disable half rate and enable 2× oversampling to recover the appropriate lane rate clock. Table 38 gives a breakdown of CDR sampling settings that must be set dependent on the LaneRate.

Table 38. CDR Operating Modes

LaneRate (Gbps)	ENHALFRATE Register 0x230[5]	CDR_OVERSAMP Register 0x230[1]
1.42 to 2.76	0	1
2.83 to 5.52	0	0
5.65 to 10.64	1	0

The CDR circuit synchronizes the phase used to sample the data on each serial lane independently. This independent phase adjustment per serial interface ensures accurate data sampling and eases the implementation of multiple serial interfaces on a PCB.

After configuring the CDR circuit, reset it and then release the reset by writing 1 and then 0 to Register 0x206[0].

Power-Down Unused PHYs

Note that any unused and enabled lanes consume extra power unnecessarily. Each lane that is not being used (SERDINx±) must be powered off by writing a 1 to the corresponding bit of PHY_PD (Register 0x201).

Equalization

To compensate for signal integrity distortions for each PHY channel due to PCB trace length and impedance, the AD9144 employs an easy to use, low power equalizer on each JESD204B channel. The AD9144 equalizers can compensate for insertion losses far greater than required by the JESD204B specification. The equalizers have two modes of operation that are determined by the EQ_POWER_MODE register setting in Register 0x268[7:6]. In low power mode (Register 0x268[7:6] = 2b'01) and operating at the maximum lane rate of 10 Gbps, the equalizer can compensate for up to 12 dB of insertion loss. In normal mode (Register 0x268[7:6] = 2b'00), the equalizer can compensate for up to 17.5 dB of insertion loss. This performance is shown in Figure 39 as an overlay to the JESD204B specification for insertion loss. Figure 39 shows the equalization performance at 10.0 Gbps, near the maximum baud rate for the AD9144.

Figure 40 and Figure 41 are provided as points of reference for hardware designers and show the insertion loss for various lengths of well laid out stripline and microstrip transmission lines. See the Hardware Considerations section for specific layout recommendations for the JESD204B channel.

Low power mode is recommended if the insertion loss of the JESD204B PCB channels is less than that of the most lossy supported channel for lower power mode (shown in Figure 39). If the insertion loss is greater than that, but still less than that of the most lossy supported channel for normal mode (shown in Figure 39), use normal mode. At 10 Gbps operation, the EQ in normal mode consumes about 4 mW more power per lane used than in low power EQ mode. Note that either mode can be used in conjunction with transmitter preemphasis to ensure functionality and/or optimize for power.

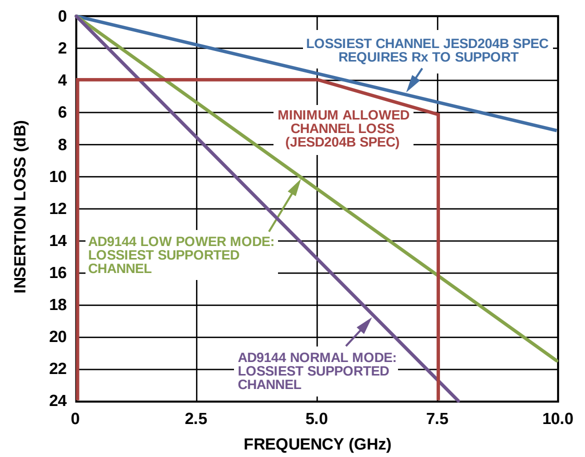


Figure 39. Insertion Loss Allowed

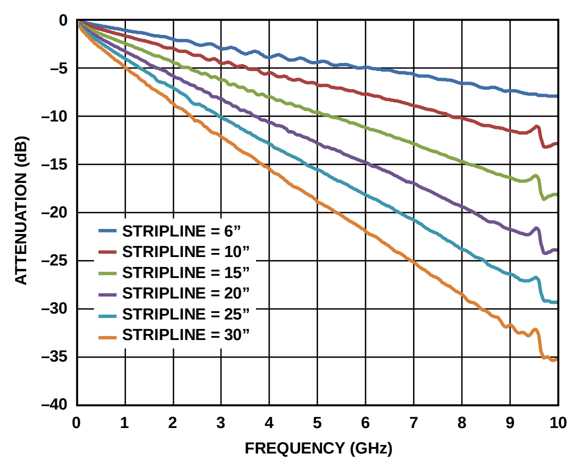


Figure 40. Insertion Loss of 50 Ω Striplines on FR4

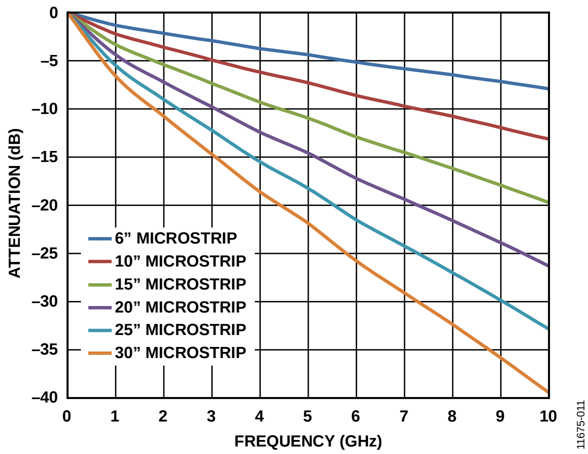


Figure 41. Insertion Loss of 50 Ω Microstrips on FR4

DATA LINK LAYER

The data link layer of the AD9144 JESD204B interface accepts the deserialized data from the PHYs and deframes and descrambles them so that data octets are presented to the transport layer to be put into DAC samples. The architecture of the data link layer is shown in Figure 42. It consists of a synchronization FIFO for each lane, a crossbar switch, a deframer, and descrambler.

The AD9144 can operate as a single link or dual link high speed JESD204B serial data interface. When operating in dual link mode, configure both links with the same JESD204B parameters because they share a common device clock and system reference. All eight lanes of the JESD204B interface handle link layer communications such as code group synchronization, frame alignment, and frame synchronization.

The AD9144 decodes 8-bit/10-bit control characters, allowing marking of the start and end of the frame and alignment between serial lanes. Each AD9144 serial interface link can issue a synchronization request by setting its $\overline{\text{SYNCOUT0±}}$-$\overline{\text{SYNCOUT1±}}$ signal low. The synchronization protocol follows Section 4.9 of the JESD204B standard. When a stream of four consecutive /K/ symbols is received, the AD9144 deactivates the synchronization request by setting the $\overline{\text{SYNCOUT0±}}$-$\overline{\text{SYNCOUT1±}}$ signal high at the next internal LMFC rising edge. Then, it waits for the transmitter to issue an ILAS. During the ILAS sequence, all lanes are aligned using the /A/ to /R/ character transition as described in the JESD204B Serial Link Establishment section. Elastic buffers hold early arriving lane data until the alignment character of the latest lane arrives. At this point, the buffers for all lanes are released and all lanes are aligned (see Figure 43).

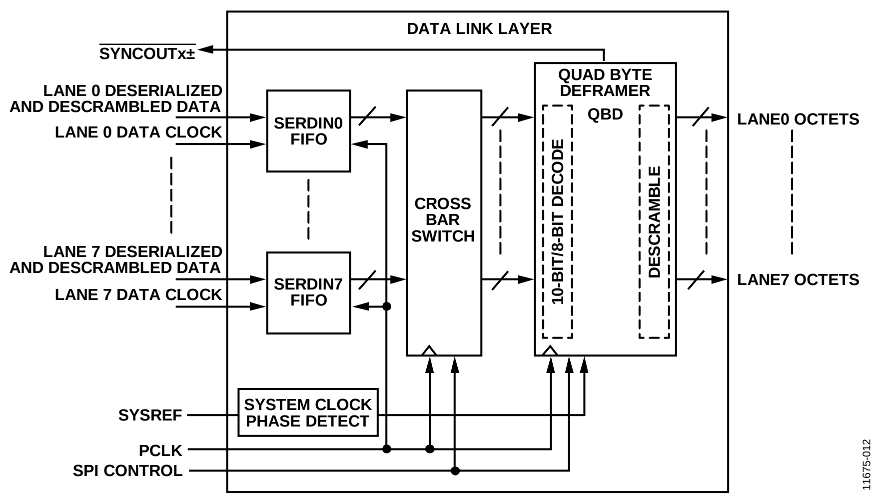


Figure 42. Data Link Layer Block Diagram

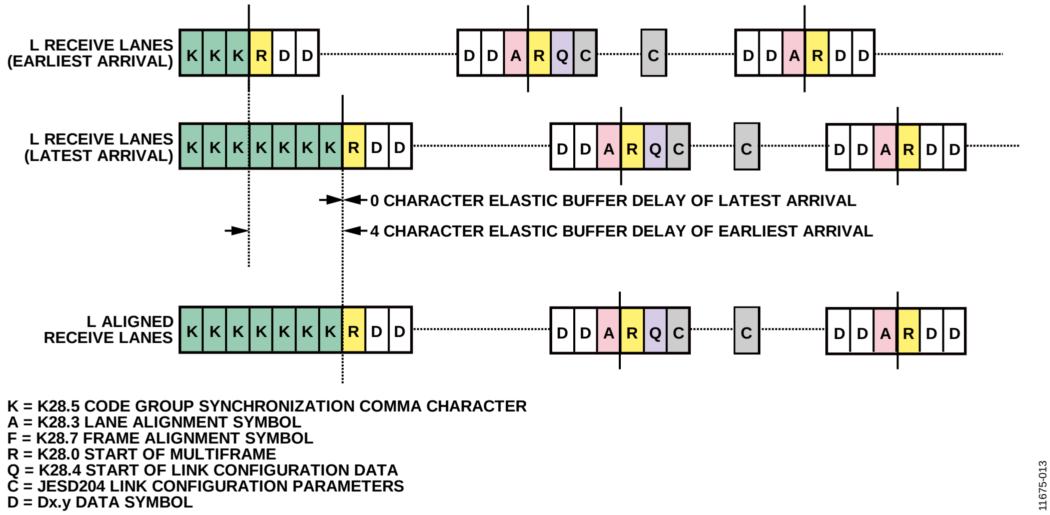


Figure 43. Lane Alignment During ILAS

JESD204B Serial Link Establishment

A brief summary of the high speed serial link establishment process for Subclass 1 is provided. See Section 5.3.3 of the JESD204B specifications document for complete details.

Step 1: Code Group Synchronization

Each receiver must locate K (K28.5) characters in its input data stream. After four consecutive K characters are detected on all link lanes, the receiver block deasserts the $\overline{\text{SYNCOUTx±}}$ signal to the transmitter block at the receiver local multiframe clock (LMFC) edge.

The transmitter captures the change in the $\overline{\text{SYNCOUTx±}}$ signal, and at a future transmitter LMFC rising edge, starts the initial lane alignment sequence (ILAS).

Step 2: Initial Lane Alignment Sequence

The main purposes of this phase are to align all the lanes of the link and verify the parameters of the link.

Before the link is established, write each of the link parameters to the receiver device to designate how data is sent to the receiver block.

The ILAS consists of four or more multiframes. The last character of each multiframe is a multiframe alignment character, /A/. The first, third, and fourth multiframes are populated with predetermined data values. Note that Section 8.2 of the JESD204B specifications document describes the data ramp that is expected during ILAS. By default, the AD9144 does not require this ramp. Register 0x47E[0] can be set high to require the data ramp. The deframer uses the final /A/ of each lane to align the ends of the multiframes within the receiver. The second multiframe contains an R (K.28.0), Q (K.28.4), and then data corresponding to the link parameters. Additional multiframes can be added to the ILAS if needed by the receiver. By default, the AD9144 uses four multiframes in the ILAS (this can be changed in Register 0x478). If using Subclass 1, exactly four multiframes must be used.

After the last /A/ character of the last ILAS, multiframe data begins streaming. The receiver adjusts the position of the /A/ character such that it aligns with the internal LMFC of the receiver at this point.

Step 3: Data Streaming

In this phase, data is streamed from the transmitter block to the receiver block.

Optionally, data can be scrambled. Scrambling does not start until the very first octet following the ILAS.

The receiver block processes and monitors the data it receives for errors, including:

- Bad running disparity (8-bit/10-bit error)
- Not in table (8-bit/10-bit error)
- Unexpected control character
- Bad ILAS
- Interlane skew error (through character replacement)

If any of these errors exist, they are reported back to the transmitter in one of a few ways (see the JESD204B Error Monitoring section for details).

- $\overline{\text{SYNCOUTx±}}$ signal assertion: resynchronization ($\overline{\text{SYNCOUTx±}}$ signal pulled low) is requested at each error for the last two errors. For the first three errors, an optional resynchronization request can be asserted when the error counter reaches a set error threshold.
- For the first three errors, each multiframe with an error in it causes a small pulse on $\overline{\text{SYNCOUTx±}}$.
- Errors can optionally trigger an IRQ event, which can be sent to the transmitter.

Various test modes for verifying the link integrity can be found in the JESD204B Test Modes section.

Lane FIFO

The FIFOs in front of the crossbar switch and deframer synchronize the samples sent on the high speed serial data interface with the deframer clock by adjusting the phase of the incoming data. The FIFO absorbs timing variations between the data source and the deframer; this allows up to two PClock cycles of drift from the transmitter. The FIFO_STATUS_REG_0 register and FIFO_STATUS_REG_1 register (Register 0x30C and Register 0x30D, respectively) can be monitored to identify whether the FIFOs are full or empty.

Lane FIFO IRQ

An aggregate lane FIFO error bit is also available as an IRQ event. Use Register 0x01F[1] to enable the FIFO error bit, and then use Register 0x023[1] to read back its status and reset the IRQ signal. See the Interrupt Request Operation section for more information.

Crossbar Switch

Register 0x308 to Register 0x30B allow arbitrary mapping of physical lanes (SERDINx±) to logical lanes used by the SERDES deframers.

Table 39. Crossbar Registers

Address	Bits	Logical Lane
0x308	[2:0]	LOGICAL_LANE0_SRC
0x308	[5:3]	LOGICAL_LANE1_SRC
0x309	[2:0]	LOGICAL_LANE2_SRC
0x309	[5:3]	LOGICAL_LANE3_SRC
0x30A	[2:0]	LOGICAL_LANE4_SRC
0x30A	[5:3]	LOGICAL_LANE5_SRC
0x30B	[2:0]	LOGICAL_LANE6_SRC
0x30B	[5:3]	LOGICAL_LANE7_SRC

Write each LOGICAL_LANEy_SRC with the number (x) of the desired physical lane (SERDINx±) from which to get data. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default LOGICAL_LANE0_SRC = 0, so Logical Lane 0 gets data from Physical Lane 0 (SERDIN0±). If instead the user wants to use SERDIN4± as the source for Logical Lane 0, the user must write LOGICAL_LANE0_SRC = 4.

Lane Inversion

Register 0x334 allows inversion of desired logical lanes, which can be used to ease routing of the SERDINx± signals. For each Logical Lane x, set Bit x of Register 0x334 to 1 to invert it.

Deframers

The AD9144 consists of two quad byte deframers (QBDs). Each deframer takes in the 8-bit/10-bit encoded data from the deserializer (via the crossbar switch), decodes it, and descrambles it into JESD204B frames before passing it to the transport layer to be converted to DAC samples. The deframer processes four symbols (or octets) per processing clock (PClock) cycle.

In single link mode, Deframer 0 is used exclusively and Deframer 1 remains inactive. In dual link mode, both QBDs are active and must be configured separately using the LINK_PAGE bit (Register 0x300[2]) to select which link you are configuring. The LINK_MODE bit (Register 0x300[3]) =1 for dual link, or 0 for single link.

Each deframer uses the JESD204B parameters that the user has programmed into the register map to identify how the data has been packed and unpack it. The JESD204B parameters are discussed in detail in the Transport Layer section; many of the parameters are also needed in the transport layer to convert JESD204B frames into samples.

Descrambler

The AD9144 provides an optional descrambler block using a self synchronous descrambler with a polynomial: $1 + x^{14} + x^{15}$.

Enabling data scrambling reduces spectral peaks that are produced when the same data octets repeat from frame to frame. It also makes the spectrum data independent so that possible frequency-selective effects on the electrical interface do not cause data-dependent errors. Descrambling of the data is enabled by setting the SCR bit (Register 0x453[7]) to 1.

Syncing LMFC Signals

The first step in guaranteeing synchronization across links and devices begins with syncing the LMFC signals. Each DAC dual (DAC Dual A: DAC0/DAC1 and DAC Dual B: DAC2/DAC3) has its own LMFC signal. In Subclass 0, the LMFC signals for each of the two links are synchronized to an internal processing clock. In Subclass 1, all LMFC signals (for all duals and devices) are synchronized to an external SYSREF signal. All LMFC sync registers are paged as described in the Dual Paging section.

SYSREF Signal

The SYSREF signal is a differential source synchronous input that synchronizes the LMFC signals in both the transmitter and receiver in a JESD204B Subclass 1 system to achieve deterministic latency.

The SYSREF signal is an active high signal that is sampled by the device clock rising edge. It is best practice that the device clock and SYSREF signals be generated by the same source, such as the AD9516-x clock generator, so that the phase alignment between the signals is fixed. When designing for optimum deterministic latency operation, consider the timing distribution skew of the SYSREF signal in a multipoint link system (multichip).

The AD9144 supports a single pulse or step, or a periodic SYSREF± signal. The periodicity can be continuous, strobed, or gapped periodic. The SYSREF± signal can always be dc-coupled (with a common-mode voltage of 0 V to 2 V). When dc-coupled, a small amount of common-mode current (<500 µA) is drawn from the SYSREF± pins. See Figure 44 for the SYSREF± internal circuit.

To avoid this common-mode current draw, a 50% duty-cycle periodic SYSREF± signal can be used with ac coupling capacitors. If ac-coupled, the ac coupling capacitors combine with the resistors shown in Figure 44 to make a high-pass filter with RC time constant τ = RC. Select C such that τ > 4/SYSREF Freq. In addition, the edge rate must be sufficiently fast—at least 1.3 V/ns is recommended per Table 5—to meet the SYSREF vs. DAC clock keep out window (KOW) requirements.

It is possible to use ac-coupled mode without meeting the frequency to time-constant constraint above by using SYSREF hysteresis (Register 0x081 and Register 0x082). However, this increases the DAC clock KOW (Table 5 does not apply) by an amount depending on SYSREF frequency, level of hysteresis, capacitor choice, and edge rate.

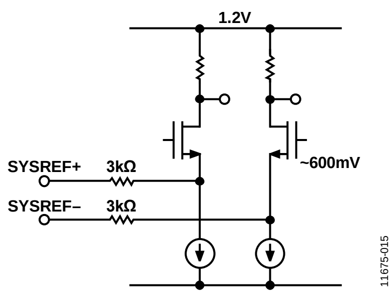


Figure 44. SYSREF± Input Circuit

Sync Processing Modes Overview

The AD9144 supports various LMFC sync processing modes. These modes are one shot, continuous, windowed continuous, and monitor modes. All sync processing modes perform a phase check to see that the LMFC is phase aligned to an alignment edge. In Subclass 1, the SYSREF pulse acts as the alignment edge; in Subclass 0, an internal processing clock acts as the alignment edge. If the signals are not in phase, a clock rotation occurs to align the signals. The sync modes are described below. See the Sync Procedure section for details on the procedure for syncing the LMFC signals.

One Shot Sync Mode (SYNCMODE = 0x1)

In one shot sync mode, a phase check occurs on only the first alignment edge that is received after the sync machine is armed. If the phase error is larger than a specified window error tolerance, a phase adjustment occurs. Though an LMFC synchronization occurs only once, the SYSREF signal can still be continuous.

Continuous Sync Mode (SYNCMODE = 0x2)

Continuous mode must only be used in Subclass 1 with a periodic SYSREF± signal. In continuous mode, a phase check/alignment occurs on every alignment edge.

Continuous mode differs from the one shot mode in two ways. First, no SPI cycle is required to arm the device; the alignment edge seen after continuous mode is enabled results in a phase check. Second, a phase check (and when necessary, clock rotation) occurs on every alignment edge in continuous mode. The one caveat to the previous statement is that when a phase rotation cycle is underway, subsequent alignment edges are ignored until the logic lane is ready again.

The maximum acceptable phase error (in DAC clock cycles) between the alignment edge and the LMFC edge is set in the error window tolerance register. If continuous sync mode is used with a non zero error window tolerance, then a phase check occurs on every SYSREF pulse, but an alignment occurs only if the phase error is greater than the specified error window tolerance. If the jitter of the SYSREF± signal violates the KOW specification given in Table 5 and therefore causes phase error uncertainty, the error tolerance can be increased to avoid constant clock rotations. Note that this means the latency is less deterministic by the size of the window. If the error window tolerance must be set above 3, Subclass 0 with a one shot sync is recommended, which in the AD9144 implementation is deterministic to within 4 DAC clock cycles.

For debug purposes, SYNCARM (Register 0x03A[6]) can be used to inform the user that alignment edges are being received in continuous mode. Because the SYNCARM bit is self cleared after an alignment edge is received, the user can arm the sync (SYNCARM (Register 0x03A[6]) = 1), and then read back SYNCARM. If SYNCARM = 0, the alignment edges are being received and phase checks are occurring. Arming the sync machine in this mode does not affect the operation of the device.

One Shot then Monitor Sync Mode (SYNCMODE = 0x9)

In one shot then monitor mode, the user can monitor the phase error in real time. Use this sync mode with a periodic SYSREF± signal. A phase check and alignment occurs on the first alignment edge received after the sync machine is armed. On all subsequent alignment edges the phase is monitored and reported, but no clock phase adjustment occurs.

The phase error can be monitored on the SYNC_CURRERR_L register, (Register 0x03C[3:0]). Immediately after an alignment occurs, CURRERR = 0 to indicate that there is no difference between the alignment edge and the LMFC edge. On every subsequent alignment edge, the phase is checked. If the alignment is lost, the phase error is reported in the SYNC_CURRERR_L register in DAC clock cycles. If the phase error is beyond the selected window tolerance (Register 0x034[2:0]), one bit of Register 0x03D[7:6] is set high depending on whether the phase error is on low or high side.

When an alignment occurs, snapshots of the last phase error (Register 0x03C[3:0]) and the corresponding error flags (Register 0x03D[7:6]) are placed into readable registers for reference (Register 0x038 and Register 0x039, respectively).

Sync Procedure

The procedure for enabling the sync is as follows:

1. Set Register 0x008 to 0x03 to sync the LMFC for both duals (DAC0/DAC1 and DAC2/DAC3)
2. Set the desired sync processing mode. The sync processing mode settings are listed in Table 40.
3. For Subclass 1, set the error window according to the uncertainty of the SYSREF± signal relative to the DAC clock and the tolerance of the application for deterministic latency uncertainty. Sync window tolerance settings are given in Table 41.
4. Enable sync by writing SYNCENABLE (Register 0x03A[7] = 1).
5. If in one shot mode, arm the sync machine by writing SYNCARM (Register 0x03A[6] = 1).
6. If in Subclass 1, ensure that at least one SYSREF pulse is sent to the device.
7. Check the status by reading the following bit fields:
   a) SYNC_BUSY (Register 0x03B[7]) = 0 to indicate that the sync logic is no longer busy.
   b) SYNC_LOCK (Register 0x03B[3]) = 1 to indicate that the signals are aligned. This bit updates on every phase check.
   c) SYNC_WLIM (Register 0x03B[1]) = 0 to indicate that the phase error is not beyond the specified error window. This bit updates on every phase check.
   d) SYNC_ROTATE (Register 0x03B[2]) = 1 if the phases were not aligned before the sync and an alignment occurred, this indicates that a clock alignment occurred. This bit is sticky and can be cleared only by writing to SYNCCLRSTKY control bit (Register 0x03A[5]).
   e) SYNC_TRIP (Register 0x03B[0]) = 1 to indicate alignment edge received and phase check occurred. This bit is sticky and can be cleared only by writing to SYNCCLRSTKY control bit (Register 0x03A[5]).

Table 40. Sync Processing Modes

Sync Processing Mode	SYNCMODE (Register 0x03A[3:0])
One shot	0x01
Continuous	0x02
One shot then monitor	0x09

Table 41. Sync Window Tolerance

Sync Error Window Tolerance	ERRWINDOW (Register 0x034[2:0])
±1/2 DAC clock cycles	0x00
±1 DAC clock cycles	0x01
±2 DAC clock cycles	0x02
±3 DAC clock cycles	0x03

LMFC Sync IRQ

The sync status bits (SYNCLOCK, SYNCROTATE, SYNCTRIP, and SYNCWLIM) are available as IRQ events.

Use Register 0x021[3:0] to enable the sync status bits for DAC Dual A (DAC0 and DAC1), and then use Register 0x025[3:0] to read back their statuses and reset the IRQ signals.

Use Register 0x022[3:0] to enable the sync status bits for DAC Dual B (DAC2 and DAC3), and then use Register 0x026[3:0] read back their statuses and reset the IRQ signals.

See the Interrupt Request Operation section for more information.

Deterministic Latency

JESD204B systems contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the link from power cycle to power cycle with each new link establishment. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9144 supports JESD204B Subclass 0 and Subclass 1 operation, but not Subclass 2. Write the subclass to Register 0x301[2:0] and once per link to Register 0x458[7:5].

Subclass 0

This mode gives deterministic latency to within 4 DAC clock cycles. It does not require any signal on the SYSREF± pins, which can be left disconnected.

Subclass 0 still requires that all lanes arrive within the same LMFC cycle and the dual DACs must be synchronized to each other.

Minor Subclass 0 Caveats

Because the AD9144 requires an ILAS, the nonmultiple converter single lane (NMCDA-SL) case from the JESD204A specification is only supported when using the optional ILAS.

Error reporting using $\overline{\text{SYNCOUTx±}}$ is not supported when using Subclass 0 with F = 1.

Subclass 1

This mode gives deterministic latency and allows links to be synced to within ½ a DAC clock period. It requires an external SYSREF± signal that is accurately phase aligned to the DAC clock.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links and devices must be ≤10 PClock periods. This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Link Delay

The link delay of a JESD204B system is the sum of fixed and variable delays from the transmitter, channel and receiver as shown in Figure 47.

For proper functioning, all lanes on a link must be read during the same LMFC period. Section 6.1 of the JESD204B specification states that the LMFC period must be larger than the maximum link delay. For the AD9144, this is not necessarily the case; instead, the AD9144 uses a local LMFC for each link ($LMFC_{Rx}$) that can be delayed from the SYSREF aligned LMFC. Because the LMFC is periodic, this can account for any amount of fixed delay. As a result, the LMFC period must only be larger than the variation in the link delays, and the AD9144 can achieve proper performance with a smaller total latency. Figure 45 and Figure 46 show a case where the link delay is larger than an LMFC period. Note that it can be accommodated by delaying $LMFC_{Rx}$.

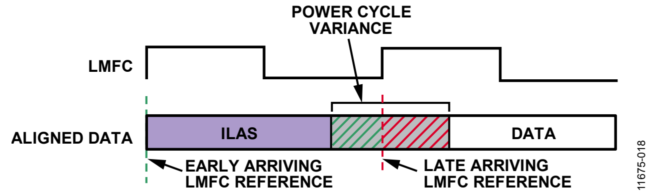


Figure 45. Link Delay > LMFC Period Example

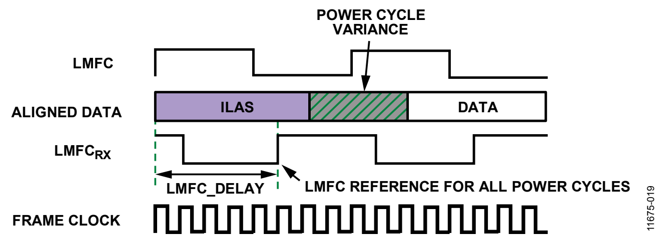


Figure 46. LMFC_DELAY to Compensate for Link Delay > LMFC

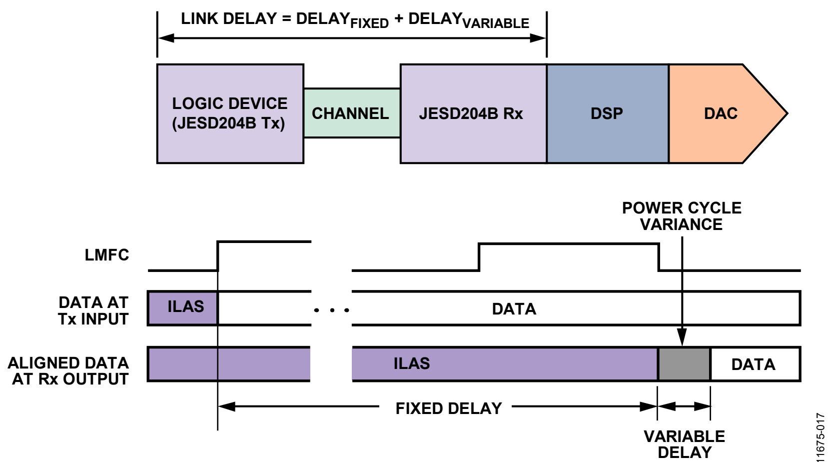


Figure 47. JESD204B Link Delay = Fixed Delay + Variable Delay

The method for setting the LMFCDel and LMFCVar is described in the Link Delay Setup section.

Setting LMFCDel appropriately ensures that all the corresponding data samples arrive in the same LMFC period. Then LMFCVar is written into the receive buffer delay (RBD) to absorb all link delay variation. This ensures that all data samples have arrived before reading. By setting these to fixed values across runs and devices, deterministic latency is achieved.

The RBD described in the JESD204B specification takes values from 1 to K FrameClock cycles, while the RBD of the AD9144 takes values from 0 to 10 PClock cycles. As a result, up to 10 PClock cycles of total delay variation can be absorbed. Because LMFCVar is in PClock cycles, and LMFCDel is in FrameClock cycles, a conversion between these two units is needed. The PClockFactor, or number of Frame Clock Cycles per PClock cycle, is equal to 4/F. For more information on this relationship, see the Clock Relationships section.

Two examples follow that show how to determine LMFCVar and LMFCDel. After they are calculated, write LMFCDel into both Register 0x304 and Register 0x305 for all devices in the system, and write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

Link Delay Setup Example, With Known Delays

All the known system delays can be used to calculate LMFCVar and LMFCDel as described in the Link Delay Setup section.

The example shown in Figure 48 is demonstrated in the following steps according to the procedure outlined in the Link Delay Setup section. Note that this example is in Subclass 1 to achieve deterministic latency, which has a PClockFactor (4/F) of 2 FrameClock Cycles per PClock Cycle, and uses K = 32 (frames/multiframe). Because PCBFixed << PClockPeriod, PCBFixed is negligible in this example and not included in the calculations.

1. Find the receiver delays using Table 8.
   $RxFixed$ = 17 PClock cycles
   $RxVar$ = 2 PClock cycles
2. Find the transmitter delays. The equivalent table in the example JESD core (implemented on a GTH or GTX transceiver on a Virtex-6 FPGA) states that the delay is 56 ± 2 byte clock cycles.
   Because the PClockRate = ByteRate/4 as described in the Clock Relationships section, the transmitter delays in PClock cycles are:
   $TxFixed = 54/4 = 13.5$ PClock cycles
   $TxVar = 4/4 = 1$ PClock cycle
3. Calculate MinDelayLane as follows:
   $MinDelayLane = \text{floor}(RxFixed + TxFixed + PCBFixed)$
   $= \text{floor}(17 + 13.5 + 0)$
   $= \text{floor}(30.5)$
   $MinDelayLane = 30$
4. Calculate MaxDelayLane as follows:
   $MaxDelayLane = \text{ceiling}(RxFixed + RxVar + TxFixed + TxVar + PCBFixed))$
   $= \text{ceiling}(17 + 2 + 13.5 + 1 + 0)$
   $= \text{ceiling}(33.5)$
   $MaxDelayLane = 34$
5. Calculate LMFCVar as follows:
   $LMFCVar = (MaxDelay + 1) - (MinDelay - 1)$
   $= (34 + 1) - (30 - 1) = 35 - 29$
   $LMFCVar = 6$ PClock cycles
6. Calculate LMFCDel as follows:
   $LMFCDel = ((MinDelay - 1) \times PClockFactor) \% K$
   $= ((30 - 1) \times 2) \% 32 = (29 \times 2) \% 32$
   $= 58 \% 32$
   $LMFCDel = 26$ FrameClock cycles
7. Write LMFCDel to both Register 0x304 and Register 0x305 for all devices in the system. Write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

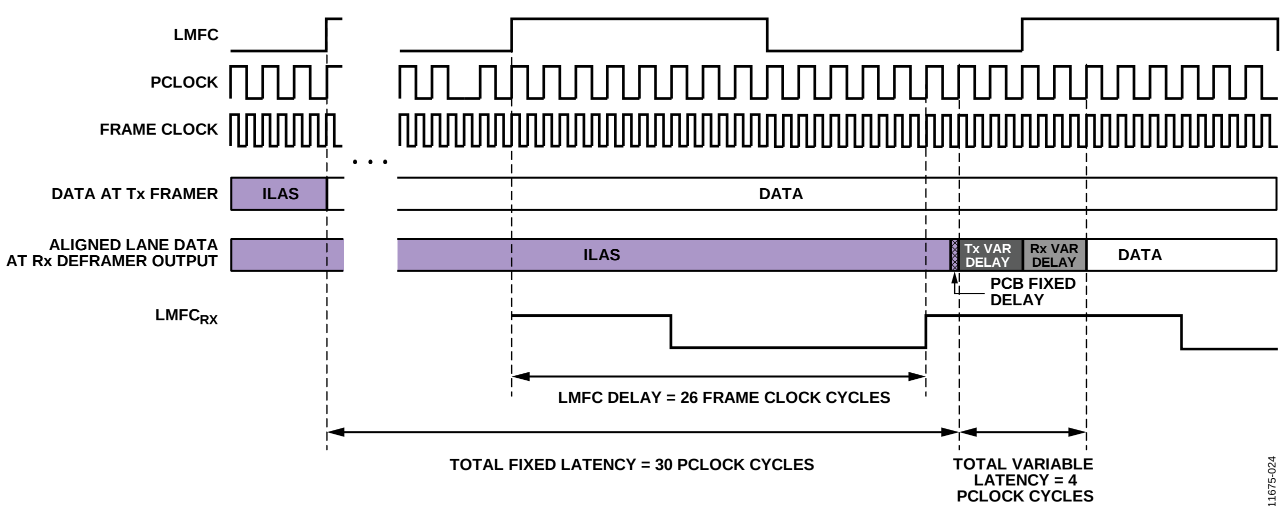


Figure 48. LMFC_DELAY Calculation Example

Link Delay Setup Example, Without Known Delay

If the system delays are not known, the AD9144 can read back the link latency between $LMFC_{RX}$ for each link and the SYSREF aligned LMFC. This information is then used to calculate LMFCVar and LMFCDel, as shown in the Without Known Delays section.

Figure 50 shows how DYN_LINK_LATENCY_x (Register 0x302 and Register 0x303) provides a readback showing the delay (in PClock cycles) between $LMFC_{RX}$ and the transition from ILAS to the first data sample. By repeatedly power-cycling and taking this measurement, the minimum and maximum delays across power cycles can be determined and used to calculate LMFCVar and LMFCDel.

The example shown in Figure 50 is demonstrated in the following steps according to the procedure outlined in the Without Known Delays section. Note that this example is in Subclass 1 to achieve deterministic latency, which has a PClockFactor (FrameClockRate/PClkRate) of 2 and uses K = 16; therefore PClocksPerMF = 8.

1. In Figure 50, for Link A, Link B, and Link C, the system containing the AD9144 (including the transmitter) is power cycled and configured 20 times. The AD9144 is configured as described in the Device Setup Guide. As the point of this exercise is to determine LMFCDel and LMFCVar, the LMFCDel is programmed to 0 and the DYN_ LINK_LATENCY_x is read from Register 0x302 and Register 0x303 for Link 0 and Link 1, respectively. The variation in the link latency over the 20 runs is shown in Figure 50 in grey.
   - Link A gives readbacks of 6, 7, 0, and 1. Note that the set of recorded delay values rolls over the edge of a multiframe at the boundary K/PClockFactor = 8. Add PClocksPerMF = 8 to low set. Delay values range from 6 to 9.
   - Link B gives Delay values from 5 to 7.
   - Link C gives Delay values from 4 to 7.
2. Calculate the minimum of all Delay measurements across all power cycles, links, and devices:
   MinDelay = min(all *Delay* values) = 4
3. Calculate the maximum of all Delay measurements across all power cycles, links, and devices:
   MaxDelay = max(all *Delay* values) = 9
4. Calculate the total Delay variation (with guard band) across all power cycles, links, and devices:
   $LMFCVar = (MaxDelay + 1) - (MinDelay - 1)$
   $= (9 + 1) - (4 - 1) = 10 - 3 = 7$ PClock cycles
5. Calculate the minimum delay in FrameClock cycles (with guard band) across all power cycles, links, and devices:
   $LMFCDel = ((MinDelay - 1) \times PClockFactor) \% K$
   $= ((4 - 1) \times 2) \% 16 = (3 \times 2) \% 16$
   $= 6 \% 16 = 6$ FrameClock cycles
6. Write LMFCDel to both Register 0x304 and Register 0x305 for all devices in the system. Write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

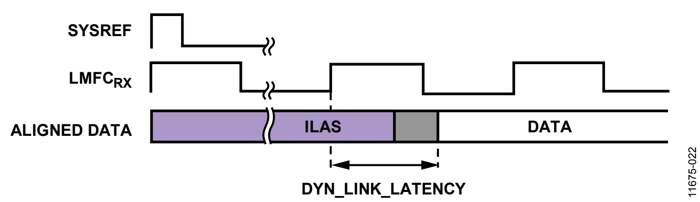


Figure 49. DYN_LINK_LATENCY Illustration

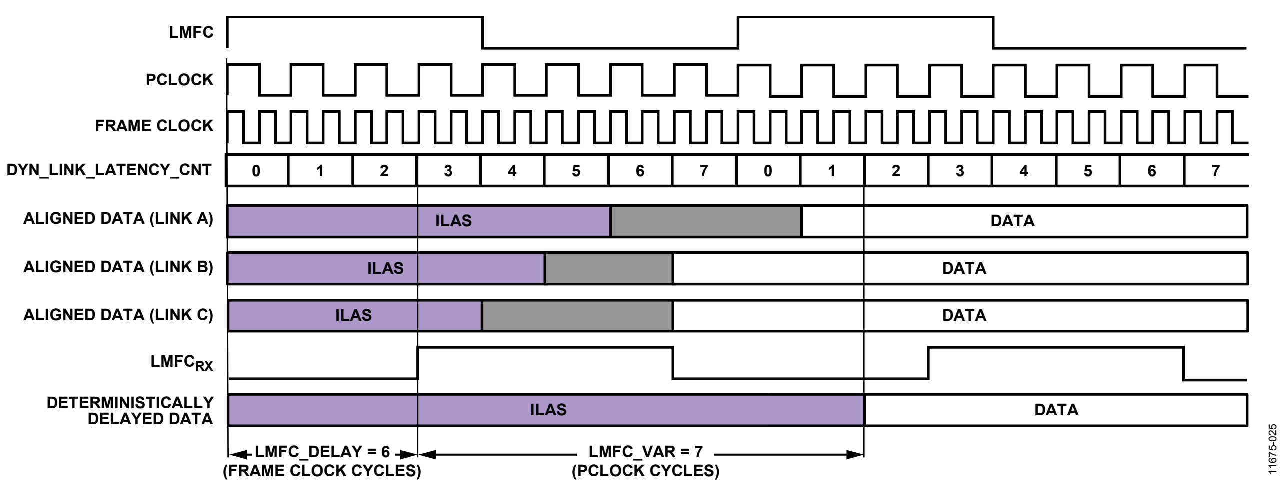


Figure 50. Multilink Synchronization Settings, Derived Method Example

TRANSPORT LAYER

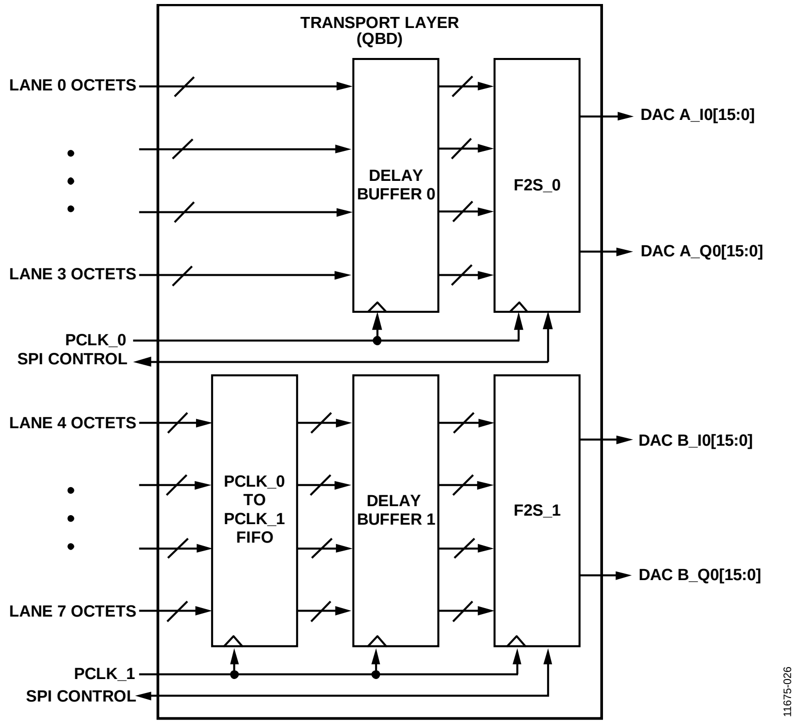


Figure 51. Transport Layer Block Diagram

The transport layer receives the descrambled JESD204B frames and converts them to DAC samples based on the programmed JESD204B parameters shown in Table 42. A number of device parameters are defined in Table 43.

Table 42. JESD204B Transport Layer Parameters

Parameter	Description
F	Number of octets per frame per lane: 1, 2, or 4.
K	Number of frames per multiframe.
	K = 32 if F = 1, K = 16 or 32 otherwise.
L	Number of lanes per converter device (per link), as follows.
	1, 2, 4, or 8 (single link mode).
	1, 2, or 4 (dual link mode).
M	Number of converters per device (per link), as follows.
	1, 2, or 4 (single link mode).
	1 or 2 (dual link mode).
S	Number of samples per converter, per frame: 1 or 2.

Table 43. JESD204B Device Parameters

Parameter	Description
CF	Number of control words per device clock per link. Not supported, must be 0.
CS	Number of control bits per conversion sample. Not supported, must be 0.
HD	High density user data format. Used when samples must be split across lanes. Set to 1 when F = 1, otherwise 0.
N	Converter resolution = 16.
N' (aka NP)	Total number of bits per sample = 16.

Certain combinations of these parameters, called JESD204B operating modes, are supported by the AD9144. See Table 44 and Table 45 for a list of supported modes, along with their associated clock relationships.

Table 44. Single Link JESD204B Operating Modes

	Mode									
Parameter	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Count)	4	4	4	4	2	2	2	2	1	1
L (Lane Count)	8	8	4	2	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	2	1	1	1	1
F (Octets per Frame, per Lane)	1	2	2	4	1	2	2	4	1	2
K[1] (Frames per Multiframe)	32	16/32	16/32	16/32	32	16/32	16/32	16/32	32	16/ 32
HD (High Density)	1	0	0	0	1	0	0	0	1	0
N (Converter Resolution)	16	16	16	16	16	16	16	16	16	16
NP (Bits per Sample)	16	16	16	16	16	16	16	16	16	16
Example Clocks for 10 Gbps Lane Rate										
PClock Rate (MHz)	250	250	250	250	250	250	250	250	250	250
FrameClock Rate (MHz)	1000	500	500	250	1000	500	500	250	1000	500
Data Rate (MHz)	1000	1000	500	250	1000	1000	500	250	1000	500

[1] K must be 32 in Mode 0, Mode 4, and Mode 9. It can be 16 or 32 in all other modes.

Table 45. Dual Link JESD204B Operating Modes for Link 0 and Link 1

	Mode					
Parameter	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Count)	2	2	2	2	1	1
L (Lane Count)	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	1
F (Octets per Frame per Lane)	1	2	2	4	1	2
K[1] (Frames per Multiframe)	32	16/32	16/32	16/32	32	16/32
HD (High Density)	1	0	0	0	1	0
N (Converter Resolution)	16	16	16	16	16	16
NP (Bits per Sample)	16	16	16	16	16	16
Example Clocks for 10 Gbps Lane Rate						
PClock Rate (MHz)	250	250	250	250	250	250
FrameClock Rate (MHz)	1000	500	500	250	1000	500
Data Rate (MHz)	1000	1000	500	250	1000	500

[1] K must be 32 in Mode 4 and Mode 9. It can be 16 or 32 in all other modes.

Configuration Parameters

The AD9144 modes refer to the link configuration parameters for L, K, M, N, NP, S, and F. Table 46 provides the description and addresses for these settings.

Table 46. Configuration Parameters

JESD204B Setting	Description	Address
L − 1	Number of lanes − 1.	0x453[4:0]
F − 1	Number of ((octets per frame) per lane) − 1.	0x454[7:0]
K − 1	Number of frames per multiframe − 1.	0x455[4:0]
M − 1	Number of converters − 1.	0x456[7:0]
N − 1	Converter bit resolution − 1.	0x457[4:0]
NP − 1	Bit packing per sample − 1.	0x458[4:0]
S − 1	Number of ((samples per converter) per frame) − 1.	0x459[4:0]
HD	High density format. Set to 1 if F = 1. Leave at 0 if F ≠ 1.	0x45A[7]
F[1]	F parameter, in ((octets per frame) per lane).	0x476[7:0]
DID	Device ID. Match the Device ID sent by the transmitter.	0x450[7:0]
BID	Bank ID. Match the Bank ID sent by the transmitter.	0x451[3:0]
LID0	Lane ID for lane 0. Match the Lane ID sent by the transmitter on Logical Lane 0.	0x452[4:0]
JESDV	JESD Version. Match the version sent by the transmitter (0x0 = JESD204A, 0x1 = JESD204B).	0x459[7:5]

[1] F must be programmed in two places.

Data Flow Through the JESD204B Receiver

The link configuration parameters determine how the serial bits on the JESD204B receiver interface are deframed and passed on to the DACs as data samples. Figure 52 shows a detailed flow of the data through the various hardware blocks for Mode 4 (L = 4, M = 2, S = 1, F = 1). Simplified flow diagrams for all other modes are provided in Figure 53 through Figure 61.

Single and Dual Link Configuration

The AD9144 uses the settings contained in Table 44 and Table 45. Mode 0 to Mode 10 can be used for single link operation. Mode 4 to Mode 10 can also be used for dual link operation.

To use dual link mode, set LINK_MODE (Register 0x300[3]) to 1. In dual link mode, Link 1 must be programmed with identical parameters to Link 0. To write to Link 1, set LINK_PAGE (Register 0x300[2]) to 1.

If single link mode is being used, a small amount of power can be saved by powering down the output buffer for $\overline{\text{SYNCOUT1}}$±, which can be done by setting Register 0x203[0] = 1.

Checking Proper Configuration

As a convenience, the AD9144 provides some quick configuration checks. Register 0x030[5] is high if an illegal LMFC_DELAY is used. Register 0x030[3] is high if an unsupported combination of L, M, F, and S is used. Register 0x030[2] is high if an illegal K is used. Register 0x030[1] is high if an illegal SUBCLASSV is used.

Deskewing and Enabling Logical Lanes

After proper configuration, the logical lanes must be deskewed and enabled to capture data.

Set Bit x in Register 0x46C to 1 to deskew Logical Lane x and to 0 if that logical lane is not being used. Then, set Bit x in Register 0x47D to 1 to enable Logical Lane x and to 0 if that logical lane is not being used.

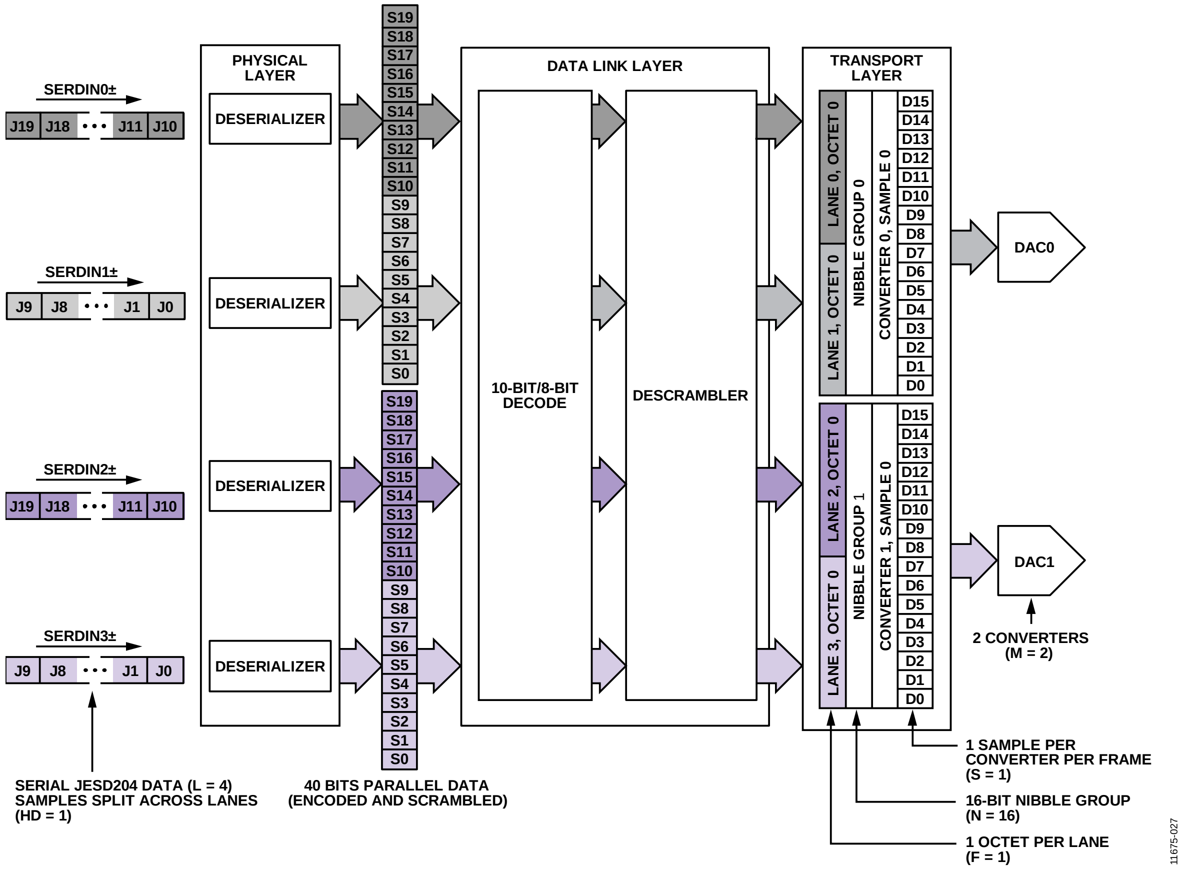


Figure 52. JESD204B Mode 4 Data Deframing

Mode Configuration Maps

Table 47 to Table 56 contain the SPI configuration map for each mode shown in Figure 53 through Figure 61. Figure 53 through Figure 61 show the associated data flow through the deframing process of the JESD204B receiver for each of the modes. Mode 0 to Mode 10 apply to single link operation. Mode 4 to Mode 10 also apply to dual link operation. Register 0x300 must be set accordingly for single or dual link operation as previously discussed.

Additional details regarding all the SPI registers can be found in the Register Maps and Descriptions section.

Table 47. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 0

Address	Setting	Description
0x453	0x07 or 0x87	Register 0x453[7] = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x7: L = 8 lanes per converter
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x03	Register 0x456[7:0] = 0x03: M = 4 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0xF: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: JESD204B version; Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x80	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0xFF	Register 0x47D[7:0] = 0xFF: 8 lanes enabled, set one bit per lane to enable

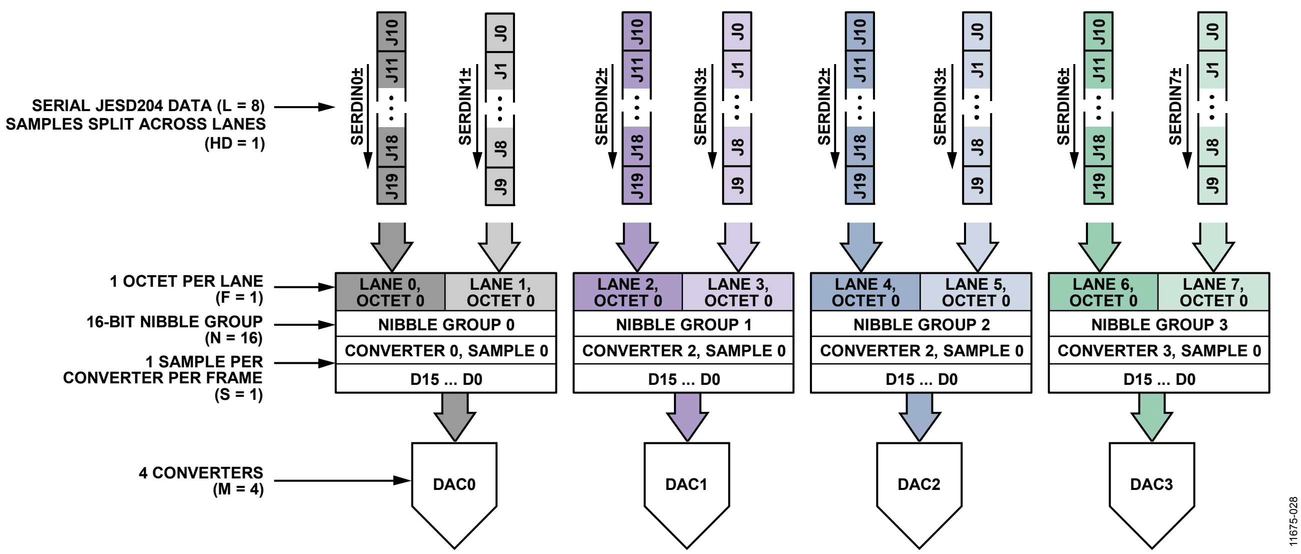


Figure 53. JESD204B Mode 0 Data Deframing

Table 48. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 1

Address	Setting	Description
0x453	0x07 or 0x87	Register 0x453[7] = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x7: L = 8 lanes per converter
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x03	Register 0x456[7:0] = 0x03: M = 4 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x21	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x1: S = 2 samples per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0xFF	Register 0x47D[7:0] = 0xFF: 8 lanes enabled, set one bit per lane to enable

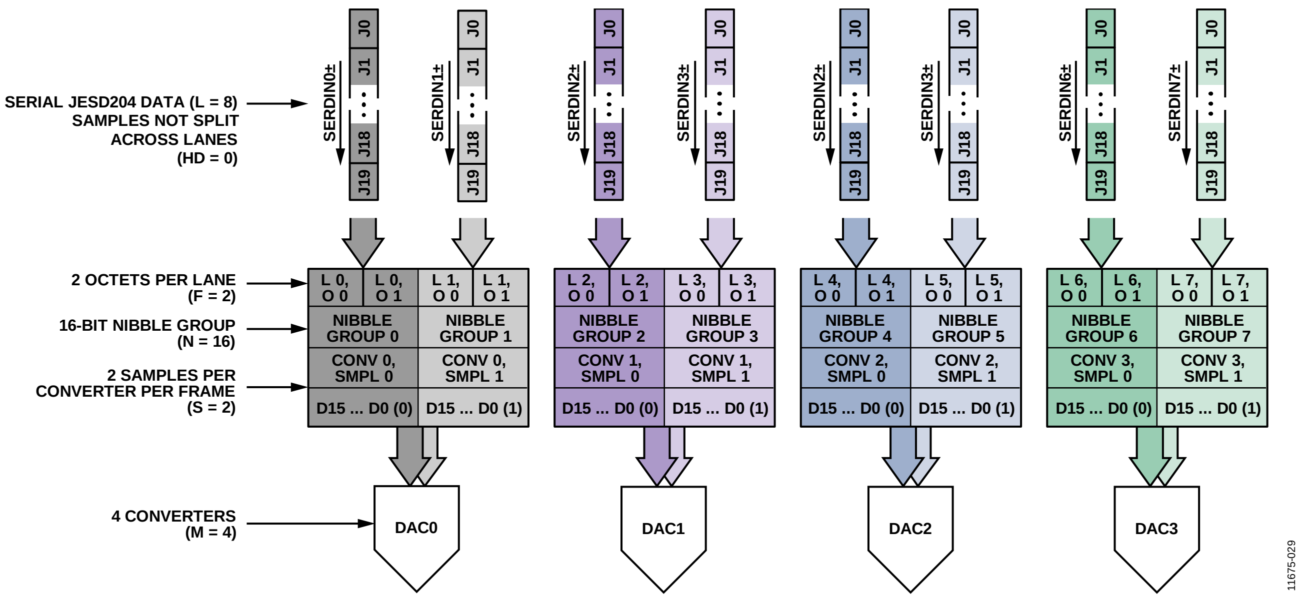


Figure 54. JESD204B Mode 1 Data Deframing

Table 49. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 2

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453[7] = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x3: L = 4 lanes per converter
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x03	Register 0x456[7:0] = 0x03: M = 4 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0x0F	Register 0x47D[7:0] = 0x0F: 4 lanes enabled, set one bit per lane to enable

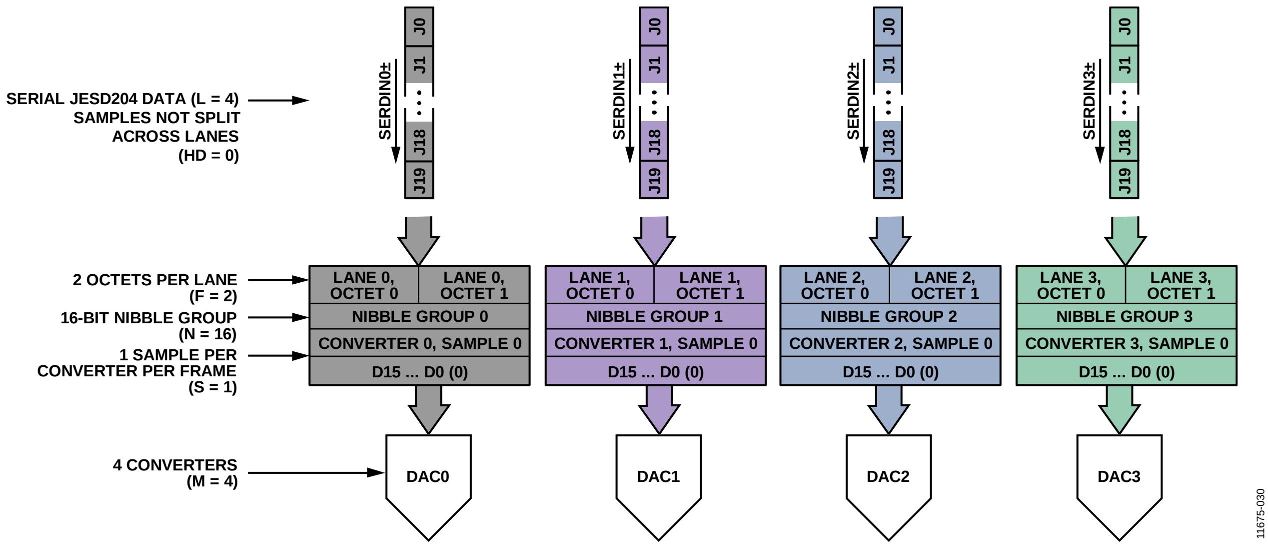


Figure 55. JESD204B Mode 2 Data Deframing

Table 50. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 3

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453[7] = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x1: L = 2 lanes per converter
0x454	0x03	Register 0x454[7:0] = 0x03: F = 4 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x03	Register 0x456[7:0] = 0x03: M = 4 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] =0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x04	Register 0x476[7:0] = 0x04: F = 4 octets per frame
0x47D	0x03	Register 0x47D[7:0] = 0x03: 2 lanes enabled, set one bit per lane to enable

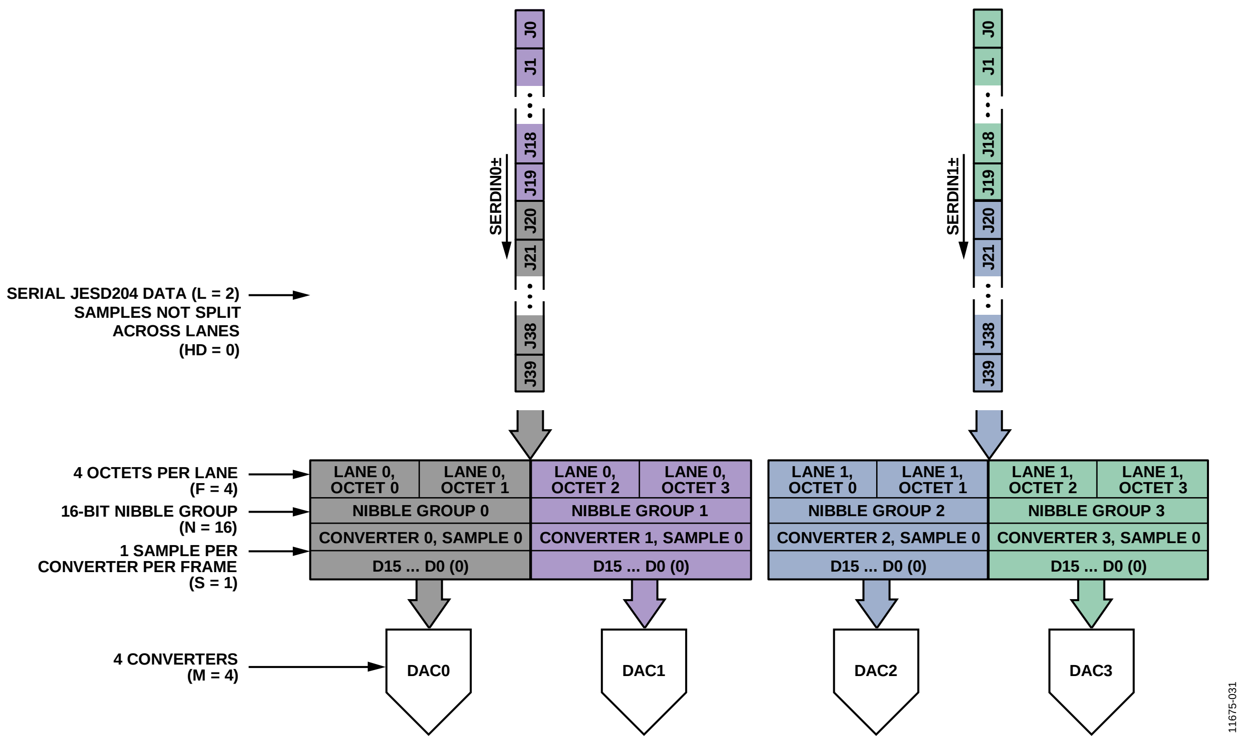


Figure 56. JESD204B Mode 3 Data Deframing

Table 51. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 4

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453[7] = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x3: L = 4 lanes per converter
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K =16 or 32 frames per multiframe
0x456	0x01	Register 0x456[7:0] = 0x01: M = 2 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x01	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0x0F	Register 0x47D[7:0] = 0x0F: 4 lanes enabled, set one bit per lane to enable

See Figure 52 for an illustration of the AD9144 JESD204B Mode 4 data deframing process.

Table 52. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 5

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453[7] = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x3: L = 4 lanes per converter
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x01	Register 0x456[7:0] = 0x01: M = 2 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x21	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x1: S = 2 samples per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0x0F	Register 0x47D[7:0] = 0x0F: 4 lanes enabled, set one bit per lane to enable

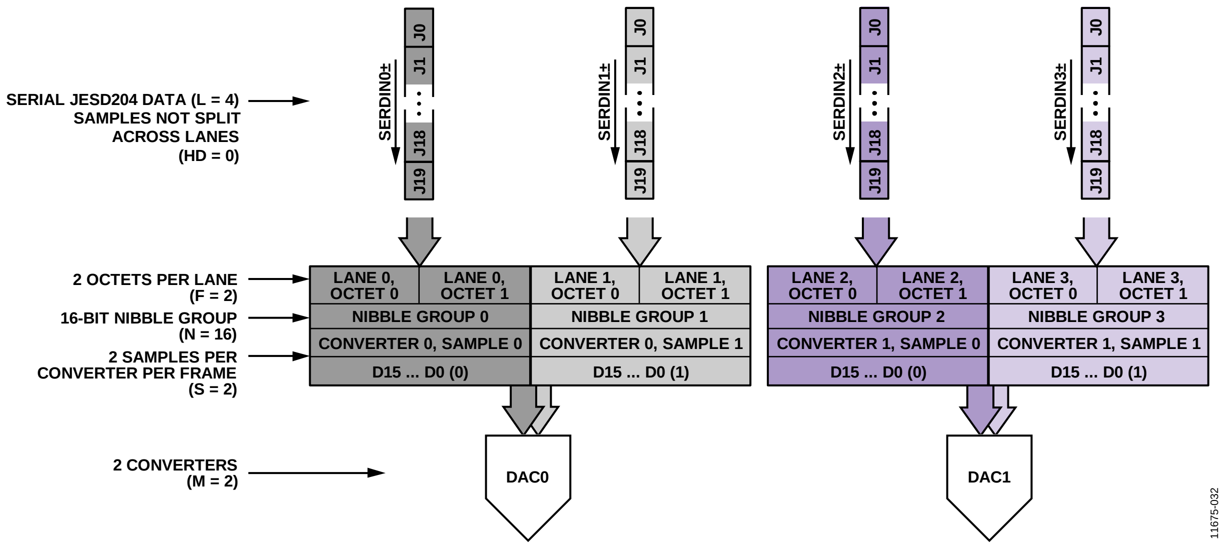


Figure 57. JESD204B Mode 5 Data Deframing

Table 53. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 6

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x1: L = 2 lanes per converter
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x01	Register 0x456[7:0] = 0x01: M = 2 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0x03	Register 0x47D[7:0] = 0x03: 2 lanes enabled, set one bit per lane to enable

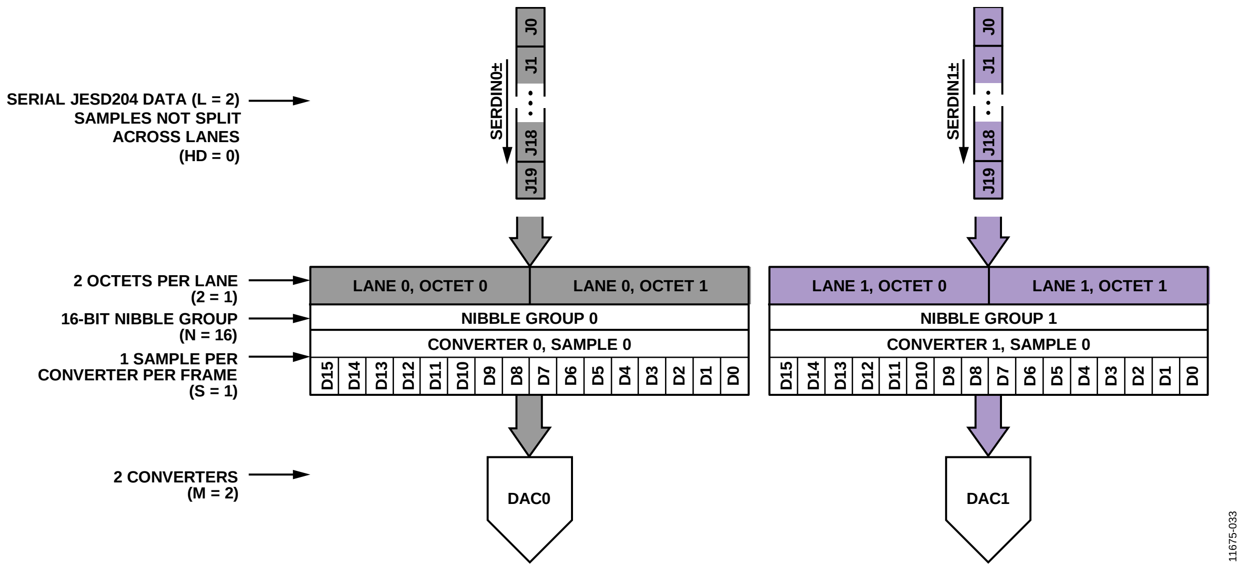


Figure 58. JESD204B Mode 6 Data Deframing

Table 54. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 7

Address	Setting	Description
0x453	0x00 or 0x80	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x0: L = 1 lane per converter
0x454	0x03	Register 0x454[7:0] = 0x03: F = 4 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x01	Register 0x456[7:0] = 0x01: M = 2 converters per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x04	Register 0x476[7:0] = 0x04: F = 4 octets per frame
0x47D	0x01	Register 0x47D[7:0] = 0x01: 1 lane enabled, set one bit per lane to enable

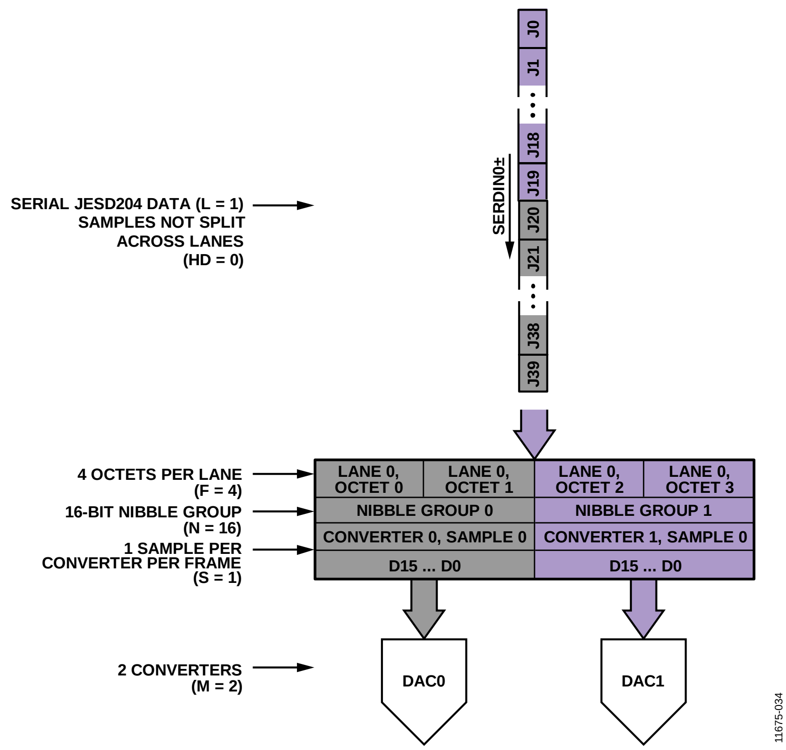


Figure 59. JESD204B Mode 7 Data Deframing

Table 55. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 9

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x1: L = 2 lanes per converter
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: Set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x01	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0x03	Register 0x47D[7:0] = 0x03: 2 lanes enabled, set one bit per lane to enable

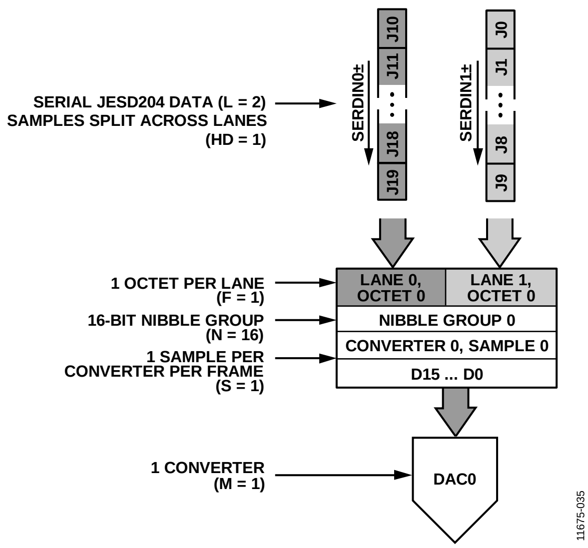


Figure 60. JESD204B Mode 9 Data Deframing

Table 56. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 10

Address	Setting	Description
0x453	0x00 or 0x80	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x0: L = 1 lane per converter
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per device
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version, Register 0x459[4:0] = 0x0: S = 1 sample per converter
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0x01	Register 0x47D[7:0] = 0x01: 1 lane enabled, set one bit per lane to enable

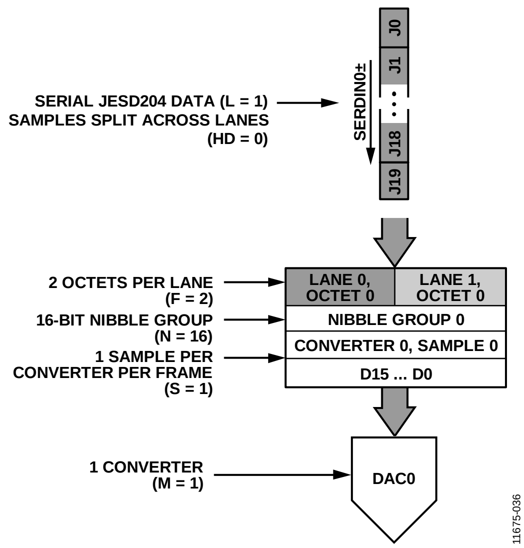


Figure 61. JESD204B Mode 10 Data Deframing

JESD204B TEST MODES

PHY PRBS Testing

The JESD204B receiver on the AD9144 includes a PRBS pattern checker on the back end of its physical layer. This functionality enables bit error rate (BER) testing of each physical lane of the JESD204B link. The PHY PRBS pattern checker does not require that the JESD204B link be established. It can synchronize with a PRBS7, PRBS15, or PRBS31 data pattern. PRBS pattern verification can be done on multiple lanes at once. The error counts for failing lanes are reported for one JESD204B lane at a time. The process for performing PRBS testing on the AD9144 is as follows:

1. Start sending a PRBS7, PRBS15, or PRBS31 pattern from JESD204B transmitter.
2. Select and write the appropriate PRBS pattern to Register 0x316[3:2], as shown in Table 57.
3. Enable the PHY test for all lanes being tested by writing to PHY_TEST_EN (Register 0x315). Each bit of Register 0x315 enables the PRBS test for the corresponding lane. For example, writing a 1 to Bit 0 enables the PRBS test for Physical Lane 0.
4. Toggle PHY_TEST_RESET (Register 0x316[0]) from 0 to 1 then back to 0.
5. Set PHY_PRBS_ERROR_THRESHOLD (Register 0x319 to Register 0x317) as desired.
6. Write a 0 and then a 1 to PHY_TEST_START (Register 0x316[1]). The rising edge of PHY_TEST_START starts the test.
7. Wait 500 ms.
8. Stop the test by writing PHY_TEST_START (Register 0x316[1]) = 0.
9. Read the PRBS test results.
    a. Each bit of PHY_PRBS_PASS (Register 0x31D) corresponds to one SERDES lane. 0 = fail, 1 = pass.
    b. The number of PRBS errors seen on each failing lane can be read by writing the lane number to check (0 to 7) in the PHY_SRC_ERR_CNT (Register 0x316[6:4]) and reading the PHY_PRBS_ERR_COUNT (Register 0x31C to Register 0x31A). The maximum error count is 2^{24-1}. If all bits of Register 0x31C to Register 0x31A are high, the maximum error count on the selected lane has been exceeded.

Table 57. PHY PRBS Pattern Selection

PHY_PRBS_PAT_SEL Setting (Register 0x316[3:2])	PRBS Pattern
0b00 (default)	PRBS7
0b01	PRBS15
0b10	PRBS31

Transport Layer Testing

The JESD204B receiver in the AD9144 supports the short transport layer (STPL) test as described in the JESD204B standard. This test can be used to verify the data mapping between the JESD204B transmitter and receiver. To perform this test, this function must be implemented in the logic device and enabled there. Before running the test on the receiver side, the link must be established and running without errors (see the Device Setup Guide).

The STPL test ensures that each sample from each converter is mapped appropriately according to the number of converters (M) and the number of samples per converter (S). As specified in the JESD204B standard, the converter manufacturer specifies what test samples are transmitted. Each sample must have a unique value. For example, if M = 2 and S = 2, there are 4 unique samples transmitted repeatedly until the test is stopped. The expected sample must be programmed into the device and the expected sample is compared to the received sample one sample at a time until all have been tested. The process for performing this test on the AD9144 is described as follows:

1. Synchronize JESD204B link.
2. Enable STPL test at the JESD204B Tx.
3. Select Converter 0 Sample 0 for testing. Write SHORT_TPL_DAC_SEL (Register 0x32C[3:2]) = 0 and SHORT_TPL_SP_SEL (Register 0x32C[5:4]) = 0.
4. Set the expected test sample for Converter 0, Sample 0. Program the expected 16-bit test sample into the SHORT_TPL_REF_SP registers (Register 0x32E and Register 0x32D).
5. Enable the STPL test. Write SHORT_TPL_TEST_EN (Register 0x32C[0]) = 1.
6. Toggle the STPL reset. SHORT_TPL_TEST_RESET (Register 0x32C[1]) from 0 to 1 then back to 0.
7. Check for failures. Read SHORT_TPL_FAIL (Register 0x32F[0]), 0 = pass, 1 = fail.
8. Repeat Steps 3 to Step 7 for each sample of each converter. $Conv_0Sample_0$ through $Conv_{M-1}Sample_{S-1}$.

Repeated CGS and ILAS Test

As per section 5.3.3.8.2 of the JESD204B specification, the AD9144 can check that a constant stream of /K28.5/ characters is being received, or that CGS followed by a constant stream of ILAS is being received.

To run a repeated CGS test, send a constant stream of /K28.5/ characters to the AD9144 SERDES inputs. Next, set up the device and enable the links as described in the Device Setup Guide section. Ensure that the /K28.5/ characters are being received by verifying that the $\overline{\text{SYNCOUTx±}}$ has been de-asserted and that CGS has passed for all enabled link lanes by reading Register 0x470. Program Register 0x300[2] = 0 to monitor the status of lanes on Link 0, and Register 0x300[2] = 1 to monitor the status of lanes on Link 1 for dual link mode.

To run the CGS followed by a repeated ILAS sequence test, follow the Device Setup Guide section, but before performing the last write (enabling the links), enable the ILAS test mode by writing a 1 to Register 0x477[7]. Then, enable the links. When the device recognizes 4 CGS characters on each lane, it de-asserts the SYNCOUTx±. At this point, the transmitter starts sending a repeated ILAS sequence.

Read Register 0x473 to verify that initial lane synchronization has passed for all enabled link lanes. Program Register 0x300[2] = 0 to monitor the status of lanes on Link 0, and Register 0x300[2] = 1 to monitor the status of lanes on Link 1 for dual link mode.

JESD204B ERROR MONITORING

Disparity, Not in Table, and Unexpected Control Character Errors

As per section 7.6 of the JESD204B specification, the AD9144 can detect disparity errors, not in table errors, and unexpected control character errors, and can optionally issue a sync request and reinitialize the link when errors occur.

Note that the disparity error counter counts all characters with invalid disparity, regardless of whether they are in the 8-bit/10-bit decoding table. This is a minor deviation from the JESD204B specification, which only counts disparity errors when they are in the 8-bit/10-bit decoding table.

Checking Error Counts

The error count can be checked for disparity errors, not in table errors, and unexpected control character errors. The error counts are on a per lane and per error type basis. Note that the lane select and counter select are programmed into Register 0x46B and the error count is read back from the same address. To check the error count, complete the following steps:

1. Select the desired link lane and error type of the counter to view. Write these to Register 0x46B according to Table 58.
   To select a link lane, first select a link (Register 0x300[2] = 0 to select Link 0 or Register 0x300[2] = 1 to select Link 1 (dual link only)).
   Note that when using Link 1, Link Lane x refers to Logical Lane x + 4.
2. Read the error count from Register 0x46B. Note the maximum error count is equal to the error threshold set in Register 0x47C.

Table 58. Error Counters

Addr.	Bits	Variable	Description
0x46B	[6:4]	LaneSel	LaneSel = x to monitor the error count of Link Lane x. See the notes on link lane in Step 1 of the Checking Error Counts section.
	[1:0]	CntrSel	CntrSel = 0b00 for bad running disparity counter. CntrSel = 0b01 for not in table error counter. CntrSel = 0b10 for unexpected control character counter.

Check for Error Count Over Threshold

In addition to reading the error count per lane and error type as described in the Checking Error Counts section, the user can check a register to see if the error count for a given error type has reached a programmable threshold.

The same error threshold is used for the three error types (disparity, not in table, and unexpected control character). The error counters are on a per error type basis. To use this feature, complete the following steps:

1. Program the desired error count threshold into ERRORTHRES (Register 0x47C).
2. Read back the error status for each error type to see if the error count has reached the error threshold.
   - Disparity errors are reported in Register 0x46D.
   - Not in table errors are reported in Register 0x46E.
   - Unexpected control characters are reported in Register 0x46F.

Error Counter and IRQ Control

The user can write to Register 0x46D and Register 0x46F to reset or disable the error counts and to reset the IRQ for a given lane. Note that these are the same registers that are used to report error count over threshold (see the Check for Error Count Over Threshold section), so the readback is not the value that was written. For each error type

1. Select the link lane to access. To select a link lane, first select a link (Register 0x300[2] = 0 to select Link 0, Register 0x300[2] = 1 to select Link 1 (dual link only)). Note that when using Link 1, Link Lane x refers to Logical Lane x + 4.
2. Decide whether you want to reset the IRQ, disable the error count, and/or reset the error count for the given lane and error type.
3. Write the link lane and desired reset or disable action to Register 0x46D to Register 0x46F according to Table 59.

Table 59. Error Counter and IRQ Control: Disparity (Register 0x46D), Not In Table (Register 0x46E), Unexpected Control Character (Register 0x46F)

Bits	Variable	Description
7	RstIRQ	RstIRQ = 1 to reset IRQ for the lane selected in Bits[2:0].
6	Disable_ErrCnt	Disable_ErrCnt = 1 to disable the error count for the lane selected in Bits[2:0].
5	RstErrCntr	RsteErrCntr = 1 to reset the error count for the lane selected in Bits[2:0].
[2:0]	LaneAddr	LaneAddr = x to monitor the error count of Link Lane x. See the notes on link lane in Step 1 of the Checking Error Counts section.

Monitoring Errors via SYNCOUTx±

When one or more disparity, not in table, or unexpected control character error occurs, the error is reported on the SYNCOUTx± pins as per section 7.6 of the JESD204B specification. The JESD204B specification states that the SYNCOUTx± signal is asserted for exactly 2 frame periods when an error occurs. For the AD9144, the width of the SYNCOUTx± pulse can be programmed to ½, 1, or 2 PClock cycles. The settings to achieve a SYNCOUTx± pulse of 2 frame clock cycles are given in Table 60.

Table 60. Setting SYNCOUTx± Error Pulse Duration

JESD Mode IDs	PClockFactor (Frames/PClock)	SYNCB_ERR_DUR (Register 0x312[5:4]) Setting[1]
0, 4, 9	4	0 (default)
1, 2, 5, 6, 10	2	1
3, 7	1	2

[1] These register settings assert the SYNCOUTx± signal for 2 frame clock cycles pulse widths.

Disparity, NIT, Unexpected Control Character IRQs

For disparity, not in table, and unexpected control character errors, error count over the threshold events are available as IRQ events. Enable these events by writing to Register 0x47A[7:5]. The IRQ event status can be read at the same address (Register 0x47A[7:5]) after the IRQs are enabled.

See the Error Counter and IRQ Control section for information on resetting the IRQ. See the Interrupt Request Operation section for more information on IRQs.

Errors Requiring Reinitializing

A link reinitialization automatically occurs when four invalid disparity characters are received as per section 7.1 of the JESD specification. When a link reinitialization occurs, the resync request is 5 frames and 9 octets long.

The user can optionally reinitialize the link when the error count for disparity errors, not in table errors, or unexpected control characters reaches a programmable error threshold. The process to enable the reinitialization feature for certain error types is as follows:

1. Set THRESHOLD_MASK_EN (Register 0x477[3]) = 1. Note that when this bit is set, unmasked errors do not saturate at either threshold or maximum value.
2. Enable the sync assertion mask for each type of error by writing to the SYNC_ASSERTION_MASK (Register 0x47B[7:5]) according to Table 61.
3. Program the desired error counter threshold into ERRORTHRES (Register 0x47C).
4. For each error type enabled in the SYNC_ASSERTION_MASK register, if the error counter on any lane reaches the programmed threshold, SYNCOUTx± falls, issuing a sync request. Note that all error counts are reset when a link reinitialization occurs. The IRQ does not reset and must be reset manually.

Table 61. Sync Assertion Mask

Addr.	Bit No.	Bit Name	Description
0x47B	7	BADDIS_S	Set to 1 to assert SYNCOUTx± if the disparity error count reaches the threshold
	6	NIT_S	Set to 1 to assert SYNCOUTx± if thenot in table error count reaches the threshold
	5	UCC_S	Set to 1 to assert SYNCOUTx± if the unexpected control character count reaches the threshold

CGS, Frame Sync, Checksum, and ILAS Monitoring

Register 0x470 to Register 0x473 can be monitored to verify that each stage of JESD204B link establishment has occurred. Program Register 0x300[2] = 0 to monitor the status of the lanes on Link 0, and Register 0x300[2] = 1 to monitor the status of the lanes on Link 1.

Bit x of CODEGRPSYNCFLAG (Register 0x470) is high if Link Lane x received at least 4 K28.5 characters and passed code group synchronization.

Bit x of FRAMESYNCFLAG (Register 0x471) is high if Link Lane x completed initial frame synchronization.

Bit x of GOODCHKSUMFLG (Register 0x472) is high if the checksum sent over the lane matches the sum of the JESD 204B parameters sent over the lane during ILAS for Link Lane x. The parameters can be added either by summing the individual fields in registers or summing the packed register. If Register 0x300[6] = 0 (default), the calculated checksums are the lower 8 bits of the sum of the following fields: DID, BID, LID, SCR, L − 1, F − 1, K − 1, M − 1, N − 1, SUBCLASSV, NP − 1, JESDV, S − 1, and HD. If Register 0x300[6] = 1, the calculated checksums are the lower 8 bits of the sum of Register 0x400 to Register 0x40C and LID.

Bit x of INITIALLANESYNC (Register 0x473) is high if Link Lane x passed the initial lane alignment sequence.

CGS, FrameSync, Checksum, and ILAS IRQs

Fail signals for CGS, FrameSync, CheckSum, and ILAS are available as IRQ events. Enable them by writing to Register 0x47A[3:0]. The IRQ event status can be read at the same address (Register 0x47A[3:0]) after the IRQs are enabled. Write a 1 to Register 0x470[7] to reset the CGS IRQ. Write a 1 to Register 0x471 to reset the FrameSync IRQ. Write a 1 to Register 0x472 to reset the CheckSum IRQ. Write a 1 to Register 0x473 to reset the ILAS IRQ.

See the Interrupt Request Operation section for more information.

Configuration Mismatch IRQ

The AD9144 has a configuration mismatch flag that is available as an IRQ event. Use Register 0x47B[3] to enable the mismatch flag (it is enabled by default), and then use Register 0x47B[4] to read back its status and reset the IRQ signal. See the Interrupt Request Operation section for more information.

The configuration mismatch event flag is high when the link configuration settings (in Register 0x450 to Register 0x45D) do not match the JESD204B transmitted settings (Register 0x400 to Register 0x40D). All these registers are paged per link (in Register 0x300).

Note that this function is different from the good checksum flags in Register 0x472. The good checksum flags ensure that the transmitted checksum matches a calculated checksum based on the transmitted settings. The configuration mismatch event ensures that the transmitted settings match the configured settings.

HARDWARE CONSIDERATIONS

Power Supply Recommendations

The power supply domains are described in Table 62. The power supplies can be grouped into separate PCB domains as show in Figure 62. All the AD9144 supply domains must remain as noise free as possible for the best operation. Power supply noise has a frequency component that affects performance, and is specified in V rms terms.

An LC filter on the output of the power supply is recommended to attenuate the noise, and must be placed as close to the AD9144 as possible. An effective filter is shown in Figure 62. This filter scheme reduces high frequency noise components. Each of the power supply pins of the AD9144 must also have a 0.1 μF capacitor connected to the ground plane, as shown in Figure 62. Place the capacitor as close to the supply pin as possible. Adjacent power pins can share a bypass capacitor. Connect the ground pins of the AD9144 to the ground plane using vias.

Power and Ground Planes

Solid ground planes are recommended to avoid ground loops and to provide a solid, uninterrupted ground reference for the high speed transmission lines that require controlled impedances. Do not use segmented power planes as a reference for controlled impedances unless the entire length of the controlled impedance trace traverses across only a single segmented plane. These and additional guidelines for the topology of high speed transmission lines are described in the JESD204B Serial Interface Inputs (SERDIN0± to SERDIN7±) section.

Table 62. Power Supplies

Supply Domain	Voltage (V)	Circuitry
DVDD12[1]	1.2	Digital core
PVDD12[2]	1.2	DAC PLL
SVDD12[3]	1.2	JESD204B receiver interface
CVDD12[1]	1.2	DAC clocking
IOVDD	1.8	SPI interface
V_{TT}[4]	1.2	V_{TT}
SIOVDD33	3.3	Sync LVDS transmit
AVDD33	3.3	DAC

[1] This supply requires a 1.3 V supply when operating at maximum DAC sample rates. See Table 3 for details.
[2] This supply may be combined with CVDD12 on the same regulator with a separate supply filter network and sufficient bypass capacitors near the pins.
[3] This supply requires a 1.3 V supply when operating at maximum interface rates. See Table 4 for details.
[4] This supply can be connected to SVDD12 and does not need separate circuitry.

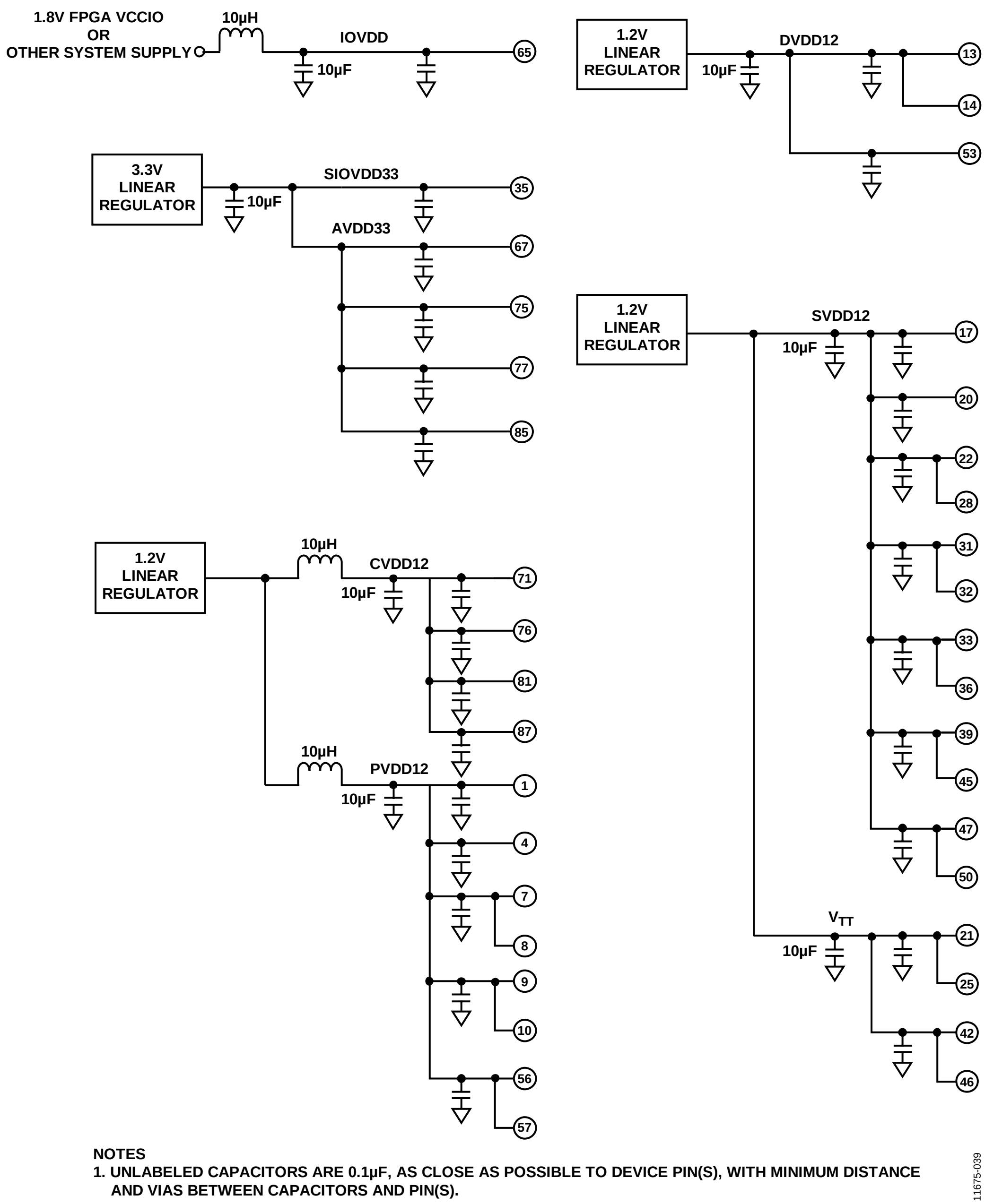


Figure 62. JESD204B Interface PCB Power Domain Recommendation

JESD204B Serial Interface Inputs (SERDIN0± to SERDIN7±)

When considering the layout of the JESD204B serial interface transmission lines, there are many factors to consider to maintain optimal link performance. Among these factors are insertion loss, return loss, signal skew, and the topology of the differential traces.

Insertion Loss

The JESD204B specification limits the amount of insertion loss allowed in the transmission channel (see Figure 39). The AD9144 equalization circuitry allows significantly more loss in the channel than is required by the JESD204B specification. It is still important that the designer of the PCB minimize the amount of insertion loss by adhering to the following guidelines:

- Keep the differential traces short by placing the AD9144 as near to the transmitting logic device as possible and routing the trace as directly as possible between the devices.
- Route the differential pairs on a single plane using a solid ground plane as a reference.
- Use a PCB material with a low dielectric constant (<4) to minimize loss, if possible.

When choosing between the stripline and microstrip techniques, keep in mind the following considerations: stripline has less loss (see Figure 40 and Figure 41) and emits less EMI, but requires the use of vias that can add complexity to the task of controlling the impedance; whereas microstrip is easier to implement if the component placement and density allow for routing on the top layer and eases the task of controlling the impedance.

If using the top layer of the PCB is problematic or the advantages of stripline are desirable, follow these recommendations:

- Minimize the number of vias.
- If possible, use blind vias to eliminate via stub effects and use micro vias to minimize via inductance.
- If using standard vias, use the maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair (see Figure 63).
- For each via pair, place a pair of ground vias adjacent to them to minimize the impedance discontinuity (see Figure 63).

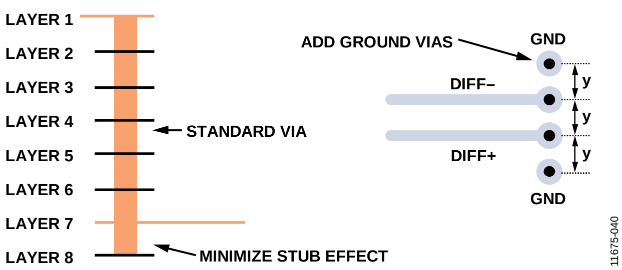


Figure 63. Minimizing Stub Effect and Adding Ground Vias for Differential Stripline Traces

Return Loss

The JESD204B specification limits the amount of return loss allowed in a converter device and a logic device, but does not specify return loss for the channel. However, every effort must be made to maintain a continuous impedance on the transmission line between the transmitting logic device and the AD9144. As mentioned in the Insertion Loss section, minimizing the use of vias, or eliminating them all together, reduces one of the primary sources for impedance mismatches on a transmission line. Maintain a solid reference beneath (for microstrip) or above and below (for stripline) the differential traces to ensure continuity in the impedance of the transmission line. If the stripline technique is used, follow the guidelines listed in the Insertion Loss section to minimize impedance mismatches and stub effects.

Another primary source for impedance mismatch is at either end of the transmission line, where care must be taken to match the impedance of the termination to that of the transmission line. The AD9144 handles this internally with a calibrated termination scheme for the receiving end of the line. See the Interface Power-Up and Input Termination section for details on this circuit and the calibration routine.

Signal Skew

There are many sources for signal skew, but the two sources to consider when laying out a PCB are interconnect skew within a single JESD204B link and skew between multiple JESD204B links. In each case, keeping the channel lengths matched to within 15 mm is adequate for operating the JESD204B link at speeds of up to 10.6 Gbps. Managing the interconnect skew within a single link is fairly straightforward. Managing multiple links across multiple devices is more complex. However, follow the 15 mm guideline for length matching.

Topology

Structure the differential SERDINx± pairs to achieve 50 Ω to ground for each half of the pair. Stripline vs. microstrip trade-offs are described in the Insertion Loss section. In either case, it is important to keep these transmission lines separated from potential noise sources such as high speed digital signals and noisy supplies. If using stripline differential traces, route them using a coplanar method, with both traces on the same layer. Although this does not offer more noise immunity than the broadside routing method (traces routed on adjacent layers), it is easier to route and manufacture so that the impedance continuity is maintained. An illustration of broadside vs. coplanar is shown in Figure 64.

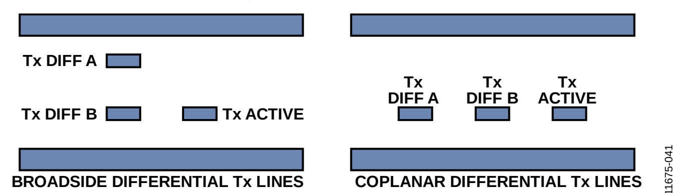


Figure 64. Broadside vs. Coplanar Differential Stripline Routing Techniques

When considering the trace width vs. copper weight and thickness, the speed of the interface must be considered. At multigigabit speeds, the skin effect of the conducting material confines the current flow to the surface. Maximize the surface area of the conductor by making the trace width made wider to reduce the losses. Additionally, loosely couple differential traces to accommodate the wider trace widths. This helps reduce the crosstalk and minimize the impedance mismatch when the traces must separate to accommodate components, vias, connectors, or other routing obstacles. Tightly coupled vs. loosely coupled differential traces are shown in Figure 65.

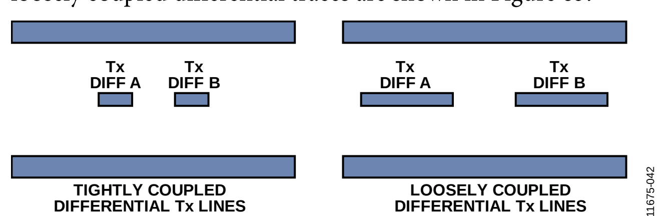


Figure 65. Tightly Coupled vs. Loosely Coupled Differential Traces

AC Coupling Capacitors

The AD9144 requires that the JESD204B input signals be ac-coupled to the source. These capacitors must be 100 nF and placed as close as possible to the transmitting logic device. To minimize the impedance mismatch at the pads, select the package size of the capacitor so that the pad size on the PCB matches the trace width as closely as possible.

SYNCOUTx±, SYSREF±, and CLK± Signals

The SYNCOUTx± and SYSREF± signals on the AD9144 are low speed LVDS differential signals. Use controlled impedance traces routed with 100 Ω differential impedance and 50 Ω to ground when routing these signals. As with the SERDIN0± to SERDIN7± data pairs, it is important to keep these signals separated from potential noise sources such as high speed digital signals and noisy supplies.

Separate the SYNCOUTx± signal from other noisy signals, because noise on the SYNCOUTx± might be interpreted as a request for K characters. The SYNCOUTx± signal has two modes of operation available for use. Register 0x2A5[0] defaults to 0, which sets the SYNCOUTx± swing to normal swing mode. When this bit is set to 1, the SYNCOUTx± swing is configured for high swing mode. For more details, see Table 8.

It is important to keep similar trace lengths for the CLK± and SYSREF± signals from the clock source to each of the devices on either end of the JESD204B links, see Figure 66. If using a clock chip that can tightly control the phase of CLK± and SYSREF±, the trace length matching requirements are greatly reduced.

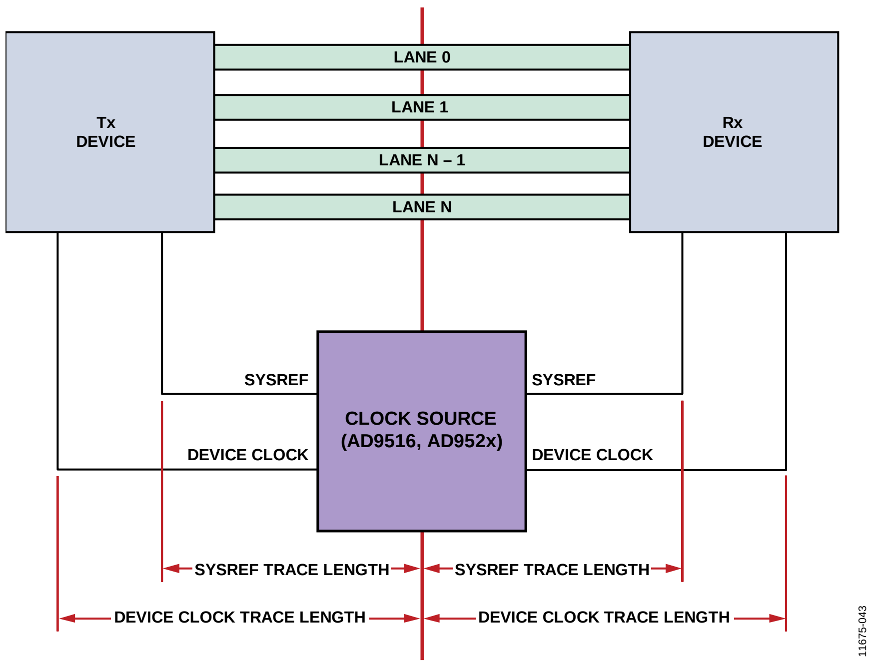


Figure 66. SYSREF Signal and Device Clock Trace Length

DIGITAL DATAPATH

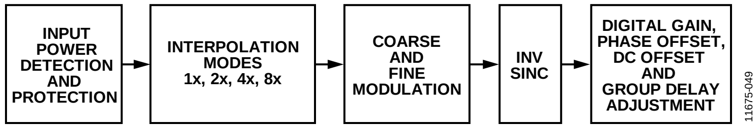


Figure 67. Block Diagram of Digital Datapath

The block diagram in Figure 67 shows the functionality of the digital datapath (all blocks can be bypassed). The digital processing includes an input power detection block, three half-band interpolation filters, a quadrature modulator consisting of a fine resolution NCO and $f_{DAC}/4$ and $f_{DAC}/8$ coarse modulation block, an inverse sinc filter, and gain, phase, offset, and group delay adjustment blocks.

The interpolation filters take independent I and Q data streams. If using the modulation function, I and Q must be quadrature data to function properly.

Note that the pipeline delay changes when digital datapath functions are enabled/disabled. If fixed DAC pipeline latency is desired, do not reconfigure these functions after initial configuration.

DUAL PAGING

Digital datapath registers are paged to allow configuration of either DAC dual independently or both simultaneously. Table 63 shows how to use the dual paging register.

Table 63. Paging Modes

DUAL_PAGE Reg. 0x008[1:0]	Duals Paged	DACs Updated
1	A	DAC0 and DAC1
2	B	DAC2 and DAC3
3 (default)	A and B	DAC0, DAC1, DAC2, and DAC3

Several functions are paged by DAC dual, such as input data format, downstream protection, interpolation, modulation, inverse sinc, digital gain, phase offset, dc offset, group delay, IQ swap, datapath PRBS, LMFC sync, and NCO alignment.

DATA FORMAT

BINARY_FORMAT (Register 0x110[7]), paged as described in the Dual Paging section) controls the expected input data format. By default it is 0, which means the input data must be in twos complement. It can also be set to 1, which means input data is in offset binary (0x0000 is negative full scale and 0xFFFF is positive full scale).

INTERPOLATION FILTERS

The transmit path contains three half-band interpolation filters, which each provide a 2× increase in output data rate and a low-pass function. The filters can be cascaded to provide a 4× or 8× interpolation ratio. Table 64 shows how to select each available interpolation mode, their usable bandwidths, and their maximum data rates. Note that $f_{DATA} = f_{DAC}/InterpolationFactor$. Interpolation mode is paged as described in the Dual Paging section. Register 0x030[0] is high if an unsupported interpolation mode is selected.

Table 64. Interpolation Modes and Usable Bandwidth

Interpolation Mode	INTERP_MODE Reg 0x112[2:0]	Usable Bandwidth	Maximum f_{DATA} (MHz)
1× (Bypass)	0x00	f_{DATA}	1060[1]
2×	0x01	$0.4 \times f_{DATA}$	1060[1]
4×	0x03	$0.4 \times f_{DATA}$	700
8×	0x04	$0.4 \times f_{DATA}$	350

[1] The maximum speed for 1× interpolation is limited by the JESD interface.

Filter Performance

The interpolation filters interpolate between existing data in such a way that they minimize changes in the incoming data while suppressing the creation of interpolation images. This is shown for each filter in Figure 68.

The usable bandwidth (as shown in Table 64) is defined as the frequency band over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 85 dB.

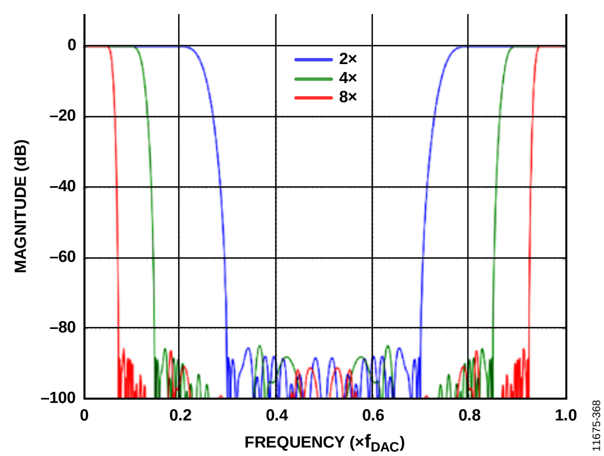


Figure 68. All Band Responses of Interpolation Filters

Filter Performance Beyond Specified Bandwidth

The interpolation filters are specified to 0.4 × f_{DATA} (with pass band). The filters can be used slightly beyond this ratio at the expense of increased pass-band ripple and decreased interpolation image rejection.

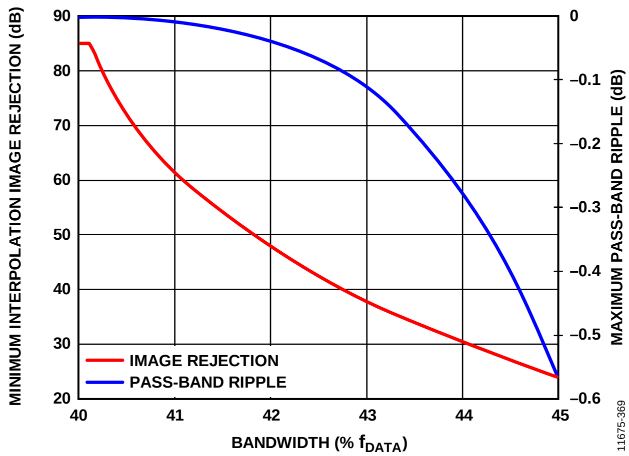


Figure 69. Interpolation Filter Performance Beyond Specified Bandwidth

Figure 69 shows the performance of the interpolation filters beyond 0.4 × f_{DATA}. Note that the ripple increases much slower than the image rejection decreases. This means that if the application can tolerate degraded image rejection from the interpolation filters, more bandwidth can be used.

DIGITAL MODULATION

The AD9144 has digital modulation features to modulate the baseband quadrature signal to the desired DAC output frequency.

The coarse modulation modes (f_{DAC}/4 and f_{DAC}/8) allow modulation by those particular frequencies. The NCO fine modulation mode allows modulating by a programmable frequency at the cost of 30 mW to 120 mW, depending on the DAC rate. Modulation mode is selected as shown in Table 65 and paged as described in the Dual Paging section.

Table 65. Modulation Mode Selection

Modulation Mode	MODULATION_TYPE Register 0x111[3:2]
None	0b00
NCO Fine Modulation	0b01
Coarse – f_{DAC}/4	0b10
Coarse – f_{DAC}/8	0b11

NCO Fine Modulation

This modulation mode uses an NCO, a phase shifter, and a complex modulator to modulate the signal by a programmable carrier signal as shown in Figure 70. This allows output signals to be placed anywhere in the output spectrum with very fine frequency resolution.

The NCO produces a quadrature carrier to translate the input signal to a new center frequency. A quadrature carrier is a pair of sinusoidal waveforms of the same frequency, offset 90° from each other. The frequency of the quadrature carrier is set via an FTW. The quadrature carrier is mixed with the I and Q data and then summed into the I and Q datapaths, as shown in Figure 70.

$$-f_{DAC}/2 \le f_{CARRIER} < +f_{DAC}/2$$

$$FTW = (f_{CARRIER}/f_{DAC}) \times 2^{48}$$

where *FTW* is a 48-bit twos complement number.

The frequency tuning word is set as shown in Table 66 and paged as described in the Dual Paging section.

Table 66. NCO FTW Registers

Address	Value	Description
0x114	FTW[7:0]	8 LSBs of FTW
0x115	FTW[15:8]	Next 8 bits of FTW
0x116	FTW[23:16]	Next 8 bits of FTW
0x117	FTW[31:24]	Next 8 bits of FTW
0x118	FTW[39:32]	Next 8 bits of FTW
0x119	FTW[47:40]	8 MSBs of FTW

Unlike other registers, the FTW registers are not updated immediately upon writing. Instead, the FTW registers update on the rising edge of FTW_UPDATE_REQ (Register 0x113[0]). After an update request, FTW_UPDATE_ACK (Register 0x113[1]) must be high to acknowledge that the FTW has updated.

SEL_SIDEBAND (Register 0x111[1]; paged as described in the Dual Paging section) is a convenience bit that can be set to use the negative modulation result. This is equivalent to flipping the sign of FTW.

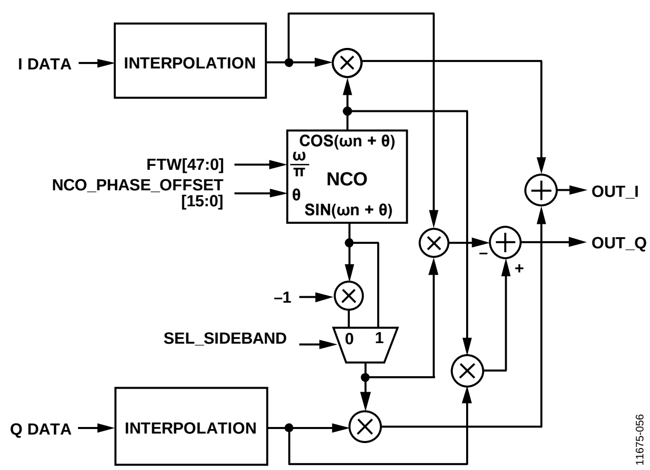


Figure 70. NCO Modulator Block Diagram

NCO Phase Offset

The phase offset feature allows rotation of the I and Q phases. Unlike phase adjust, this feature moves the phases of both I and Q channels together. Phase offset can be used only when using NCO fine modulation.

$$-180° \leq DegreesOffset < +180°$$
$$PhaseOffset = (DegreesOffset/180°) \times 2^{15}$$

where *PhaseOffset* is a 16-bit twos complement number.

The NCO phase offset is set as shown in Table 67 and paged as described in the Dual Paging section. Because this function is part of the fine modulation block, phase offset is not updated immediately upon writing. Instead, it updates on the rising edge of FTW_ UPDATE_REQ (Register 0x113[0]) along with the FTW.

Table 67. NCO Phase Offset Registers

Address	Value
0x11A	PhaseOffsetI[7:0]
0x11B	PhaseOffset[15:8]

INVERSE SINC

The AD9144 provides a digital inverse sinc filter to compensate the DAC roll-off over frequency. The filter is enabled by setting the INVSINC_ENABLE bit (Register 0x111[7]; paged as described in the Dual Paging section) and is enabled by default.

The inverse sinc ($sinc^{-1}$) filter is a seven-tap FIR filter. Figure 71 shows the frequency response of sin(x)/x roll-off, the inverse sinc filter, and the composite response. The composite response has less than ±0.05 dB pass-band ripple up to a frequency of 0.4 × f_{DACCLK}. To provide the necessary peaking at the upper end of the pass band, the inverse sinc filter shown has an intrinsic insertion loss of about 3.8 dB; in many cases, this can be partially compensated as described in the Digital Gain section.

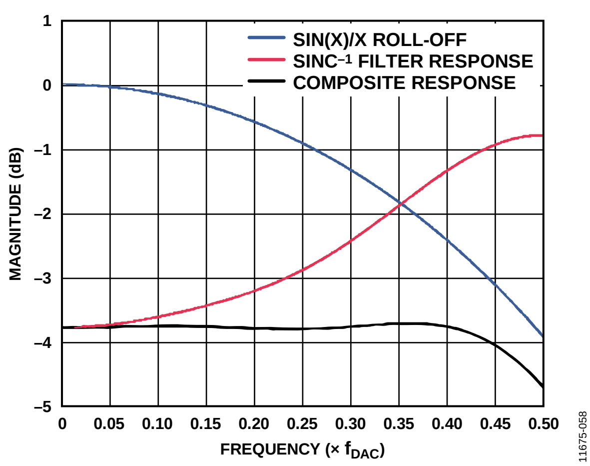


Figure 71. Responses of sin(x)/x Roll-Off, the Sinc^{-1} Filter, and the Composite of the Two Input Signal Power Detection and Protection

DIGITAL GAIN, PHASE ADJUST, DC OFFSET, AND GROUP DELAY

Digital gain, phase adjust, and dc offset (as described in the Digital Gain section, Phase Adjust section, and DC Offset section) allow compensation of imbalances in the I and Q paths due to analog mismatches between DAC I/Q outputs, quadrature modulator I/Q baseband inputs, and DAC/modulator interface I/Q paths. These imbalances can cause the two following issues:

- An unwanted sideband signal to appear at the quadrature modulator output with significant energy. This can be tuned out using digital gain and phase adjust. Tuning the quadrature gain and phase adjust values can optimize complex image rejection in single sideband radios or can optimize the error vector magnitude (EVM) in zero IF (ZIF) architectures.
- The I/Q mismatch can cause LO leakage through a modulator, which can be tuned out using dc offset.

Group delay allows adjustment of the delay through the DAC, which can be used to adjust digital predistortion (DPD) loop delay.

Digital Gain

Digital gain can be used to independently adjust the digital signal magnitude being fed into each DAC. This is useful to balance the gain between I and Q channels of a dual or to cancel out the insertion loss of the inverse sinc filter. Digital gain must be enabled when using the blanking state machine (see the Downstream Protection section). If digital gain is disabled TXENx must be tied high.

Digital gain is enabled by setting the DIG_GAIN_ENABLE bit (Register 0x111[5], paged as described in the Dual Paging section). In addition to enabling the function the amount of digital gain (GainCode) desired must be programmed. By default, digital gain is enabled and GainCode is 0xAEA.

$$0 \leq Gain \leq 4095/2048$$
$$-\infty \text{ dB} \leq dBGain \leq 6.018 \text{ dB}$$
$$Gain = GainCode \times (1/2048)$$
$$dBGain = 20 \times \log10(Gain)$$
$$GainCode = 2048 \times Gain = 2048 \times 10^{dBGain/20}$$

where *GainCode* is a 12-bit unsigned binary number.

The I/Q digital gain is set as shown in Table 68 and paged as described in the Dual Paging section.

The default GainCode (0xAEA = 2.7 dB), is appropriate to counteract the insertion loss of the inverse sinc filter without causing digital clipping when using 2× interpolation. This value can be read off of Figure 71 at 0.25 × f_{DAC}, as that is the Nyquist rate when using a 2× interpolation. Recommended GainCode values for 4× and 8× interpolation are 0xBB3 (3.3 dB) and 0xBF8 (3.5 dB), respectively.

Table 68. Digital Gain Registers

Addr.	Value	Description
0x111[5]	DIG_GAIN_ENABLE	Set to 1 to enable digital gain
0x13C	GainCodeI[7:0]	I DAC LSB gain code
0x13D	GainCodeI[11:8]	I DAC MSB gain code
0x13E	GainCodeQ[7:0]	Q DAC LSB gain code
0x13F	GainCodeQ[11:8]	Q DAC MSB gain code

Phase Adjust

Ordinarily, the I and Q channels of each DAC pair have an angle of 90° between them. The phase adjust feature changes the angle between the I and Q channels, which can help balance the phase into a modulator.

$$-14 \le DegreesAdjust < 14$$
$$PhaseAdj = (DegreesAdjust/14) \times 2^{12}$$

where *PhaseAdj* is a 13-bit twos complement number.

The phase adjust is set as shown in Table 69 and paged as described in the Dual Paging section.

Table 69. I/Q Phase Adjustment Registers

Addr.	Value	Description
0x111[4]	PHASE_ADJ_ENABLE	Set to 1 to enable phase adjust
0x11C	PhaseAdj[7:0]	LSB phase adjust code
0x11D	PhaseAdj[12:8]	MSB phase adjust code

DC Offset

The dc offset feature is used to individually offset the data into the I or Q DACs. This can be used to cancel LO leakage.

The offset is programmed individually for I and Q as a 16-bit twos complement number in LSBs, plus a 5-bit twos complement number in sixteenths of an LSB, as shown in Table 70. DC offset is paged as described in the Dual Paging section.

$$-2^{15} \le LSBsOffset < 2^{15}$$
$$-16 \le SixteenthsOffset \le 15$$

Table 70. DC Offset Registers

Addr.	Value	Description
0x135[0]	DC_OFFSET_ON	Set to 1 to enable dc offset
0x136	LSBsOffsetI[7:0]	I DAC LSB dc offset code
0x137	LSBsOffsetI[15:8]	I DAC MSB dc offset code
0x138	LSBsOffsetQ[7:0]	Q DAC LSB dc offset code
0x139	LSBsOffsetQ[15:8]	Q DAC MSB dc offset code
0x13A	SixteenthsOffsetI	I DAC sub-LSB dc offset code
0x13B	SixteenthsOffsetQ	Q DAC sub-LSB dc offset code

Group Delay

Group delay can be used to delay both I and Q channels together. This can be useful, for example, for DPD loop delay adjust.

$$-4 \le DACClockCycles \le 3.5$$
$$GroupDelay = (DACClockCycles \times 2) + 8$$

where *GroupDelay* is a 4-bit twos complement number.

Write GroupDelay to GROUP_DELAY (Register 0x014). This is paged as described in the Dual Paging section.

I TO Q SWAP

I_TO_Q (Register 0x111[0]; paged as described in the Dual Paging section) is a convenience bit that can be set to send the I datapath to the Q DAC and the Q datapath to the I DAC. Note that this swap occurs at the end of the datapath (after any modulation, digital gain, phase adjust, and phase offset).

NCO ALIGNMENT

The NCO alignment block is used to phase align the NCO output from multiple converters. Two NCO alignment modes are supported by the AD9144. The first is a SYSREF± alignment mode that phase aligns the NCO outputs to the rising edge of a SYSREF± pulse. The second alignment mode is a data key alignment; when this mode is enabled, the AD9144 aligns the NCO outputs when a user specified data pattern arrives at the DAC input. Note that the NCO alignment is per dual, and is paged as described in the Dual Paging section.

SYSREF± NCO Alignment

As with the LMFC alignment, in Subclass 1, a SYSREF± pulse can be used to phase align the NCO outputs of multiple devices in a system and multiple channels on the same device. Note that in Subclass 0, this alignment mode can be used to align the NCO outputs within a device to an internal processing clock edge. No SYSREF± edge is needed in Subclass 0, but multichip alignment cannot be achieved. The steps to achieve a SYSREF NCO alignment are as follows:

1. Set NCO_ALIGN_MODE (Register 0x050[1:0]= 0b01) for SYSREF NCO alignment mode.
2. Set NCO_ALIGN_ARM (Register 0x050[7] = 1).
3. Perform an LMFC alignment to force the NCO phase align (see the Syncing LMFC Signals section). The phase alignment occurs on the next SYSREF edge.
   Note that if in one shot sync mode, the LMFC alignment block must be armed by setting Register 0x03A[6] = 1. If in continuous mode or one shot then monitor mode, the LMFC align block does not need to be armed; the NCO align automatically trips on the next SYSREF± edge.
4. Check the alignment status. If NCO phase alignment was successful, NCO_ALIGN_PASS (Register 0x050[4]) = 1. If phase alignment failed, NCO_ALIGN_FAIL (Register 0x050[3]) = 1.

Data Key NCO Alignment

In addition to supporting the SYSREF± alignment mode, the AD9144 supports a mode where the NCO phase alignment occurs when a user-specified pattern is seen at the DAC input. The steps to achieve a data key NCO alignment are as follows:

1. Set NCO_ALIGN_MODE (Register 0x050[1:0]) = 0b10.
2. Write the expected 16-bit data key for the I and Q datapath into NCOKEYI (Register 0x051 to Register 0x052) and NCOKEYQ (Register 0x053 to Register 0x054), respectively.
3. Set NCO_ALIGN_ARM (Register 0x050[7]) = 1).
4. Send the expected 16-bit I and Q data keys to the device to achieve NCO alignment.
5. Check the alignment status. If the expected data key was seen at the DAC input, then NCO_ALIGN_MTCH (Register 0x050[5])= 1. If NCO phase alignment was successful, NCO_ALIGN_PASS (Register 0x050[4]) = 1. If phase alignment failed, NCO_ALIGN_FAIL (Register 0x050[3] = 1).

Multiple device NCO alignment can be achieved with the data key alignment mode. To achieve multichip NCO alignment, program the same expected data key on all devices, arm all devices, and then send the data key to all devices/channels at the same time.

NCO Alignment IRQ

An IRQ event showing whether the NCO align was tripped is available.

Use Register 0x021[4] to enable DAC Dual A (DAC0 and DAC1), and then use Register 0x025[4] to read back its status and reset the IRQ signal.

Use Register 0x022[4] to enable DAC Dual B (DAC2 and DAC3), and then use Register 0x026[4] to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

DOWNSTREAM PROTECTION

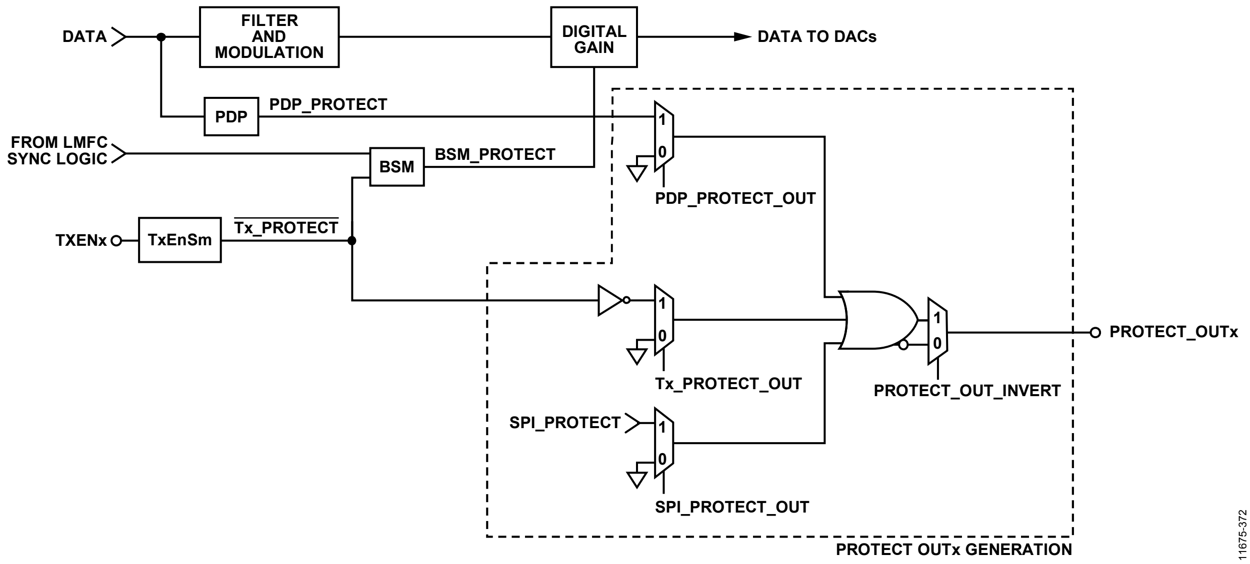


Figure 72. Downstream Protection Block Diagram

The AD9144 has several blocks designed to protect the power amplifier (PA) of the system, as well as other downstream blocks. It consists of a power detection and protection (PDP) block, a blanking state machine (BSM), and a transmit enable state machine (TxEnSM).

The PDP block can be used to monitor incoming data. If a moving average of the data power goes above a threshold, the PDP block provides a signal (PDP_PROTECT) that can be routed externally.

The TxEnSM is a simpler block that controls delay between TXENx and the $\overline{\text{Tx\_PROTECT}}$ signal. The $\overline{\text{Tx\_PROTECT}}$ signal is used as an input to the BSM and its inverse can optionally be routed externally. Optionally, the TxEnSM can also power down its associated DAC dual.

The BSM gently ramps data entering the DAC and flushes the datapath. The BSM is activated by the $\overline{\text{Tx\_PROTECT}}$ signal or automatically by the LMFC sync logic during a rotation. For proper function, digital gain must be enabled; tie TXEN high if disabling digital gain.

Finally, some simple logic takes the outputs from each of those blocks and uses them to generate a desired PROTECT_OUTx signal on an external pin. This signal can be used to enable/disable downstream components, such as a PA.

Power Detection and Protection

The input signal PDP block is designed to detect the average power of the DAC input signal and to prevent overrange signals from being passed to the next stage, which may potentially cause destructive breakdown on power sensitive devices, such as PAs. The protection function provides a signal (PDP_PROTECT) that can be routed externally to shut down a PA.

The PDP block uses a separate path with a shorter latency than the datapath to ensure that PDP_PROTECT gets triggered before the overrange signal reaches the analog DAC cores. The sum of the I^2 and Q^2 are calculated as a representation of the input signal power (only the top seven MSBs of data samples are used). The calculated sample power numbers are accumulated through a moving average filter whose output is the average of the input signal power in a certain number of samples. When the output of the averaging filter is larger than the threshold, the internal signal PDP_PROTECT goes high, which can optionally be configured to trigger a signal on the PROTECT_OUTx. The PDP block is configured as shown in Table 71 and paged as described in the Dual Paging section.

The choice of PDP_AVG_TIME (Register 0x062) and PDP_THRESHOLD (Register 0x060 to Register 0x061) for effective protection are application dependent. Experiment with real-world vectors to ensure proper configuration. The PDP_POWER readback (Register 0x063 to Register 0x064) can help by storing the maximum power when a set threshold was passed.

Table 71. PDP Registers

Addr.	Bit No.	Value	Description
0x060	[7:0]	PDP_THRESHOLD[7:0]	Power that triggers PDP_PROTECT. 8 LSBs.
0x061	[4:0]	PDP_THRESHOLD[12:8]	5 MSBs.
0x062	7	PDP_ENABLE	Set to 1 to enable PDP.
	[3:0]	PDP_AVG_TIME	Can be set from 0 to 10. Averages across $2^{(9 + PDP\_AVG\_TIME)}$, IQ sample pairs.
0x063	[7:0]	PDP_POWER[7:0]	If PDP_THRESHOLD is crossed, this reads back the maximum power seen. If not, this reads back the instantaneous power. 8 LSBs.
0x064	[4:0]	PDP_POWER[12:8]	5 MSBs.

Power Detection and Protection IRQ

The PDP_PROTECT signal is available as an IRQ event.

Use Register 0x021[7] to enable PDP_PROTECT for Dual A (DAC0 and DAC1), and then use Register 0x025[7] to read back its status and reset the IRQ signal.

Use Register 0x022[7] to enable PDP_PROTECT for Dual B (DAC2 and DAC3), and then use Register 0x026[7] to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

Transmit Enable State Machine

The TxEnSM is a simple block that controls the delay between the TXENx signal and the $\overline{\text{TX\_PROTECT}}$ signal. This signal is used as an input to the BSM and its inverse can be routed to an external pin (PROTECT_OUTx) to turn downstream components on or off as desired.

The TXENx signal can be used to power down their associated DAC duals. If DUALA_MASK (Register 0x012[0]) = 1, a falling edge of TXENx causes DAC Dual A (DAC0 and DAC1) to power down. If DUALB_MASK (Register 0x012[1]) = 1, a falling edge of TXENx causes DAC Dual B (DAC2 and DAC3) to power down. On a rising edge of TXENx, without DUALA_MASK and DUALB_MASK enabled, the output is valid after the BSM settles (see the Blanking State Machine (BSM) section). If the masks are enabled, an additional delay is imposed; the output is not valid until the BSM settles and the DACs fully power on (nominally an additional ~35 µs).

The TxEnSM is configured as shown in Table 72 and is paged as described in the Dual Paging section.

Table 72. TxEnSM Registers

Addr.	Bit No.	Value	Description
0x11F	[7:6]	FALL_COUNTERS	Number of fall counters to use (1 to 2).
	[5:4]	RISE_COUNTERS	Number of rise counters to use (0 to 2).
0x121	[7:0]	RISE_COUNT_0	Delay TX_PROTECT rise from TXEN rising edge by 32 × RISE_COUNT_0 DAC clock cycles.
0x122	[7:0]	RISE_COUNT_1	Delay TX_PROTECT rise from TXEN rising edge by 32 × RISE_COUNT_1 DAC clock cycles.
0x123	[7:0]	FALL_COUNT_0	Delay TX_PROTECT rise from TXEN rising edge by 32 × FALL_COUNT_0 DAC clock cycles. Must be at least 0x12.
0x124	[7:0]	FALL_COUNT_1	Delay TX_PROTECT rise from TXEN rising edge by 32 × FALL_COUNT_1 DAC clock cycles.

Blanking State Machine (BSM)

The BSM gently ramps data entering the DAC and flushes the datapath.

On a falling edge of $\overline{\text{TX\_PROTECT}}$ (the TXENx signal delayed by the TxEnSM), the datapath holds the latest data value and the digital gain gently ramps from its set value to 0. At the same time, the datapath is flushed with zeroes.

On a rising edge of $\overline{\text{TX\_PROTECT}}$, the TXENx signal is delayed by the TxEnSM; data is allowed to flow through the datapath again and the digital gain gently ramps the data from 0 up to the set digital gain.

Both of the above functions are also triggered automatically by the LMFC sync logic during a rotation to prevent glitching on the output.

Ramping

For proper ramping, digital gain must be enabled; tie TXEN high if disabling digital gain.

The step size to use when ramping gain to 0 or its assigned value can be controlled via the GAIN_RAMP_DOWN_STEP registers (Register 0x142 and Register 0x143) and the GAIN_RAMP_UP_STEP registers (Register 0x140 and Register 0x141). These registers are paged as described in the Dual Paging section.

The current BSM state can be read back as shown in Table 73.

Table 73. Blanking State Machine Ramping Readbacks

Address	Value	Description
0x147[7:6]	0b00	Data is being held at midscale.
	0b01	Ramping gain to 0. Data ramping to midscale.
	0b10	Ramping gain to assigned value. Data ramping to normal amplitude.
	0b11	Data at normal amplitude.

Blanking State Machine IRQ

Blanking completion is available as an IRQ event.

Use Register 0x021[5] to enable blanking completion for DAC Dual A (DAC0 and DAC1), and then use Register 0x025[5] to read back its status and reset the IRQ signal.

Use Register 0x022[5] to enable blanking completion for DAC Dual B (DAC2 and DAC3),and then use Register 0x026[5] to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

PROTECT_OUTx Generation

Register 0x013 controls which signals are OR'ed into the external PROTECT_OUTx signal. Register 0x11F[2] can be used to invert the PROTECT_OUTx signal, By default, PROTECT_OUTx is high when output is valid. Both of these registers are paged as described in the Dual Paging section.

Table 74. PROTECT_OUTx Registers

Addr.	Bit No.	Value	Description
0x013	6	PDP_PROTECT_OUT	1: PDP block triggers PROTECT_OUT
	5	TX_PROTECT_OUT	1: TXEnSM triggers PROTECT_OUT
	3	SPI_PROTECT_OUT	1: SPI_PROTECT triggers PROTECT_OUT
	2	SPI_PROTECT	Sets SPI_PROTECT
0x11F	2	PROTECT_OUT_INV ERT	Inverts PROTECT_OUTx

DATAPATH PRBS

The datapath PRBS can be used to verify that the AD9144 datapath is receiving and correctly decoding data. The datapath PRBS verifies that the JESD204B parameters of the transmitter and receiver match, the lanes of the receiver are mapped appropriately, lanes have been appropriately inverted, if necessary, and in general that the start-up routine has been implemented correctly.

The datapath PRBS is paged as described in the Dual Paging section. To run the datapath PRBS test, complete the following steps:

1. Set up the device in the desired operating mode. See the Device Setup Guide section for details on setting up the device.
2. Send PRBS7 or PRBS15 data.
3. Write Register 0x14B[2] = 0 for PRBS7 or 1 for PRBS15.
4. Write Register 0x14B[1:0] = 0b11 to enable and reset the PRBS test.
5. Write Register 0x14B[1:0] = 0b01 to enable the PRBS test and release reset.
6. Wait 500 ms.
7. Check the status by checking the IRQ for DAC0 to DAC3 PRBS as described in the Datapath PRBS IRQ section.
8. If there are failures, set Register 0x008 = 0x01 to view the status of Dual A (DAC0/DAC1). Set Register 0x08 = 0x02 to view the status of Dual B (DAC2/DAC3).
9. Read Register 0x14B[7:6]. Bit 6 is 0 if the I DAC of the selected dual has any errors. Bit 7 is 0 if the Q DAC of the selected dual has any errors. This must match the IRQ.
10. Read Register 0x14C to read the error count for the I DAC of the selected dual. Read Register 0x14D to read the error count for the Q DAC of the selected dual.

Note that the PRBS processes 32 bits at a time, and compares the 32 new bits to the previous set of 32 bits. It detects (and reports) only 1 error in every group of 32 bits, so the error count partly depends on when the errors are seen. For example

- Bits: 32 good, 31 good, 1 bad; 32 good [2 errors]
- Bits: 32 good, 22 good, 10 bad; 32 good [2 errors]
- Bits: 32 good, 31 good, 1 bad; 31 good, 1 bad; 32 good [3 errors]

Datapath PRBS IRQ

The PRBS fail signals for each DAC are available as IRQ events. Use Register 0x020[3:0] to enable the fail signals, and then use Register 0x024[3:0] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

DC TEST MODE

As a convenience, the AD9144 provides a dc test mode, which is enabled by setting Register 0x520[2]. When this mode is enabled, the datapath is given 0 (midscale) for its data.

In conjunction with dc offset, this test mode can provide desired dc data to the DACs. This test mode can also provide sinusoidal data to the DACs by combining digital modulation (to set frequency) and dc offset (to set amplitude). See the DC Offset section.

INTERRUPT REQUEST OPERATION

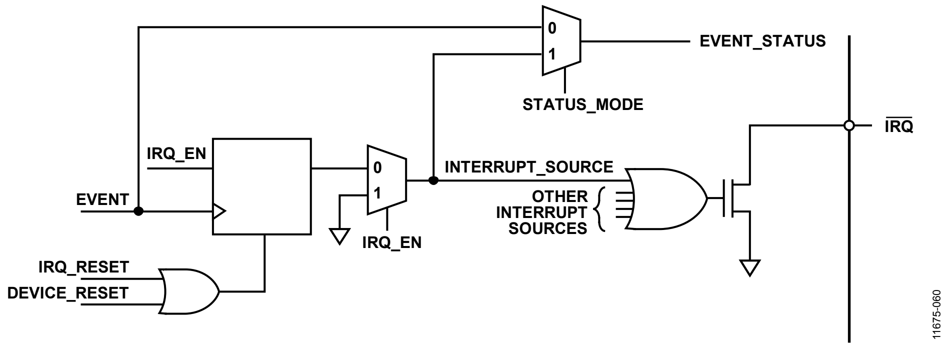


Figure 73. Simplified Schematic of IRQ Circuitry

The AD9144 provides an interrupt request output signal on Pin 60 (IRQ) that can be used to notify an external host processor of significant device events. On assertion of the interrupt, query the device to determine the precise event that occurred. The IRQ pin is an open-drain, active low output. Pull the IRQ pin high external to the device. This pin can be tied to the interrupt pins of other devices with open-drain outputs to wire; OR these pins together.

Figure 73 shows a simplified block diagram of how the IRQ blocks works. If IRQ_EN is low, the INTERRUPT_SOURCE signal is set to 0. If IRQ_EN is high, any rising edge of EVENT causes the INTERRUPT_SOURCE signal to be set high. If any INTERRUPT_SOURCE signal is high, the IRQ pin is pulled low. INTERRUPT_SOURCE can be reset to 0 by either an IRQ_RESET signal or a DEVICE_RESET.

Depending on STATUS_MODE, the EVENT_STATUS bit reads back EVENT or INTERRUPT_SOURCE. The AD9144 has several IRQ register blocks, which can monitor up to 75 events (depending on device configuration). Certain details vary by IRQ register block as described in Table 75. Table 76 shows which registers the IRQ_EN, IRQ_RESET, and STATUS_MODE signals in Figure 73 are coming from, as well as the address where EVENT_STATUS is read back.

Table 75. IRQ Register Block Details

Register Block	EVENT Reported	EVENT_STATUS
0x01F to 0x026	Per chip	INTERRUPT_SOURCE if IRQ is enabled, if not, it is EVENT
0x46D to 0x46F; 0x470 to 0x473; 0x47A	Per link and lane	INTERRUPT_SOURCE if IRQ is enabled, if not, 0
0x47B[4]	Per link	INTERRUPT_SOURCE if IRQ is enabled, if not, 0

INTERRUPT SERVICE ROUTINE

Interrupt request management starts by selecting the set of event flags that require host intervention or monitoring. Enable the events that require host action so that the host is notified when they occur. For events requiring host intervention upon IRQ activation, run the following routine to clear an interrupt request:

1. Read the status of the event flag bits that are being monitored.
2. Disable the interrupt by writing 0 to IRQ_EN.
3. Read the EVENT source. For Register 0x01F to Register 0x026, EVENT_STATUS has a live readback. For other events, see their registers.
4. Perform any actions that may be required to clear the cause of the EVENT. In many cases, no specific actions may be required.
5. Verify that the EVENT source is functioning as expected.
6. Clear the interrupt by writing 1 to IRQ_RESET.
7. Enable the interrupt by writing 1 to IRQ_EN.

Table 76. IRQ Register Block Address of IRQ Signal Details

	Address of IRQ Signals			
Register Block	**IRQ_EN**	**IRQ_RESET**	**STATUS_MODE**	**EVENT_STATUS**
0x01F to 0x026	0x01F to 0x022; R/W per chip	0x023 to 0x026; W per chip	STATUS_MODE = IRQ_EN	0x023 to 0x26; R per chip
0x46D to 0x46F	0x47A; W per link	0x46D to 0x46F; W per link and lane	N/A, STATUS_MODE = 1	0x47A; R per link
0x470 to 0x473	0x47A; W per link	0x470 to 0x473; W per link	N/A, STATUS_MODE = 1	0x47A; R per link
0x47B[4]	0x47B[3]; R/W per link; 1 by default	0x47B[4]; W per link	N/A, STATUS_MODE = 1	0x47B[4]; R per link

DAC INPUT CLOCK CONFIGURATIONS

The AD9144 DAC sample clock (DACCLK) can be sourced directly through CLK± (Pin 2 and Pin 3) or by clock multiplication through the CLK± differential input. Clock multiplication employs the on-chip PLL that accepts a reference clock operating at a submultiple of the desired DACCLK rate. The PLL then multiplies the reference clock up to the desired DACCLK frequency, which is used to generate all the internal clocks required by the DAC. The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed DACCLK.

The second mode bypasses the clock multiplier circuitry and allows DACCLK to be sourced directly to the DAC core. This mode enables the user to source a very high quality clock directly to the DAC core.

DRIVING THE CLK± INPUTS

The CLK± differential input circuitry is shown in Figure 74 as a simplified circuit diagram of the input. The on-chip clock receiver has a differential input impedance of 10 kΩ. It is self biased to a common-mode voltage of about 600 mV. The inputs can be driven by differential PECL or LVDS drivers with ac-coupling between the clock source and the receiver.

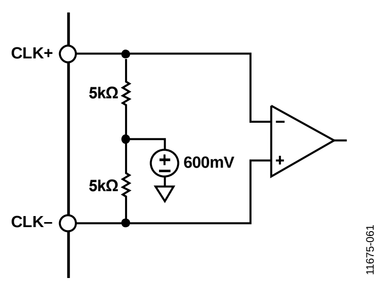


Figure 74. Clock Receiver Input Simplified Equivalent Circuit

The minimum input drive level to the differential clock input is 400 mV p-p differential. The optimal performance is achieved when the clock input signal is between 800 mV p-p differential and 1000 mV p-p differential. Whether using the on-chip clock multiplier or sourcing the DACCLK directly (the CLK± pins are used in both cases), it is necessary that the input clock signal to the device has low jitter and fast edge rates to optimize the DAC noise performance. Direct clocking with a low noise clock produces the lowest noise spectral density at the DAC outputs.

The clocks and clock receiver are powered down by default. The clocks must be enabled by writing to Register 0x080. To enable all clocks on the device, write Register 0x080 = 0x00. Register 0x080, Bit 7 powers up the clocks for DAC0 and DAC1. Bit 6 powers up the clocks for DAC2 and DAC3, Bit 5 powers up the digital clocks, Bit 4 powers up the SERDES clocks, and Bit 3 powers up the clock receiver.

CLOCK MULTIPLICATION

The on-chip PLL clock multiplier circuit can be used to generate the DAC sample rate clock from a lower frequency reference clock. The PLL is integrated on chip, including the VCO and the loop filter. The VCO operates over the frequency range of 6 GHz to 12 GHz.

The PLL configuration parameters must be programmed before the PLL is enabled. Step by step instructions on how to program the PLL can be found in the Starting the PLL section. The functional block diagram of the clock multiplier is shown in Figure 77.

The clock multiplication circuit generates the DAC sampling clock from the REFCLK input, which is fed in on the CLK± differential pins (Pin 2 and Pin 3). The frequency of the REFCLK input is referred to as f_{REF}.

The REFCLK input is divided by the variable RefDivFactor. Select the RefDivFactor variable to ensure that the frequency into the phase frequency detector (PFD) block is between 35 MHz and 80 MHz. The valid values for RefDivFactor are 1, 2, 4, 8, 16, or 32. Each RefDivFactor maps to the appropriate REF_DIV_MODE register control according to Table 77. The REF_DIV_MODE register is programmed through Register 0x08C[2:0].

Table 77. Mapping of RefDivFactor to REF_DIV_MODE

DAC Reference Frequency Range (MHz)	Divide by (RefDivFactor)	REF_DIV_MODE Reg. 0x08C[2:0]
35 to 80	1	0
80 to 160	2	1
160 to 320	4	2
320 to 640	8	3
640 to 1000	16	4

The range of f_{REF} is 35 MHz to 1 GHz, and the output frequency of the PLL is 420 MHz to 2 GHz. Use the following equations to determine the RefDivFactor:

$$35\text{ MHz} < \frac{f_{REF}}{RefDivFactor} < 80\text{ MHz} \quad (1)$$

where:
RefDivFactor is the reference divider division ratio.
f_{REF} is the reference frequency on the CLK± input pins.

The BCount value is the divide ratio of the loop divider. It is set to divide the f_{DACCLK} to frequency match the f_{REF}/RefDivFactor. Select BCount so that the following equation is true:

$$\frac{f_{DACCLK}}{2 \times BCount} = \frac{f_{REF}}{RefDivFactor} \quad (2)$$

where:
BCount is the feedback loop divider ratio.
f_{DACCLK} is the DAC sample clock.

The BCount value is programmed with Bits[7:0] of Register 0x085. It is programmable from 6 to 127.

The PFD compares f_{REF}/RefDivRate to f_{DAC}/(2 × BCount) and pulses the charge pump up or down to control the frequency of the VCO. A low noise VCO is tunable over an octave with an oscillation range of 6 GHz to 12 GHz.

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}.

$$f_{VCO} = f_{DACCLK} \times LODivFactor \tag{3}$$

and from Equation 2, the DAC sample clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = 2 \times BCount \times \frac{f_{REF}}{RefDivFactor} \tag{4}$$

The LODivFactor is chosen to keep f_{VCO} in the operating range between 6 GHz and 12 GHz. The valid values for LODivFactor are 4, 8, and 16. Each LODivFactor maps to a LO_DIV_MODE value. The LO_DIV_MODE (Register 0x08B[1:0]) is programmed as described in Table 78.

Table 78. DAC VCO Divider Selection

DAC Frequency Range (MHz)	Divide by (LODivFactor)	LO_DIV_MODE Register 0x08B[1:0]
>1500	4	1
750 to 1500	8	2
420 to 750	16	3

Table 79 lists some common frequency examples for the RefDivFactor, LODivFactor, and BCount values that are needed to configure the PLL properly.

Table 79. Common Frequency Examples

Frequency (MHz)	f_{DACCLK} (MHz)	f_{VCO} (MHz)	RefDiv-Factor	LODiv-Factor	BCount
368.64	1474.56	11796.48	8	8	16
184.32	1474.56	11796.48	4	8	16
307.2	1228.88	9831.04	8	8	16
122.88	983.04	7864.35	2	8	8
61.44	983.04	7864.35	1	8	8
491.52	1966.08	7864.35	8	4	16
245.76	1966,08	7864.35	4	4	16

The RF PLL filter is fully integrated on-chip and is a standard passive third-order filter with five 4-bit programmable components (see Figure 75). The C1, C2, C3, R1, and R3 filter components are programmed with Register 0x087 through Register 0x089. Figure 75 and Figure 76 include example loop filter values for synthesizer configurations that typically result in excellent performance.

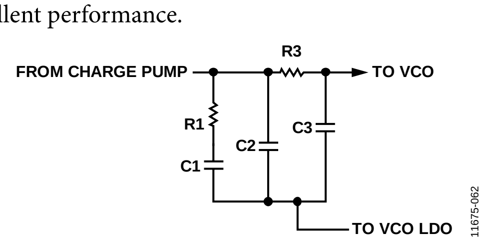


Figure 75. Loop Filter

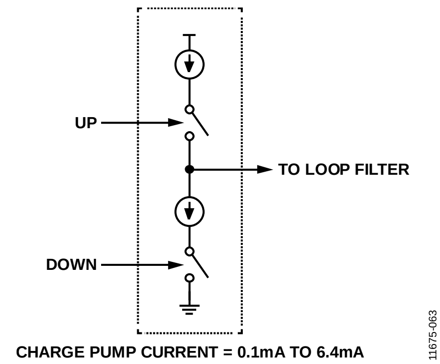


Figure 76. Charge Pump

The tables present different parameter sets based on f_{VCO}. Which table to use is determined by the frequency into the PFD block of the PLL. Table 96 to Table 98 also provide an optimized VCO temperature compensation coefficient to ensure that initial band calibration does not result in a loss of lock over temperature drift.

Table 80. Lookup Table Reference

PFD Reference Frequency (f_{REF}/RefDivFactor)	Lookup Table
35 MHz to 50 MHz	40 MHz (see Table 96)
50 MHz to 70 MHz	60 MHz (see Table 97)
70 MHz to 80 MHz	80 MHz (see Table 98)

Select the parameters from the row with the needed VCO frequency (f_{VCO}), or, if the f_{VCO} being used is between table values, select the next lowest f_{VCO} from the table. The columns labeled Band, Index, and VCO K_V (varactor gain) are informational, for readability. The other columns contain data that is retrieved, formatted by the user, and then written into the device. The upper column headers show the appropriate registers and bit positions for each setting that the user must write.

The VCO parameters are in the columns with VCO in the heading. The last six columns are for setting the charge pump current and loop filter for a specific configuration. The user must extract the VCO parameters as provided by Analog Devices from Table 96 to Table 98 and write them into the device in the registers and positions indicated without modification. However, the user can change the charge pump and loop filter parameters to suit the particular application, if desired.

The charge pump current is 6-bit programmable and varies from 0.1 mA to 6.4 mA in 0.1 mA steps. The charge pump current is programmed into Register 0x08A for the DAC PLL. The charge pump calibration must be run one time during chip initialization to reduce reference spurs. This calibration is on by default.

Charge pump calibration is run during the first power-up of the PLL, and the coefficient of the calibration is held for all subsequent starts. The PLL is enabled by writing 0x10 into Register 0x083, but the configuration registers must be programmed before the PLL is enabled. The calibration tries to match the up and down current, which minimizes the spurs at the reference frequency that appears at the DAC output. The charge pump calibration takes 64 reference clock cycles. Bit 5 in Register 0x084 notifies the user that the charge pump calibration is completed and is valid.

When the temperature coefficient for the VCO, VCO_VAR_REF_TC, is set properly, the device automatically selects one of the 512 VCO bands. Note that, to set this properly, the user must write 0x73 to Register 0x1C4. The PLL settings selected by the device ensure that the PLL remains locked over the full −40°C to +85°C operating temperature range of the device without further adjustment. The PLL remains locked over the full temperature range even if the temperature during initialization is at one of the temperature extremes.

Check the PLL lock bit to make sure that the calibration completed properly. The PLL lock bit is Bit 1 of Register 0x084.

STARTING THE PLL

The programming sequence for the DAC PLL is as follows:

1. Determine the VCO frequency based on the DAC frequency requirements.
2. Determine the VCO divider ratio to achieve the desired DAC frequency. Program the VCO divider ratio in Register 0x08B[1:0].
3. Determine the BCount ratio to achieve the desired PLL reference frequency (35 MHz to 80 MHz). Program the BCount ratio in Register 0x085[7:0].
4. Determine the reference divider ratio to achieve the desired PLL reference frequency. Program the reference divider ratio in Register 0x08C[2:0].
5. Determine the loop filter and other control parameters. Program as shown in the column header of Table 96 to Table 98. Each table was optimized for a particular PLL reference frequency (40 MHz, 60 MHz, or 80 MHz); use the closest frequency to the actual PLL reference frequency. After a table is chosen, select the parameters from the row containing the VCO frequency (f_{VCO}) being used or the next lowest f_{VCO} if the value falls between table values listed. Write the registers listed in the table with their corresponding values.
6. Enable the DAC PLL synthesizer by setting Register 0x083[4] to 1.

Register 0x084[5] notifies the user that the DAC PLL calibration is completed and is valid.

Register 0x084[1] notifies the user that the PLL has locked.

Register 0x084[7] and Register 0x084[6] notify the user that the DAC PLL hit the upper or lower edge of its operating band, respectively. If either of these bits are high, recalibrate the DAC PLL by setting Register 0x083[7] to 0 and then 1.

DAC PLL IRQ

The DAC PLL lock and lost signals are available as IRQ events. Use Register 0x01F[5:4] to enable these signals, and then use Register 0x023[5:4] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

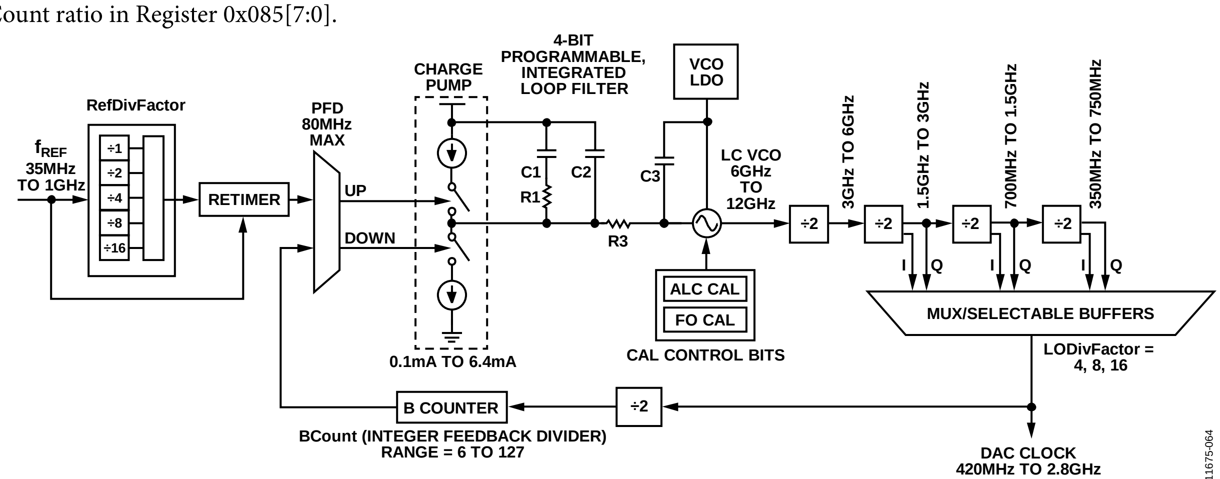


Figure 77. Device Clock PLL Block Diagram

ANALOG OUTPUTS

TRANSMIT DAC OPERATION

Figure 78 shows a simplified block diagram of the transmit path DACs. The DAC core consists of a current source array, a switch core, digital control logic, and full-scale output current control. The DAC full-scale output current (I_{OUTFS}) is nominally 20.48 mA. The output currents from the OUTx± pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load.

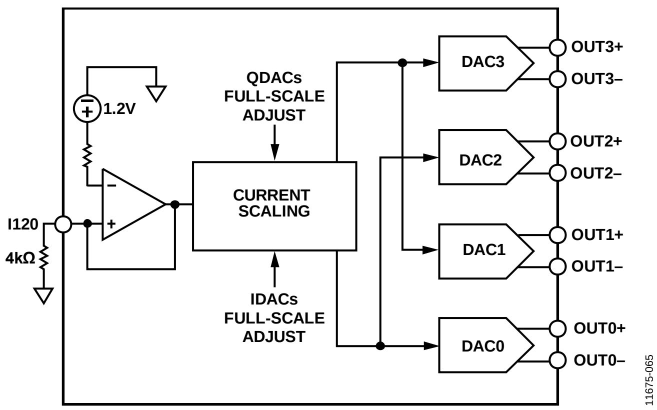


Figure 78. Simplified Block Diagram of DAC Core

The DAC has a 1.2 V band gap reference. A 4 kΩ external resistor, R_{SET}, must be connected from the I120 pin to the ground plane. This resistor, along with the reference control amplifier, sets up the correct internal bias currents for the DAC. Because the full-scale current is inversely proportional to this resistor, the tolerance of R_{SET} is reflected in the full-scale output amplitude.

DACFSC_x (where x is a number from 0 to 3 that corresponds to DAC0 through DAC3) is a 10-bit twos complement value that controls the full-scale current of each of the four DAC outputs. These values are stored in Register 0x040 to Register 0x047, as shown in Table 81.

The typical full-scale current for each DAC is given by:

$I_{OUTFS} = 20.48 + (DACFSC\_x \times 13.1\ mA)/2^{(10-1)}$

For nominal values of V_{REF} (1.2 V), R_{SET} (4 kΩ), and DACFSC_x (0, which is midscale in twos complement), the full-scale current of the DAC is typically 20.48 mA. The DAC full-scale current can be adjusted from 13.9 mA to 27.0 mA, by programming the appropriate DACFSC_x values in Register 0x040 to Register 0x047. Analog output full-scale current vs. DAC gain code is plotted in Figure 79.

Table 81. DAC Full-Scale Current Registers

Address	Value	Description
0x040[1:0]	DACFSC_0[9:8]	Dual A I DAC MSB gain code
0x041[7:0]	DACFSC_0[7:0]	Dual A I DAC LSB gain code
0x042[1:0]	DACFSC_1[9:8]	Dual A Q DAC MSB gain code
0x043[7:0]	DACFSC_1[7:0]	Dual A Q DAC LSB gain code
0x044[1:0]	DACFSC_2[9:8]	Dual B I DAC MSB gain code
0x045[7:0]	DACFSC_2[7:0]	Dual B I DAC LSB gain code
0x046[1:0]	DACFSC_3[9:8]	Dual B Q DAC MSB gain code
0x047[7:0]	DACFSC_3[7:0]	Dual B IQDAC LSB gain code

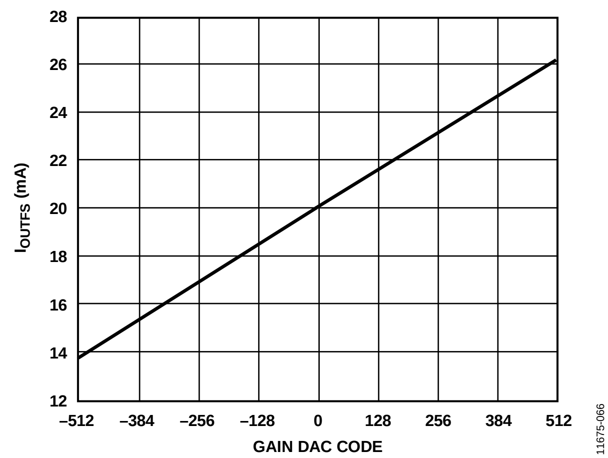


Figure 79. DAC Full-Scale Current (I_{OUTFS}) vs. DAC Gain Code

Transmit DAC Transfer Function

The output currents from the OUTx+ and OUTx– pins are complementary, meaning that the sum of the positive and negative currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load. OUTx± provides the maximum output current when all bits are high for binary data. The output currents vs. DACCODE for the DAC outputs using binary format are expressed as

$$I_{OUTP} = \frac{DACCODE_{BIN}}{2^N - 1} \times I_{OUTFS} \quad (5)$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP} \quad (6)$$

where $DACCODE_{BIN}$ is the 16-bit input to the DAC in unsigned binary. $DACCODE_{BIN}$ has a range of 0 to $2^N - 1$.

If the data format is twos complement then the output currents are expressed as

$$I_{OUTP} = \frac{DACCODE_{TWOS} + 2^{N-1}}{2^N - 1} \times I_{OUTFS} \quad (7)$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP} \quad (8)$$

where $DACCODE_{TWOS}$ is the 16-bit input to the DAC in twos complement. $DACCODE_{TWOS}$ has a range of -2^{N-1} to $2^{N-1} - 1$.

Powering Down Unused DACs

Power down any unused DAC outputs to avoid burning excess power. The DAC power downs are located in Register 0x011. Register 0x011, Bit 6 corresponds to DAC0, Bit 5 to DAC1, Bit 4 to DAC2, and Bit 3 to DAC3. Write a 1 to each bit to power down the appropriate DACs.

Register 0x011, Bit 7 and Bit 2, must stay low to enable the band gap and DAC master bias, respectively.

For more information on which DACs to power down, see the DAC Power-Down Setup section.

Self Calibration

The AD9144 has a self calibration feature that improves the DAC dc and ac linearity in zero or low IF applications. The performance improvement includes the INL/DNL, second and fourth harmonic distortions (HD2 and HD4), and second-order intermodulation distortion (IMD2) of the device. Figure 80 and Figure 81 show the typical DAC INL and DNL before and after the calibration. Figure 82 and Figure 83 show the calibration effect on the HD2, HD4, and IMD2 performance. The improvement from calibration decreases with the DAC output frequency. For improvement in HD2 and HD4, it is recommended to run the calibration routine when the desired output frequency is below 100 MHz. For improvement in IMD2, it is recommended to run the routine when the desired output frequency is below 200 MHz. A single run of the routine is sufficient to obtain the desired performance for both ac and dc performance.

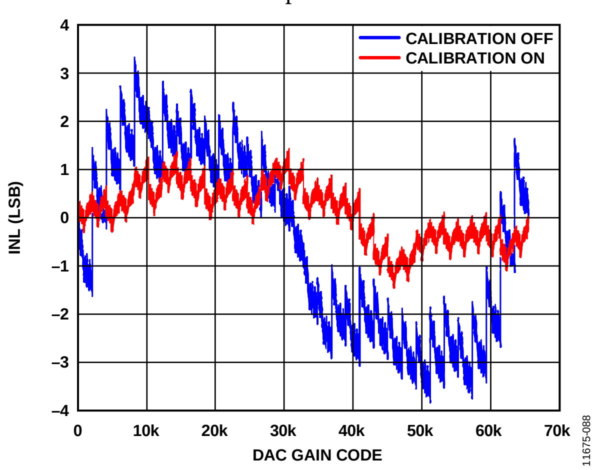


Figure 80. Pre- and Post-Calibration, INL

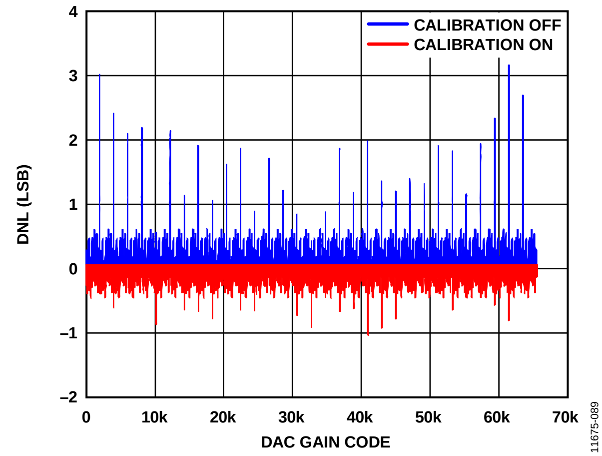


Figure 81. Pre- and Post-Calibration, DNL

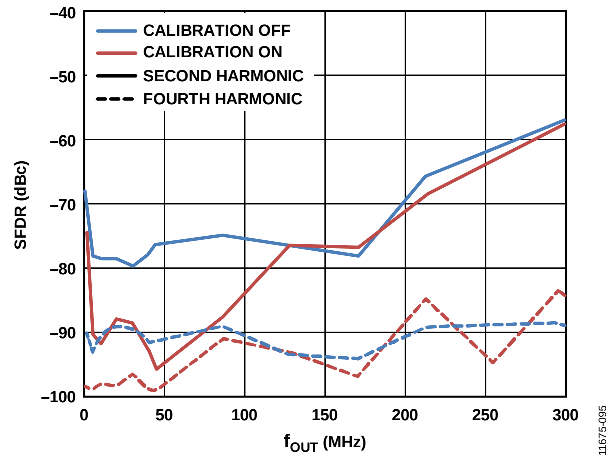


Figure 82. Pre- and Post-Calibration, HD2 and HD4

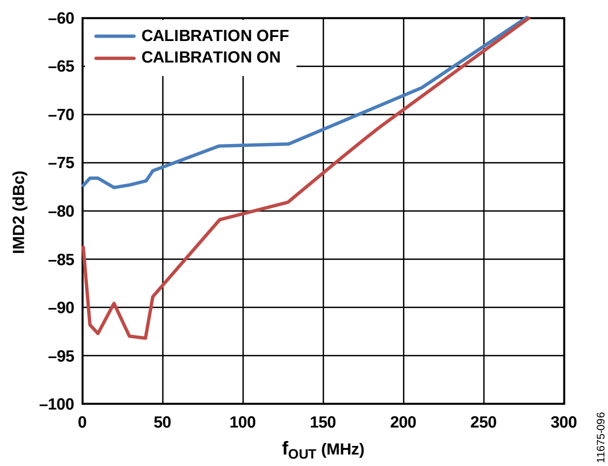


Figure 83. Pre- and Post-Calibration, IMD2

When using all four DACs, follow the procedure in Table 82 to perform a device self calibration. However, when using fewer than four DACs, follow the calibration routine shown in Table 83.

Table 82. Device Self Calibration Procedure for 4-Converter Setup

Addr.	SPI Data Byte	Description
0x0E7	0x38	Enable calibration clock.
0x0E8	0x0F	Calibrate all DACs.
0x0ED	0xA2	Configure initial value.
0x0E2	0x01	Enable averaged calibration.
0x0E2	0x03	Start averaged calibration.
Read 0x023[7:6]	0b10	CAL_PASS (Register 0x023[7]) = 1 to indicate that the calibration passed. If CAL_PASS = 0, check CAL_FAIL (Register 0x023[6]). If both CAL_PASS = 0 and CAL_FAIL = 0, calibration is either still running or it never ran. Try waiting ~100 ms and re-read CAL_PASS and CAL_FAIL, or re-run the calibration routine.
0x0E7	0x30	Disable calibration clock.

If using fewer than four converters, the calibration routine in Table 83 must be used. See DAC Power-Down Setup for notes on which DACs to power down when using fewer than four converters.

Table 83. Device Self Calibration Procedure with Fewer than Four Converters Enabled

Addr.	Bit	SPI Data Byte	Description
0x0E7		0x38	Use highest comparator speed and set calibration clock divider
0x0E8			Select DACs to calibrate
	3	0b0 or 0b1	1 if DAC3 is enabled
	2	0b0 or 0b1	1 if DAC2 is enabled
	1	0b0 or 0b1	1 if DAC1 is enabled
	0	0b0 or 0b1	1 if DAC0 is enabled
0x0ED		0xA2	Configure initial value
0x0E9		0x01	Enable calibration
0x0E9		0x03	Start calibration
0x0E7		0x30	Disable calibration clock

For each DAC calibrated, check the calibration status by writing a 1 in the corresponding bit of CAL_INDEX (Register 0x0E8) and reading Register 0x0E9. If the calibration completed correctly, CAL_FIN (Register 0x0E9[7]) = 1 to indicate that calibration is complete, and Register 0x0E9[6:4] = 0 to indicate that no errors have occurred.

Self Calibration IRQ

Self calibration pass and fail signals are available as IRQ events. Use Register 0x01F[7:6] to enable these signals, and then use Register 0x023[7:6] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

DEVICE POWER DISSIPATION

The AD9144 has eight supply rails, AVDD33, DVDD12, SVDD12, SIOVDD33, CVDD12, IOVDD, V_{TT}, and PVDD12, which can be driven from five regulators to achieve optimum performance, as shown in Figure 62.

The AVDD33 supply powers the DAC core circuitry. The power dissipation of the AVDD33 supply rail is independent of the digital operating mode and sample rate. The current drawn from the AVDD33 supply rail is typically 160 mA (540 mW) when the full-scale current of DAC0 to DAC3 are set to the nominal value of 20.48 mA.

PVDD12 powers the DAC PLLs and varies depending on the DAC sample rate. CVDD12 can be combined with the PVDD12 regulator but requires proper bypass capacitor networks near the pins. CVDD12 powers the clock tree, and the current varies directly with the DAC sample rate. DVDD12 powers the DSP core, and the current draw depends on the number of DSP functions and the DAC sample rate used. SVDD12 supplies the SERDES lanes and associated circuitry including the equalizers, SERDES PLL, PHY, and up to the input of the DSP. The current depends on the number lanes and the lane bit rate. IOVDD powers the SPI circuit and draws very small current.

SIOVDD33 powers the equalizers for the SERDES lanes. The V_{TT} termination voltage draws very small current of <5 mA.

TEMPERATURE SENSOR

The AD9144 has a band gap temperature sensor for monitoring the temperature changes of the AD9144. The temperature must be calibrated against a known temperature to remove the device-to-device variation on the band gap circuit used to sense the temperature.

To monitor temperature change, the user must take a reading at a known ambient temperature for a single-point calibration of each AD9144 device.

$$Tx = T_{REF} + 7.3 \times (CODE\_X - CODE\_REF)/1000$$

where:
CODE_X is the readback code at the unknown temperature, *Tx*.
CODE_REF is the readback code at the calibrated temperature, T_{REF}.

To use the temperature sensor, it must be enabled by setting Register 0x12F[0] to 1. The user must write a 1 to Register 0x134[0] before reading back the die temperature from Register 0x132 and Register 0x133.

START-UP SEQUENCE

Table 84 through Table 93 show the register writes needed to set up the AD9144 with f_{DAC} = 1474.56 MHz, 2× interpolation, and the DAC PLL enabled with a 368.64 MHz reference clock. The JESD204B interface is configured in Mode 4, dual link mode, Subclass 1, and scrambling is enabled with all eight SERDES lanes running at 7.3728 Gbps, inputting twos complement formatted data. No remapping of lanes with the crossbar is done in this example.

The sequence of steps to properly start up the AD9144 are as follows:

1. Set up the SPI interface, power up necessary circuit blocks, make required writes to the configuration register, and set up the DAC clocks (see Step 1: Start Up the DAC).
2. Set the digital features of the AD9144 (see Step 2: Digital Datapath).
3. Set up the JESD204B links (see Step 3: Transport Layer).
4. Set up the physical layer of the SERDES interface (see Step 4: Physical Layer).
5. Set up the data link layer of the SERDES interface. This procedure is for quick startup or debug only and does not guarantee deterministic latency (see Step 5: Data Link Layer).
6. Check for errors on Link 0 and Link 1 (see Step 6: Error Monitoring).

These steps are outlined in detail in the following sections in tables that list the required register write and read commands.

STEP 1: START UP THE DAC

Power-Up and DAC Initialization

Table 84. Power-Up and DAC Initialization

Command	Address	Value	Description
W	0x000	0xBD	Soft reset
W	0x000	0x3C	Deassert reset, set 4-wire SPI
W	0x011	0x00	Enable reference, DAC channels, and master DAC
W	0x080	0x00	Power up all clocks
W	0x081	0x00	Power up SYSREF receiver, disable hysteresis

Required Device Configurations

Table 85. Required Device Configuration

Command	Address	Value	Description
W	0x12D	0x8B	Digital datapath configuration
W	0x146	0x01	Digital datapath configuration
W	0x2A4	0xFF	Clock configuration
W	0x1C4	0x73	DAC PLL configuration
W	0x291	0x49	SERDES PLL configuration
W	0x29C	0x24	SERDES PLL configuration
W	0x29F	0x73	SERDES PLL configuration
W	0x232	0xFF	JESD interface configuration
W	0x333	0x01	JESD interface configuration

Configure the DAC PLL

Table 86. Configure DAC PLL

Command	Address	Value	Description
W	0x08B	0x02	Set the VCO LO divider to 8 so that 6 GHz ≤ $f_{VCO} = f_{DACCLK} \times 2^{(LODivMode + 1)}$ ≤ 12 GHz.
W	0x08C	0x03	Set the reference clock divider to 8 so that the reference clock into the PLL is less than 80 MHz.
W	0x085	0x10	Set the B counter to 16 to divide the DAC clock down to 2× the reference clock.
W	0x1B5	0x80	Write VCO Varactor to 0 from Table 96. Leave Bit 7 high.
W	0x1BB	0x04	Write VCO bias reference and TC from Table 96.
W	0x1B4	0x78	Write VCO calibration offset from Table 96.
W	0x1C5	0x08	Write VCO Varactor Ref from Table 96.
W	0x08A	0x0A	Write charge pump current from Table 96.
W	0x087	0xC3	Set C1 and C2 from Table 96.
W	0x088	0xEF	Set R1 and C3 from Table 96.
W	0x089	0x0B	Set R3 from Table 96.
W	0x083	0x10	Enable DAC PLL.
R	0x084	0x01	Verify that Bit 1 reads back high for PLL locked.

STEP 2: DIGITAL DATAPATH

Table 87. Digital Datapath

Command	Address	Value	Description
W	0x112	0x01	Set the interpolation to 2×
W	0x110	0x00	Set twos complement data format

STEP 3: TRANSPORT LAYER

Table 88. Link 0 Transport Layer

Command	Address	Value	Description
W	0x200	0x00	Power up the interface
W	0x201	0x00	Enable all lanes
W	0x300	0x08	Bit 3 = 1 for dual link, Bit 2 = 0 to access Link 0 registers
W	0x450	0x00	Set the device ID to match Tx (0x00 in this example)
W	0x451	0x00	Set the bank ID to match Tx (0x00 in this example)
W	0x452	0x00	Set the lane ID to match Tx (0x00 in this example)
W	0x453	0x83	Set descrambling and L = 4 (in n – 1 notation)
W	0x454	0x00	Set F = 1 (in n – 1 notation)
W	0x455	0x1F	Set K = 32 (in n – 1 notation)
W	0x456	0x01	Set M = 2 (in n – 1 notation)
W	0x457	0x0F	Set N = 16 (in n – 1 notation)
W	0x458	0x2F	Set Subclass 1 and NP = 16 (in n – 1 notation)
W	0x459	0x20	Set JESD 204B Version and S = 1 (in n – 1 notation)
W	0x45A	0x80	Set HD = 1
W	0x45D	0x45	Set checksum for Lane 0
W	0x46C	0x0F	Deskew Lane 0 to Lane3
W	0x476	0x01	Set F (not in n – 1 notation)
W	0x47D	0x0F	Enable Lane 0 to Lane 3

Table 89. Link 1 Transport Layer

Command	Address	Value	Description
W	0x300	0x0C	Bit 3 = 1 for dual link, Bit 2 = 1 to access registers for Link 1
W	0x450	0x00	Set the device ID to match Tx (0x00 in this example)
W	0x451	0x00	Set the bank ID to match Tx (0x00 in this example)
W	0x452	0x04	Set the lane ID to match Tx (0x04 in this example)
W	0x453	0x83	Set descrambling and L = 4 (in n – 1 notation)
W	0x454	0x00	Set F = 1 (in n – 1 notation)
W	0x455	0x1F	Set K = 32 (in n – 1 notation)
W	0x456	0x01	Set M = 2 (in n – 1 notation)
W	0x457	0x0F	Set N = 16 (in n – 1 notation)
W	0x458	0x2F	Set Subclass 1 and NP = 16 (in n – 1 notation)
W	0x459	0x20	Set JESD 204B and S = 1 (in n – 1 notation)
W	0x45A	0x80	Set HD
W	0x45D	0x45	Set checksum for Lane 0
W	0x46C	0x0F	Deskew Lane 4 to Lane 7
	0x476	0x01	Set F (not in n – 1 notation)
W	0x47D	0x0F	Enable Lane 4 to Lane 7

STEP 4: PHYSICAL LAYER

Table 90. Physical Layer

Command	Address	Value	Description
W	0x2AA	0xB7	JESD interface termination setting
W	0x2AB	0x87	JESD interface termination setting
W	0x2B1	0xB7	JESD interface termination setting
W	0x2B2	0x87	JESD interface termination setting
W	0x2A7	0x01	Autotune PHY setting
W	0x2AE	0x01	Autotune PHY setting
W	0x314	0x01	SERDES SPI configuration
W	0x230	0x28	Configure CDRs in half rate mode
W	0x206	0x00	Resets CDR logic
W	0x206	0x01	Release CDR logic reset
W	0x289	0x04	Configure PLL divider to 1 along with PLL required configuration
W	0x280	0x01	Enable SERDES PLL
R	0x281	0x01	Verify that Bit 0 reads back high for SERDES PLL lock
W	0x268	0x62	Set EQ mode to low power

STEP 5: DATA LINK LAYER

Note that this procedure does not guarantee deterministic latency.

Table 91. Data Link Layer—Does not Guarantee Deterministic Latency

Command	Address	Value	Description
W	0x301	0x01	Set subclass = 1
W	0x304	0x00	Set the LMFC delay setting to 0
W	0x305	0x00	Set the LMFC delay setting to 0
W	0x306	0x0A	Set the LMFC receive buffer delay to 10
W	0x307	0x0A	Set the LMFC receive buffer delay to 10
W	0x03A	0x01	Set sync mode = one shot sync
W	0x03A	0x81	Enable the sync machine
W	0x03A	0xC1	Arm the sync machine
SYSREF±			Ensure that at least one SYSREF± edge is sent to the device
W	0x300	0x0B	Bit 1 and Bit 0 = 1 to enable Link 0 and Link 1, Bit 2 = 0 to access Link 0

STEP 6: ERROR MONITORING

Link 0 Checks

Confirm the registers in Table 92 readback as noted and system tasks are completed as described.

Table 92. Link 0 Checks

Command	Address	Value	Description
R	0x470	0x0F	Acknowledge that four consecutive K28.5 characters have been detected on Lane 0 to Lane 3.
$\overline{\text{SYNCOUT0}}$±			Confirm $\overline{\text{SYNCOUT0}}$± is high.
SERDINx±			Apply ILAS and data to SERDES input pins.
R	0x471	0x0F	Check for frame sync on all lanes.
R	0x472	0x0F	Check for good checksum.
R	0x473	0x0F	Check for ILAS.

Link 1 Checks

Confirm the registers in Table 93 readback as noted and system tasks are completed as described.

Table 93. Link 1 Checks

Command	Address	Value	Description
W	0x300	0x0F	Bit 2 = 1 to access Link 1.
R	0x470	0x0F	Acknowledge that four consecutive K28.5 characters have been detected on Lane 4 to Lane 7.
$\overline{\text{SYNCOUT1}}$±			Confirm $\overline{\text{SYNCOUT1}}$± is high.
SERDINx±			Apply ILAS and data to SERDES input pins.
R	0x471	0x0F	Check for frame sync on all lanes.
R	0x472	0x0F	Check for good checksum.
R	0x473	0x0F	Check for ILAS.

REGISTER MAPS AND DESCRIPTIONS

In the following tables, register addresses (Reg. column) and reset (Reset column) values are hexadecimal and in the read/write (R/W) column, R means read only, W means write only, R/W means read/write, and N/A means not applicable. All values in the register address and reset columns are hexadecimal numbers.

DEVICE CONFIGURATION REGISTER MAP

Table 94. Device Configuration Register Map

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	SPI_INTFCONFA	SOFT RESET_M	LSBFIRST_ M	ADDRINC_M	SDOACTIVE_M	SDOACTIVE	ADDRINC	LSBFIRST	SOFTRESET	0x00	R/W
0x003	CHIPTYPE	CHIPTYPE								0x04	R
0x004	PRODIDL	PRODIDL								0x44	R
0x005	PRODIDH	PRODIDH								0x91	R
0x006	CHIPGRADE	PROD_GRADE				DEV_REVISION				0x02	R
0x008	SPI_PAGEINDX	RESERVED						DUAL_PAGE		0x03	R/W
0x011	PWRCNTRL0	PD_BG	PD_DAC_0	PD_DAC_1	PD_DAC_2	PD_DAC_3	PD_DACM	RESERVED		0x7C	R/W
0x012	TXENMASK	RESERVED						DUALB_ MASK	DUALA_ MASK	0x00	R/W
0x013	PWRCNTRL3	RESERVED	PDP_ PROTECT_ OUT	TX_PROTECT_ OUT	RESERVED	SPI_PROTECT_OUT	SPI_PROTECT	RESERVED		0x20	R/W
0x014	GROUP_DLY	RESERVED				GROUP_DLY				0x88	R/W
0x01F	IRQEN_ STATUSMODE0	IRQEN_ SMODE_ CALPASS	IRQEN_ SMODE_ CALFAIL	IRQEN_ SMODE_ DACPLLLOST	IRQEN_SMODE _ DACPLLLOCK	IRQEN_SMODE_ SERPLLLOST	IRQEN_SMODE_ SERPLLLOCK	IRQEN_ SMODE_ LANEFIFOERR	RESERVED	0x00	R/W
0x020	IRQEN_ STATUSMODE1	RESERVED				IRQEN_SMODE_ PRBS3	IRQEN_SMODE_ PRBS2	IRQEN_ SMODE_ PRBS1	IRQEN_ SMODE_ PRBS0	0x00	R/W
0x021	IRQEN_ STATUSMODE2	IRQEN_ SMODE_ PDPERR0	RESERVED	IRQEN_ SMODE_ BLNKDONE0	IRQEN_SMODE _NCO_ALIGN0	IRQEN_SMODE_ SYNC_LOCK0	IRQEN_SMODE_ SYNC_ROTATE0	IRQEN_ SMODE_ SYNC_ WLIM0	IRQEN_ SMODE_ SYNC_TRIP0	0x00	R/W
0x022	IRQEN_ STATUSMODE3	IRQEN_ SMODE_ PDPERR1	RESERVED	IRQEN_ SMODE_ BLNKDONE1	IRQEN_SMODE _NCO_ ALIGN1	IRQEN_SMODE_ SYNC_LOCK1	IRQEN_ SMODE_SYNC_ ROTATE1	IRQEN_ SMODE_ SYNC_ WLIM1	IRQEN_ SMODE_ SYNC_TRIP1	0x00	R/W
0x023	IRQ_STATUS0	CALPASS	CALFAIL	DACPLL- LOST	DACPLLLOCK	SERPLLLOST	SERPLLLOCK	LANEFIFO- ERR	RESERVED	0x00	R
0x024	IRQ_STATUS1	RESERVED				PRBS3	PRBS2	PRBS1	PRBS0	0x00	R
0x025	IRQ_STATUS2	PDPERR0	RESERVED	BLNK- DONE0	NCO_ ALIGN0	SYNC_ LOCK0	SYNC_ ROTATE0	SYNC_ WLIM0	SYNC_ TRIP0	0x00	R
0x026	IRQ_STATUS3	PDPERR1	RESERVED	BLNK- DONE1	NCO_ ALIGN1	SYNC_ LOCK1	SYNC_ ROTATE1	SYNC_ WLIM1	SYNC_ TRIP1	0x00	R
0x030	JESD_CHECKS	RESERVED		ERR_DLYOVER	ERR_WINLIMIT	ERR_JESDBAD	ERR_KUNSUPP	ERR_ SUBCLASS	ERR_ INTSUPP	0x00	R
0x034	SYNC_ ERRWINDOW	RESERVED					ERRWINDOW			0x00	R/W
0x038	SYNC_LASTERR_L	RESERVED				LASTERROR				0x00	R
0x039	SYNC_LASTERR_H	LASTUN- DER	LASTOVER	RESERVED						0x00	R
0x03A	SYNC_CONTROL	SYNC- ENABLE	SYNCARM	SYNCCLR- STKY	SYNCCLRLAST	SYNCMODE				0x00	R/W
0x03B	SYNC_STATUS	SYNC_ BUSY	RESERVED			SYNC_LOCK	SYNC_ ROTATE	SYNC_WLIM	SYNC_ TRIP	0x00	R
0x03C	SYNC_CURRERR_L	RESERVED				CURRERROR				0x00	R
0x03D	SYNC_CURRERR_ H	CURRUN- DER	CURROVER	RESERVED						0x00	R

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x040	DACGAIN0_1	RESERVED						DACFSC_0[9:8]		0x00	R/W
0x041	DACGAIN0_0	DACFSC_0[7:0]								0x00	R/W
0x042	DACGAIN1_1	RESERVED						DACFSC_1[9:8]		0x00	R/W
0x043	DACGAIN1_0	DACFSC_1[7:0]								0x00	R/W
0x044	DACGAIN2_1	RESERVED						DACFSC_2[9:8]		0x00	R/W
0x045	DACGAIN2_0	DACFSC_2[7:0]								0x00	R/W
0x046	DACGAIN3_1	RESERVED						DACFSC_3[9:8]		0x00	R/W
0x047	DACGAIN3_0	DACFSC_3[7:0]								0x00	R/W
0x050	NCOALIGN_ MODE	NCO_ ALIGN_ ARM	RESERVED	NCO_ALIGN_ MTCH	NCO_ALIGN_ PASS	NCO_ALIGN_FAIL	RESERVED	NCO_ALIGN_MODE		0x00	R/W
0x051	NCOKEY_ILSB	NCOKEYI[7:0]								0x00	R/W
0x052	NCOKEY_IMSB	NCOKEYI[15:8]								0x00	R/W
0x053	NCOKEY_QLSB	NCOKEYQ[7:0]								0x00	R/W
0x054	NCOKEY_QMSB	NCOKEYQ[15:8]								0x00	R/W
0x060	PDP_THRES0	PDP_THRESHOLD[7:0]								0x00	R/W
0x061	PDP_THRES1	RESERVED			PDP_THRESHOLD[12:8]					0x00	R/W
0x062	PDP_AVG_TIME	PDP_ ENABLE	RESERVED			PDP_AVG_TIME				0x00	R/W
0x063	PDP_POWER0	PDP_POWER[7:0]								0x00	R
0x064	PDP_POWER1	RESERVED			PDP_POWER[12:8]					0x00	R
0x080	CLKCFG0	PD_CLK01	PD_CLK23	PD_CLK_DIG	PD_SERDES_ PCLK	PD_CLK_REC	RESERVED			0xF8	R/W
0x081	SYSREF_ACTRL0	RESERVED			PD_SYSREF	HYS_ON	SYSREF_RISE	HYS_CNTRL1		0x10	R/W
0x082	SYSREF_ACTRL1	HYS_CNTRL0								0x00	R/W
0x083	DACPLLCNTRL	RECAL_ DACPLL	RESERVED		ENABLE_ DACPLL	RESERVED				0x00	R/W
0x084	DACPLLSTATUS	DACPLL_ OVER- RANGE_H	DACPLL_ OVER- RANGE_L	DACPLL_ CAL_VALID	RESERVED			DACPLL_ LOCK	RESERVED	0x00	R
0x085	DACINTEGER- WORD0	B_COUNT								0x08	R/W
0x087	DACLOOPFILT1	LF_C2_WORD				LF_C1_WORD				0x88	R/W
0x088	DACLOOPFILT2	LF_R1_WORD				LF_C3_WORD				0x88	R/W
0x089	DACLOOPFILT3	LF_ BYPASS_ R3	LF_ BYPASS_R1	LF_BYPASS_ C2	LF_BYPASS_C1	LF_R3_WORD				0x08	R/W
0x08A	DACCPCNTRL	RESERVED		CP_CURRENT						0x20	R/W
0x08B	DACLOGENCNTRL	RESERVED						LO_DIV_MODE		0x02	R/W
0x08C	DACLDOCNTRL1	RESERVED					REF_DIV_MODE			0x01	R/W
0x0E2	CAL_CTRL_ GLOBAL	RESERVED						CAL_START_ AVG	CAL_EN_ AVG	0x00	R/W
0x0E7	CAL_CLKDIV	RESERVED				CAL_CLK_EN	RESERVED			0x30	R/W
0x0E8	CAL_PAGE	RESERVED				CAL_PAGE				0x0F	R/W
0x0E9	CAL_CTRL	CAL_FIN	CAL_ ACTIVE	CAL_ERRHI	CAL_ERRLO	RESERVED		CAL_START	CAL_EN	0x00	R/W
0x0ED	CAL_INIT	CAL_INIT								A6	R/W
0x110	DATA_FORMAT	BINARY_ FORMAT	RESERVED							00	R/W
0x111	DATAPATH_CTRL	INVSINC_ ENABLE	RESERVED	DIG_GAIN_ ENABLE	PHASE_ADJ_ ENABLE	MODULATION_TYPE		SEL_SIDE- BAND	I_TO_Q	0xA0	R/W
0x112	INTERP_MODE	RESERVED					INTERP_MODE			0x01	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x113	NCO_FTW_ UPDATE	RESERVED						FTW_UPDATE_ ACK	FTW_ UPDATE_ REQ	0x00	R/W
0x114	FTW0	FTW[7:0]								0x00	R/W
0x115	FTW1	FTW[15:8]								0x00	R/W
0x116	FTW2	FTW[23:16]								0x00	R/W
0x117	FTW3	FTW[31:24]								0x00	R/W
0x118	FTW4	FTW[39:32]								0x00	R/W
0x119	FTW5	FTW[47:40]								0x10	R/W
0x11A	NCO_PHASE_ OFFSET0	NCO_PHASE_OFFSET[7:0]								0x00	R/W
0x11B	NCO_PHASE_ OFFSET1	NCO_PHASE_OFFSET[15:8]								0x00	R/W
0x11C	PHASE_ADJ0	PHASE_ADJ[7:0]								0x00	R/W
0x11D	PHASE_ADJ1	RESERVED			PHASE_ADJ[12:8]					0x00	R/W
0x11F	TXEN_SM_0	FALL_COUNTERS		RISE_COUNTERS		RESERVED	PROTECT_OUT_ INVERT	RESERVED		0x83	R/W
0x121	TXEN_RISE_ COUNT_0	RISE_COUNT_0								0x0F	R/W
0x122	TXEN_RISE_ COUNT_1	RISE_COUNT_1								0x00	R/W
0x123	TXEN_FALL_ COUNT_0	FALL_COUNT_0								0xFF	R/W
0x124	TXEN_FALL_ COUNT_1	FALL_COUNT_1								0xFF	R/W
0x12D	DEVICE_CONFIG_ REG_0	DEVICE_CONFIG_0								0x46	R/W
0x12F	DIE_TEMP_CTRL0	RESERVED							AUXADC_ ENABLE	0x20	R/W
0x132	DIE_TEMP0	DIE_TEMP[7:0]								0x00	R
0x133	DIE_TEMP1	DIE_TEMP[15:8]								0x00	R
0x134	DIE_TEMP_ UPDATE	RESERVED							DIE_TEMP_ UPDATE	0x00	R/W
0x135	DC_OFFSET_CTRL	RESERVED							DC_OFFSET_ ON	0x00	R/W
0x136	IPATH_DC_ OFFSET_1PART0	LSB_OFFSET_I[7:0]								0x00	R/W
0x137	IPATH_DC_ OFFSET_1PART1	LSB_OFFSET_I[15:8]								0x00	R/W
0x138	QPATH_DC_ OFFSET_1PART0	LSB_OFFSET_Q[7:0]								0x00	R/W
0x139	QPATH_DC_ OFFSET_1PART1	LSB_OFFSET_Q[15:8]								0x00	R/W
0x13A	IPATH_DC_ OFFSET_2PART	RESERVED			SIXTEENTH_OFFSET_I					0x00	R/W
0x13B	QPATH_DC_ OFFSET_2PART	RESERVED			SIXTEENTH_OFFSET_Q					0x00	R/W
0x13C	IDAC_DIG_GAIN0	IDAC_DIG_GAIN[7:0]								0xEA	R/W
0x13D	IDAC_DIG_GAIN1	RESERVED				IDAC_DIG_GAIN[11:8]				0x0A	R/W
0x13E	QDAC_DIG_ GAIN0	QDAC_DIG_GAIN[7:0]								0xEA	R/W
0x13F	QDAC_DIG_GAIN1	RESERVED				QDAC_DIG_GAIN[11:8]				0x0A	R/W
0x140	GAIN_RAMP_UP_ STEP0	GAIN_RAMP_UP_STEP[7:0]								0x04	R/W
0x141	GAIN_RAMP_ UP_STEP1	RESERVED				GAIN_RAMP_UP_STEP[11:8]				0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x142	GAIN_RAMP_ DOWN_STEP0	GAIN_RAMP_DOWN_STEP[7:0]								0x09	R/W
0x143	GAIN_RAMP_ DOWN_STEP1	RESERVED				GAIN_RAMP_DOWN_STEP[11:8]				0x00	R/W
0x146	DEVICE_CONFIG_ REG_1	DEVICE_CONFIG_1								0x00	R/W
0x147	BSM_STAT	SOFTBLANKRB		RESERVED						0x00	R
0x14B	PRBS	PRBS_ GOOD_Q	PRBS_ GOOD_I	RESERVED			PRBS_MODE	PRBS_RESET	PRBS_EN	0x10	R/W
0x14C	PRBS_ERROR_I	PRBS_COUNT_I								0x00	R
0x14D	PRBS_ERROR_Q	PRBS_COUNT_Q								0x00	R
0x1B4	DACPLLT4	RESERVED	VCO_CAL_OFFSET				RESERVED			0x78	R/W
0x1B5	DACPLLT5	RESERVED				VCO_VAR				0x83	R/W
0x1B6	DACPLLT6	RESERVED				VCO_LVL_OUT				0x4A	R/W
0x1BB	DACPLLTB	RESERVED			VCO_BIAS_TCF		VCO_BIAS_REF			0x0C	R/W
0x1BD	DACPLLTD	RESERVED					VCO_CAL_REF_TCF			0x00	R/W
0x1C4	DEVICE_CONFIG_ REG_2	DEVICE_CONFIG_2								0x33	R/W
0x200	MASTER_PD	RESERVED							SPI_PD_ MASTER	0x01	R/W
0x201	PHY_PD	SPI_PD_PHY								0x00	R/W
0x203	GENERIC_PD	RESERVED						SPI_ SYNC1_PD	SPI_ SYNC2_PD	0x00	R/W
0x206	CDR_RESET	RESERVED							SPI_CDR_ RESETN	0x01	R/W
0x230	CDR_OPERATING_ MODE_REG_0	RESERVED		ENHALFRATE	RESERVED			CDR_OVER- SAMP	RESERVED	0x28	R/W
0x232	DEVICE_CONFIG_ REG_3	DEVICE_CONFIG_3								0x0	R/W
0x268	EQ_BIAS_REG	EQ_POWER_MODE		RESERVED						0x62	R/W
0x280	SERDESPLL_ ENABLE_CNTRL	RESERVED					RECAL_ SERDESPLL	RESERVED	ENABLE_ SERDESPLL	0x00	R/W
0x281	PLL_STATUS	RESERVED		SERDES_PLL_ OVERRANGE_ H	SERDES_PLL_ OVERRANGE_L	SERDES_PLL_CAL_ VALID_RB	RESERVED		SERDES_PLL_ LOCK_RB	0x00	R
0x289	REF_CLK_ DIVIDER_LDO	RESERVED					DEVICE_ CONFIG_4	SERDES_PLL_DIV_MODE		0x00	R/W
0x291	DEVICE_CONFIG_ REG_5	DEVICE_CONFIG_5								0x46	R/W
0x29C	DEVICE_CONFIG_ REG_6	DEVICE_CONFIG_6								0x17	R/W
0x29F	DEVICE_CONFIG_ REG_7	DEVICE_CONFIG_7								0x33	R/W
0x2A4	DEVICE_CONFIG_ REG_8	DEVICE_CONFIG_8								0x4B	R/W
0x2A5	SYNCOUTB_ SWING	RESERVED							SYNCOUTB_ SWING_MD	0x00	R/W
0x2A7	TERM_BLK1_ CTRLREG0	RESERVED							RCAL_ TERMBLK1	0x00	R/W
0x2AA	DEVICE_CONFIG_ REG_9	DEVICE_CONFIG_9								0xC3	R/W
0x2AB	DEVICE_CONFIG_ REG_10	DEVICE_CONFIG_10								0x93	R/W
0x2AE	TERM_BLK2_ CTRLREG0	RESERVED							RCAL_ TERMBLK2	0x00	R/W
0x2B1	DEVICE_CONFIG_ REG_11	DEVICE_CONFIG_11								0xC3	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x2B2	DEVICE_CONFIG_REG_12	DEVICE_CONFIG_12								0x93	R/W
0x300	GENERAL_JRX_CTRL_0	RESERVED	CHECKSUM_MODE	RESERVED		LINK_MODE	LINK_PAGE	LINK_EN		0x00	R/W
0x301	GENERAL_JRX_CTRL_1	RESERVED					SUBCLASSV_LOCAL			0x01	R/W
0x302	DYN_LINK_LATENCY_0	RESERVED			DYN_LINK_LATENCY_0					0x00	R
0x303	DYN_LINK_LATENCY_1	RESERVED			DYN_LINK_LATENCY_1					0x00	R
0x304	LMFC_DELAY_0	RESERVED			LMFC_DELAY_0					0x00	R/W
0x305	LMFC_DELAY_1	RESERVED			LMFC_DELAY_1					0x00	R/W
0x306	LMFC_VAR_0	RESERVED			LMFC_VAR_0					0x06	R/W
0x307	LMFC_VAR_1	RESERVED			LMFC_VAR_1					0x06	R/W
0x308	XBAR_LN_0_1	RESERVED		LOGICAL_LANE1_SRC			LOGICAL_LANE0_SRC			0x08	R/W
0x309	XBAR_LN_2_3	RESERVED		LOGICAL_LANE3_SRC			LOGICAL_LANE2_SRC			0x1A	R/W
0x30A	XBAR_LN_4_5	RESERVED		LOGICAL_LANE5_SRC			LOGICAL_LANE4_SRC			0x2C	R/W
0x30B	XBAR_LN_6_7	RESERVED		LOGICAL_LANE7_SRC			LOGICAL_LANE6_SRC			0x3E	R/W
0x30C	FIFO_STATUS_REG_0	LANE_FIFO_FULL								0x00	R
0x30D	FIFO_STATUS_REG_1	LANE_FIFO_EMPTY								0x00	R
0x312	SYNCB_GEN_1	RESERVED		SYNCB_ERR_DUR		RESERVED				0x00	R/W
0x314	SERDES_SPI_REG	SERDES_SPI_CONFIG								0x00	R/W
0x315	PHY_PRBS_TEST_EN	PHY_TEST_EN								0x00	R/W
0x316	PHY_PRBS_TEST_CTRL	RESERVED	PHY_SRC_ERR_CNT			PHY_PRBS_PAT_SEL		PHY_TEST_START	PHY_TEST_RESET	0x00	R/W
0x317	PHY_PRBS_TEST_THRESHOLD_LOBITS	PHY_PRBS_THRESHOLD[7:0]								0x00	R/W
0x318	PHY_PRBS_TEST_THRESHOLD_MIDBITS	PHY_PRBS_THRESHOLD[15:8]								0x00	R/W
0x319	PHY_PRBS_TEST_THRESHOLD_HIBITS	PHY_PRBS_THRESHOLD[23:16]								0x00	R/W
0x31A	PHY_PRBS_TEST_ERRCNT_LOBITS	PHY_PRBS_ERR_CNT[7:0]								0x00	R
0x31B	PHY_PRBS_TEST_ERRCNT_MIDBITS	PHY_PRBS_ERR_CNT[15:8]								0x00	R
0x31C	PHY_PRBS_TEST_ERRCNT_HIBITS	PHY_PRBS_ERR_CNT[23:16]								0x00	R
0x31D	PHY_PRBS_TEST_STATUS	PHY_PRBS_PASS								0xFF	R
0x32C	SHORT_TPL_TEST_0	RESERVED		SHORT_TPL_SP_SEL		SHORT_TPL_DAC_SEL		SHORT_TPL_TEST_RESET	SHORT_TPL_TEST_EN	0x00	R/W
0x32D	SHORT_TPL_TEST_1	SHORT_TPL_REF_SP_LSB								0x00	R/W
0x32E	SHORT_TPL_TEST_2	SHORT_TPL_REF_SP_MSB								0x00	R/W
0x32F	SHORT_TPL_TEST_3	RESERVED							SHORT_TPL_FAIL	0x00	R
0x333	DEVICE_CONFIG_REG_13	DEVICE_CONFIG_13								0x00	R/W
0x334	JESD_BIT_INVERSE_CTRL	JESD_BIT_INVERSE								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x400	DID_REG	DID_RD								0x00	R
0x401	BID_REG	ADJCNT_RD				BID_RD				0x00	R
0x402	LID0_REG	RESERVED	ADJDIR_RD	PHADJ_RD	LID0_RD					0x00	R
0x403	SCR_L_REG	SCR_RD	RESERVED		L-1_RD					0x00	R
0x404	F_REG	F-1_RD								0x00	R
0x405	K_REG	RESERVED			K-1_RD					0x00	R
0x406	M_REG	M-1_RD								0x00	R
0x407	CS_N_REG	CS_RD		RESERVED	N-1_RD					0x00	R
0x408	NP_REG	SUBCLASSV_RD			NP-1_RD					0x00	R
0x409	S_REG	JESDV_RD			S-1_RD					0x00	R
0x40A	HD_CF_REG	HD_RD	RESERVED		CF_RD					0x00	R
0x40B	RES1_REG	RES1_RD								0x00	R
0x40C	RES2_REG	RES2_RD								0x00	R
0x40D	CHECKSUM_REG	FCHK0_RD								0x00	R
0x40E	COMPSUM0_REG	FCMP0_RD								0x00	R
0x412	LID1_REG	RESERVED			LID1_RD					0x00	R
0x415	CHECKSUM1_REG	FCHK1_RD								0x00	R
0x416	COMPSUM1_REG	FCMP1_RD								0x00	R
0x41A	LID2_REG	RESERVED			LID2_RD					0x00	R
0x41D	CHECKSUM2_REG	FCHK2_RD								0x00	R
0x41E	COMPSUM2_REG	FCMP2_RD								0x00	R
0x422	LID3_REG	RESERVED			LID3_RD					0x00	R
0x425	CHECKSUM3_REG	FCHK3_RD								0x00	R
0x426	COMPSUM3_REG	FCMP3_RD								0x00	R
0x42A	LID4_REG	RESERVED			LID4_RD					0x00	R
0x42D	CHECKSUM4_REG	FCHK4_RD								0x00	R
0x42E	COMPSUM4_REG	FCMP4_RD								0x00	R
0x432	LID5_REG	RESERVED			LID5_RD					0x00	R
0x435	CHECKSUM5_REG	FCHK5_RD								0x00	R
0x436	COMPSUM5_REG	FCMP5_RD								0x00	R
0x43A	LID6_REG	RESERVED			LID6_RD					0x00	R
0x43D	CHECKSUM6_REG	FCHK6_RD								0x00	R
0x43E	COMPSUM6_REG	FCMP6_RD								0x00	R
0x442	LID7_REG	RESERVED			LID7_RD					0x00	R
0x445	CHECKSUM7_REG	FCHK7_RD								0x00	R
0x446	COMPSUM7_REG	FCMP7_RD								0x00	R
0x450	ILS_DID	DID								0x00	R/W
0x451	ILS_BID	ADJCNT				BID				0x00	R/W
0x452	ILS_LID0	RESERVED	ADJDIR	PHADJ	LID0					0x00	R/W
0x453	ILS_SCR_L	SCR	RESERVED		L-1					0x83	R/W
0x454	ILS_F	F-1								0x00	R/W
0x455	ILS_K	RESERVED			K-1					0x1F	R/W
0x456	ILS_M	M-1								0x01	R/W
0x457	ILS_CS_N	CS		RESERVED	N-1					0x0F	R/W
0x458	ILS_NP	SUBCLASSV			NP-1					0x2F	R/W
0x459	ILS_S	JESDV			S-1					0x20	R/W
0x45A	ILS_HD_CF	HD	RESERVED		CF					0x80	R/W
0x45B	ILS_RES1	RES1								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x45C	ILS_RES2	RES2								0x00	R/W
0x45D	ILS_CHECKSUM	FCHK0								0x45	R/W
0x46B	ERRCNTRMON_RB	READERRORCNTR								0x00	R
0x46B	ERRCNTRMON	RESERVED	LANESEL			RESERVED		CNTRSEL		0x00	R/W
0x46C	LANEDESKEW	LANEDESKEW								0x0F	R/W
0x46D	BADDISPARITY_RB	BADDIS								0x00	R
0x46D	BADDISPARITY	RST_IRQ_ DIS	DISABLE_ ERR_CNTR_ DIS	RST_ERR_ CNTR_DIS	RESERVED		LANE_ADDR_DIS			0x00	R/W
0x46E	NIT_RB	NIT								0x00	R
0x46E	NIT_W	RST_IRQ_ NIT	DISABLE_ ERR_CNTR_ NIT	RST_ERR_ CNTR_NIT	RESERVED		LANE_ADDR_NIT			0x00	R/W
0x46F	UNEXPECTED-CONTROL_RB	UCC								0x00	R
0x46F	UNEXPECTED-CONTROL_W	RST_IRQ_ UCC	DISABLE_ ERR_CNTR_ UCC	RST_ERR_ CNTR_UCC	RESERVED		LANE_ADDR_UCC			0x00	R/W
0x470	CODEGRPSYNCFLG	CODEGRPSYNC								0x00	R/W
0x471	FRAMESYNCFLG	FRAMESYNC								0x00	R/W
0x472	GOODCHKSUMFLG	GOODCHECKSUM								0x00	R/W
0x473	INITLANESYNCFLG	INITIALLANESYNC								0x00	R/W
0x476	CTRLREG1	F								0x01	R/W
0x477	CTRLREG2	ILAS_ MODE	RESERVED			THRESHOLD_ MASK_EN	RESERVED			0x00	R/W
0x478	KVAL	KSYNC								0x01	R/W
0x47A	IRQVECTOR_MASK	BADDIS_ MASK	NIT_MASK	UCC_ MASK	RESERVED	INITIALLANESYNC_ MASK	BADCHECK SUM_MASK	FRAMESYNC_ MASK	CODEGRP SYNC_MASK	0x00	R/W
0x47A	IRQVECTOR_FLAG	BADDIS_ FLAG	NIT_FLAG	UCC_FLAG	RESERVED	INITIALLANESYNC_ FLAG	BADCHECKSUM _FLAG	FRAMESYNC_ FLAG	CODEGRP SYNC_FLAG	0x00	R
0x47B	SYNCASSERTION-MASK	BADDIS_S	NIT_S	UCC_S	CMM	CMM_ENABLE	RESERVED			0x008	R/W
0x47C	ERRORTHRES	ETH								0xFF	R/W
0x47D	LANEENABLE	LANE_ENA								0x0F	R/W
0x47E	RAMP_ENA	RESERVED							ENA_RAMP_ CHECK	0x00	R/W
0x520	DIG_TEST0	RESERVED						DC_TEST_ MODE	RESERVED	0x1C	R/W
0x521	DC_TEST_VALUEI0	DC_TEST_VALUEI[7:0]								0x00	R/W
0x522	DC_TEST_VALUEI1	DC_TEST_VALUEI[15:8]								0x00	R/W
0x523	DC_TEST_ VALUEQ0	DC_TEST_VALUEQ[7:0]								0x00	R/W
0x524	DC_TEST_ VALUEQ1	DC_TEST_VALUEQ[15:8]								0x00	R/W

DEVICE CONFIGURATION REGISTER DESCRIPTIONS

Table 95. Device Configuration Register Descriptions

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x000	SPI_INTFCONFA	7	SOFTRESET_M		Soft Reset (Mirror).	0x0	R
		6	LSBFIRST_M		LSB First (Mirror).	0x0	R
		5	ADDRINC_M		Address Increment (Mirror).	0x0	R
		4	SDOACTIVE_M		SDO Active (Mirror).	0x0	R
		3	SDOACTIVE		SDO Active.	0x0	R/W
		2	ADDRINC		Address Increment. Controls whether addresses are incremented or decremented during multibyte data transfers.	0x0	R/W
				1	Addresses are incremented during multibyte data transfers		
				0	Addresses are decremented during multibyte data transfers		
		1	LSBFIRST		LSB First. Controls whether input and output data are oriented as LSB first or MSB first.	0x0	R/W
				1	Shift LSB in first		
				0	Shift MSB in first		
		0	SOFTRESET		Soft Reset. Setting this bit initiates a reset. This bit is autoclearing after the soft reset is complete.	0x0	R/W
				1	Assert soft reset		
0x003	CHIPTYPE	[7:0]	CHIPTYPE		The product type is “High Speed DAC”, which is represented by a code of 0x04.	0x4	R
0x004	PRODIDL	[7:0]	PRODIDL		Product Identification Low.	0x44	R
0x005	PRODIDH	[7:0]	PRODIDH		Product Identification High.	0x91	R
0x006	CHIPGRADE	[7:4]	PROD_GRADE		Product Grade.	0x0	R
		[3:0]	DEV_REVISION		Device Revision.	0x2	R
0x008	SPI_PAGEINDX	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DUAL_PAGE		Dual Paging. Selects which dual DAC pair is accessed and written to when changing digital features, such as digital gain, dc offset, NCO FTW, etc. This paging affects Registers: 0x013-0x014, 0x034-0x03d, 0x050-0x064,0x110-0x124, and 0x135-0x14D.	0x3	R/W
				0b01	Read and write Dual A		
				0b10	Read and write Dual B		
				0b11	Write both duals; read Dual A		
0x011	PWRCNTRL0	7	PD_BG		Reference Power-Down. Powers down the band gap reference for the entire chip. Circuits will not be provided with bias currents.	0x0	R/W
				1	Power down reference		
		6	PD_DAC_0		Powers Down DAC0. Powers down the I-channel DAC of Dual A.	0x1	R/W
				1	Powers down DAC0		
		5	PD_DAC_1		Powers Down DAC1. Powers down the Q-channel DAC of Dual A.	0x1	R/W
				1	Powers down DAC 1		
		4	PD_DAC_2		Powers Down DAC2. Powers down the I-channel DAC of Dual B.	0x1	R/W
				1	Powers down DAC 2		
		3	PD_DAC_3		Powers Down DAC3. Powers down the Q-channel DAC of Dual B.	0x1	R/W
				1	Powers down DAC 3		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		2	PD_DACM		Powers Down the DAC Master Bias. The master bias cell provides currents and DAC full-scale adjustments to the four DACs. With the DAC master bias powered down, the DACs are inoperative.	0x1	R/W
				1	Powers down the DAC master bias		
		[1:0]	RESERVED		Reserved.	0x0	R
0x012	TXENMASK	[7:2]	RESERVED		Reserved.	0x0	R
		1	DUALB_MASK		Dual B TXEN1 Mask. Power down Dual B on a falling edge of TXEN1.	0x0	R/W
				1	If TXEN1 is low, power down DAC2 and DAC3		
		0	DUALA_MASK		Dual A TXEN0 Mask. Power down Dual A on a falling edge of TXEN0.	0x0	R/W
				1	If TXEN0 is low, power down DAC0 and DAC1		
0x013	PWRCNTRL3	7	RESERVED		Reserved.	0x0	R
		6	PDP_PROTECT_ OUT	1	PDP_PROTECT triggers PROTECT_OUTx.	0x0	R/W
		5	TX_PROTECT_OUT	1	TX_PROTECT triggers PROTECT_OUTx.	0x1	R/W
		4	RESERVED		Reserved.	0x0	R
		3	SPI_PROTECT_ OUT	1	SPI_PROTECT triggers PROTECT_OUTx.	0x0	R/W
		2	SPI_PROTECT		SPI_PROTECT	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x014	GROUP_DLY	[7:4]	RESERVED		Reserved.	0x8	R
		[3:0]	GROUP_DLY		Group Delay Control. Delays the I and Q channel outputs together. 0 = minimum delay. 15 = maximum delay. The range of the delay is −4 to +3.5 DAC clock periods, and the resolution is 1/2 DAC clock period.	0x8	R/W
0x01F	IRQEN_ STATUSMODE0	7	IRQEN_SMODE_ CALPASS		Calibration Pass Detection Status Mode.	0x0	R/W
				1	If CALPASS goes high, it latches and pulls $\overline{IRQ}$ low		
				0	CALPASS shows current status		
		6	IRQEN_SMODE_ CALFAIL		Calibration Fail Detection Status Mode.	0x0	R/W
				1	If CALFAIL goes high, it latches and pulls $\overline{IRQ}$ low		
				0	CALFAIL shows current status		
		5	IRQEN_SMODE_ DACPLLLOST		DAC PLL Lost Detection Status Mode.	0x0	R/W
				1	If DACPLLLOST goes high, it latches and pulls $\overline{IRQ}$ low		
				0	DACPLLLOST shows current status		
		4	IRQEN_SMODE_ DACPLLLOCK		DAC PLL Lock Detection Status Mode.	0x0	R/W
				1	If DACPLLLOCK goes high, it latches and pulls $\overline{IRQ}$ low		
				0	DACPLLLOCK shows current status		
		3	IRQEN_SMODE_ SERPLLLOST		SERDES PLL Lost Detection Status Mode.	0x0	R/W
				1	If SERPLLLOST goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SERPLLLOST shows current status		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		2	IRQEN_SMODE_SERPLLLOCK		SERDES PLL Lock Detection Status Mode.	0x0	R/W
				1	If SERPLLLOCK goes high, it latches and pulls IRQ low		
				0	SERPLLLOCK shows current status		
		1	IRQEN_SMODE_LANEFIFOERR		Lane FIFO Error Detection Status Mode.	0x0	R/W
				1	If LANEFIFOERR goes high, latches and pulls IRQ low		
				0	LANEFIFOERR shows current status		
		0	RESERVED		Reserved.	0x0	R
0x020	IRQEN_STATUSMODE1	[7:4]	RESERVED		Reserved.	0x0	R
		3	IRQEN_SMODE_PRBS3		DAC3 PRBS Error Status Mode..	0x0	R/W
				1	If PRBS3 goes high, it latches and pulls IRQ low		
				0	PRBS3 shows current status		
		2	IRQEN_SMODE_PRBS2		DAC2 PRBS Error Status Mode.	0x0	R/W
				1	If PRBS2 goes high, it latches and pulls IRQ low		
				0	PRBS2 shows current status		
		1	IRQEN_SMODE_PRBS1		DAC1 PRBS Error Status Mode.	0x0	R/W
				1	If PRBS1 goes high, it latches and pulls IRQ low		
				0	PRBS1 shows current status		
		0	IRQEN_SMODE_PRBS0		DAC0 PRBS Error Status Mode.	0x0	R/W
				1	If PRBS0 goes high, it latches and pulls IRQ low		
				0	PRBS0 shows current status		
0x021	IRQEN_STATUSMODE2	7	IRQEN_SMODE_PDPERR0		Dual A PDP Error.	0x0	R/W
				1	If PDPERR0 goes high, it latches and pulls IRQ low		
				0	PDPERR0 shows current status		
		6	RESERVED		Reserved.	0x0	R
		5	IRQEN_SMODE_BLNKDONE0		Dual A Blanking Done Status Mode.	0x0	R/W
				1	If BLNKDONE0 goes high, it latches and pulls IRQ low		
				0	BLNKDONE0 shows current status		
		4	IRQEN_SMODE_NCO_ALIGN0		Dual A NCO Align Tripped Status Mode	0x0	R/W
				1	If NCO_ALIGN0 goes high, it latches and pulls IRQ low		
				0	NCO_ALIGN0 shows current status		
		3	IRQEN_SMODE_SYNC_LOCK0		Dual A Alignment Locked Status Mode.	0x0	R/W
				1	If SYNC_LOCK0 goes high, it latches and pulls IRQ low		
				0	SYNC_LOCK0 shows current status		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		2	IRQEN_SMODE_ SYNC_ROTATE0		Dual A Alignment Rotate Status Mode.	0x0	R/W
				1	If SYNC_ROTATE0 goes high, it latches and pulls IRQ low		
				0	SYNC_ROTATE0 shows current status		
		1	IRQEN_SMODE_ SYNC_WLIM0		Dual A Outside Window Status Mode.	0x0	R/W
				1	If SYNC_WLIM0 goes high, it latches and pulls IRQ low		
				0	SYNC_WLIM0 shows current status		
		0	IRQEN_SMODE_ SYNC_TRIP0		Dual A Alignment Tripped Status Mode.	0x0	R/W
				1	If SYNC_TRIP0 goes high, it latches and pulls IRQ low		
				0	SYNC_TRIP0 shows current status		
0x022	IRQEN_ STATUSMODE3	7	IRQEN_SMODE_ PDPERR1		Dual B PDP Error.	0x0	R/W
				1	If PDPERR1 goes high, it latches and pulls IRQ low		
				0	PDPERR1 shows current status		
		6	RESERVED		Reserved.	0x0	R
		5	IRQEN_SMODE_ BLNKDONE1		Dual B Blanking Done Status Mode.	0x0	R/W
				1	If BLNKDONE1 goes high, it latches and pulls IRQ low		
				0	BLNKDONE1 shows current status		
		4	IRQEN_SMODE_ NCO_ALIGN1		Dual B NCO Align Tripped Status Mode	0x0	R/W
				1	If NCO_ALIGN1 goes high, it latches and pulls IRQ low		
				0	NCO_ALIGN1 shows current status		
		3	IRQEN_SMODE_ SYNC_LOCK1		Dual B Alignment Locked Status Mode.	0x0	R/W
				1	If SYNC_LOCK1 goes high, it latches and pulls IRQ low		
				0	SYNC_LOCK1 shows current status		
		2	IRQEN_SMODE_ SYNC_ROTATE1		Dual B Alignment Rotate Status Mode.	0x0	R/W
				1	If SYNC_ROTATE1 goes high, it latches and pulls IRQ low		
				0	SYNC_ROTATE1 shows current status		
		1	IRQEN_SMODE_ SYNC_WLIM1		Dual B Outside Window Status Mode.	0x0	R/W
				1	If SYNC_WLIM1 goes high, it latches and pulls IRQ low		
				0	SYNC_WLIM1 shows current status		
		0	IRQEN_SMODE_ SYNC_TRIP1		Dual B Alignment Tripped Status Mode.	0x0	R/W
				1	If SYNC_TRIP1 goes high, it latches and pulls IRQ low		
				0	SYNC_TRIP1 shows current status		
0x023	IRQ_STATUS0	7	CALPASS		Calibration Pass Status. If IRQEN_SMODE_CALPASS is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Calibration passed		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		6	CALFAIL		Calibration Fail Detection Status. If IRQEN_SMODE_CALFAIL is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Calibration failed		
		5	DACPLLLOST		DAC PLL Lost Status. If IRQEN_SMODE_DACPLLLOST is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC PLL lock was lost		
		4	DACPLLLOCK		DAC PLL Lock Status. If IRQEN_SMODE_DACPLLLOCK is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC PLL locked		
		3	SERPLLLOST		SERDES PLL Lost Status. If IRQEN_SMODE_SERPLLLOST is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	SERDES PLL lock was lost		
		2	SERPLLLOCK		SERDES PLL Lock Status. If IRQEN_SMODE_SERPLLLOCK is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	SERDES PLL locked		
		1	LANEFIFOERR		Lane FIFO Error Status. If IRQEN_SMODE_LANEFIFOERR is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. A lane FIFO error occurs when there is a full or empty condition on any of the FIFOs between the deserializer block and the core digital. This error requires a link disable and reenable to remove it. The status of the lane FIFOs can be found in Register 0x30C (FIFO full), and Register 0x30D (FIFO empty).	0x0	R
				1	Lane FIFO error		
		0	RESERVED		Reserved.	0x0	R
0x024	IRQ_STATUS1	[7:4]	RESERVED		Reserved.	0x0	R
		3	PRBS3		DAC3 PRBS Error Status. If IRQEN_SMODE_PRBS3 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC3 failed PRBS		
		2	PRBS2		DAC2 PRBS Error Status. If IRQEN_SMODE_PRBS2 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC2 failed PRBS		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		1	PRBS1		DAC1 PRBS Error Status. If IRQEN_SMODE_PRBS1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 failed PRBS		
		0	PRBS0		DAC0 PRBS Error Status. If IRQEN_SMODE_PRBS0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 failed PRBS		
0x025	IRQ_STATUS2	7	PDPERR0		Dual A PDP Error. If IRQEN_SMODE_PAERR0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Data into Dual A over power threshold		
		6	RESERVED		Reserved.	0x0	R
		5	BLNKDONE0		Dual A Blanking Done Status. If IRQEN_SMODE_BLNKDONE0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual A blanking done		
		4	NCO_ALIGN0		Dual A NCO Align Tripped Status. If IRQEN_SMODE_NCO_ALIGN0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual A NCO align tripped		
		3	SYNC_LOCK0		Dual A LMFC Alignment Locked Status. If IRQEN_SMODE_SYNC_LOCK0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual A LMFC alignment locked		
		2	SYNC_ROTATE0		Dual A LMFC Alignment Rotate Status. If IRQEN_SMODE_SYNC_ROTATE0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual A LMFC alignment rotated		
		1	SYNC_WLIM0		Dual A Outside Window Status. If IRQEN_SMODE_SYNC_WLIM0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual A LMFC phase outside of window		
		0	SYNC_TRIP0		Dual A LMFC Alignment Tripped Status. If IRQEN_SMODE_SYNC_TRIP0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual A LMFC alignment tripped		
0x026	IRQ_STATUS3	7	PDPERR1		Dual B PDP Error. If IRQ_SMODE_PDPERR1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Data into Dual B over power threshold		
		6	RESERVED		Reserved.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		5	BLNKDONE1		Dual B Blanking Done Status. If IRQEN_SMODE_BLNKDONE1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual B blanking done		
		4	NCO_ALIGN1		Dual B NCO Align Tripped Status. If IRQEN_SMODE_NCO_ALIGN1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual B NCO align tripped		
		3	SYNC_LOCK1		Dual B LMFC Alignment Locked Status. If IRQEN_SMODE_SYNC_LOCK1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual B LMFC alignment locked		
		2	SYNC_ROTATE1		Dual B LMFC Alignment Rotate Status. If IRQEN_SMODE_SYNC_ROTATE1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual B LMFC alignment rotated		
		1	SYNC_WLIM1		Dual B Outside Window Status. If IRQEN_SMODE_SYNC_WLIM1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual B LMFC phase outside of window		
		0	SYNC_TRIP1		Dual B LMFC Alignment Tripped Status. If IRQEN_SMODE_SYNC_TRIP1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Dual B LMFC alignment tripped		
0x030	JESD_CHECKS	[7:6]	RESERVED		Reserved.	0x0	R
		5	ERR_DLYOVER		Error: LMFC_Delay > JESD_K Parameter.	0x0	R
				1	LMFC_Delay > JESD_K		
		4	ERR_WINLIMIT		Unsupported Window Limit.	0x0	R
				1	Unsupported SYSREF window limit		
		3	ERR_JESDBAD		Unsupported M/L/S/F Selection.	0x0	R
				1	This JESD combination is not supported		
		2	ERR_KUNSUPP		Unsupported K Values. 16 and 32 are supported.	0x0	R
				1	K value unsupported		
		1	ERR_SUBCLASS		Unsupported Subclass Value. 0 and 1 are supported.	0x0	R
				1	Unsupported subclass value		
		0	ERR_INTSUPP		Unsupported Interpolation Rate Factor. 1, 2, 4, 8 are supported.	0x0	R
				1	Unsupported interpolation rate factor		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x034	SYNC_ERRWINDOW	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	ERRWINDOW		LMFC Sync Error Window. The error window allows the SYSREF sample phase to vary within the confines of the window without triggering a clock adjustment. This is useful if SYSREF cannot be guaranteed to always arrive in the same period of the device clock associated with the target phase. Error window tolerance = ± ERRWINDOW	0x0	R/W
0x038	SYNC_LASTERR_L	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	LASTERROR		LMFC Sync Last Alignment Error. 4-bit twos complement value that represents the phase error (in number of DAC clock cycles) when the clocks were last adjusted.		R
0x039	SYNC_LASTERR_H	7	LASTUNDER		LMFC Sync Last Error Under Flag.	0x0	R
				1	Last phase error was beyond lower window tolerance boundary		
		6	LASTOVER		LMFC Sync Last Error Over Flag.	0x0	R
				1	Last phase error was beyond upper window tolerance boundary		
		[5:0]	RESERVED		Reserved.	0x0	R
0x03A	SYNC_CONTROL	7	SYNCENABLE		LMFC Sync Logic Enable.	0x0	R/W
				1	Enable sync logic		
				0	Disable sync logic		
		6	SYNCARM		LMFC Sync Arming Strobe.	0x0	R/W
				1	Sync one shot armed		
		5	SYNCCLRSTKY		LMFC Sync Sticky Bit Clear. On a rising edge, this bit clears SYNC_ROTATE and SYNC_TRIP.	0x0	R/W
		4	SYNCCLRLAST		LMFC Sync Clear Last Error. On a rising edge, this bit clears LASTERROR, LASTUNDER, LASTOVER.	0x0	R/W
		[3:0]	SYNCMODE		LMFC Sync Mode.	0x0	R/W
				0b0001	Sync one shot mode		
				0b0010	Sync continuous mode		
				0b1000	Sync monitor only mode		
				0b1001	Sync one shot, then monitor		
0x03B	SYNC_STATUS	7	SYNC_BUSY		LMFC Sync Machine Busy.	0x0	R
				1	Sync logic SM is busy		
		[6:4]	RESERVED		Reserved.	0x0	R
		3	SYNC_LOCK		LMFC Sync Alignment Locked.	0x0	R
				1	Sync logic aligned within window		
		2	SYNC_ROTATE		LMFC Sync Rotated.	0x0	R
				1	Sync logic rotated with SYSREF (sticky)		
		1	SYNC_WLIM		LMFC Sync Alignment Limit Range.	0x0	R
				1	Phase error outside window threshold		
		0	SYNC_TRIP		LMFC Sync Tripped After Arming.	0x0	R
				1	Sync received SYSREF pulse (sticky)		
0x03C	SYNC_CURRERR_L	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CURRERROR		LMFC Sync Alignment Error. 4-bit twos complement value that represents the phase error in number of DAC clock cycles (ie, number of DAC clocks between LMFC edge and SYSREF edge). When an adjustment of the clocks is made on any given SYSREF, the value of the phase error is placed into SYNC_ LASTERR, and SYNC_CURRERR is forced to 0.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x03D	SYNC_CURRERR_H	7	CURRUNDER		LMFC Sync Current Error Under Flag.	0x0	R
				1	Current phase error is beyond lower window tolerance boundary		
		6	CURROVER		LMFC Sync Current Error Over Flag.	0x0	R
				1	Current phase error is beyond upper window tolerance boundary		
		[5:0]	RESERVED		Reserved.	0x0	R
0x040	DACGAIN0_1	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DACFSC_0[9:8]		2 MSBs of I-Channel DAC Gain Dual A. A 10-bit twos complement value that is mapped to analog full-scale current for DAC 0 as shown: 01111111111 = 27.0 mA 0000000000 = 20.48 mA 1000000000 = 13.9 mA	0x0	R/W
0x041	DACGAIN0_0	[7:0]	DACFSC_0[7:0]		8 LSBs of I-Channel DAC Gain Dual A.	0x0	R/W
0x042	DACGAIN1_1	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DACFSC_1[9:8]		2 MSBs of Q-Channel DAC Gain Dual A. A 10-bit twos complement value that is mapped to analog full-scale current for DAC 1 as shown in Register 0x040. 01111111111 = 27.0 mA 0000000000 = 20.48 mA 1000000000 = 13.9 mA	0x0	R/W
0x043	DACGAIN1_0	[7:0]	DACFSC_1[7:0]		8 LSBs of Q-Channel DAC Gain Dual A.	0x0	R/W
0x044	DACGAIN2_1	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DACFSC_2[9:8]		2 MSBs of I-Channel DAC Gain Dual B. A 10-bit twos complement value that is mapped to analog full-scale current for DAC as shown in Register 0x040. 01111111111 = 27.0 mA 0000000000 = 20.48 mA 1000000000 = 13.9 mA	0x0	R/W
0x045	DACGAIN2_0	[7:0]	DACFSC_2[7:0]		8 LSBs of I-Channel DAC Gain Dual B.	0x0	R/W
0x046	DACGAIN3_1	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DACFSC_3[9:8]		2 MSBs of Q-Channel DAC Gain Dual B. A 10-bit twos complement value that is mapped to analog full-scale current for DAC 3 as shown in Register 0x40. 01111111111 = 27.0 mA 0000000000 = 20.48 mA 1000000000 = 13.9 mA	0x0	R/W
0x047	DACGAIN3_0	[7:0]	DACFSC_3[7:0]		8 LSBs of Q-Channel DAC Gain Dual B.	0x0	R/W
0x050	NCOALIGN_MODE	7	NCO_ALIGN_ARM		Arm NCO Align. On a rising edge, arms the NCO align operation.	0x0	R/W
		6	RESERVED		Reserved.	0x0	R
		5	NCO_ALIGN_MTCH		NCO Align Data Match.	0x0	R
				1	Key NCO align data match		
				0	If finished, NCO not aligned on data match		
		4	NCO_ALIGN_PASS		NCO Align Pass.	0x0	R
				1	NCO align takes effect		
				0	Clear not taken effect yet		
		3	NCO_ALIGN_FAIL		NCO Align Fail.	0x0	R
				1	NCO reset during rotate		
				0	Not finished yet		
		2	RESERVED		Reserved.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		[1:0]	NCO_ALIGN_ MODE		NCO Align Mode.	0x0	R/W
				00	NCO align disabled		
				10	NCO align on data key		
				01	NCO align on SYSREF		
0x051	NCOKEY_ILSB	[7:0]	NCOKEYI[7:0]		NCO Data Key for I Channel.	0x0	R/W
0x052	NCOKEY_IMSB	[7:0]	NCOKEYI[15:8]		NCO Data Key for I Channel.	0x0	R/W
0x053	NCOKEY_QLSB	[7:0]	NCOKEYQ[7:0]		NCO Data Key for Q Channel.	0x0	R/W
0x054	NCOKEY_QMSB	[7:0]	NCOKEYQ[15:8]		NCO Data Key for Q Channel.	0x0	R/W
0x060	PDP_THRES0	[7:0]	PDP_THRES-HOLD[7:0]		PDP_THRESHOLD is the average power threshold for comparison. If the moving average of signal power crosses this threshold, PDP_PROTECT is set high.	0x0	R/W
0x061	PDP_THRES1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	PDP_ THRESHOLD[12:8]		See Register 0x60.	0x0	R/W
0x062	PDP_AVG_TIME	7	PDP_ENABLE	1	Enable average power calculation.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	PDP_AVG_TIME		Can be set from 0-10. Averages across 2^(9+PDP_AVG_TIME) IQ sample pairs.	0x0	R/W
0x063	PDP_POWER0	[7:0]	PDP_POWER[7:0]		If PDP_POWER has not gone over PDP_THRESHOLD, PDP_POWER reads back the moving average of the signal power ($I^2 + Q^2$). If PDP_THRESHOLD is crossed, PDP_POWER will hold the max value until it's corresponding IRQ is cleared (0x025[7 or 0x026[7]). Only 7 data MSBs are used in calculating power.	0x0	R
0x064	PDP_POWER1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	PDP_POWER[12:8]		See Register 0x063.	0x0	R
0x080	CLKCFG0	7	PD_CLK01		Power-Down Clock for Dual A. This bit disables the digital and analog clocks for Dual A.	0x1	R/W
		6	PD_CLK23		Power-Down Clock for Dual B. This bit disables the digital and analog clocks for Dual B.	0x1	R/W
		5	PD_CLK_DIG		Power-Down Clocks to all DACs. This bit disables the digital and analog clocks for both duals. This includes all reference clocks, PCLK, DAC clocks, and digital clocks.	0x1	R/W
		4	PD_SERDES_PCLK		Serdes PLL Clock Power-Down. This bit disables the reference clock to the SERDES PLL, which is needed to have an operational serial interface.	0x1	R/W
		3	PD_CLK_REC		Clock Receiver Power-Down. This bit powers down the analog DAC clock receiver block. With this bit set, clocks are not passed to internal nets.	0x1	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x081	SYSREF_ACTRL0	[7:5]	RESERVED		Reserved.	0x0	R
		4	PD_SYSREF		Power-Down SYSREF Buffer. This bit powers down the SYSREF receiver. For Subclass 1 operation to work, this buffer must be enabled.	0x1	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		3	HYS_ON		Hysteresis Enabled. This bit enables the programmable hysteresis control for the SYSREF receiver. Using hysteresis gives some noise resistance, but delays the SYSREF± edge an amount depending on HYS_CNTRL and the SYSREF± edge rate. The SYSREF± KOW is not guaranteed when using hysteresis.	0x0	R/W
		2	SYSREF_RISE		Select DAC Clock Edge to Sample SYSREF.	0x0	R/W
				0	Use falling edge of DAC clock to sample SYSREF for alignment		
				1	Use rising edge of DAC clock to sample SYSREF for alignment		
		[1:0]	HYS_CNTRL1		Hysteresis Control Bits[9:8]. HYS_CNTRL is a 10-bit thermometer-coded number. Each bit set adds 10 mV of differential hysteresis to the SYSREF receiver.	0x0	R/W
0x082	SYSREF_ACTRL1	[7:0]	HYS_CNTRL0		Hysteresis Control Bits[7:0].	0x0	R/W
0x083	DACPLLCNTRL	7	RECAL_DACPLL		Recalibrate DAC PLL. On a rising edge of this bit, recalibrate the DAC PLL.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R
		4	ENABLE_DACPLL		Synthesizer Enable. This bit enables and calibrates the DAC PLL.	0x0	R/W
		[3:0]	RESERVED		Reserved.	0x0	R
0x084	DACPLLSTATUS	7	DACPLL_ OVERRANGE_H		DAC PLL High Overrange. This bit indicates that the DAC PLL hit the upper edge of its operating band. Recalibrate.	0x0	R
		6	DACPLL_ OVERRANGE_L		DAC PLL Low Overrange. This bit indicates that the DAC PLL hit the lower edge of its operating band. Recalibrate.	0x0	R
		5	DACPLL_CAL_ VALID		DAC PLL Calibration Valid. This bit indicates that the DAC PLL has been successfully calibrated.	0x0	R
		[4:2]	RESERVED		Reserved.	0x0	R
		1	DACPLL_LOCK		DAC PLL Lock Bit. This bit is set high by the PLL when it has achieved lock.	0x0	R
		0	RESERVED		Reserved.	0x0	R
0x085	DACINTEGERWORD0	[7:0]	B_COUNT		Integer Division Word. This bit controls the integer feedback divider for the DAC PLL. Determine the frequency of the DAC clock by the following equations (see the Clock Multiplication section for more details): $f_{DAC} = f_{REF}/(REF\_DIVRATE) \times 2 \times B\_COUNT$ $f_{VCO} = f_{REF}/(REF\_DIVRATE) \times 2 \times B\_COUNT \times LO\_DIV\_MODE$ Minimum value is 6.	0x8	R/W
0x087	DACLOOPFILT1	[7:4]	LF_C2_WORD		C2 Control Word. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with C2.	0x8	R/W
		[3:0]	LF_C1_WORD		C1 Control Word. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with C1.	0x8	R/W
0x088	DACLOOPFILT2	[7:4]	LF_R1_WORD		R1 Control Word. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with R1.	0x8	R/W
		[3:0]	LF_C3_WORD		C3 Control Word. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with C3.	0x8	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x089	DACLOOPFILT3	7	LF_BYPASS_R3		Bypass R3 Resistor. When this bit is set, bypass the R3 capacitor (set to 0 pF) when R3_WORD is set to 0.	0x0	R/W
		6	LF_BYPASS_R1		Bypass R1 Resistor. When this bit is set, bypass the R1 capacitor (set to 0 pF) when R1_WORD is set to 0.	0x0	R/W
		5	LF_BYPASS_C2		Bypass C2 Capacitor. When this bit is set, bypass the C2 capacitor (set to 0 pF) when C2_WORD is set to 0.	0x0	R/W
		4	LF_BYPASS_C1		Bypass C1 Capacitor. When this bit is set, bypass the C1 capacitor (set to 0 pF) when C1_WORD is set to 0.	0x0	R/W
		[3:0]	LF_R3_WORD		R3 Control Word. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with R3.	0x8	R/W
0x08A	DACCPCNTRL	[7:6]	RESERVED		Reserved.	0x0	R
		[5:0]	CP_CURRENT		Charge Pump Current Control. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for the values associated with charge pump current.	0x20	R/W
0x08B	DACLOGENCNTRL	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	LO_DIV_MODE		This range controls the RF clock divider between the VCO and DAC clock rates. The options are 4×, 8×, or 16× division. Choose the LO_DIV_MODE so that 6 GHz < f_{VCO} < 12 GHz (see the Clock Multiplication section for more details):	0x2	R/W
				01	DAC clock = VCO/4		
				10	DAC clock = VCO/8		
				11	DAC clock = VCO/16		
0x08C	DACLDOCNTRL1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	REF_DIV_MODE		Reference Clock Division Ratio. This field controls the amount of division that is done to the input clock at the CLK+/CLK− pins before it is presented to the PLL as a reference clock. The reference clock frequency must be between 35 MHz and 80 MHz, but the CLK+/CLK− input frequency can range from 35 MHz to 1 GHz. The user sets this division to achieve a 35 MHz to 80 MHz PLL reference frequency. For more details see the Clock Multiplication section.	0x1	R/W
				000	1		
				001	2		
				010	4		
				011	8		
				100	16		
0x0E2	CAL_CTRL_GLOBAL	[7:2]	RESERVED		Reserved.	0x0	R
		1	CAL_START_AVG		Averaged Calibration Start. On rising edge, calibrate the DACs. Only use if calibrating all DACs.	0x0	R/W
		0	CAL_EN_AVG		Averaged Calibration Enable. Set prior to starting calibration with CAL_START_AVG. While this bit is set, calibration can be performed, and the results are applied.	0x0	R/W
				1	Enable averaged calibration		
0x0E7	CAL_CLKDIV	[7:4]	RESERVED		Must write the default value for proper operation.	0x3	R/W
		3	CAL_CLK_EN		Enable Self Calibration Clock.	0x0	R/W
				1	Enable calibration clock		
				0	Disable calibration clock		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		[2:0]	RESERVED		Reserved.	0x0	R
0x0E8	CAL_PAGE	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CAL_PAGE		DAC Calibration Paging. Selects which of the DACs are being accessed for calibration or calibration readback. This paging affects Register 0x0E9 and Register 0x0ED. Calibration: any number of DACs can be accessed simultaneously to write and calibrate. Write a 1 to Bit x to include DAC x. Readback: only one DAC at a time can be accessed when reading back CAL_CTRL (Register 0x0E9). Write a 1 to Bit x to read from DAC x (the other bits must be 0).	0xF	R/W
0x0E9	CAL_CTRL	7	CAL_FIN		Calibration finished. This bit is high when the calibration has completed. If the calibration completes and either CAL_ERRHI or CAL_ERRLO is high, then the calibration cannot be considered valid and are considered a timeout event.	0x0	R
				1	Calibration ran and is finished		
		6	CAL_ACTIVE		Calibration Active. This bit is high while the calibration is in progress.	0x0	R
				1	Calibration is running		
		5	CAL_ERRHI		SAR Data Error: Too High. This bit is set at the end of a calibration cycle if any of the calibration DACs has overranged to the high side. This typically means that the algorithm adjusts the calibration preset of the calibration DACs and runs another cycle.	0x0	R
				1	Data saturated high		
		4	CAL_ERRLO		SAR Data Error: Too Low. This bit is set at the end of a calibration cycle if any of the calibration DACs has overranged to the low side. This typically means that the algorithm adjusts the calibration preset of the calibration DACs and runs another cycle.	0x0	R
				1	Data saturated low		
		[3:2]	RESERVED		Reserved.	0x0	R
		1	CAL_START		Calibration Start. The rising edge of this bit kicks off a calibration sequence for the DACs that have been selected in the CAL_INDX register.	0x0	R/W
				0	Normal operation		
				1	Start calibration state machine		
		0	CAL_EN		Calibration Enable. Enable the calibration DAC of the converter. Enable to calibration engine and machines. Prepare for a calibration start. For calibration coefficients to be applied to the calibrated DACs, this bit must be high.	0x0	R/Wr
				0	Do not use calibration DACs		
				1	Use calibration DACs		
0x0ED	CAL_INIT	[7:0]	CAL_INIT		Initialize Calibration. Must be written to 0xA2 before starting calibration or averaged calibration.	0xA6	R/W
0x110	DATA_FORMAT	7	BINARY_FORMAT		Binary or Twos Complementary Format on the Data Bus.	0x0	R/W
				0	Input data is twos complement		
				1	Input data is offset binary		
		[6:0]	RESERVED		Reserved.	0x0	R
0x111	DATAPATH_CTRL	7	INVSINC_ENABLE		Enable Inverse Sinc Filter.	0x1	R/W
				1	Enable inverse sinc filter		
				0	Disable inverse sinc filter		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		6	RESERVED		Reserved.	0x0	R
		5	DIG_GAIN_ENABLE		Enable Digital Gain.	0x1	R/W
				1	Enable digital gain function		
				0	Disable digital gain function		
		4	PHASE_ADJ_ ENABLE		Enable Phase Compensation.	0x0	R/W
				1	Enable phase adjust compensation		
				0	Disable phase adjust compensation		
		[3:2]	MODULATION_TYPE		Selects Type Of Modulation Operation.	0x0	R/W
				00	No modulation		
				01	Fine modulation (uses FTW)		
				10	f_S/4 coarse modulation		
				11	f_S/8 coarse modulation		
		1	SEL_SIDEBAND		Spectrum Inversion Control. Can only be used with fine modulation. This causes the negative sideband to be selected and is equivalent to changing the sign of FTW.	0x0	R/W
		0	I_TO_Q		Send I Data into Q DAC. Swap I and Q data at the end of the digital datapath prior to entering DACs.	0x0	R/W
0x112	INTERP_MODE	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	INTERP_MODE		Interpolation Mode.	0x1	R/W
				000	1× mode		
				001	2× mode		
				011	4× mode		
				100	8× mode		
0x113	NCO_FTW_UPDATE	[7:2]	RESERVED		Reserved.	0x0	R
		1	FTW_UPDATE_ACK		Frequency tuning word update acknowledge. This readback is high when an FTW has been updated.	0x0	R
		0	FTW_UPDATE_REQ		Frequency tuning word update request from SPI. Unlike most registers, those relating to fine NCO modulation (Register 0x114 to Register 0x11B) are not updated immediately upon writing to them. Once the desired FTW and phase offset values are written, set this bit. These registers update on the rising edge of this bit. It is only after this update that the internal state matches Register 0x114 to Register 0x11B. Confirmation that this update has occurred can be made by reading back bit 1 of this register and ensuring it is set high for the update acknowledge.	0x0	R/W
0x114	FTW0	[7:0]	FTW[7:0]		NCO Frequency Tuning Word.	0x0	R/W
0x115	FTW1	[7:0]	FTW[15:8]		NCO Frequency Tuning Word.	0x0	R/W
0x116	FTW2	[7:0]	FTW[23:16]		NCO Frequency Tuning Word.	0x0	R/W
0x117	FTW3	[7:0]	FTW[31:24]		NCO Frequency Tuning Word.	0x0	R/W
0x118	FTW4	[7:0]	FTW[39:32]		NCO Frequency Tuning Word.	0x0	R/W
0x119	FTW5	[7:0]	FTW[47:40]		NCO Frequency Tuning Word.	0x10	R/W
0x11A	NCO_PHASE_ OFFSET0	[7:0]	NCO_PHASE_ OFFSET[7:0]		8 LSBs of NCO Phase Offset. NCO_PHASE_OFFSET changes the phase of both I and Q data, and is only functional when using NCO fine modulation. It is a 16-bit twos complement number ranging from −180 to+180 degrees in steps of .0055°.	0x0	R/W
0x11B	NCO_PHASE_ OFFSET1	[7:0]	NCO_PHASE_ OFFSET[15:8]		8 MSBs of NCO Phase Offset.	0x0	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x11C	PHASE_ADJ0	[7:0]	PHASE_ADJ[7:0]		8 LSBs of Phase Compensation Word. Phase compensation changes the phase between the I and Q data. PHASE_ADJ is a 13-bit twos complement value. The control ranges from −14° to +14° with 0.0035° resolution steps.	0x0	R/W
0x11D	PHASE_ADJ1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	PHASE_ADJ[12:8]		5 MSBs of Phase Compensation Word.	0x0	R/W
0x11F	TXEN_SM_0	[7:6]	FALL_COUNTERS		Fall Counters. The number of counters to use to delay TX_PROTECT fall from TXENx falling edge. Must be set to 1 or 2.	0x2	R/W
		[5:4]	RISE_COUNTERS		Rise Counters. The number of counters to use to delay TX_PROTECT rise from TXENx rising edge.	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		2	PROTECT_OUT_ INVERT		PROTECT_OUTx Invert.	0x0	R/W
				0	PROTECT_OUTx is high when output is valid. Suitable for enabling downstream components during transmission		
				1	PROTECT_OUTx is high when output is invalid. Suitable for disabling downstream components when not transmitting		
		[1:0]	RESERVED		Must write the default value for proper operation.	0x3	R/W
0x121	TXEN_RISE_COUNT_ 0	[7:0]	RISE_COUNT_0		First counter used to delay TX_PROTECT rise from TXENx rising edge. Delays by 32 × RISE_COUNT_0 DAC clock cycles.	0xF	R/W
0x122	TXEN_RISE_COUNT_ 1	[7:0]	RISE_COUNT_1		Second counter used to delay TX_PROTECT rise from TXENx rising edge. Delays by 32 × RISE_COUNT_1 DAC clock cycles.	0x0	R/W
0x123	TXEN_FALL_ COUNT_0	[7:0]	FALL_COUNT_0		First counter used to delay TX_PROTECT fall from TXENx falling edge. Delays by 32 × FALL_COUNT_0 DAC clock cycles. Must be set to a minimum of 0x12.	0xFF	R/W
0x124	TXEN_FALL_ COUNT_1	[7:0]	FALL_COUNT_1		Second counter used to delay TX_PROTECT fall from TXENx falling edge. Delays by 32 × FALL_COUNT_1 DAC clock cycles.	0xFF	R/W
0x12D	DEVICE_CONFIG_ REG_0	[7:0]	DEVICE_CONFIG_0		Must be set to 0x8B for proper digital datapath configuration.	0x46	R/W
0x12F	DIE_TEMP_CTRL0	[7:1]	RESERVED		Must write the default value for proper operation.	0x10	R/W
		0	AUXADC_ENABLE		Enables the AUX ADC Block.	0x0	R/W
				0	AUX ADC disable		
				1	AUX ADC enable		
0x132	DIE_TEMP0	[7:0]	DIE_TEMP[7:0]		Aux ADC Readback Value.	0x0	R
0x133	DIE_TEMP1	[7:0]	DIE_TEMP[15:8]		Aux ADC Readback Value.	0x0	R
0x134	DIE_TEMP_UPDATE	[7:1]	RESERVED		Reserved.	0x0	R
		0	DIE_TEMP_ UPDATE		Die Temperature Update. On a rising edge, a new temperature code is generated.	0x0	R/W
0x135	DC_OFFSET_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	DC_OFFSET_ON		DC Offset On.	0x0	R/W
				1	Enables dc offset module		
0x136	IPATH_DC_OFFSET_ 1PART0	[7:0]	LSB_OFFSET_I[7:0]		8 LSBs of IPath DC Offset. LSB_OFFSET_I is a 16-bit twos complement number that is added to incoming data.	0x0	R/W
0x137	IPATH_DC_OFFSET_ 1PART1	[7:0]	LSB_OFFSET_I[15:8]		8 MSBs of IPath DC Offset. LSB_OFFSET_I is a 16-bit twos complement number that is added to incoming I data.	0x0	R/W
0x138	QPATH_DC_OFFSET_ 1PART0	[7:0]	LSB_OFFSET_ Q[7:0]		8 LSBs of QPath DC Offset. LSB_OFFSET_Q is a 16-bit twos complement number that is added to incoming Q data.	0x0	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x139	QPATH_DC_OFFSET_1PART1	[7:0]	LSB_OFFSET_Q[15:8]		8 MSBs of QPath DC Offset. LSB_OFFSET_Q is a 16-bit twos complement number that is added to incoming Q data.	0x0	R/W
0x13A	IPATH_DC_OFFSET_2PART	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	SIXTEENTH_OFFSET_I		SIXTEENTH_OFFSET_I is a 5-bit twos complement number in 16ths of an LSB that is added to incoming I data.	0x0	R/W
				x	x/16 LSB DC offset		
0x13B	QPATH_DC_OFFSET_2PART	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	SIXTEENTH_OFFSET_Q		SIXTEENTH_OFFSET_Q is a 5-bit twos complement number in 16ths of an LSB that is added to incoming Q data.	0x0	R/W
				x	x/16 LSB DC offset		
0x13C	IDAC_DIG_GAIN0	[7:0]	IDAC_DIG_GAIN[7:0]		8 LSBs of I DAC Digital Gain. IDAC_DIG_GAIN is the digital gain of the IDAC. The digital gain is a multiplier from 0 to 4095/2048 in steps of 1/2048.	0xEA	R/W
0x13D	IDAC_DIG_GAIN1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	IDAC_DIG_GAIN[11:8]		4 MSBs of I DAC Digital Gain	0xA	R/W
0x13E	QDAC_DIG_GAIN0	[7:0]	QDAC_DIG_GAIN[7:0]		8 LSBs of Q DAC Digital Gain. QDAC_DIG_GAIN is the digital gain of the QDAC. The digital gain is a multiplier from 0 to 4095/2048 in steps of 1/2048.	0xEA	R/W
0x13F	QDAC_DIG_GAIN1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	QDAC_DIG_GAIN[11:8]		4 MSBs of Q DAC Digital Gain.	0xA	R/W
0x140	GAIN_RAMP_UP_STEP0	[7:0]	GAIN_RAMP_UP_STEP[7:0]		8 LSBs of Gain Ramp Up Step. GAIN_RAMP_UP_STEP controls the amplitude step size of the BSM's ramping feature when the gain is being ramped to its assigned value.	0x4	R/W
				0x0	Smallest ramp up step size		
				0xFFF	Largest ramp up step size		
0x141	GAIN_RAMP_UP_STEP1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GAIN_RAMP_UP_STEP[11:8]		4 MSBs of Gain Ramp Up Step. See Register 0x140 for description.	0x0	R/W
0x142	GAIN_RAMP_DOWN_STEP0	[7:0]	GAIN_RAMP_DOWN_STEP[7:0]		8 LSBs of Gain Ramp Down Step. GAIN_RAMP_DOWN_STEP controls the amplitude step size of the BSM's ramping feature when the gain is being ramped to zero.	0x9	R/W
				0	Smallest ramp down step size		
				0xFFF	Largest ramp down step size		
0x143	GAIN_RAMP_DOWN_STEP1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GAIN_RAMP_DOWN_STEP[11:8]		4 MSBs of Gain Ramp Down Step. See Register 0x142 for description.	0x0	R/W
0x146	DEVICE_CONFIG_REG_1	[7:0]	DEVICE_CONFIG_1		Must be set to 0x01 for proper digital datapath configuration.	0x0	R/W
0x147	BSM_STAT	[7:6]	SOFTBLANKRB		Blanking State.	0x0	R
				00	Data is fully blanked		
				01	Ramping from data process to full blanking		
				10	Ramping from fully blanked to data process		
				11	Data is being processed		
		[5:0]	RESERVED		Reserved.	0x0	R
0x14B	PRBS	7	PRBS_GOOD_Q		Good Data Indicator Imaginary Channel.	0x0	R
				0	Incorrect sequence detected		
				1	Correct PRBS sequence detected		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		6	PRBS_GOOD_I		Good Data Indicator Real Channel.	0x0	R
				0	Incorrect sequence detected		
				1	Correct PRBS sequence detected		
		[5:3]	RESERVED		Reserved.	0x0	R
		2	PRBS_MODE		Polynomial Select	0x0	R/W
				0	7-bit: $x^7 + x^6 + 1$		
				1	15-bit: $x^{15} + x^{14} + 1$		
		1	PRBS_RESET		Reset Error Counters.	0x0	R/W
				0	Normal operation		
				1	Reset counters		
		0	PRBS_EN		Enable PRBS Checker.	0x0	R/W
				0	Disable		
				1	Enable		
0x14C	PRBS_ERROR_I	[7:0]	PRBS_COUNT_I		Error Count Value Real Channel.	0x0	R
0x14D	PRBS_ERROR_Q	[7:0]	PRBS_COUNT_Q		Error Count Value Imaginary Channel.	0x0	R
0x1B4	DACPLLT4	7	RESERVED		Reserved.	0x0	R
		[6:3]	VCO_CAL_OFFSET		Starting Offset for VCO Calibration. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with VCO calibration offset.	0xF	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x1B5	DACPLLT5	[7:4]	RESERVED		Must write the default value for proper operation.	0x8	R/W
		[3:0]	VCO_VAR		Varactor KVO Setting. See the Lookup Tables for Three Different DAC PLL Reference Frequenciessection associated with VCO varactor reference.	0x3	R/W
0x1B6	DACPLLT6	[7:4]	RESERVED		Must write the default value for proper operation.	0x4	R/W
		[3:0]	VCO_LVL_OUT		VCO Amplitude Control. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with the VCO output level.	0xA	R/W
0x1BB	DACPLLTB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:3]	VCO_BIAS_TCF		Temperature Coefficient for VCO Bias. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section for values associated with VCO bias temperature coefficient.	0x1	R/W
		[2:0]	VCO_BIAS_REF		VCO Bias Control. See the Lookup Tables for Three Different DAC PLL Reference Frequencies section values associated with VCO bias reference.	0x4	R/W
0x1BD	DACPLLTD	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	VCO_CAL_REF_TCF		Temperature Coefficient for Calibration Reference. This field sets the temperature coefficient of the current used to set the VCO band calibration reference voltage.	0x0	R/W
0x1C4	DEVICE_CONFIG_REG_2	[7:0]	DEVICE_CONFIG_2		Must be set to 0x73 for proper DAC PLL configuration.	0x33	R/W
0x200	MASTER_PD	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_PD_MASTER		Power Down the Entire JESD Receiver Analog (All Eight Channels Plus Bias).	0x1	R/W
0x201	PHY_PD	[7:0]	SPI_PD_PHY		SPI Override to Power Down the Individual PHYs. Set Bit x to power down the corresponding SERDINx± PHY	0x0	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x203	GENERIC_PD	[7:2]	RESERVED		Reserved.	0x0	R
		1	SPI_SYNC1_PD		Power down LVDS buffer for $\overline{\text{SYNCOUT0}}$±.	0x0	R/W
		0	SPI_SYNC2_PD		Power down LVDS buffer for $\overline{\text{SYNCOUT1}}$±.	0x0	R/W
0x206	CDR_RESET	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_CDR_RESETN		Resets the Digital Control Logic for All PHYs.	0x1	R/W
				0	Hold CDR in reset		
				1	Enable CDR		
0x230	CDR_OPERATING_ MODE_REG_0	[7:6]	RESERVED		Reserved.	0x0	R
		5	ENHALFRATE		Enables Half-Rate CDR Operation. Set to 1 when 5.65 Gbps ≤ lane rate ≤ 10.64.	0x1	R/W
		[4:2]	RESERVED		Must write the default value for proper operation.	0x2	R/W
		1	CDR_OVERSAMP		Enables Oversampling of the Input Data. Set to 1 when 1.42 Gbps ≤ lane rate ≤ 2.76 Gbps.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R
0x232	DEVICE_CONFIG_ REG_3	[7:0]	DEVICE_CONFIG_3		Must be set to 0xFF for proper JESD interface configuration.	0x0	R/W
0x268	EQ_BIAS_REG	[7:6]	EQ_POWER_ MODE		Control the Equalizer Power/Insertion Loss Capability.	0x1	R/W
				00	Normal mode		
				01	Low power mode		
		[5:0]	RESERVED		Must write the default value for proper operation.	0x22	R/W
0x280	SERDESPLL_ ENABLE_CNTRL	[7:3]	RESERVED		Reserved.	0x0	R
		2	RECAL_SERDESPLL		Recalibrate SERDES PLL. On a rising edge, recalibrate the SERDES PLL.	0x0	R/W
		1	RESERVED		Reserved.	0x0	R
		0	ENABLE_ SERDESPLL		Enable the SERDES PLL. Setting this bit enables and calibrates the SERDES PLL.	0x0	R/W
0x281	PLL_STATUS	[7:6]	RESERVED		Reserved.	0x0	R
		5	SERDES_PLL_ OVERRANGE_H		SERDES PLL High Overrange. This bit indicates that the DAC PLL hit the lower edge of its operating band. Recalibrate.	0x0	R
		4	SERDES_PLL_ OVERRANGE_L		SERDES PLL Low Overrange. This bit indicates that the DAC PLL hit the lower edge of its operating band. Recalibrate.	0x0	R
		3	SERDES_PLL_CAL_ VALID_RB		SERDES PLL Calibration Valid. This bit indicates that the SERDES PLL has been successfully calibrated.	0x0	R
		[2:1]	RESERVED		Reserved.	0x0	R
		0	SERDES_PLL_ LOCK_RB		SERDES PLL Lock. This bit is set high by the PLL when it has achieved lock.	0x0	R
0x289	REF_CLK_DIVIDER_ LDO	[7:3]	RESERVED		Reserved.	0x0	R
		2	DEVICE_CONFIG_4		Must be set to 1 for proper SERDES PLL configuration.	0x0	R/W
		[1:0]	SERDES_PLL_DIV_ MODE		SERDES PLL Reference Clock Division Factor. This field controls the division of the SERDES PLL reference clock before it is fed into the SERDES PLL Phase Frequency Detector (PFD). It must be set so f_{REF}/DivFactor is between 35 and 80MHz.	0x0	R/W
				00	Divide by 4 for 5.65 Gbps to 10.64 Gbps lane rate		
				01	Divide by 2 for 2.83 Gbps to 5.52 Gbpslane rate		
				10	Divide by 1 for 1.42 Gbps to 2.76 Gbps lane rate		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x291	DEVICE_CONFIG_REG_5	[7:0]	DEVICE_CONFIG_5		Must be set to 0x49 for proper SERDES PLL configuration.	0x46	R/W
0x29C	DEVICE_CONFIG_REG_6	[7:0]	DEVICE_CONFIG_6		Must be set to 0x24 for proper SERDES PLL configuration.	0x17	R/W
0x29F	DEVICE_CONFIG_REG_7	[7:0]	DEVICE_CONFIG_7		Must be set to 0x73 for proper SERDES PLL configuration.	0x33	R/W
0x2A4	DEVICE_CONFIG_REG_8	[7:0]	DEVICE_CONFIG_8		Must be set to 0xFF for proper clock configuration.	0x4B	R/W
0x2A5	SYNCOUTB_SWING	[7:1]	RESERVED		Reserved.	0x0	R
		0	SYNCOUTB_SWING_MD		$\overline{\text{SYNCOUTx±}}$ Swing Mode. Sets the output differential swing mode for the $\overline{\text{SYNCOUTx±}}$ pins. See Table 8 for details.	0x0	R/W
				0	Normal Swing Mode		
				1	High Swing Mode		
0x2A7	TERM_BLK1_CTRLREG0	[7:1]	RESERVED		Reserved.	0x0	R
		0	RCAL_TERMBLK1		Termination Calibration. The rising edge of this bit calibrates PHY0, PHY1, PHY6, and PHY7 terminations to 50 Ω.	0x0	R/W
0x2AA	DEVICE_CONFIG_REG_9	[7:0]	DEVICE_CONFIG_9		Must be set to 0xB7 for proper JESD interface termination configuration.	0xC3	R/W
0x2AB	DEVICE_CONFIG_REG_10	[7:0]	DEVICE_CONFIG_10		Must be set to 0x87 for proper JESD interface termination configuration.	0x93	R/W
0x2AE	TERM_BLK2_CTRLREG0	[7:1]	RESERVED		Reserved.	0x0	R
		0	RCAL_TERMBLK2		Terminal Calibration. The rising edge of this bit calibrates PHY2, PHY3, PHY4 and PHY5 terminations to 50 Ω.	0x0	R/W
0x2B1	DEVICE_CONFIG_REG_11	[7:0]	DEVICE_CONFIG_11		Must be set to 0xB7 for proper JESD interface termination configuration.	0xC3	R/W
0x2B2	DEVICE_CONFIG_REG_12	[7:0]	DEVICE_CONFIG_12		Must be set to 0x87 for proper JESD interface termination configuration.	0x93	R/W
0x300	GENERAL_JRX_CTRL_0	7	RESERVED		Reserved.	0x0	R
		6	CHECKSUM_MODE		Checksum Mode. This bit controls the locally generated JESD204B link parameter checksum method. The value is stored in the FCMP registers (Register 0x40E, Register 0x416, Register 0x41E, Register 0x426, Register 0x42E, Register 0x436, Register 0x43E, and Register 0x446).	0x0	R/W
				0	Checksum is calculated by summing the individual fields in the link configuration table as defined in Section 8.3, Table 20 of the JESD204B standard		
				1	Checksum is calculated by summing the registers containing the packed link configuration fields (Σ[0x450:0x45C] modulo 256).		
		[5:4]	RESERVED		Reserved.	0x0	R
		3	LINK_MODE		Link Mode. This register selects either single link or dual link mode.	0x0	R/W
				0	Single link mode		
				1	Dual link mode		
		2	LINK_PAGE		Link Paging. Selects which link's register map is used. This paging affects Registers 0x401 to 0x47E.	0x0	R/W
				0	Use Link 0 register map		
				1	Use Link 1 register map		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		[1:0]	LINK_EN		Link Enable. These bits bring up the JESD204B receiver digital circuitry: Bit 0 for Link 0 and Bit 1 for Link 1. Enable the link only after the following has occurred: all JESD204B parameters are set, the DAC PLL is enabled and locked (Register 0x084[1] = 1), and the JESD204B PHY is enabled (Register 0x200 = 0x00) and calibrated (Register 0x281[2] = 0).	0x0	R/W
				0b00	Disable both JESD Link 1 and JESD Link 0		
				0b01	Disable JESD Link 1, enable JESD Link 0		
				0b10	Enable JESD Link 1, disable JESD Link 0		
				0b11	Enable both JESD Link 1 and JESD Link 0		
0x301	GENERAL_JRX_CTRL_1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	SUBCLASSV_LOCAL		JESD204B Subclass.	0x1	R/W
				000	Subclass 0		
				001	Subclass 1		
0x302	DYN_LINK_LATENCY_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	DYN_LINK_LATENCY_0		Dynamic Link Latency: Link 0. Latency between the $LMFC_{Rx}$ for link 0 and the last arriving LMFC boundary in units of PCLK cycles. See the Deterministic Latency section.	0x0	R
0x303	DYN_LINK_LATENCY_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	DYN_LINK_LATENCY_1		Dynamic Link Latency: Link 1. Latency between the $LMFC_{Rx}$ for link 1 and the last arriving LMFC boundary in units of PCLK cycles. See the Deterministic Latency section.	0x0	R
0x304	LMFC_DELAY_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_DELAY_0		LMFC Delay: Link 0 Delay from the LMFC to $LMFC_{Rx}$ for Link 0. In units of frame clock cycles for subclass 1 and PCLK cycles for subclass 0. See the Deterministic Latency section.	0x0	R/W
0x305	LMFC_DELAY_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_DELAY_1		LMFC Delay: Link 1. Delay from the LMFC to $LMFC_{Rx}$ for Link 1. In units of frame clock cycles for subclass 1 and PCLK cycles for subclass 0. See the Deterministic Latency section.	0x0	R/W
0x306	LMFC_VAR_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_VAR_0		Variable Delay Buffer: Link 0. Sets when data is read from a buffer to be consistent across links and power cycles. In units of PCLK cycles. See the Deterministic Latency section. This setting must not be more than 10.	0x6	R/W
0x307	LMFC_VAR_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_VAR_1		Variable Delay Buffer: Link 1. Sets when data is read from a buffer to be consistent across links and power cycles. In units of PCLK cycles. See the Deterministic Latency section. This setting must not be more than 10.	0x6	R/W
0x308	XBAR_LN_0_1	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE1_SRC		Logical Lane 1 Source. Selects a physical lane to be mapped onto Logical Lane 1.	0x1	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE0_SRC		Logical Lane 0 Source. Selects a physical lane to be mapped onto Logical Lane 0.	0x0	R/W
				x	Data is from SERDINx		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x309	XBAR_LN_2_3	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE3_SRC		Logical Lane 3 Source. Selects a physical lane to be mapped onto Logical Lane 3.	0x3	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE2_SRC		Logical Lane 2 source. Selects a physical lane to be mapped onto Logical Lane 2.	0x2	R/W
				x	Data is from SERDINx		
0x30A	XBAR_LN_4_5	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE5_SRC		Logical Lane 5 Source. Selects a physical lane to be mapped onto Logical Lane 5.	0x5	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE4_SRC		Logical Lane 4 Source. Selects a physical lane to be mapped onto Logical Lane 4.	0x4	R/W
				x	Data is from SERDINx		
0x30B	XBAR_LN_6_7	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE7_SRC		Logical Lane 7 Source. Selects a physical lane to be mapped onto Logical Lane 7.	0x7	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE6_SRC		Logical Lane 6 Source. Selects a physical lane to be mapped onto Logical Lane 6.	0x6	R/W
				x	Data is from SERDINx		
0x30C	FIFO_STATUS_REG_0	[7:0]	LANE_FIFO_FULL		FIFO Full Flags for Each Logical Lane. A full FIFO indicates an error in the JESD204B configuration or with a system clock. If the FIFO for Lane x is full, Bit x in this register will be high.	0x0	R
0x30D	FIFO_STATUS_REG_1	[7:0]	LANE_FIFO_EMPTY		FIFO Empty Flags for Each Logical Lane. An empty FIFO indicates an error in the JESD204B configuration or with a system clock. If the FIFO for Logical Lane x is empty, Bit x in this register will be high.	0x0	R
0x312	SYNCB_GEN_1	[7:6]	RESERVED		Reserved.	0x0	R/W
		[5:4]	SYNCB_ERR _DUR		Duration of $\overline{\text{SYNCOUTx±}}$ Low for Error. The duration applies to both $\overline{\text{SYNCOUT0}}$ and $\overline{\text{SYNCOUT1}}$. A sync error is asserted at the end of a multiframe whenever one or more disparity, not in table or unexpected control character errors are encountered.		
				0	½ PCLK cycle		
				1	1 PCLK cycle		
				2	2 PCLK cycles		
		[3:0]	RESERVED		Reserved.	0x0	R/W
0x314	SERDES_SPI_REG	[7:0]	SERDES_SPI_CONFIG		SERDES SPIConfiguration. Must be written to 0x01 as part of the Physical Layer setup step.	0x0	R/W
0x315	PHY_PRBS_TEST_EN	[7:0]	PHY_TEST_EN		PHY Test Enable. Enables the PHY BER test. Set Bit x to enable the PHY test for Lane x.	0x0	R/W
0x316	PHY_PRBS_TEST_CTRL	7	RESERVED		Reserved.	0x0	R
		[6:4]	PHY_SRC_ERR_CNT		PHY Error Count Source. Selects which PHY errors are being reported in Register 0x31A to Register 0x31C.	0x0	R/W
				x	Report Lane x error count		
		[3:2]	PHY_PRBS_PAT_SEL		PHY PRBS Pattern Select. Selects the PRBS pattern for PHY BER test.	0x0	R/W
				00	PRBS7		
				01	PRBS15		
				10	PRBS31		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		1	PHY_TEST_START		PHY PRBS Test Start. Starts and stops the PHY PRBS test.	0x0	R/W
				0	Test stopped		
				1	Test in progress		
		0	PHY_TEST_RESET		PHY PRBS Test Reset. Resets the PHY PRBS test state machine and error counters.	0x0	R/W
				0	Enable PHY PRBS test state machine		
				1	Hold PHY PRBS test state machine in reset		
0x317	PHY_PRBS_TEST_ THRESHOLD_LOBITS	[7:0]	PHY_PRBS_ THRESHOLD[7:0]		8 LSBs of PHY PRBS Error Threshold.	0x0	R/W
0x318	PHY_PRBS_TEST_ THRESHOLD_ MIDBITS	[7:0]	PHY_PRBS_ THRESHOLD[15:8]		8 ISBs of PHY PRBS Error Threshold.	0x0	R/W
0x319	PHY_PRBS_TEST_ THRESHOLD_HIBITS	[7:0]	PHY_PRBS_ THRESHOLD[23:16]		8 MSBs of PHY PRBS Error Threshold.	0x0	R/W
0x31A	PHY_PRBS_TEST_ ERRCNT_LOBITS	[7:0]	PHY_PRBS_ERR_ CNT[7:0]		8 LSBs of PHY PRBS Error Count. Reported PHY BERT error count from lane selected using Register 0x316[6:4].	0x0	R
0x31B	PHY_PRBS_TEST_ ERRCNT_MIDBITS	[7:0]	PHY_PRBS_ERR_ CNT[15:8]		8 ISBs of PHY PRBS Error Count.	0x0	R
0x31C	PHY_PRBS_TEST_ ERRCNT_HIBITS	[7:0]	PHY_PRBS_ERR_ CNT[23:16]		8 MSBs of PHY PRBS Error Count.	0x0	R
0x31D	PHY_PRBS_TEST_ STATUS	[7:0]	PHY_PRBS_PASS		PHY PRBS Test Pass/Fail. Bit x corresponds to PHY PRBS pass/fail for Physical Lane x. The bit is set to 1 while the error count for Physical Lane x is less than PHY_PRBS_THRESHOLD.	0xFF	R
0x32C	SHORT_TPL_TEST_0	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	SHORT_TPL_SP_ SEL		Short Transport Layer Sample Select. Selects which sample to check from the DAC selected via Bits[3:2].	0x0	R/W
				x	Sample x		
		[3:2]	SHORT_TPL_DAC_ SEL		Short Transport Layer Test DAC Select. Selects which DAC to sample.	0x0	R/W
				x	Sample from DAC x		
		1	SHORT_TPL_TEST_ RESET		Short Transport Layer Test Reset. Resets the result of short transport layer test.	0x0	R/W
				0	Not reset		
				1	Reset		
		0	SHORT_TPL_TEST_ EN		Short Transport Layer Test Enable. See the Subclass 0 section for details on how to perform this test.	0x0	R/W
				0	Disable		
				1	Enable		
0x32D	SHORT_TPL_TEST_1	[7:0]	SHORT_TPL_REF_ SP_LSB		Short Transport Layer Test Reference, Sample LSB. This is the lower eight bits of the expected DAC sample. It is used to compare with the received DAC sample at the output of the JESD204B receiver.	0x0	R/W
0x32E	SHORT_TPL_TEST_2	[7:0]	SHORT_TPL_REF_ SP_MSB		Short Transport Layer Test Reference, Sample MSB. This is the upper eight bits of the expected DAC sample. It is used to compare with the received DAC sample at the output of the JESD204B receiver.	0x0	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x32F	SHORT_TPL_TEST_3	[7:1]	RESERVED		Reserved.	0x0	R
		0	SHORT_TPL_FAIL		Short Transport Layer Test Fail. This bit shows whether the selected DAC sample matches the reference sample. If they match, it is a test pass, otherwise it is a test fail.	0x0	R
				0	Test pass		
				1	Test fail		
0x333	DEVICE_CONFIG_ REG_13	[7:0]	DEVICE_CONFIG_ 13		Must be set to 0x01 for proper JESD interface configuration.	00	R/W
0x334	JESD_BIT_INVERSE_ CTRL	[7:0]	JESD_BIT_INVERSE		Logical Lane Invert. Set Bit x high to invert the JESD deserialized data on Logical Lane x.	0x0	R/W
0x400	DID_REG	[7:0]	DID_RD		Device Identification Number. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x401	BID_REG	[7:4]	ADJCNT_RD		Adjustment Resolution to DAC LMFC. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0.	0x0	R
		[3:0]	BID_RD		Bank Identification: Extension to DID. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x402	LID0_REG	7	RESERVED		Reserved.	0x0	R
		6	ADJDIR_RD		Direction to Adjust DAC LMFC. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0.	0x0	R
		5	PHADJ_RD		Phase Adjustment Request to DAC Link information received on Link Lane ane 0 as specified in Section 8.3 of JESD204B. Must be 0.	0x0	R
		[4:0]	LID0_RD		Lane Identification for Lane 0. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x403	SCR_L_REG	7	SCR_RD		Transmit Scrambling Status. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	Scrambling is disabled		
				1	Scrambling is enabled		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	L-1_RD		Number of Lanes per Converter Device. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	One lane per converter		
				1	Two lanes per converter		
				3	Four lanes per converter		
0x404	F_REG	[7:0]	F-1_RD		Number of Octets per Frame. Settings of 1, 2 and 4 octets per frame are valid. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	(One octet per frame) per lane		
				1	(Two octets per frame) per lane		
				3	(Four octets per frame) per lane		
0x405	K_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	K-1_RD		Number of Frames per Multiframe. Settings of 16 or 32 are valid. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0x0F	16 frames per multiframe		
				0x1F	32 frames per multiframe		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x406	M_REG	[7:0]	M-1_RD		Number of converters per device. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0, 1, or 3.	0x0	R
				0	One converter per device		
				1	Two converters per device		
				3	Four converters per device		
0x407	CS_N_REG	[7:6]	CS_RD		Number of Control Bits per Sample. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. CS must be 0.	0x0	R
		5	RESERVED		Reserved.	0x0	R
		[4:0]	N-1_RD		Converter Resolution. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Converter resolution must be 16.	0x0	R
				0x0F	Converter resolution of 16		
0x408	NP_REG	[7:5]	SUBCLASSV_RD		Device Subclass Version. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
		[4:0]	NP-1_RD		Total Number of Bits per Sample. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 16 bits per sample.	0x0	R
				0x0F	16 bits per sample.		
0x409	S_REG	[7:5]	JESDV_RD		JESD204 Version. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				000	JESD204A		
				001	JESD204B		
		[4:0]	S-1_RD		Number of Samples per Converter per Frame Cycle. Settings of one and two are valid. See Table 34 and Table 35. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	One sample per converter per frame		
				1	Two samples per converter per frame		
0x40A	HD_CF_REG	7	HD_RD		High Density Format. See Section 5.1.3 of the JESD294B standard. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	Low density mode		
				1	High density mode: link information received on Lane 0 as specified in Section 8.3 of JESD204B		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	CF_RD		Number of Control Words per Frame Clock Period per Link. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Bits[4:0] must be 0.	0x0	R
0x40B	RES1_REG	[7:0]	RES1_RD		Reserved Field 1. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40C	RES2_REG	[7:0]	RES2_RD		Reserved Field 2. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40D	CHECKSUM_REG	[7:0]	FCHK0_RD		Checksum for Link Lane 0. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x40E	COMPSUM0_REG	[7:0]	FCMP0_RD		Computed Checksum for Link Lane 0. The JESD204B receiver computes the checksum of the link information received on Lane 0 as specified in Section 8.3 of JESD204B. The computation method is set by the CHECKSUM_MODE bit (Address 0x300[6]) and must match the likewise calculated checksum in Register 0x40D.	0x0	R
0x412	LID1_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID1_RD		Lane Identification for Link Lane 1.Link information received on Lane 0 as specified in section 8.3 of JESD204B.	0x0	R
0x415	CHECKSUM1_REG	[7:0]	FCHK1_RD		Checksum for Link Lane 1. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x416	COMPSUM1_REG	[7:0]	FCMP1_RD		Computed Checksum for Link Lane 1. See the description for Register 0x40E.	0x0	R
0x41A	LID2_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID2_RD		Lane Identification for Link Lane 2.	0x0	R
0x41D	CHECKSUM2_REG	[7:0]	FCHK2_RD		Checksum for Link Lane 2.	0x0	R
0x41E	COMPSUM2_REG	[7:0]	FCMP2_RD		Computed Checksum for Link Lane 2 (see the description for Register 0x40E).	0x0	R
0x422	LID3_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID3_RD		Lane Identification for Link Lane 3.	0x0	R
0x425	CHECKSUM3_REG	[7:0]	FCHK3_RD		Checksum for Link Lane 3.	0x0	R
0x426	COMPSUM3_REG	[7:0]	FCMP3_RD		Computed Checksum for Link Lane 3 (see the description for Register 0x40E).	0x0	R
0x42A	LID4_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID4_RD		Lane Identification for Link Lane 4.	0x0	R
0x42D	CHECKSUM4_REG	[7:0]	FCHK4_RD		Checksum for Link Lane 4.	0x0	R
0x42E	COMPSUM4_REG	[7:0]	FCMP4_RD		Computed Checksum for Link Lane 4 (see the description for Register 0x40E).	0x0	R
0x432	LID5_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID5_RD		Lane Identification for Link Lane 5.	0x0	R
0x435	CHECKSUM5_REG	[7:0]	FCHK5_RD		Checksum for Link Lane 5.	0x0	R
0x436	COMPSUM5_REG	[7:0]	FCMP5_RD		Computed Checksum for Link Lane 5 (see the description for Register 0x40E).	0x0	R
0x43A	LID6_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID6_RD		Lane Identification for Link Lane 6.	0x0	R
0x43D	CHECKSUM6_REG	[7:0]	FCHK6_RD		Checksum for Link Lane 6.	0x0	R
0x43E	COMPSUM6_REG	[7:0]	FCMP6_RD		Computed Checksum for Link Lane 6 (see the description for Register 0x40E).	0x0	R
0x442	LID7_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID7_RD		Lane Identification for Link Lane 7.	0x0	R
0x445	CHECKSUM7_REG	[7:0]	FCHK7_RD		Checksum for Link Lane 7.	0x0	R
0x446	COMPSUM7_REG	[7:0]	FCMP7_RD		Computed Checksum for Link Lane 7 (see the description for Register 0x40E).	0x0	R
0x450	ILS_DID	[7:0]	DID		Device Identification Number. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be set to value read in Register 0x400.	0x0	R/W
0x451	ILS_BID	[7:4]	ADJCNT		Adjustment Resolution to DAC LMFC Must be set to 0.	0x0	R/W
		[3:0]	BID		Bank Identification: Extension to DID Must be set to value read in Register 0x401[3:0].	0x0	R/W
0x452	ILS_LID0	7	RESERVED		Reserved.	0x0	R
		6	ADJDIR		Direction to Adjust DAC LMFC. Must be set to 0.	0x0	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		5	PHADJ		Phase Adjustment Request to DAC. Must be set to 0.	0x0	R/W
		[4:0]	LID0		Lane Identification for Link Lane 0. Must be set to the value read in Register 0x402[4:0].	0x0	R/W
0x453	ILS_SCR_L	7	SCR		Receiver Descrambling Enable.	0x1	R/W
				0	Descrambling is disabled		
				1	Descrambling is enabled		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	L-1		Number of Lanes per Converter Device. See Table 34 and Table 35.	0x3	R/W
				0	One lane per converter		
				1	Two lanes per converter		
				3	Four lanes per converter		
				7	Eight lanes per converter (single link only)		
0x454	ILS_F	[7:0]	F-1		Number of Octets per Lane per Frame. Settings of 1, 2, and 4 (octets per lane) per frame are valid. See Table 34 and Table 35.	0x0	R/W
				0	(One octet per lane) per frame		
				1	(Two octets per lane) per frame		
				3	(Four octets per lane) per frame		
0x455	ILS_K	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	K-1		Number of Frames per Multiframe. Settings of 16 or 32 are valid. Must be set to 32 when F = 1 (Register 0x476).	0x1F	R/W
				0x0F	16 frames per multiframe		
				0x1F	32 frames per multiframe		
0x456	ILS_M	[7:0]	M-1		Number of Converters per Device. See Table 34 and Table 35.	0x1	R/W
				0	One converter per link		
				1	Two converters per link		
				3	Four converters per link (single link only)		
0x457	ILS_CS_N	[7:6]	CS		Number of Control Bits per Sample. Must be set to 0. Control bits are not supported.	0x0	R/W
				0	Zero control bits per sample		
		5	RESERVED		Reserved.	0x0	R
		[4:0]	N-1		Converter Resolution. Must be set to 16 bits of resolution.	0xF	R/W
				0xF	Converter resolution of 16.		
0x458	ILS_NP	[7:5]	SUBCLASSV		Device Subclass Version.	0x1	R/W
				0	Subclass 0		
				1	Subclass 1		
		[4:0]	NP-1		Total Number of Bits per Sample. Must be set to 16 bits per sample.	0xF	R/W
				0xF	16 bits per sample.		
0x459	ILS_S	[7:5]	JESDV		JESD204 Version.	0x1	R/W
				000	JESD204A		
				001	JESD204B		
		[4:0]	S-1		Number of Samples per Converter per Frame Cycle. Settings of one and two are valid. See Table 34 and Table 35.	0x0	R/W
				0	One sample per converter per frame		
				1	Two samples per converter per frame		
0x45A	ILS_HD_CF	7	HD		High Density Format. If F = 1, HD must be set to 1. Otherwise, HD must be set to 0. See Section 5.1.3 of JESD204B standard.	0x1	R/W
				0	Low density mode		
				1	High density mode		
		[6:5]	RESERVED		Reserved.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		[4:0]	CF		Number of Control Words per Frame Clock Period per Link. Must be set to 0. Control bits are not supported.	0x0	R/W
0x45B	ILS_RES1	[7:0]	RES1		Reserved Field 1.	0x0	R/W
0x45C	ILS_RES2	[7:0]	RES2		Reserved Field 2.	0x0	R/W
0x45D	ILS_CHECKSUM	[7:0]	FCHK0		Checksum for Link Lane 0. Calculated checksum. Calculation depends on 0x300[6].	0x45	R/W
0x46B	ERRCNTRMON_RB	[7:0]	READERRORCNTR		Read JESD204B Error Counter. After selecting the lane and error counter by writing to LANESEL and CNTRSEL (both in this same register), the selected error counter is read back here.	0x0	R
0x46B	ERRCNTRMON	7	RESERVED		Reserved.	0x0	R
		[6:4]	LANESEL		Link Lane select for JESD204B error counter. Selects the lane whose errors are read back in this register.	0x0	W
				x	Selects Link Lane x		
		[3:2]	RESERVED		Reserved.	0x0	R
		[1:0]	CNTRSEL		JESD204B Error Counter Select. Selects the type of error that are read back in this register.	0x0	W
				00	BADDISCNTR: bad running disparity counter		
				01	NITCNTR: not in table error counter		
				10	UCCCNTR: Unexpected control character counter		
0x46C	LANEDESKEW	[7:0]	LANEDESKEW		Lane Deskew. Setting Bit x deskews Link Lane x	0xF	R/W
0x46D	BADDISPARITY_RB	[7:0]	BADDIS		Bad Disparity Character Error (BADDIS). Bit x is set when the bad disparity error count for Link Lane x reaches the threshold in Register 0x47C.	0x0	R
0x46D	BADDISPARITY	7	RST_IRQ_DIS		BADDIS IRQ Reset. Reset BADDIS IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERR_ CNTR_DIS		BADDIS Error Counter Disable. Disable the BADDIS error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RST_ERR_CNTR_DIS		BADDIS Error Counter Reset. Reset BADDIS error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANE_ADDR_DIS		Link Lane Address for Functions Described in Bits[7:5].	0x0	W
0x46E	NIT_RB	[7:0]	NIT		Not in table Character Error (NIT). Bit x is set when the NIT error count for Link Lane x reaches the threshold in Register 0x47C.	0x0	R
0x46E	NIT_W	7	RST_IRQ_NIT		IRQ Reset. Reset IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERR_ CNTR_NIT		Disable Error Counter. Disable the error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RST_ERR_CNTR_NIT		Reset Error Counter. Reset error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANE_ADDR_NIT		Link Lane Address for Functions Described in Bits[7:5].	0x0	W
0x46F	UNEXPECTED-CONTROL_RB	[7:0]	UCC		Unexpected Control Character Error (UCC). Bit x is set when the UCC error count for Link Lane x reaches the threshold in Register 0x47C.	0x0	R
0x46F	UNEXPECTED-CONTROL_W	7	RST_IRQ_UCC		IRQ Reset. Reset IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		6	DISABLE_ERR_CNTR_UCC		Disable Error Counter. Disable the error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RST_ERR_CNTR_UCC		Reset Error Counter. Reset error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANE_ADDR_UCC		Link Lane Address for Functions Described in Bits[7:5].	0x0	W
0x470	CODEGRPSYNCFLG	[7:0]	CODEGRPSYNC		Code Group Sync Flag (from Each Instantiated Lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x47A[0]. A loss of CODEGRPSYNC triggers sync request assertion. See the SYNCOUT and SYSREF Signals section and the Deterministic Latency section.	0x0	R/W
				0	Synchronization is lost		
				1	Synchronization is achieved		
0x471	FRAMESYNCFLG	[7:0]	FRAMESYNC		Frame Sync Flag (from Each Instantiated Lane). This register indicates the live status for each lane. Writing 1 to Bit 7 resets the IRQ. A loss of frame sync automatically initiates a synchronization sequence.	0x0	R/W
				0	Synchronization is lost		
				1	Synchronization is achieved		
0x472	GOODCHKSUMFLG	[7:0]	GOODCHECKSUM		Good Checksum Flag (from Each Instantiated Lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x47A[2].	0x0	R/W
				0	Last computed checksum is not correct		
				1	Last computed checksum is correct		
0x473	INITLANESYNCFLG	[7:0]	INITIALLANESYNC		Initial Lane Sync Flag (from Each Instantiated Lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x47A[3]. Loss of synchronization is also reported on SYNCOUT1± or SYNCOUT0±. See the SYNCOUT and SYSREF± Signal section and the Deterministic Latency section.	0x0	R/W
0x476	CTRLREG1	[7:0]	F		Number of Octets per Frame. Settings of 1, 2, and 4 are valid. See Table 34 and Table 35.	0x1	R/W
				1	One octet per frame		
				2	Two octets per frame		
				4	Four octets per frame		
0x477	CTRLREG2	7	ILAS_MODE		ILAS Test Mode. Defined in Section 5.3.3.8 of JESD204B specification.	0x0	R/W
				1	JESD204B receiver is constantly receiving ILAS frames		
				0	Normal link operation		
		[6:4]	RESERVED		Reserved.	0x0	R
		3	THRESHOLD_MASK_EN		Threshold Mask Enable. Set this bit if using SYNC_ASSERTION_MASK (Register 0x47B[7:5]).	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x478	KVAL	[7:0]	KSYNC		Number of K Multiframes During ILAS (Divided by Four). Sets the number of multiframes to send initial lane alignment sequence. Cannot be set to 0.	0x1	R/W
				x	4x multiframes during ILAS		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x47A	IRQVECTOR_MASK	7	BADDIS_MASK		Bad Disparity Mask.	0x0	W
				1	If the bad disparity count reaches ERRORTHRESH on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		6	NIT_MASK		Not in table Mask.	0x0	W
				1	If the not in table character count reaches ERRORTHRESH on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		5	UCC_MASK		Unexpected Control Character Mask.	0x0	W
				1	If the unexpected control character count reaches ERRORTHRESH on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		4	RESERVED		Reserved.	0x0	R
		3	INITIALLANESYNC_ MASK		Initial Lane Sync Mask.	0x0	W
				1	If initial lane sync (0x473) fails on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		2	BADCHECKSUM_ MASK		Bad Checksum Mask.	0x0	W
				1	If there is a bad checksum (0x472) on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		1	FRAMESYNC_ MASK		Frame Sync Mask	0x0	W
				1	If frame sync (0x471) fails on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		0	CODEGRPSYNC_ MASK		Code Group Sync Machine Mask.	0x0	W
				1	If code group sync (0x470) fails on any lane, $\overline{\text{IRQ}}$ is pulled low.		
0x47A	IRQVECTOR_FLAG	7	BADDIS_FLAG		Bad Disparity Error Count.	0x0	R
				1	Bad disparity character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46D to determine which lanes are in error.		
		6	NIT_FLAG		Not in table Error Count	0x0	R
				1	Not in table character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46E to determine which lanes are in error.		
		5	UCC_FLAG		Unexpected Control Character Error Count	0x0	R
				1	Unexpected control character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46F to determine which lanes are in error.		
		4	RESERVED		Reserved.	0x0	R
		3	INITIALLANESYNC_ FLAG		Initial Lane Sync Flag.	0x0	R
				1	Initial lane sync failed on at least one lane. Read Register 0x473 to determine which lanes are in error		
		2	BADCHECKSUM_ FLAG		Bad Checksum Flag.	0x0	R
				1	Bad checksum on at least one lane. Read Register 0x472 to determine which lanes are in error.		
		1	FRAMESYNC_ FLAG		Frame Sync Flag.	0x0	R
				1	Frame sync failed on at least one lane. Read Register 0x471 to determine which lanes are in error.		
		0	CODEGRPSYNC_ FLAG		Code Group Sync Flag.	0x0	R
				1	Code group sync failed on at least one lane. Read Register 0x470 to determine which lanes are in error		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x47B	SYNCASSERTIONMASK	7	BADDIS_S		Bad Disparity Error on Sync.	0x0	R/W
				1	Asserts a sync request on SYNCOUTx± when the bad disparity character count reaches the threshold in Register 0x47C		
		6	NIT_S		Not in table Error on Sync.	0x0	R/W
				1	Asserts a sync request on SYNCOUTx± when the not in table character count reaches the threshold in Register 0x47C		
		5	UCC_S		Unexpected Control Character Error on Sync.	0x0	R/W
				1	Asserts a sync request on SYNCOUTx± when the unexpected control character count reaches the threshold in Register 0x47C		
		4	CMM		Configuration Mismatch IRQ. If CMM_ENABLE is high, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit. If CMM_ENABLE is low, this bit is non-functional.	0x0	R/W
				1	Link Lane 0 configuration registers (Register 0x450 to Register 0x45D) do not match the JESD204B transmit settings (Register 0x400 to Register 0x40D)		
		3	CMM_ENABLE		Configuration Mismatch IRQ Enable.	0x1	R/W
				1	Enables IRQ generation if a configuration mismatch is detected		
				0	Configuration mismatch IRQ disabled		
		[2:0]	RESERVED		Reserved.	0x0	R
0x47C	ERRORTHRES	[7:0]	ETH		Error Threshold. Bad disparity, not in table, and unexpected control character errors are counted and compared to the error threshold value. When the count reaches the threshold, either an IRQ is generated or the SYNCOUTx± signal is asserted per the mask register settings, or both. Function is performed in all lanes.	0xFF	R/W
0x47D	LANEENABLE	[7:0]	LANE_ENA		Lane Enable. Setting Bit x enables Link Lane x. This register must be programmed before receiving the code group pattern for proper operation.	0xF	R/W
0x47E	RAMP_ENA	[7:1]	RESERVED		Reserved.	0x0	R
		0	ENA_RAMP_ CHECK		Enable Ramp Checking at the Beginning of ILAS.	0x0	W
				0	Disable ramp checking at beginning of ILAS; ILAS data need not be a ramp		
				1	Enable ramp checking; ILAS data needs to be a ramp starting at 00-01-02; otherwise, the ramp ILAS fails and the device does not start up		
0x520	DIG_TEST0	[7:2]	RESERVED		Must write default value for proper operation.	0x7	R/W
		1	DC_TEST_MODE		DC Test Mode	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x521	DC_TEST_VALUEI0	[7:0]	DC_TEST_ VALUEI[7:0]		DC Value LSB of DC Test Mode for I DAC.	0x0	R/W
0x522	DC_TEST_VALUEI1	[7:0]	DC_TEST_ VALUEI [15:8]		DC value MSB of DC Test Mode for I DAC.	0x0	R/W
0x523	DC_TEST_VALUEQ0	[7:0]	DC_TEST_ VALUEQ[7:0]		DC value LSB of DC Test Mode for Q DAC.	0x0	R/W
0x524	DC_TEST_VALUEQ1	[7:0]	DC_TEST_ VALUEQ[15:8]		DC value MSB of DC Test Mode for Q DAC.	0x0	R/W

LOOKUP TABLES FOR THREE DIFFERENT DAC PLL REFERENCE FREQUENCIES

It is possible to reconfigure the loop filter to tailor synthesizer performance either by substituting new values into the lookup table or by simply writing new values directly to the loop filter registers. The VCO gain constant is provided in the table to calculate a custom loop filter with standard PLL filter equations to meet any particular need.

The resolution of the integrated components combined with the programmable charge pump current yields an extremely wide range of possible loop bandwidths for a given frequency of operation.

Various DAC PLL reference frequencies are provided in Table 96 to Table 98. To enable the VCO temperature compensation, Table 96 to Table 98 list various reference frequencies. The intent is for the user to use longer, more accurate calibration times for the device to remain in operation indefinitely.

Table 96, Table 97, and Table 98 are provided for 40 MHz, 60 MHz, and 80 MHz reference frequencies, respectively. The correct table to use is the one that most closely matches the loop f_{REF} for the operating mode.

Table 96. Reference Frequency 40 MHz, Loop Bandwidth = 0.25 MHz

			DAC	Reg. 0x1B6 [3:0]	Reg. 0x1B5 [3:0]	Reg. 0x1BB [2:0]	Reg. 0x1BB [4:3]	Reg. 0x1B4 [6:3]	Reg. 0x1C5 [3:0]	Reg. 0x08A [5:0]	Reg. 0x087 [7:4]	Reg. 0x087 [3:0]	Reg. 0x088 [7:4]	Reg. 0x088 [3:0]	0x089 [3:0]
Band	Index	VCO Freq. (GHz)	VCO K_V (MHz)	VCO Output Level	VCO Vara[1]	VCO Bias Ref	VCO Bias TC[2]	VCO Cal Offset	VCO Vara[1] Ref.	Charge Pump Current	Loop Filter C2	Loop Filter C1	Loop Filter R1	Loop Filter C3	Loop Filter R3
0	1	12.605	151.8	10	0	4	0	15	8	8	12	3	14	15	11
8	2	12.245	137.3	10	0	4	0	15	8	9	12	3	14	15	11
16	3	11.906	124.9	10	0	4	0	15	8	9	12	3	14	15	11
24	4	11.588	114.2	10	0	4	0	15	8	10	12	3	14	15	11
32	5	11.288	104.9	10	0	4	0	15	8	11	12	3	14	15	11
40	6	11.007	96.74	10	0	4	0	15	8	11	12	3	14	15	11
48	7	10.742	89.57	10	0	4	0	14	8	12	12	3	14	15	11
56	8	10.492	83.23	10	0	5	1	14	9	13	12	3	14	15	11
64	9	10.258	77.58	10	0	5	1	14	9	13	12	3	14	15	11
72	10	10.036	72.54	10	0	5	1	14	9	14	12	3	14	15	11
80	11	9.8270	68.01	10	0	5	1	14	9	15	12	3	14	15	11
88	12	9.6311	63.93	10	0	5	1	14	9	15	12	3	14	15	11
96	13	9.4453	60.24	10	0	5	1	14	9	16	12	3	14	15	11
104	14	9.2698	56.89	10	0	5	1	14	9	17	12	3	14	15	11
112	15	9.1036	53.84	10	0	5	1	14	9	17	12	3	14	15	11
120	16	8.9463	51.05	10	0	5	1	14	9	18	12	3	14	15	11
128	17	8.7970	67.48	10	1	6	1	15	11	13	12	3	14	15	11
136	18	8.6553	64.22	10	1	6	1	15	11	14	12	3	14	15	11
144	19	8.5206	61.21	10	1	6	1	15	11	14	12	3	14	15	11
152	20	8.3923	58.43	10	1	6	1	15	11	15	12	3	14	15	11
160	21	8.2699	55.86	10	1	6	1	15	11	15	12	3	14	15	11
168	22	8.1531	53.48	10	1	6	1	15	11	16	12	3	14	15	11
176	23	8.0414	51.26	10	1	6	1	15	11	16	12	3	14	15	11
184	24	7.9344	49.19	10	1	6	1	15	11	17	12	3	14	15	11
192	25	7.8318	47.26	10	1	6	1	15	11	17	12	3	14	15	11
200	26	7.7332	45.46	10	1	6	1	15	11	17	12	3	14	15	11
208	27	7.6384	43.76	10	1	6	1	15	11	18	12	3	14	15	11
216	28	7.5471	42.17	10	1	6	1	15	11	18	12	3	14	15	11
224	29	7.4590	40.68	10	1	6	1	15	11	19	12	3	14	15	11
232	30	7.3740	39.27	10	1	7	2	15	12	19	12	3	14	15	11
240	31	7.2919	37.94	10	1	7	2	15	12	20	12	3	14	15	11
248	32	7.2124	36.68	10	1	7	2	15	12	20	12	3	14	15	11
256	33	7.1355	35.49	10	1	7	2	15	14	21	12	3	14	15	11
264	34	7.0610	34.37	10	1	7	2	15	14	21	12	3	14	15	11
272	35	6.9887	33.30	10	1	7	2	15	14	22	12	3	14	15	11
280	36	6.9186	32.28	10	1	7	2	15	14	22	12	3	14	15	11
288	37	6.8506	31.32	10	1	7	2	15	14	23	12	3	14	15	11
296	38	6.7846	30.41	10	1	7	2	15	14	23	12	3	14	15	11
304	39	6.7205	29.53	10	1	7	2	15	14	24	12	3	14	15	11

Band	Index	VCO Freq. (GHz)	DAC VCO K_V (MHz)	Reg. 0x1B6 [3:0] VCO Output Level	Reg. 0x1B5 [3:0] VCO Vara[1]	Reg. 0x1BB [2:0] VCO Bias Ref	Reg. 0x1BB [4:3] VCO Bias TC[2]	Reg. 0x1B4 [6:3] VCO Cal Offset	Reg. 0x1C5 [3:0] VCO Vara[1] Ref.	Reg. 0x08A [5:0] Charge Pump Current	Reg. 0x087 [7:4] Loop Filter C2	Reg. 0x087 [3:0] Loop Filter C1	Reg. 0x088 [7:4] Loop Filter R1	Reg. 0x088 [3:0] Loop Filter C3	0x089 [3:0] Loop Filter R3
312	40	6.6582	28.70	10	1	7	2	15	14	24	12	3	14	15	11
320	41	6.5978	27.91	10	1	7	2	15	14	25	12	3	14	15	11
328	42	6.5392	27.16	10	1	7	2	15	14	25	12	3	14	15	11
336	43	6.4823	26.43	10	1	7	2	15	14	26	12	3	14	15	11
344	44	6.4270	25.75	10	1	7	2	15	14	26	12	3	14	15	11
352	45	6.3734	39.20	10	3	7	3	15	12	17	12	3	14	15	11
360	46	6.3214	38.21	10	3	7	3	15	12	17	12	3	14	15	11
368	47	6.2709	37.27	10	3	7	3	15	12	17	12	3	14	15	11
376	48	6.2220	36.37	10	3	7	3	15	12	18	12	3	14	15	11
384	49	6.1745	35.50	10	3	7	3	15	12	18	12	3	14	15	11
392	50	6.1284	34.68	10	3	7	3	15	12	18	12	3	14	15	11
400	51	6.0836	33.88	10	3	7	3	15	12	18	12	3	14	15	11
408	52	6.0401	33.12	10	3	7	3	15	12	19	12	3	14	15	11
416	53	5.9977	32.38	10	3	7	3	15	12	19	12	3	14	15	11

[1] Vara is the varactor.
[2] TC is the temperature coefficient.

Table 97. Reference Frequency 60 MHz, Loop Bandwidth = 0.25 MHz

Band	Index	VCO Freq. (GHz)	DAC VCO K_V (MHz)	Reg. 0x1B6 [3:0] VCO Output Level	Reg. 0x1B5 [3:0] VCO Vara[1]	Reg. 0x1BB [2:0] VCO Bias Ref	Reg. 0x1BB [4:3] VCO Bias TC[2]	Reg. 0x1B4 [6:3] VCO Cal Offset	Reg. 0x1C5 [3:0] VCO Vara[1] Ref.	Reg. 0x08A [5:0] Charge Pump Current	Reg. 0x087 [7:4] Loop Filter C2	Reg. 0x087 [3:0] Loop Filter C1	Reg. 0x088 [7:4] Loop Filter R1	Reg. 0x088 [3:0] Loop Filter C3	Reg. 0x089 [3:0] Loop Filter R3
0	1	12.605	151.8	10	0	4	0	15	8	10	15	4	13	15	10
8	2	12.245	137.3	10	0	4	0	15	8	11	15	4	13	15	10
16	3	11.906	124.9	10	0	4	0	15	8	11	15	4	13	15	10
24	4	11.588	114.2	10	0	4	0	15	8	12	15	4	13	15	10
32	5	11.288	104.9	10	0	4	0	15	8	13	15	4	13	15	10
40	6	11.007	96.74	10	0	4	0	14	8	14	15	4	13	15	10
48	7	10.742	89.57	10	0	4	0	14	8	15	15	4	13	15	10
56	8	10.492	83.23	10	0	5	1	14	9	15	15	4	13	15	10
64	9	10.258	77.58	10	0	5	1	14	9	16	15	4	13	15	10
72	10	10.036	72.54	10	0	5	1	14	9	17	15	4	13	15	10
80	11	9.8270	68.01	10	0	5	1	14	9	18	15	4	13	15	10
88	12	9.6311	63.93	10	0	5	1	14	9	19	15	4	13	15	10
96	13	9.4453	60.24	10	0	5	1	14	9	19	15	4	13	15	10
104	14	9.2698	56.89	10	0	5	1	14	9	20	15	4	13	15	10
112	15	9.1036	53.84	10	0	5	1	13	9	21	15	4	13	15	10
120	16	8.9463	51.05	10	0	5	1	13	9	22	15	4	13	15	10
128	17	8.7970	67.48	10	1	6	1	15	11	16	15	4	13	15	10
136	18	8.6553	64.22	10	1	6	1	15	11	17	15	4	13	15	10
144	19	8.5206	61.21	10	1	6	1	15	11	17	15	4	13	15	10
152	20	8.3923	58.43	10	1	6	1	15	11	18	15	4	13	15	10
160	21	8.2699	55.86	10	1	6	1	15	11	18	15	4	13	15	10
168	22	8.1531	53.48	10	1	6	1	15	11	19	15	4	13	15	10
176	23	8.0414	51.26	10	1	6	1	15	11	19	15	4	13	15	10
184	24	7.9344	49.19	10	1	6	1	15	11	20	15	4	13	15	10
192	25	7.8318	47.26	10	1	6	1	15	11	21	15	4	13	15	10
200	26	7.7332	45.46	10	1	6	1	15	11	21	15	4	13	15	10
208	27	7.6384	43.76	10	1	6	1	15	11	22	15	4	13	15	10
216	28	7.5471	42.17	10	1	6	1	15	11	22	15	4	13	15	10
224	29	7.4590	40.68	10	1	6	1	15	11	23	15	4	13	15	10
232	30	7.3740	39.27	10	1	7	2	15	12	23	15	4	13	15	10

Band	Index	VCO Freq. (GHz)	DAC VCO K_V (MHz)	Reg. 0x1B6 [3:0] VCO Output Level	Reg. 0x1B5 [3:0] VCO Vara[1]	Reg. 0x1BB [2:0] VCO Bias Ref	Reg. 0x1BB [4:3] VCO Bias TC[2]	Reg. 0x1B4 [6:3] VCO Cal Offset	Reg. 0x1C5 [3:0] VCO Vara[1] Ref.	Reg. 0x08A [5:0] Charge Pump Current	Reg. 0x087 [7:4] Loop Filter C2	Reg. 0x087 [3:0] Loop Filter C1	Reg. 0x088 [7:4] Loop Filter R1	Reg. 0x088 [3:0] Loop Filter C3	Reg. 0x089 [3:0] Loop Filter R3
240	31	7.2919	37.94	10	1	7	2	15	12	24	15	4	13	15	10
248	32	7.2124	36.68	10	1	7	2	15	12	25	15	4	13	15	10
256	33	7.1355	35.49	10	1	7	2	15	14	25	15	4	13	15	10
264	34	7.0610	34.37	10	1	7	2	15	14	26	15	4	13	15	10
272	35	6.9887	33.30	10	1	7	2	15	14	26	15	4	13	15	10
280	36	6.9186	32.28	10	1	7	2	15	14	27	15	4	13	15	10
288	37	6.8506	31.32	10	1	7	2	15	14	27	15	4	13	15	10
296	38	6.7846	30.41	10	1	7	2	15	14	28	15	4	13	15	10
304	39	6.7205	29.53	10	1	7	2	15	14	29	15	4	13	15	10
312	40	6.6582	28.70	10	1	7	2	15	14	29	15	4	13	15	10
320	41	6.5978	27.91	10	1	7	2	15	14	30	15	4	13	15	10
328	42	6.5392	27.16	10	1	7	2	15	14	30	15	4	13	15	10
336	43	6.4823	26.43	10	1	7	2	15	14	31	15	4	13	15	10
344	44	6.4270	25.75	10	1	7	2	15	14	32	15	4	13	15	10
352	45	6.3734	39.20	10	3	7	3	15	12	20	15	4	13	15	10
360	46	6.3214	38.21	10	3	7	3	15	12	21	15	4	13	15	10
368	47	6.2709	37.27	10	3	7	3	15	12	21	15	4	13	15	10
376	48	6.2220	36.37	10	3	7	3	15	12	21	15	4	13	15	10
384	49	6.1745	35.50	10	3	7	3	15	12	22	15	4	13	15	10
392	50	6.1284	34.68	10	3	7	3	15	12	22	15	4	13	15	10
400	51	6.0836	33.88	10	3	7	3	15	12	22	15	4	13	15	10
408	52	6.0401	33.12	10	3	7	3	15	12	23	15	4	13	15	10
416	53	5.9977	32.38	10	3	7	3	15	12	23	15	4	13	15	10

[1] Vara is the varactor.
[2] TC is the temperature coefficient.

Table 98. Reference Frequency 80 MHz, Loop Bandwidth = 0.25 MHz

Band	Index	VCO Freq. (GHz)	DAC VCO K_V (MHz)	Reg. 0x1B6 [3:0] VCO Output Level	Reg. 0x1B5 [3:0] VCO Vara[1]	Reg. 0x1BB [2:0] VCO Bias Ref	Reg. 0x1BB [4:3] VCO Bias TC[2]	Reg. 0x1B4 [6:3] VCO Cal Offset	Reg. 0x1C5 [3:0] VCO Vara[2] Ref	Reg. 0x08A [5:0] Charge Pump Current	Reg. 0x087 [7:4] Loop Filter C2	Reg. 0x087 [3:0] Loop Filter C1	Reg. 0x088 [7:4] Loop Filter R1	Reg. 0x088 [3:0] Loop Filter C3	Reg. 0x089 [3:0] Loop Filter R3
0	1	12.605	151.8	10	0	4	0	15	8	8	13	4	13	15	9
8	2	12.245	137.3	10	0	4	0	15	8	9	13	4	13	15	9
16	3	11.906	124.9	10	0	4	0	15	8	10	13	4	13	15	9
24	4	11.588	114.2	10	0	4	0	15	8	11	13	4	13	15	9
32	5	11.288	104.9	10	0	4	0	15	8	11	13	4	13	15	9
40	6	11.007	96.74	10	0	4	0	14	8	12	13	4	13	15	9
48	7	10.742	89.57	10	0	4	0	14	8	13	13	4	13	15	9
56	8	10.492	83.23	10	0	5	1	14	9	13	13	4	13	15	9
64	9	10.258	77.58	10	0	5	1	14	9	14	13	4	13	15	9
72	10	10.036	72.54	10	0	5	1	14	9	15	13	4	13	15	9
80	11	9.8270	68.01	10	0	5	1	14	9	15	13	4	13	15	9
88	12	9.6311	63.93	10	0	5	1	13	9	16	13	4	13	15	9
96	13	9.4453	60.24	10	0	5	1	13	9	17	13	4	13	15	9
104	14	9.2698	56.89	10	0	5	1	13	9	18	13	4	13	15	9
112	15	9.1036	53.84	10	0	5	1	13	9	18	13	4	13	15	9
120	16	8.9463	51.05	10	0	5	1	13	9	19	13	4	13	15	9
128	17	8.7970	67.48	10	1	6	1	15	11	14	13	4	13	15	9
136	18	8.6553	64.22	10	1	6	1	15	11	14	13	4	13	15	9
144	19	8.5206	61.21	10	1	6	1	15	11	15	13	4	13	15	9
152	20	8.3923	58.43	10	1	6	1	15	11	15	13	4	13	15	9
160	21	8.2699	55.86	10	1	6	1	15	11	16	13	4	13	15	9

			DAC	Reg. 0x1B6 [3:0]	Reg. 0x1B5 [3:0]	Reg. 0x1BB [2:0]	Reg. 0x1BB [4:3]	Reg. 0x1B4 [6:3]	Reg. 0x1C5 [3:0]	Reg. 0x08A [5:0]	Reg. 0x087 [7:4]	Reg. 0x087 [3:0]	Reg. 0x088 [7:4]	Reg. 0x088 [3:0]	Reg. 0x089 [3:0]
Band	**Index**	**VCO Freq. (GHz)**	**VCO K_V (MHz)**	**VCO Output Level**	**VCO Vara[1]**	**VCO Bias Ref**	**VCO Bias TC[2]**	**VCO Cal Offset**	**VCO Vara[2] Ref**	**Charge Pump Current**	**Loop Filter C2**	**Loop Filter C1**	**Loop Filter R1**	**Loop Filter C3**	**Loop Filter R3**
168	22	8.1531	53.48	10	1	6	1	15	11	16	13	4	13	15	9
176	23	8.0414	51.26	10	1	6	1	15	11	17	13	4	13	15	9
184	24	7.9344	49.19	10	1	6	1	15	11	17	13	4	13	15	9
192	25	7.8318	47.26	10	1	6	1	15	11	18	13	4	13	15	9
200	26	7.7332	45.46	10	1	6	1	15	11	18	13	4	13	15	9
208	27	7.6384	43.76	10	1	6	1	15	11	19	13	4	13	15	9
216	28	7.5471	42.17	10	1	6	1	15	11	19	13	4	13	15	9
224	29	7.4590	40.68	10	1	6	1	15	11	20	13	4	13	15	9
232	30	7.3740	39.27	10	1	7	2	15	12	20	13	4	13	15	9
240	31	7.2919	37.94	10	1	7	2	15	12	21	13	4	13	15	9
248	32	7.2124	36.68	10	1	7	2	15	12	21	13	4	13	15	9
256	33	7.1355	35.49	10	1	7	2	15	14	22	13	4	13	15	9
264	34	7.0610	34.37	10	1	7	2	15	14	22	13	4	13	15	9
272	35	6.9887	33.30	10	1	7	2	15	14	23	13	4	13	15	9
280	36	6.9186	32.28	10	1	7	2	15	14	23	13	4	13	15	9
288	37	6.8506	31.32	10	1	7	2	15	14	24	13	4	13	15	9
296	38	6.7846	30.41	10	1	7	2	15	14	24	13	4	13	15	9
304	39	6.7205	29.53	10	1	7	2	15	14	25	13	4	13	15	9
312	40	6.6582	28.70	10	1	7	2	15	14	25	13	4	13	15	9
320	41	6.5978	27.91	10	1	7	2	15	14	26	13	4	13	15	9
328	42	6.5392	27.16	10	1	7	2	15	14	26	13	4	13	15	9
336	43	6.4823	26.43	10	1	7	2	15	14	27	13	4	13	15	9
344	44	6.4270	25.75	10	1	7	2	15	14	27	13	4	13	15	9
352	45	6.3734	39.20	10	3	7	3	15	12	18	13	4	13	15	9
360	46	6.3214	38.21	10	3	7	3	15	12	18	13	4	13	15	9
368	47	6.2709	37.27	10	3	7	3	15	12	18	13	4	13	15	9
376	48	6.2220	36.37	10	3	7	3	15	12	19	13	4	13	15	9
384	49	6.1745	35.50	10	3	7	3	15	12	19	13	4	13	15	9
392	50	6.1284	34.68	10	3	7	3	15	12	19	13	4	13	15	9
400	51	6.0836	33.88	10	3	7	3	15	12	19	13	4	13	15	9
408	52	6.0401	33.12	10	3	7	3	15	12	20	13	4	13	15	9
416	53	5.9977	32.38	10	3	7	3	15	12	20	13	4	13	15	9

[1] Vara is the varactor.
[2] TC is the temperature coefficient.

OUTLINE DIMENSIONS

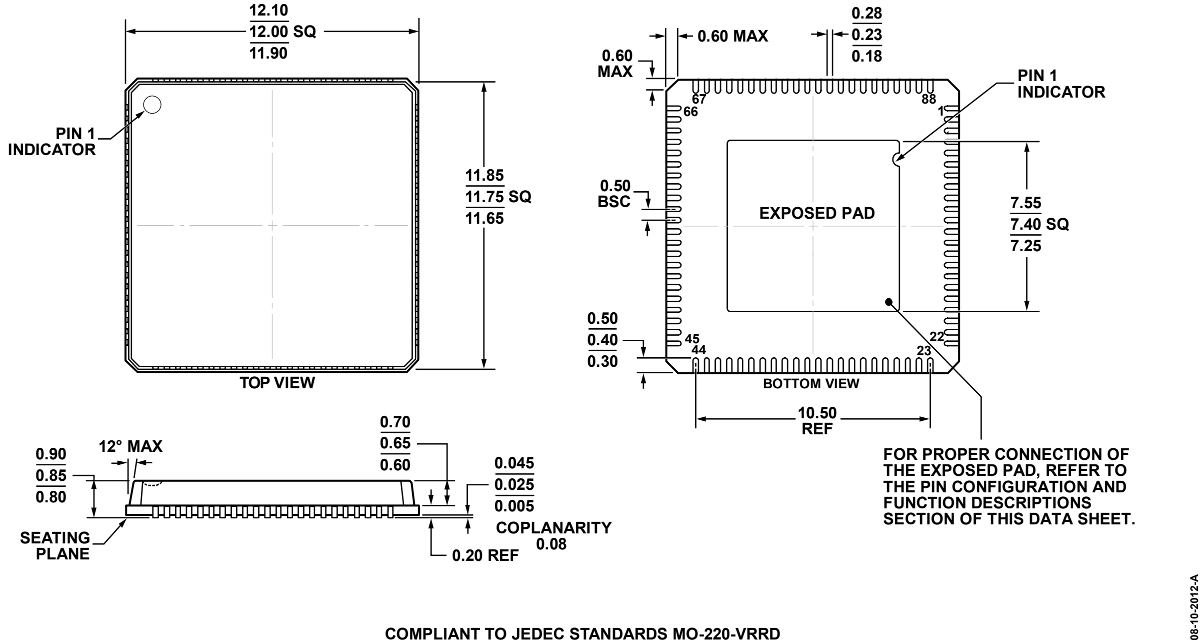


Figure 84. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-88-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9144BCPZ	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9144BCPZRL	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9144-EBZ		DPG3 Evaluation Board	
AD9144-FMC-EBZ		FMC Evaluation Board	
AD9144-M6720-EBZ		DPG3 Evaluation Board with ADRF6720 Modulator	

[1] Z = RoHS Compliant Part.