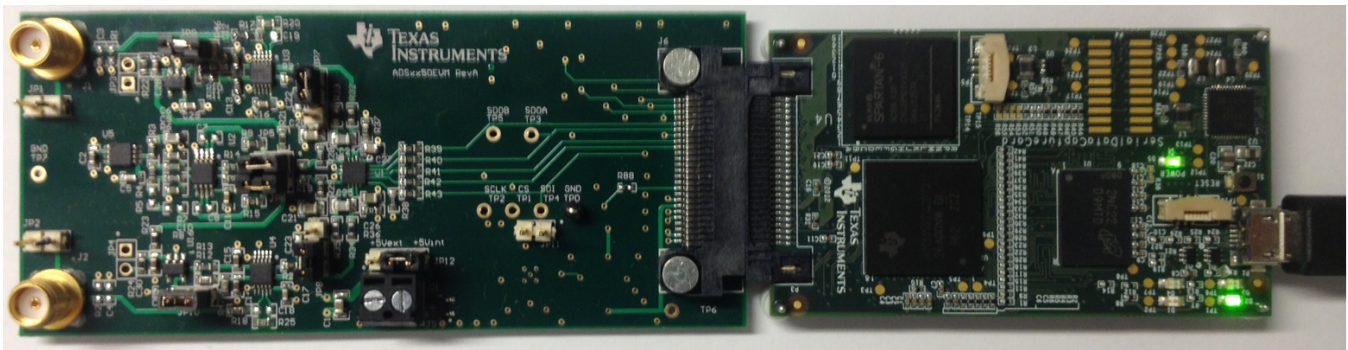


## ADS8350EVM-PDK



**ADS8350EVM-PDK**

This user's guide describes the characteristics, operation and use of the ADS8350EVM performance demonstration kit (PDK). This kit is an evaluation platform for the ADS8350, dual-channel, 16-bit, simultaneous sampling, successive approximation register (SAR) analog-to-digital converter (ADC) that supports pseudo-differential analog inputs. This EVM eases the evaluation of the ADS8350 device with hardware and software for computer connectivity through a universal serial bus (USB). This user's guide includes complete circuit descriptions, a schematic diagram, and a bill of materials.

Throughout this document, the terms demonstration kit, evaluation board, evaluation module are synonymous with the ADS8350EVM-PDK.

The following related documents are available through the Texas Instruments web site at <http://www.ti.com>.

### Related Documentation

Device	Literature Number
<a href="#">ADS8350</a>	<a href="#">SBAS580</a>
<a href="#">REF5025</a>	<a href="#">SBOS410</a>
<a href="#">OPA2350</a>	<a href="#">SBOS099</a>
<a href="#">OPA376</a>	<a href="#">SBOS432</a>
<a href="#">OPA2836</a>	<a href="#">SLOS712</a>
<a href="#">TPS3836E18</a>	<a href="#">SLVS292</a>
<a href="#">TPS7A4700</a>	<a href="#">SBVS204</a>
<a href="#">REG71055</a>	<a href="#">SBAS221</a>

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 SPI is a trademark of Motorola Inc.  
 I<sup>2</sup>C is a trademark of NXP Semiconductors.  
 All other trademarks are the property of their respective owners.

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## 1 Overview

The ADS8350EVM-PDK is a platform for evaluation of the ADS8350 analog-to-digital converter (ADC). The evaluation kit combines the ADS8350EVM board with a serial data capture card (SDCC) controller board. The SDCC controller board consists of a TI Sitara embedded microcontroller ([AM3352](#)) and a field programmable gate array (FPGA). The SDCC controller board provides an interface from the EVM to the computer through a universal serial bus (USB) port. The included software communicates with the SDCC controller board platform, and the SDCC board provides the power and digital signals used to communicate with the ADS8350EVM board. These demonstration kits include the ADS8350EVM board, the SDCC controller board, a microSD memory card, and an A-to-micro-B USB cable.

### 1.1 ADS8350EVM Features

- Contains support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI™)
- Onboard 5-V analog supply
- Onboard [REF5025](#) (2.5-V) reference
- Voltage reference buffering with [OPA2350](#)
- Onboard [OPA2836](#) (205-MHz BW, 1-mA quiescent current) ADC operational amplifier input drivers

### 1.2 ADS8350EVM-PDK Features

- USB port for computer interfacing
- Easy-to-use evaluation software for Windows XP®, Windows 7®, Windows 8® operating systems
- Data collection to text files
- Built-in analysis tools including scope, FFT, and histogram displays
- Complete control of board settings

## 2 EVM Analog Interface

The ADS8350 is a dual-channel, simultaneous-sampling ADC that supports pseudo-differential analog inputs. Each channel of the ADS8350 uses a OPA2836 dual operational amplifier to drive the inputs of the ADC. The positive input terminals of each ADC are driven by the OPA836 operational amplifier configured in the inverting configuration. The negative input terminals of each ADC are driven by the OPA836 in the buffer configuration and biased at the 2.5-V, onboard reference voltage ( $+V_{ref}$ ). The ADS8350EVM is designed for easy interfacing to multiple analog sources. SMA connectors allow the EVM to have input signals connected through coaxial cables. In addition, header connectors JP1 and JP2 provide a convenient way to connect input signals.

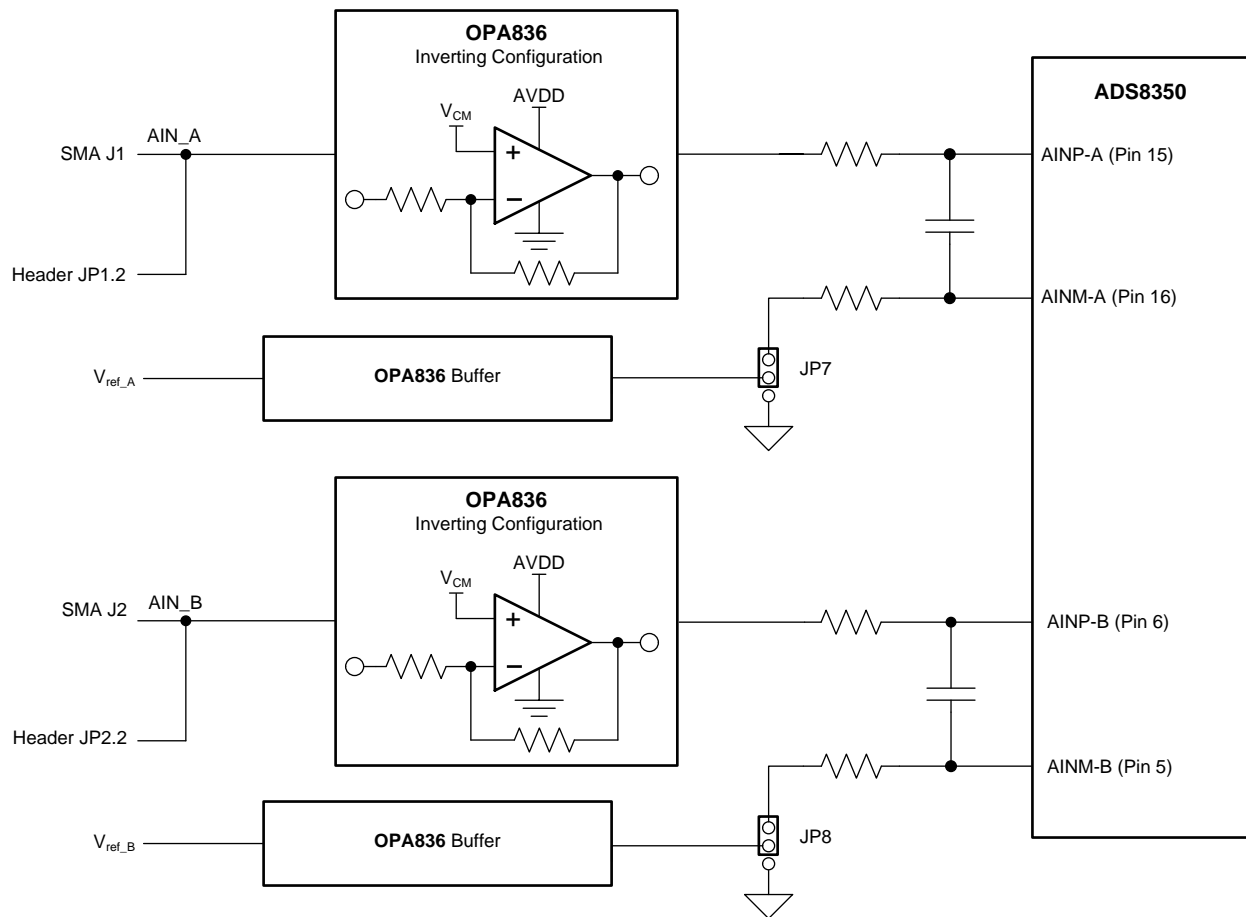

**Figure 1. ADS8350EVM Analog Interface Input Connections**

Table 1 summarizes the JP1 and JP2 analog interface connectors.

**Table 1. JP1 and JP2: Analog Interface Connections**

Terminal Number	Signal	Description
JP1.2	AIN_A	Channel A inverted input. The signal is routed through an OPA836 in the inverting configuration.
JP2.2	AIN_B	Channel B inverted input. The signal is routed through an OPA836 in the inverting configuration.

Table 2 lists the SMA analog inputs.

**Table 2. SMA Analog Interface Connections**

Terminal Number	Signal	Description
J1	AIN_A	Channel A inverted input. The signal is routed through an OPA836 in the inverting configuration.
J2	AIN_B	Channel B inverted input. The signal is routed through an OPA836 in the inverting configuration.

## 2.1 Bipolar Input Signal Configuration

When jumpers JP9 and JP10 are closed, the inverting amplifier positive input is biased with +1.25 V. This bias voltage is created by dividing the ADS8350EVM 2.5-V onboard reference by two. The bias voltage at the input results in a 2.5-V offset at the amplifier output. In this configuration, apply a bipolar input signal with 0-V common-mode voltage.

To keep the OPA836 distortion as low as possible, the input signal swing is limited from -2.3 V to +2.3 V, as shown in Figure 2.

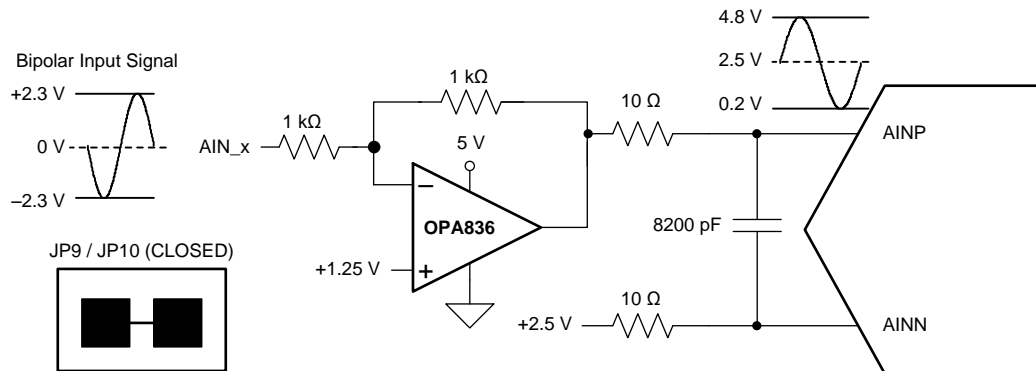


Figure 2. Bipolar Input Signal Configuration

## 2.2 Unipolar Input Signal Configuration

When jumpers JP9 and JP10 are open, the inverting amplifier positive input is biased with +2.5 V. This bias voltage is created using the ADS8350EVM 2.5-V onboard reference. In this configuration, apply a unipolar input signal with 2.5-V common-mode voltage. To keep the OPA836 distortion as low as possible, the input signal swing is limited from +0.2 V to +4.8 V, as shown in Figure 3.

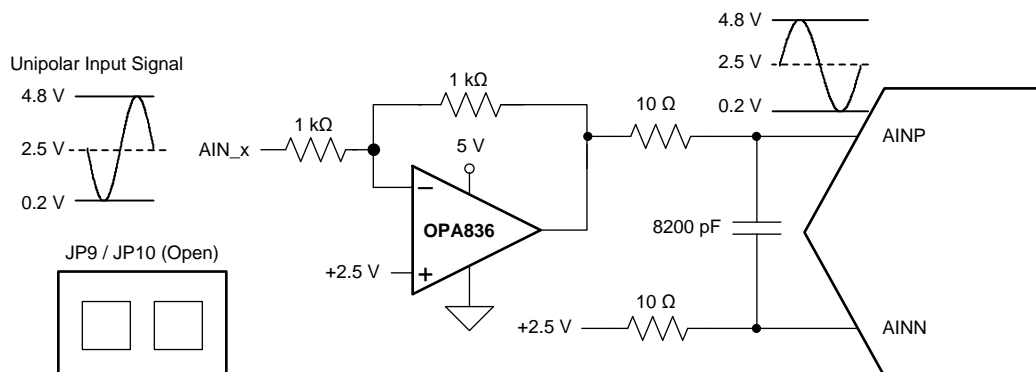
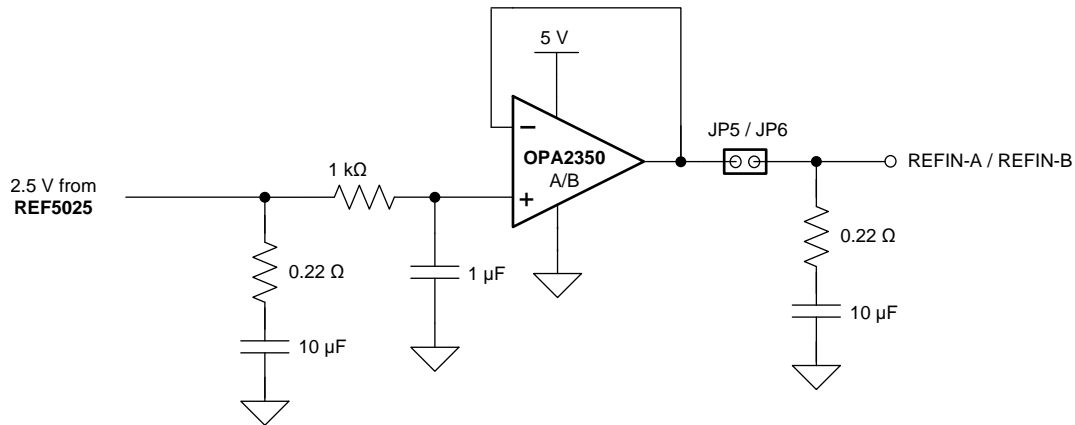


Figure 3. Unipolar Input Signal Configuration

### 2.3 ADS8350EVM Onboard Reference

The ADS8350 dual, simultaneous ADC operates with reference voltages  $V_{ref\_A}$  and  $V_{ref\_B}$  present on pins REFIN\_A and REFIN\_B, respectively. The ADS8350EVM provides an onboard 2.5-V reference source, REF5025 (U5), buffered with a dual OPA2350 amplifier and routed through jumpers JP5 and JP6. By default, the EVM is set up with jumpers JP5 and JP6 installed, as shown in Figure 4.



**Figure 4. REFIN\_A and REFIN\_B Reference Connections**

### 3 Digital Interface

Socket strip connector J6 provides the digital I/O connections between the ADS8350EVM board and the SDCC board.

Table 3 summarizes the pinout for connector J6.

**Table 3. Connector J6 Pinout**

Terminal Number	Signal	Description
J6.2, J6.10, J6.15, J6.16, J6.18	GND	Ground connections
J6.4	EVM PRESENT	EVM present, active low
J6.11, J6.12	I <sup>2</sup> C™ bus	I <sup>2</sup> C bus; used only used to program the U7 EEPROM on the EVM board
J6.13	DVDD	3.3-V digital supply from SDCC controller board
J6.34	CS	Chip select, active low
J6.36	SCLK	Serial interface clock
J6.38	SDI	Serial data input
J6.40	SDO_A	Serial data output for channel A
J6.42	SDO_B	Serial data output for channel B

#### 3.1 Serial Peripheral Interface (SPI)

The ADS8350 digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs), and FPGAs easy. The ADS8350EVM offers 47-Ω resistors between the SPI signals and connector J6 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

#### 3.2 I<sup>2</sup>C Bus for Onboard EEPROM

The ADS8350EVM has an I<sup>2</sup>C bus to communicate with the onboard EEPROM that records the board name and assembly date. It is not used in any form by the ADS8350 converter.

## 4 Power Supplies

The analog portion of the ADS8350EVM-PDK requires a 5-V supply. The ADS8350EVM-PDK is configured at the factory using the onboard regulated analog 5-V supply (+VA); and an onboard 3.3-V digital supply. Alternatively, set the AVDD analog supply voltage by connecting an external power source through two-terminal connector J5. [Table 4](#) lists the configuration details for P3.

**Table 4. Power-Supply Jumpers**

Terminal Number	Position	Function
JP12	Shunt 2-3 (default)	Onboard 5-V AVDD analog supply selected
	Shunt 1-2	External 5-V AVDD connected through two-terminal block J5
JP11	Open (default)	Open sets onboard AVDD supply to 5 V
	Closed	Closed sets onboard AVDD supply to 5.2 V

### CAUTION

The external AVDD supply applied to external two-terminal connector J5 must not exceed 5.5 V or device damage may occur. The external AVDD supply must be in the range of 5.0 V to 5.5 V for proper ADS8350EVM operation.



## 5 ADS8350EVM-PDK Initial Setup

This section presents the steps required to set up the ADS8350EVM-PDK kit before operation.

### 5.1 Default Jumper Settings

A silkscreen plot detailing the default jumper settings is shown in Figure 5. Table 5 explains the configuration for these jumpers.

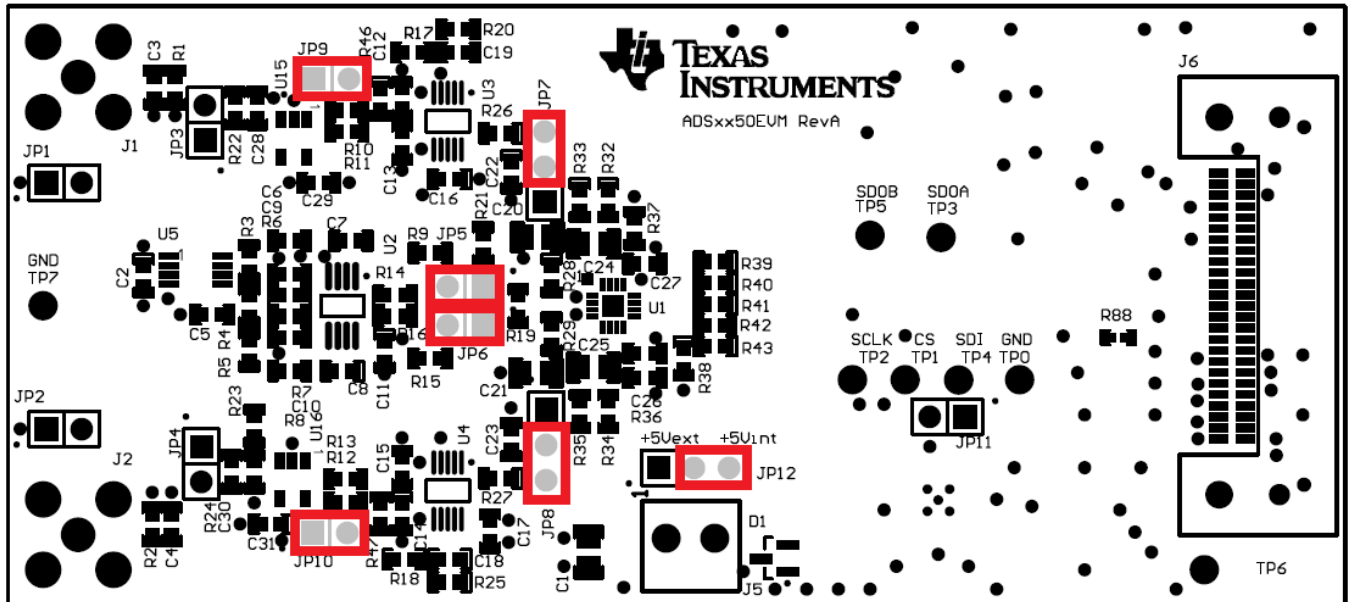


Figure 5. ADS8350EVM Default Jumper Settings

Table 5. Default Jumper Configuration

Terminal Number	Default Position	Switch Description
JP1	Open	JP1.2 header connector to inverted channel A input
JP2	Open	JP1.2 header connector to inverted channel B input
JP3	N/A	JP3 not installed on PCB board
JP4	N/A	JP4 not installed on PCB board
JP5	Closed	Closed to connect onboard 2.5-V reference to REFIN_A
JP6	Closed	Closed to connect onboard 2.5-V reference to REFIN_B
JP7	Short 2-3	Short 2-3 connects AINM_A(-) to 2.5-V
JP8	Short 2-3	Short 2-3 connects AINM_B(-) to 2.5-V
JP9	Closed	Open for channel A unipolar input signals at SMA connector; closed for channel A bipolar input signals at SMA connector.
JP10	Closed	Open for channel B unipolar input signals at SMA connector; closed for channel B bipolar input signals at SMA connector.
JP11	Open	Open sets onboard AVDD to 5 V; closed sets onboard AVDD to 5.2 V.
JP12	Short 2-3	Short 2-3 selects onboard regulated AVDD supply; short 1-2 selects external AVDD through J5.

## 5.2 Software Installation

This section presents the steps required to install the software. [Section 6](#) explains how to operate the software to acquire data.

---

**NOTE:** Ensure the microSD memory card included in the kit is installed in the microSD socket (P6) on the back of the SDCC board before connecting the EVM to the PC. Otherwise, as a result of improper boot up, Windows cannot recognize the ADS8350EVM-PDK as a connected device.

---

Complete the following steps to install the software:

- Step 1. Install the microSD memory card on the SDCC controller board.
- Step 2. Verify jumpers are in the factory-default position and connect the hardware.
- Step 3. Install the ADS8350EVM-PDK software.
- Step 4. Complete the SDCC device driver installation.

Each task is described in the following subsections.

### 5.2.1 Install the microSD Memory Card on the SDCC Controller Board

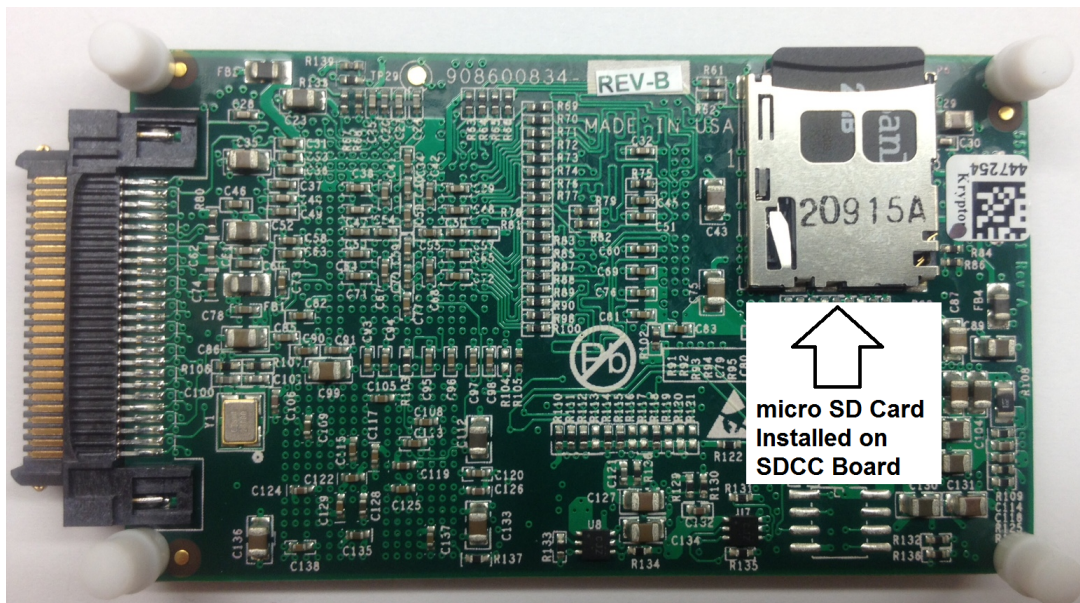
The ADS8350EVM-PDK includes a microSD memory card that contains the EVM software and SDCC controller board firmware required for the EVM operation.

---

**NOTE:** Ensure the microSD memory card that contains the software is installed in the microSD socket (P6) on the back of the SDCC board.

[Figure 6](#) shows the bottom view of the SDCC controller board with the microSD card installed.

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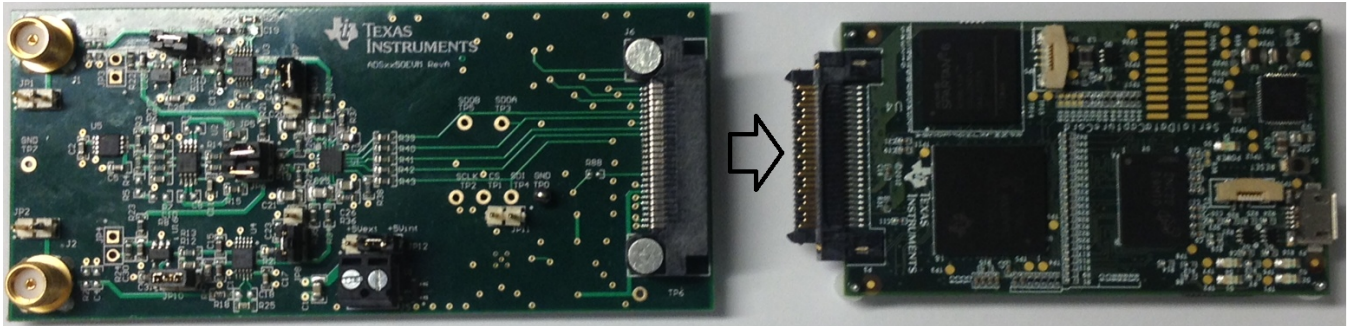
**Figure 6. Bottom View of SDCC Board with microSD Memory Card Installed**

The microSD memory card is formatted at the factory with the necessary firmware files for the SDCC controller board to boot properly. In addition to the SDCC firmware files (app and MLO files), the microSD memory card contains the ADS8350EVM-PDK software installation files inside the *ADS8350 EVM V#.#.#* folder. *<V#.#.#>* refers to the installation software version number, and increments with software installer releases.

### 5.2.2 Verify Jumpers are in the Factory-Default Position and Connect the Hardware

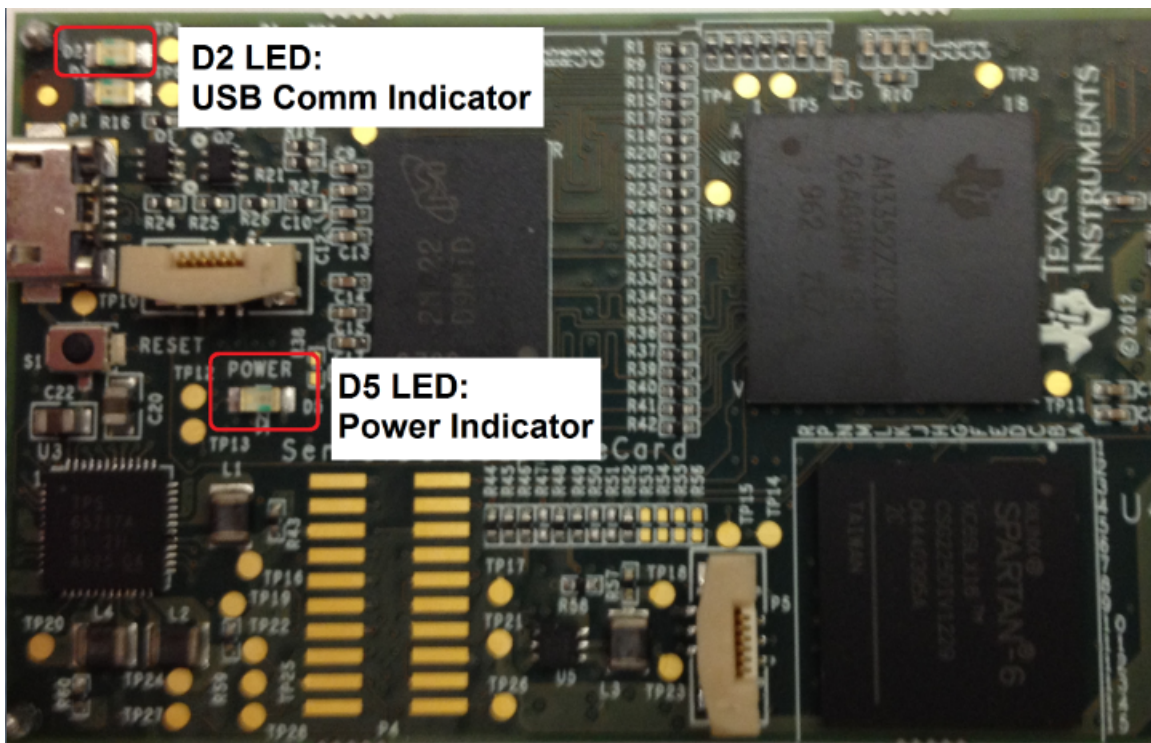
The ADS8350EVM-PDK includes both the ADS8350EVM and the SDCC controller board; however, the devices are shipped unconnected. Follow these steps to verify that ADS8350EVM-PDK kit is configured and connected properly.

- Step 1. Verify the microSD card is installed on the back of the SDCC board, as shown in [Figure 6](#).
- Step 2. Verify the ADS8350EVM jumpers are configured as shown in [Figure 5](#).
- Step 3. Connect the ADS8350EVM board to the SDCC controller board as [Figure 7](#) illustrates.



**Figure 7. Connecting ADS8350EVM Board to SDCC Controller Board**

- Step 4. Connect the SDCC controller board to the PC through the micro USB cable.
- Step 5. Verify that the LED D5 Power Good indicator is illuminated. Wait approximately ten seconds and verify that diode D2 blinks, indicating that USB communication with the host PC is functioning properly. [Figure 8](#) shows the location of the LED indicators in the SDCC controller board.



**Figure 8. LED Indicators on the SDCC Board**

### 5.2.3 Install the ADS8350EVM-PDK Software

The ADS8350 EVM V#.#. # software must be installed on the PC. This software supports the ADS8350EVM-PDK. The user must have administrator privileges to install the EVM software. The following steps list the directions to install the software.

1. Open Windows explorer and find the microSD memory card in the browser as a storage device.
2. Navigate to the ... \ADS8350 EVM Vx.x.\Volume1 folder.
3. Run the installer by double-clicking the file *setup.exe*. This action installs the EVM GUI software and the required and SDCC device driver components.
4. After the installer begins, a welcome screen displays. Click *Next* to continue.
5. A prompt appears with the destination directory; select the default directory under: ... \Program Files(x86)\Texas Instruments\ADS8350evm\.

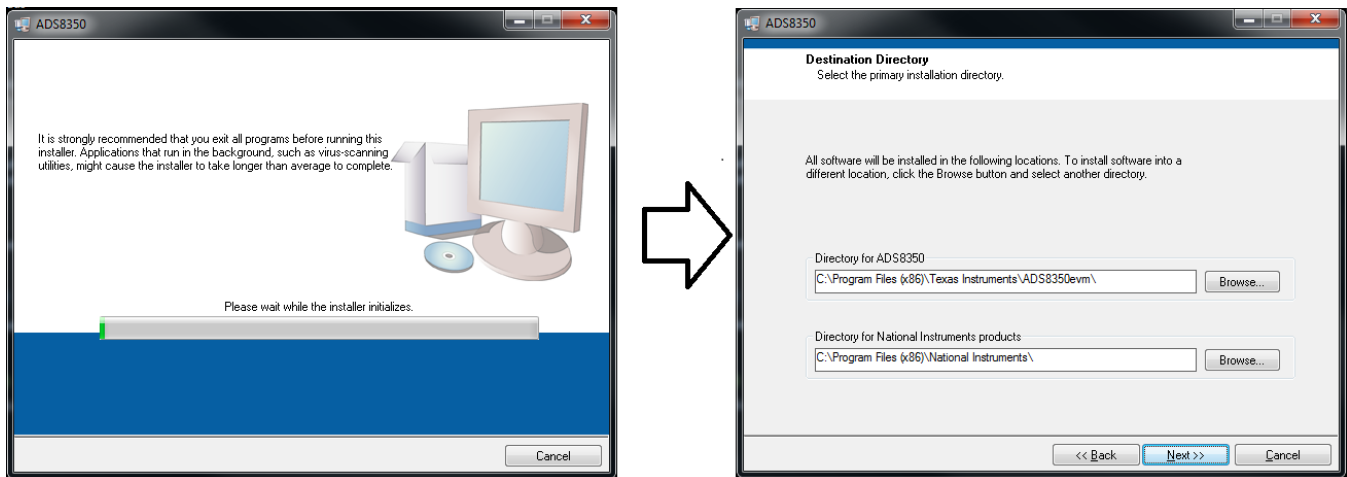


Figure 9. Welcome Screen and Destination Directory Screens

6. One or more software license agreements appear. Select *I Accept the License Agreement* and click *Next*.
7. The *Start Installation* screen appears. Click *Next*.

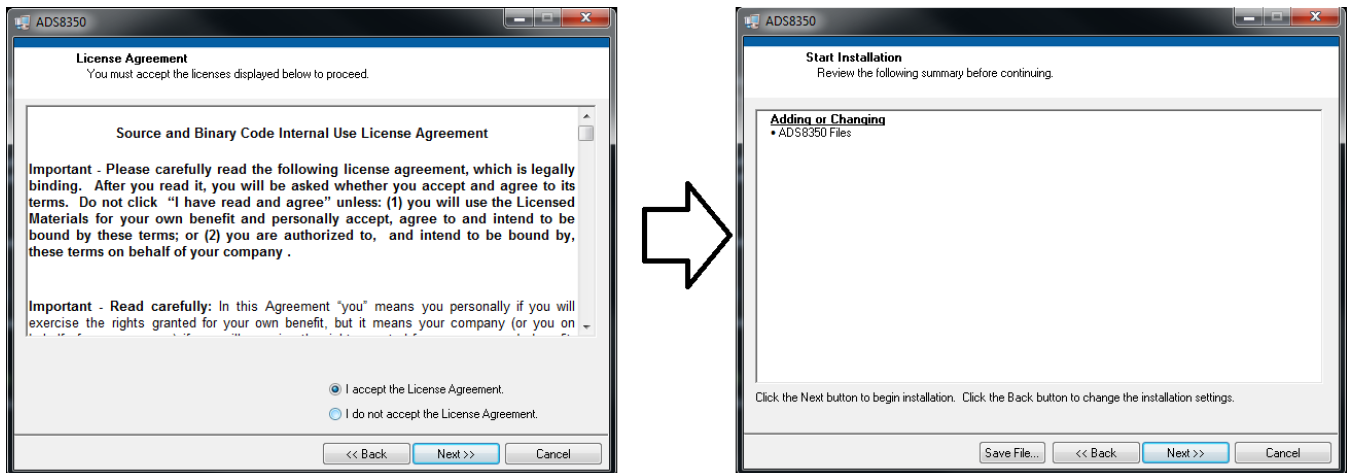


Figure 10. License Agreement and Start Installation Screens

8. A progress bar appears; this step takes a few minutes.
9. The progress bar is followed by an installation complete notice.

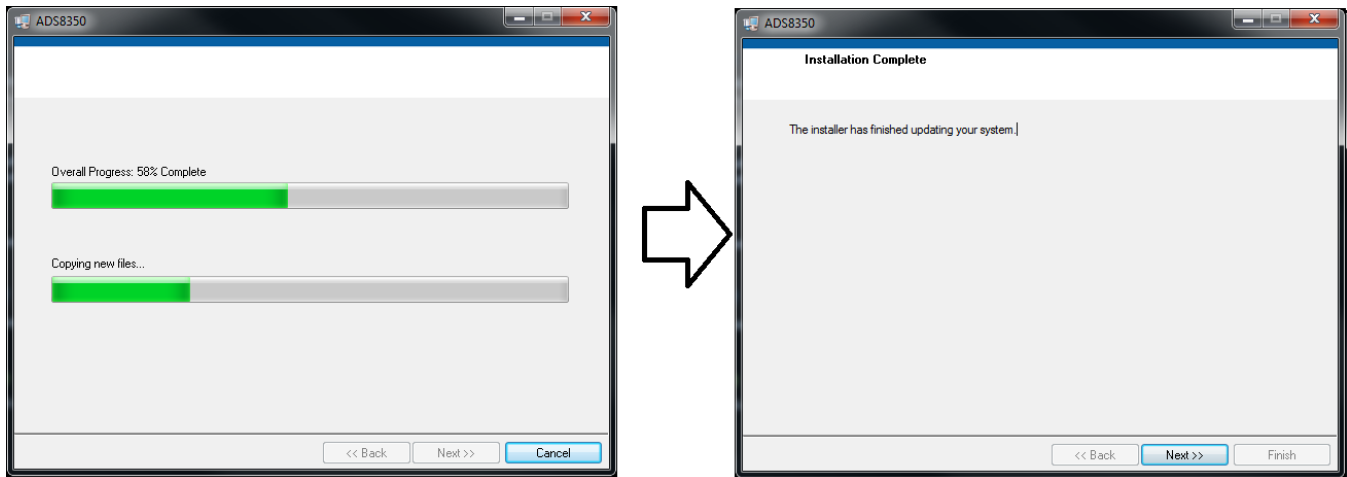


Figure 11. Progress Bar and Installation Complete Screens

#### 5.2.4 Complete the SDCC Device Driver Installation

During installation of the SDCC device driver, a prompt may appear with the Windows security message shown in Figure 12. Select *Install this driver software anyway* to install the driver required for proper operation of the software. The drivers contained within the installers are safe for installation to your system.

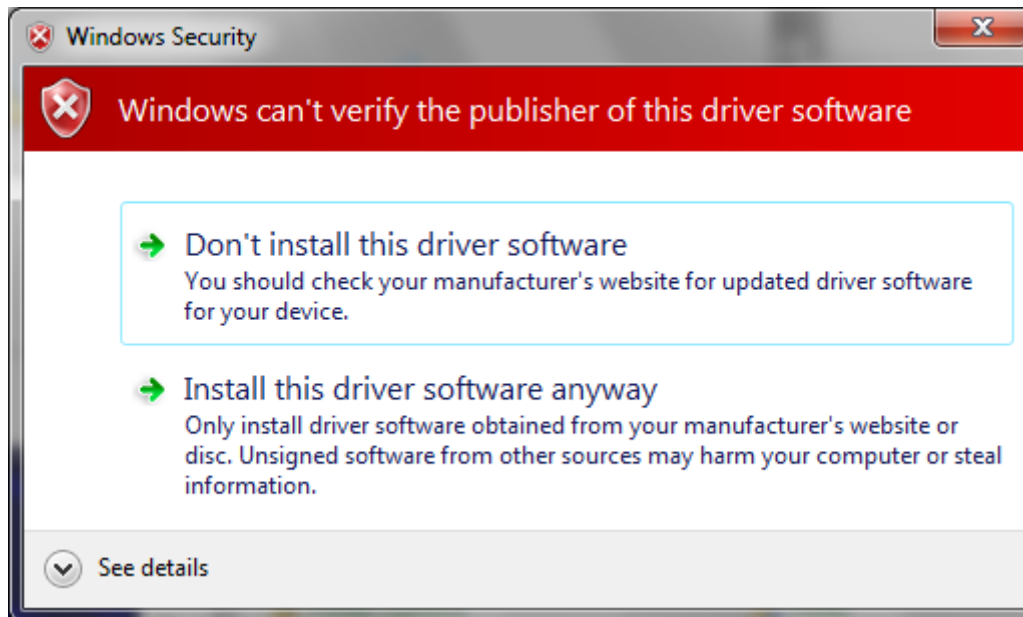


Figure 12. Windows 7 Driver Installation Warning

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**NOTE:** Driver installation prompts do not appear if the SDCC device driver has been installed on your system previously.

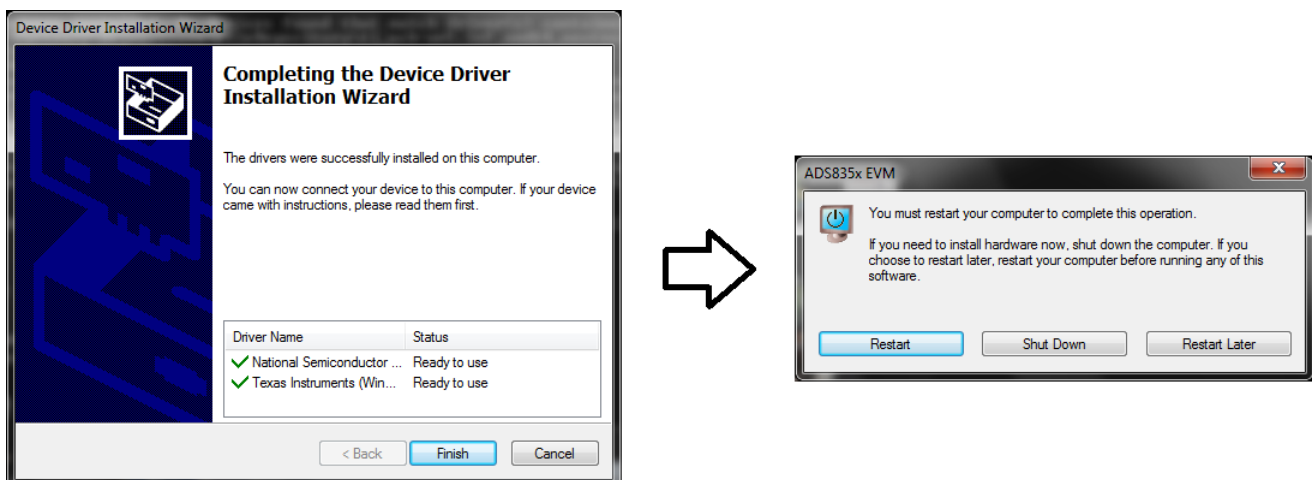
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The following steps describe how to install the SDCC device driver.

- Step 1. Immediately after the ADS8350 EVM software installation is complete, prompts appear to install the SDCC device driver, as shown in [Figure 13](#) and [Figure 14](#)
- Step 2. A computer restart may be required to finish the software installation. If prompted, restart the PC to complete the installation.



**Figure 13. SDCC Device Driver Installation**



**Figure 14. SDCC Device Driver Completion**

## 6 ADS8350EVM-PDK Kit Operation

This section describes how to use ADS8350EVM-PDK and the ADS8350EVM software to configure the EVM and acquire data.

### 6.1 About the SDCC Controller Board

The SDCC controller board provides the USB interface between the PC and the ADS8350EVM. The controller board is designed around the AM335x processor, a USB 2.0 high-speed capability, 32-bit ARM core. The SDCC controller board incorporates an onboard FPGA subsystem and 256MB of onboard DDR SRAM memory.

The SDCC controller board is not sold as a development board, and it is not available separately. TI cannot offer support for the SDCC controller board except as part of this EVM kit.

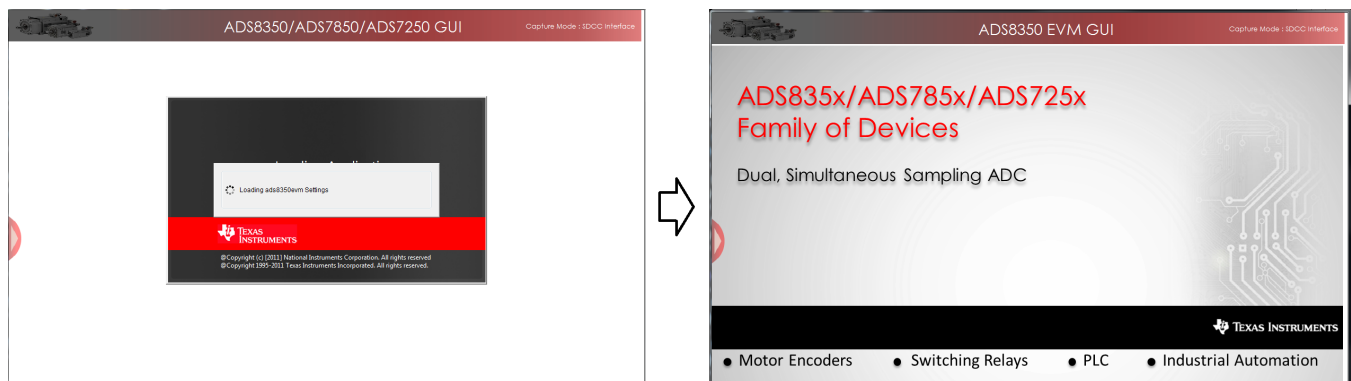
### 6.2 Loading the ADS8350EVM-PDK Software

The ADS8350 EVM software provides control over the settings of the ADS8350. Adjust the ADS8350EVM settings when the EVM is not acquiring data. During acquisition, all controls are disabled and settings cannot be changed.

Settings on the ADS8350EVM correspond to settings described in the [ADS8350 product data sheet](http://www.ti.com) (available for download at <http://www.ti.com>); see the product data sheet for details.

To load the *ADS8350 EVM* software, follow these steps:

- Step 1. Make sure the EVM kit is configured and powered up as explained in [Section 5](#).
- Step 2. Start the ADS8350 EVM software. Go to *Start* → *All Programs* → *Texas Instruments* → *ADS8350 EVM* and click *ADS8350 EVM* to run the software.
- Step 3. Verify that the software detects the ADS8350EVM. The GUI identifies the EVM hardware that is connected to the controller board and displays *Loading the ADS8350evm Settings*. After the settings are loaded, *ADS8350EVM GUI* displays at the top of the GUI screen, as shown in [Figure 15](#).

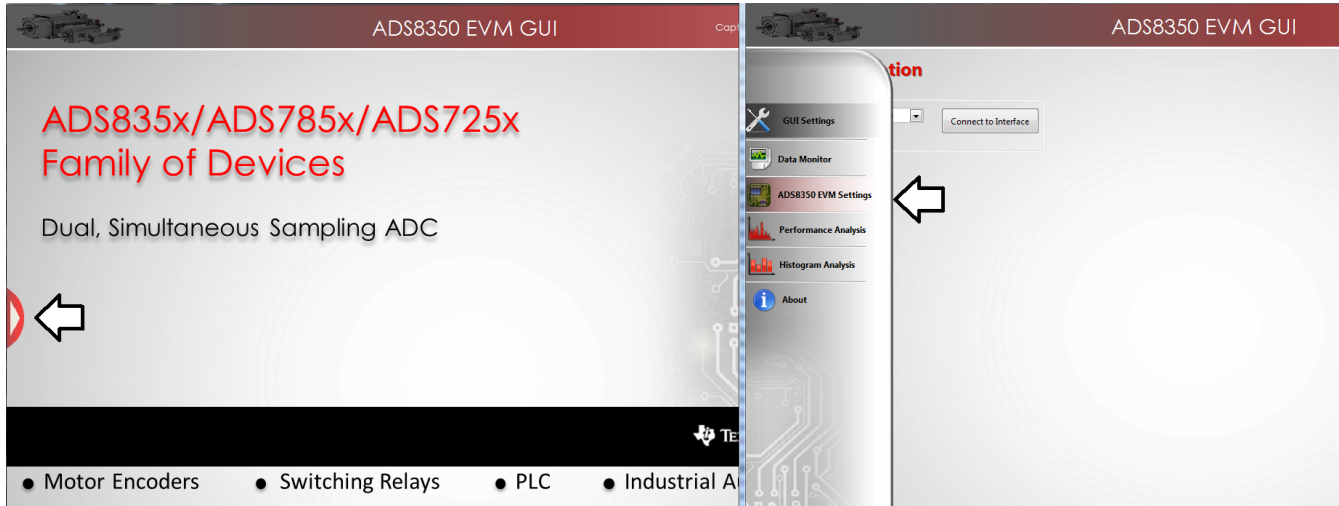


**Figure 15. GUI Display Prompt**

### 6.3 ADS8350EVM Settings

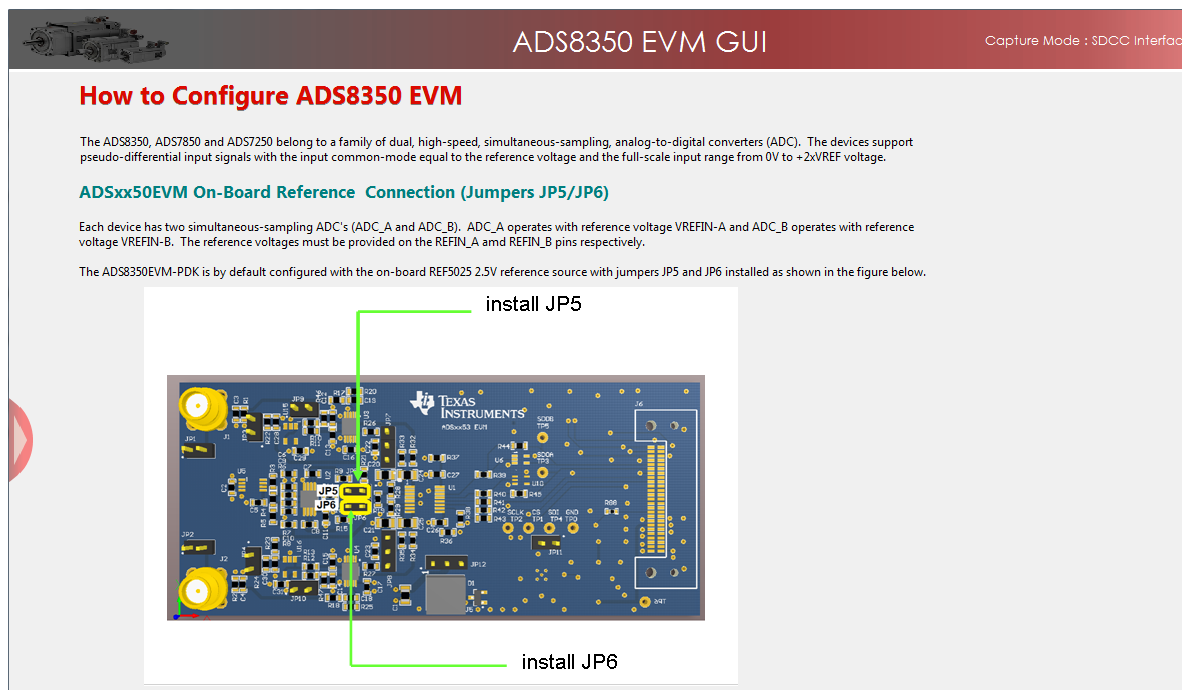
Configure the ADS8350EVM for evaluation. The *ADS8350EVM Settings* page explains in detail the analog input connections available on the evaluation board. In order to configure the EVM analog input connections, follow these steps:

1. Load the *ADS8350EVM Settings* page in the GUI. Hover the cursor over the red arrow at the left-center side of the GUI screen; a menu with different GUI pages appears. Click on *ADS8350 EVM Settings*, as shown in [Figure 16](#).



**Figure 16. Open the ADS8350EVM Settings Page**

2. The ADS8350 dual, simultaneous ADC requires reference voltages  $V_{ref\_A}$  and  $V_{ref\_B}$  present on pins REFIN-A and REFIN\_B, respectively. The ADS8350EVM provides an onboard 2.5-V reference source, REF5025 (U5), buffered with a dual OPA2350 amplifier and routed through jumpers JP5 and JP6. Therefore, jumpers JP5 and JP6 must be installed. [Figure 17](#) shows the reference connections as described on the *ADS8350EVM Settings* page of the GUI.



**Figure 17. ADS8350EVM Settings Page**



3. Scroll down in the *ADS8350EVM Settings* page and find the *ADS8350 Analog Inputs* connections descriptions on the GUI. The ADS8350EVM can be driven with a signal generator producing a bipolar source signal centered on GND or a unipolar signal centered at  $+V_{ref} / 2$ . Jumpers JP9 and JP10 are installed when supporting a bipolar signal centered at GND. Jumpers JP9 and JP10 must be removed when supporting a unipolar signal source signal centered at 2.5-V. [Figure 18](#) shows jumpers JP9 and JP10 on the *ADS8350EVM Settings* page of the GUI.

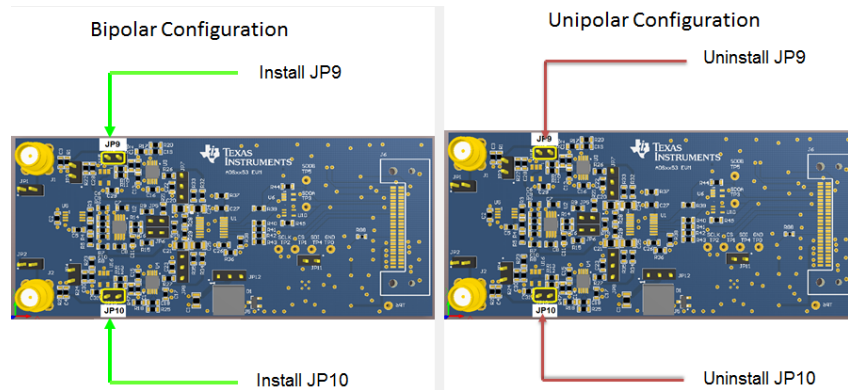


Figure 18. Bipolar or Unipolar Signal Jumper Settings Description on the GUI

#### 6.4 Capturing Data with the ADS8350EVM-PDK

Access the *Data Monitor* page in the GUI to monitor data acquired by the ADS8350. This GUI page displays the acquired data versus time. To access the *Data Monitor* page, hover the cursor over the red arrow at the left center side of the GUI screen; a menu with different GUI pages appear. Click on the *Data Monitor* option in the menu, as shown in [Figure 19](#)

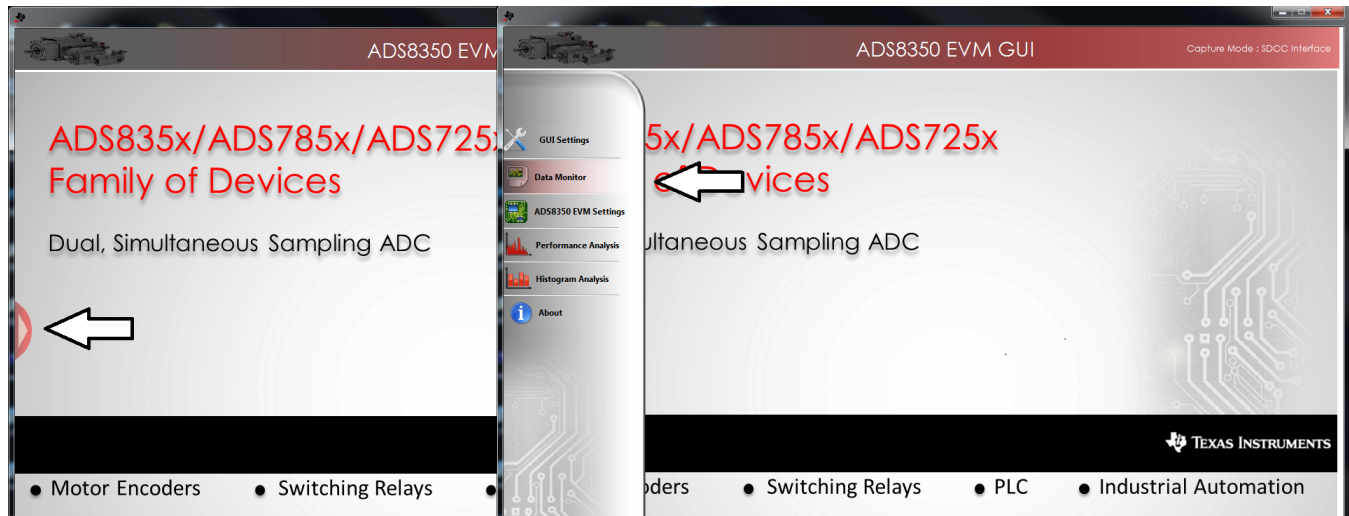


Figure 19. Open the *Data Monitor* page on the GUI

Figure 20 shows the *Data Monitor* page of the EVM GUI. Configure the device sampling rate and capture settings by using the *Capture Settings* portion of the *Data Monitor* page. The change in configuration settings are executed immediately after pressing the *Configure Device* button. The following list describes the different options available on the *Data Monitor* page.

**# of Samples**— This option is used to select the number of samples captured in a block.

The number of samples captured in a block are contiguous. The drop-down menu is used to select a data block in the range of 1024 samples to 1,048,576 samples per channel. This control provides a drop-down list for values restricted to  $2^n$ , where  $n$  is an integer.

**SCLK**— This control sets the clock frequency used by the SPI interface to capture data.

By configuring the SCLK frequency, the data rate of the ADS8350 is configured. The ADS8351EVM-PDK software supports SCLK frequencies of 24 MHz, 20 MHz, and 16.2 MHz. These SCLK frequencies correspond to data rates of 750 kSPS, 625 kSPS, and 506.2 kSPS respectively.

**Device Status**— This panel shows the current clock frequency and data rate of the ADS8350.

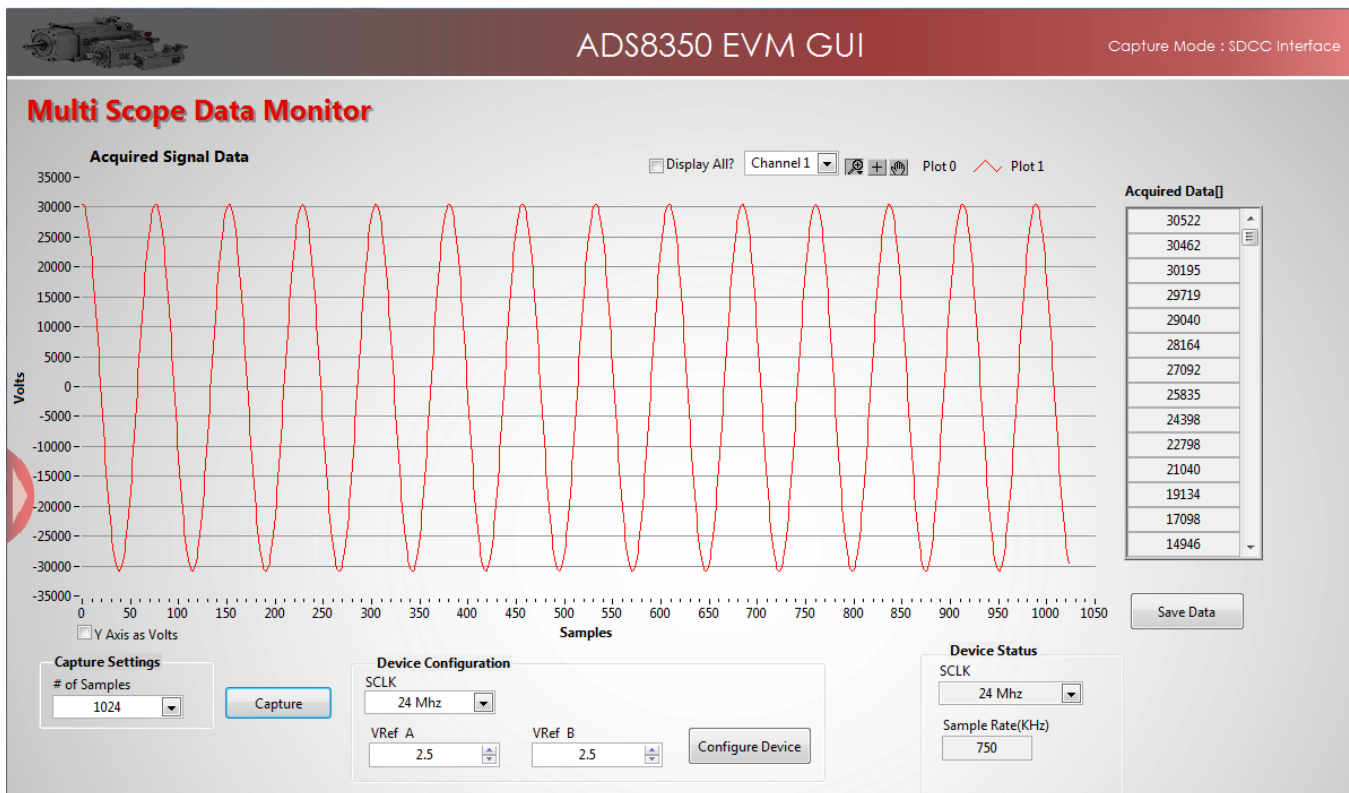


Figure 20. Data Monitor Page

### 6.4.1 Data Collection to Text Files

The *Data Monitor* page of the GUI allows data to be saved in a tab-delimited text file format that can be imported into Excel®, or other spreadsheet software tools. The text file contains the raw ADC data of both channel A and channel B in decimal data format. Information such as the device name, date and time, the sampling frequency, and number of samples of the data record are also stored. In order to save any data captured by the EVM, click on the *Save Data* button and specify the file path and file name of the data file, as shown in [Figure 21](#).

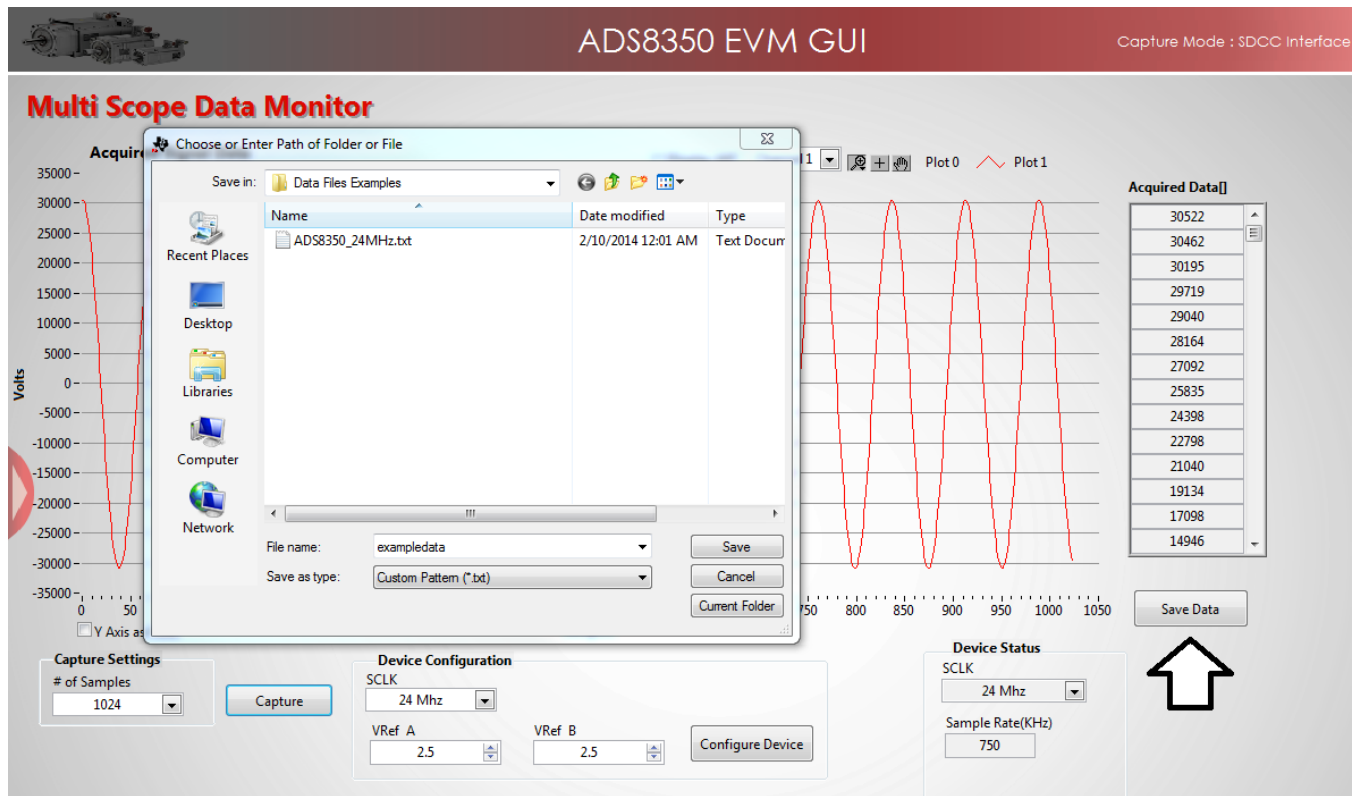


Figure 21. Saving Data to a Text File

### 6.5 FFT Analysis

The *Performance Analysis* page in the GUI performs the fast fourier transform (FFT) of the captured data, and displays the resulting frequency domain plots of channel A and channel B of the ADS8350. This page also calculates key ADC dynamic performance parameters, such as signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and spurious-free dynamic range (SFDR). [Figure 22](#) shows the FFT performance analysis display. The FFT calculated parameters are shown on the right side of the display.

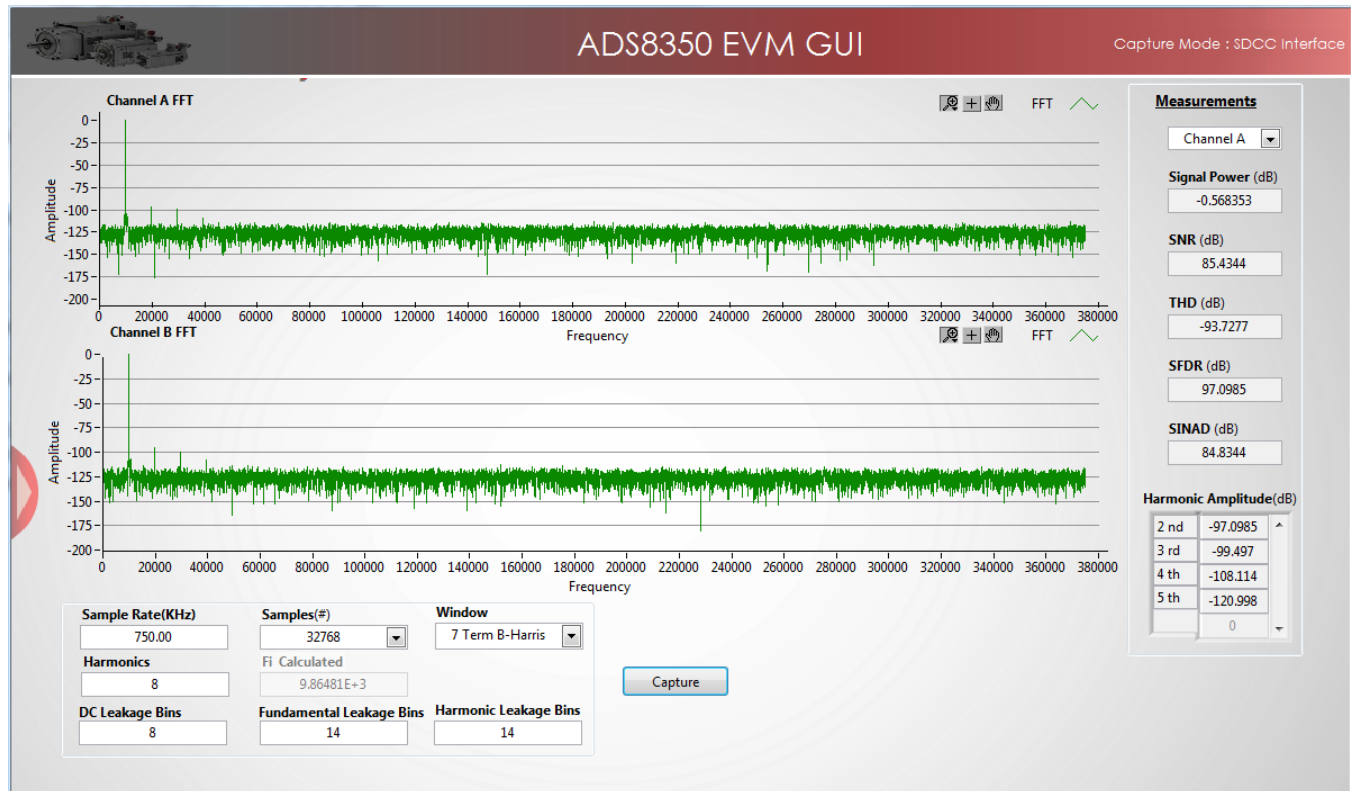


Figure 22. FFT Performance Analysis Page

### 6.5.1 FFT Analysis Settings and Controls

**Sample Rate (kHz)**— This field indicates the sampling frequency of the ADC data (kHz).

**Samples (#)**— The FFT requires a time domain record with a number of samples that is a power of 2. The Samples (#) drop-down menu provides a list of values that satisfy this requirement.

**Fi Calculated**— This field displays the frequency of the largest amplitude input signal computed from the FFT data, typically the fundamental frequency.

**Window**— The window function is a mathematical function that reduces the signal to zero at the end points of the data block.

In applications where coherent sampling cannot be achieved, a window-weighting function can be applied to the data to minimize spectral leakage. The following options are available:

- None (no window weighting function applied; use for coherent data)
- Hanning
- Hamming
- Blackman-Harris
- Exact Blackman
- Blackman
- Flat Top
- 4-Term Blackman-Harris
- 7-Term Blackman-Harris
- Low Sidelobe

For a more thorough discussion of windowing, refer to IEEE1241-2000.

**Harmonics**— This field sets the number of harmonics that are included in the FFT performance calculations.

**Leakage Bins**— These fields provide for the removal of the unwanted frequency bins that may be the result of noncoherent data sampling.

Set the *Fundamental Leakage Bins* and *Harmonic Leakage Bins* fields to the number of adjacent bins on either side of the fundamental or harmonic frequencies to include the main frequency power. The *DC Leakage Bins* field allows the number of frequency bins that are a result of the dc portion of the measurement to be excluded from the calculations.

## 6.6 Histogram Analysis

Histogram testing is commonly used when characterizing ADCs. A histogram is merely a count of the number of times a code has occurred in a particular data set. The *Histogram Analysis* page of the GUI creates a histogram of the data of the acquired data set and displays it. Figure 23 shows the *Histogram Analysis* page of the GUI.

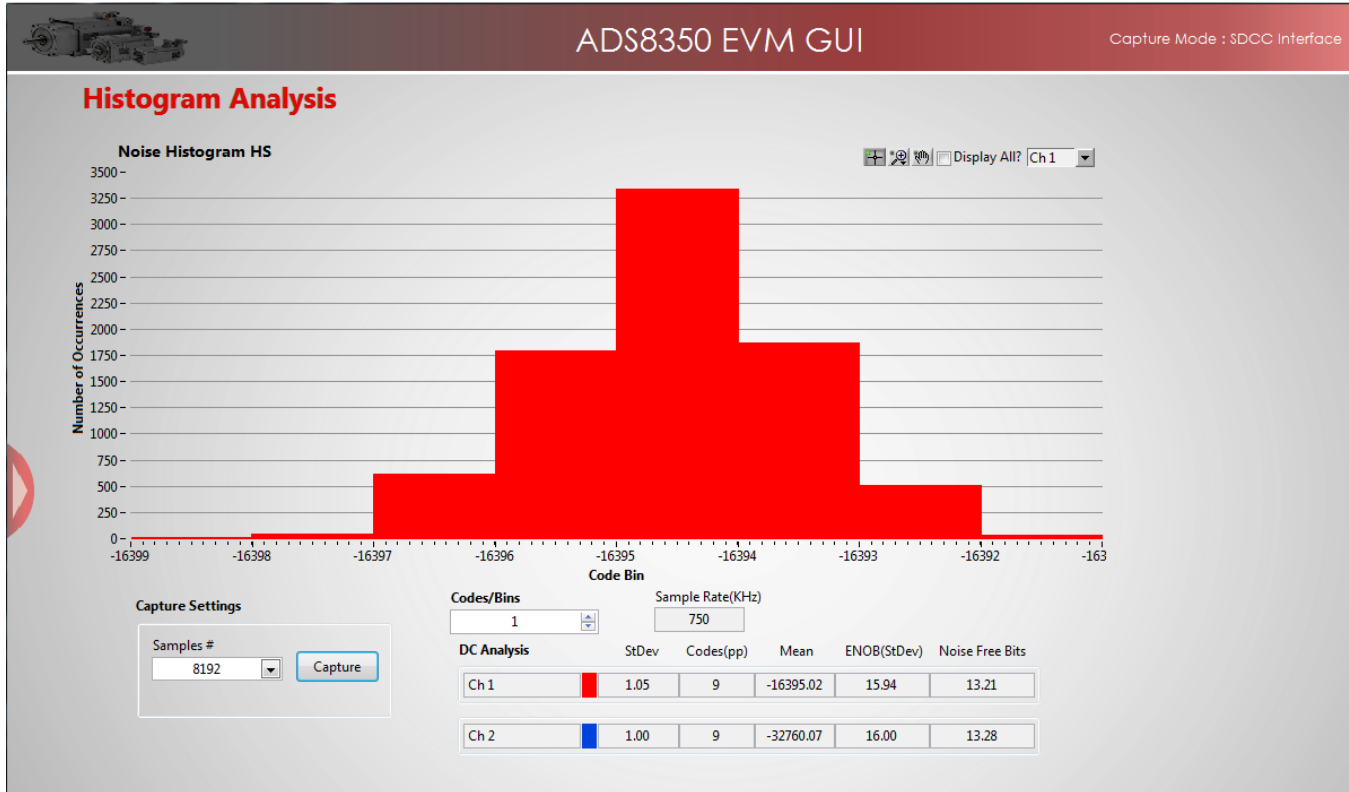


Figure 23. Histogram Analysis Page

The *DC Analysis* table shown in Figure 23 displays several parameters of the captured data set:

- The *StDev* column displays the standard deviation of the data set. This value is equivalent to the RMS noise of the signal when analyzing a dc data set.
- The *Codes(pp)* column shows the peak-to-peak spread of the codes in the data set; for a dc data set, this range would be the peak-to-peak noise.
- The *Mean* column displays the average value of the data set.
- The *ENOB(StDev)* column displays the effective number of bits of the converter, as calculated from the standard deviation or RMS noise.
- The *Noise Free Bits* column displays the effective bits of the converter when calculated using the peak-to-peak noise.

## 6.7 Troubleshooting

If the ADS8350EVM software stops responding while the ADS8350EVM-PDK is connected, unplug the USB cable from the EVM, unload the ADS8350EVM-PDK software, reconnect the ADS8350EVM-PDK to the PC, and reload the ADS8350EVM software.

When initially setting up the ADS8350 GUI, the software detects the EVM hardware, and loads the appropriate hardware settings. If the EVM hardware is not detected, the GUI defaults to the *Capture Mode: Software Debug* mode of operation using a preloaded captured data file for demonstration purposes.

While using the EVM-PDK hardware for data acquisition, keep the GUI in the *Capture Mode: SDCC interface* mode of operation. The GUI indicates the selected mode of operation on the top-right corner of the GUI display. In order to select the SDCC interface mode of operation, navigate to the *GUI Settings* page and select the *SDCC Interface* option on the *Capture Mode* drop-down menu, as shown in [Figure 24](#) and [Figure 25](#).



Figure 24. Open the *GUI Settings* page

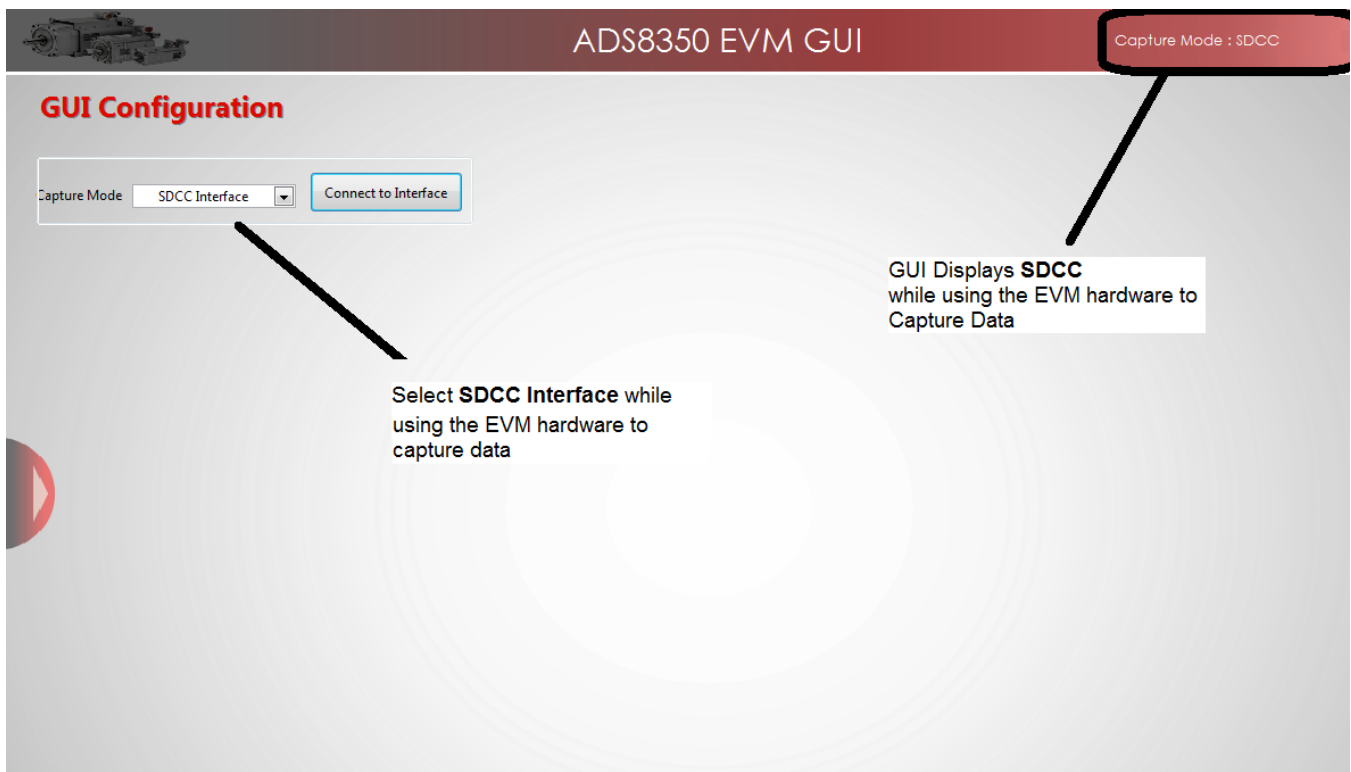


Figure 25. Set Capture Mode to *SDCC Interface* While Using the EVM Hardware

## 7 Bill of Materials, PCB Layout, and Schematics

Table 6 lists the bill of materials. Section 7.2 shows the PCB layout for the ADS8350EVM. The schematics for the ADS8350EVM are appended to the end of this user's guide.

### 7.1 Bill of Materials

**NOTE:** All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant.

**Table 6. ADS8350EVM Bill of Materials**

Item No.	Qty	Ref Des	Description	Vendor	Part Number
1	11	C1, C20, C21, C39, C41, C42, C43, C44, C45, C46, C54	CAP, CERM, 10uF, 16V, +/-10%, X5R, 0805	Murata	GRM21BR61C106KE15L
2	11	C2, C5, C9, C10, C12, C13, C14, C15, C28, C30, C40	CAP, CERM, 1uF, 6.3V, +/-10%, X7R, 0603	Murata	GRM188R70J105KA01D
3	0	C3, C4, C7, C8, C18, C19, C22, C23	Not Install	Not Install	Not Install
4	4	C6, C26, C27, C51	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	TDK	C1608X5R0J106M
5	8	C11, C16, C17, C29, C31, C48, C52, C53	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A6
6	2	C24, C25	CAP CER 8200PF 50V 5% NP0 0805	TDK	C2012C0G1H822J060AA
7	2	C47, C50	CAP, CERM, 2.2uF, 16V, +/-10%, X5R, 0603	Murata	GRM188R61C225KE15D
8	1	C49	CAP, CERM, 0.22uF, 16V, +/-10%, X5R, 0603	TDK	GRM188R61C224KA88D
9	1	D1	DIODE ZENER 5.9V 250MW SOT23	NXP Semiconductors	PLVA659A.215
10	2	J1, J2	Connector, TH, SMA	TE Connectivity	142-0701-201
11	1	J5	2 Terminal Block 3.5MM 2POS PCB	On Shore Technology Inc	ED555/2DS
12	1	J6	SAMTEC, dual-row, right-angle, female, latching	SAMTEC	ERF8-025-01-L-D-RA-L-TR
13	0	J7	NOT INSTALL: MOLEX Connector for microSD Card	Molex Inc	Not Install (MOLEX 502570-0893)
14	0	JP3, JP4	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	SAMTEC	TSW-102-07-G-S
15	7	JP1, JP2, JP5, JP6, JP9, JP10, JP11	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	SAMTEC	TSW-102-07-G-S
16	3	JP7, JP8, JP12	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	SAMTEC	TSW-103-07-G-S
17	1	R3	RES, 0.22 ohm, 1%, 0.1W, 0603	Panasonic Electronic Components	ERJ-3RQFR22V
18	7	R4, R14, R16, R36, R37, R89, R90	RES, 0 ohm, 5%, 0.1W, 0603	Vishay Dale	CRCW06030000Z0EA
19	2	R6, R7	RES, 100 ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW0603100RFKEA
20	8	R9, R15, R31, R39, R40, R41, R42, R43	RES, 47.0 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0747RL
21	8	R10, R12, R17, R18, R20, R25, R46, R47	RES, 1.00k ohm, 0.1%, 0.1W, 0603	Susumu	RG1608P-102-B-T5
22	2	R11, R13	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW06031K00FKEA
23	4	R21, R22, R23, R24	RES, 20.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060320K0FKEA
24	2	R26, R27	RES, 1.00 ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW06031R00FKEA



**Table 6. ADS8350EVM Bill of Materials (continued)**

Item No.	Qty	Ref Des	Description	Vendor	Part Number
25	2	R28, R29	RES, 0.1 ohm, 1%, 0.1W, 0603	Panasonic Electronic Components	ERJ-3RSFR10V
26	4	R32, R33, R34, R35	RES, 10.0 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0710RL
27	2	R38, R86	RES, 100k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100KJNEA
28	6	R70, R71, R72, R73, R74, R75	RES, 10k ohm, 5%, 0.063W, 0402	Vishay Dale	CRCW040210K0JNED
29	1	R76	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060310K0FKEA
30	2	R80, R84	RES, 0 ohm, 5%, 0.125W, 0805	Vishay Dale	CRCW08050000Z0EA
31	0	R1, R2, R5, R8, R19, R30	Not Install		Not Install
32	0	R83, R87, R88	Not Install		Not Install
33	1	U1	Dual, 750kSPS, 16 BIT Simultaneous Sampling ADC	Texas Instruments	ADS8350IRTE
34	1	U2	High-Speed, Single-Supply, Rail-to-Rail OPA	Texas Instruments	OPA2350EA
35	2	U3, U4	Very Low-Power, Rail-to-Rail Out, Negative Rail In, VFB Op Amp 205MHz	Texas Instruments	OPA2836IDGS
36	1	U5	Low Noise, Low Drift, Precision Voltage Reference	Texas Instruments	REF5025IDGK
37	1	U7	Atmel I2C Compatible (2-Wire) Serial EEPROM	Atmel	AT24C02C-XHM
38	1	U8	36-vA, 1-A, 4.17uVRMS RF LDO Voltage Regulator	Texas Instruments	TPS7A4700RGW
39	1	U9	60mA, 5.5V, Buck/Boost Charge Pump	Texas Instruments	REG71055DDC
40	1	U14	NanoPower Supervisory Circuit	Texas Instruments	TPS3836E18DBVT
41	2	U15, U16	Low Noise, Low Quiescent Current, Precision OPA	Texas Instruments	OPA376AIDBVT
42	7	N/A	Conn Shunt, Pitch 0.100"; Height 0.240" , Gold Plated	SAMTEC	SNT-100-BK-G
43	1	TP0	TEST POINT PC MINI .040"D BLACK	Keystone Electronics	5001
44	0	TP1, TP2, TP3, TP4, TP5, TP6	Not Install	Keystone Electronics	Not Install
45	2	N/A	BUMPON CYLINDRICAL .375X.135 BLK	3M	SJ61A8

## 7.2 PCB Layout

Figure 26 through Figure 29 show the PCB layouts for the ADS8350EVM.

**NOTE:** Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS8350EVM PCBs.

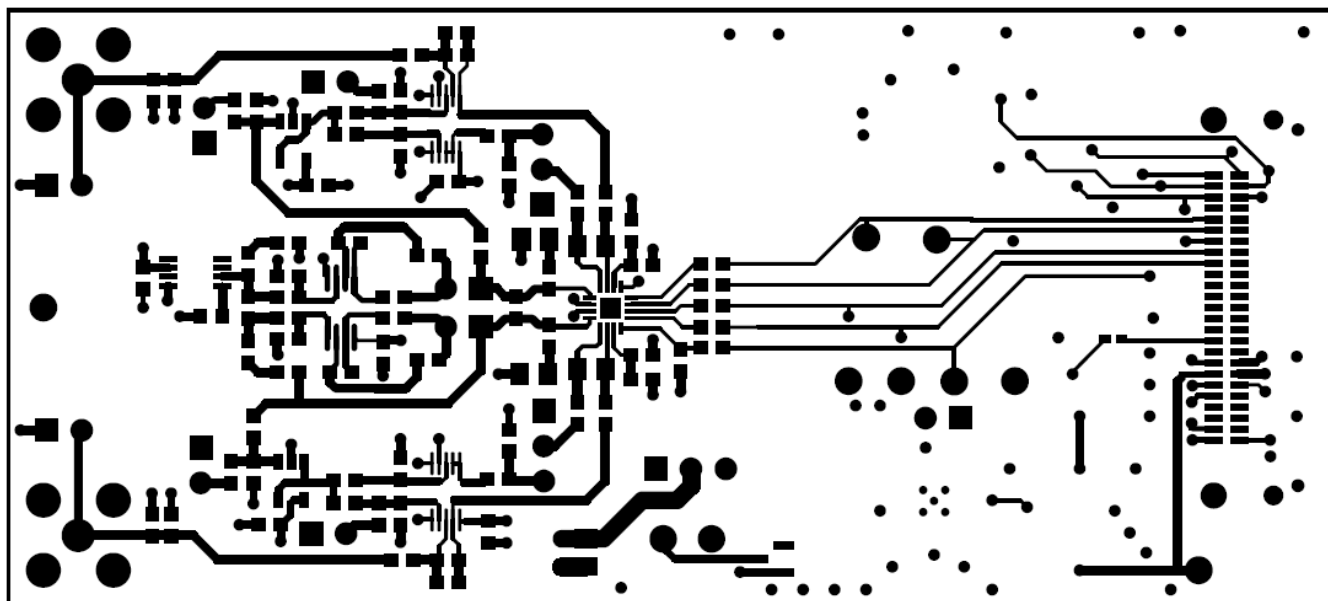


Figure 26. ADS8350EVM PCB: Top Layer

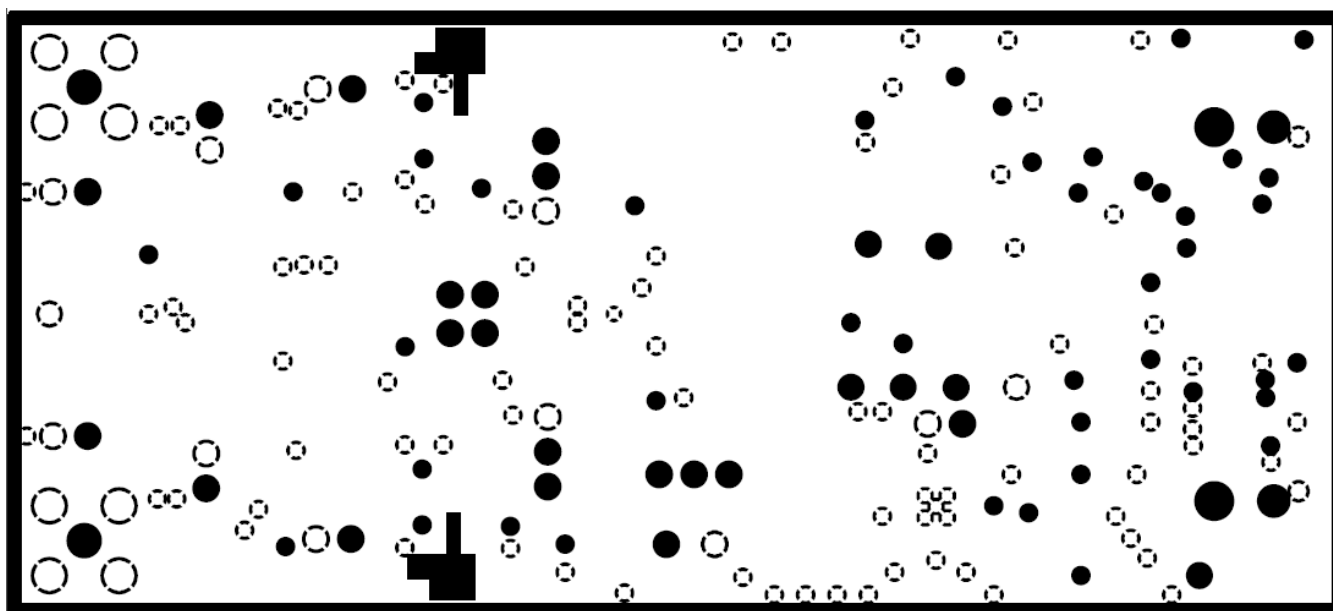


Figure 27. ADS8350EVM PCB: Ground Layer

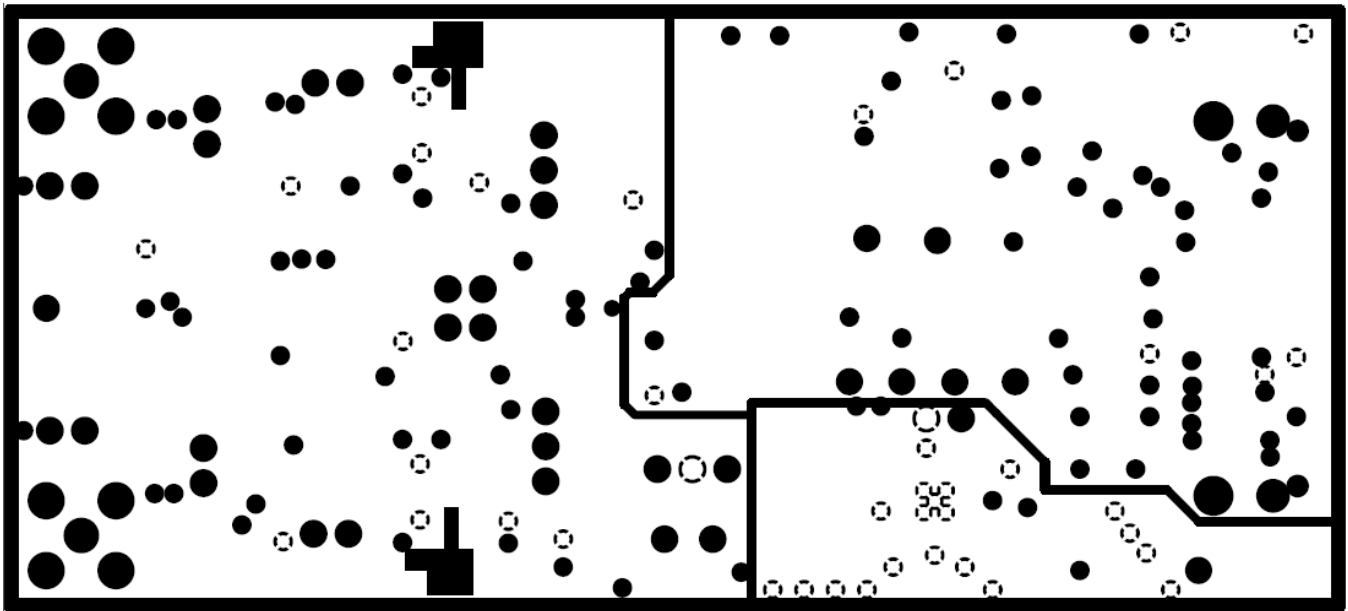


Figure 28. ADS8350EVM PCB: Power Layer

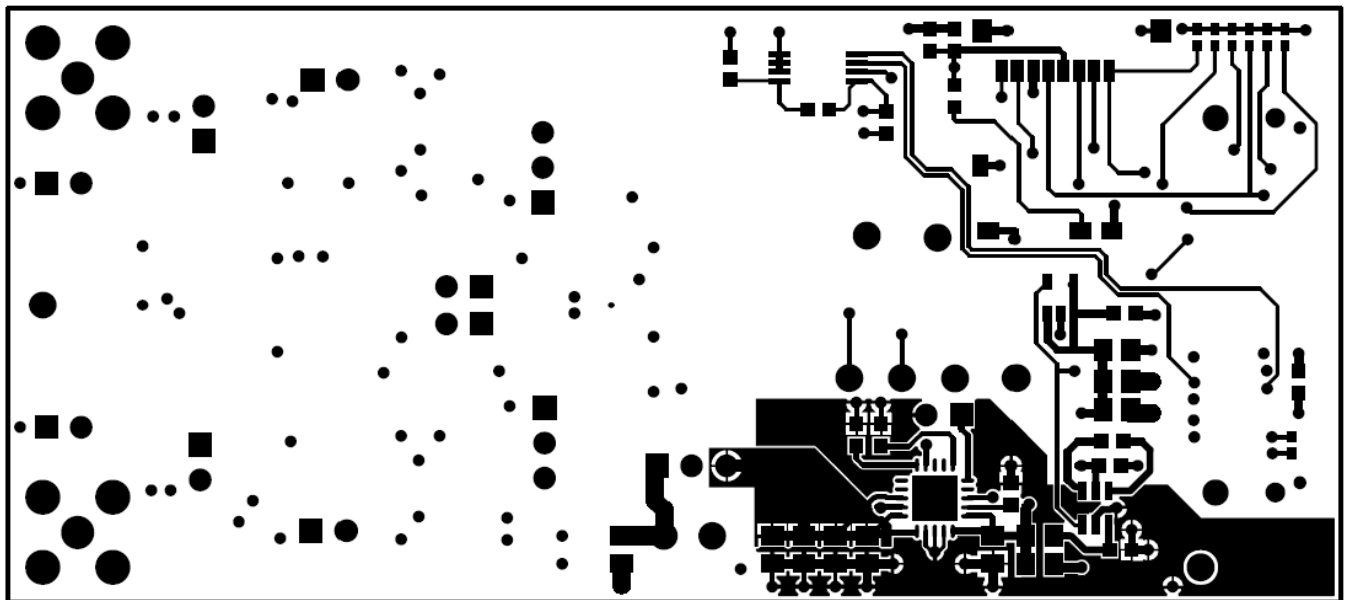
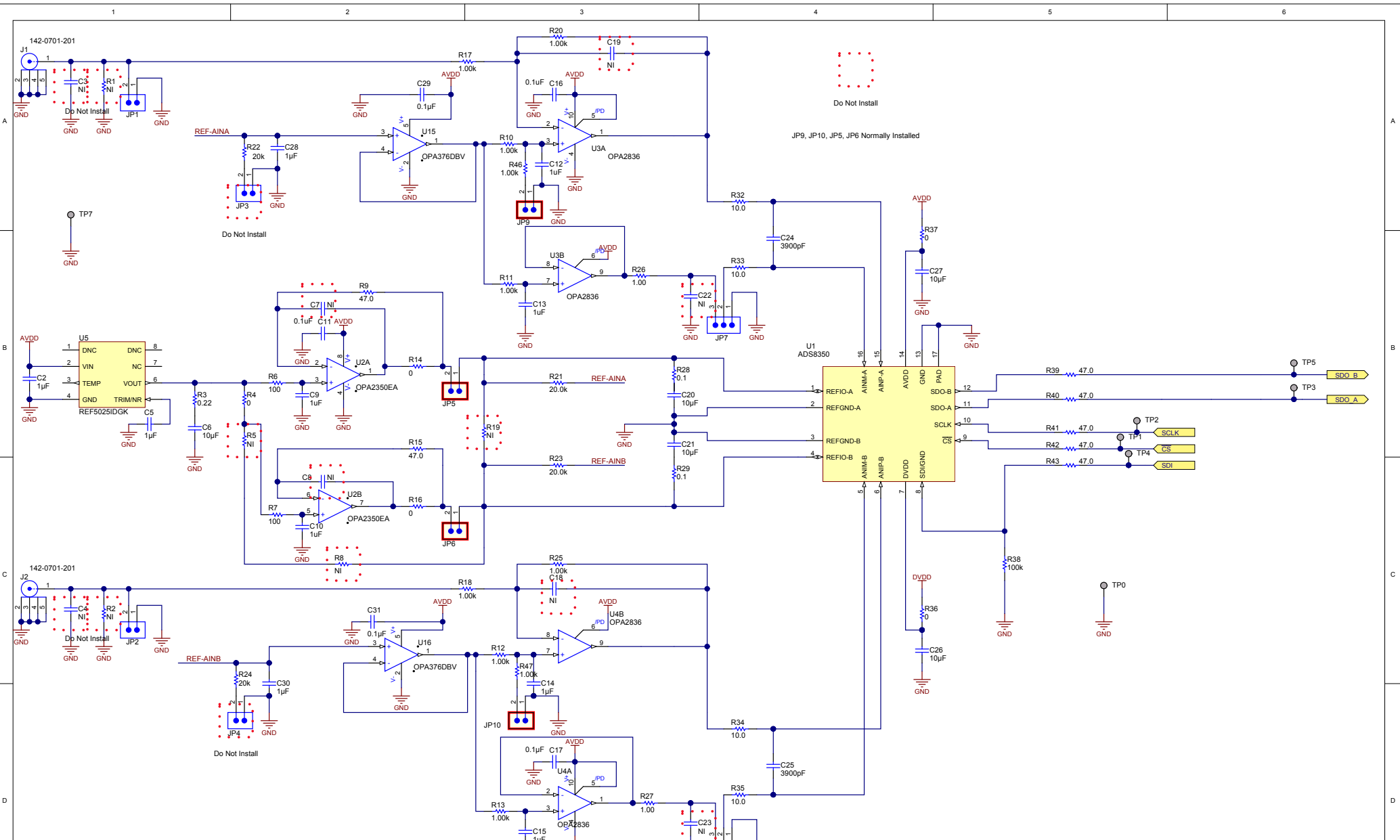


Figure 29. ADS8350EVM PCB: Bottom Layer

### 7.3 Schematics

The schematics for the ADS8350EVM are appended to the end of this user's guide.



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Designed for: Public Release	Mod. Date: 3/31/2014
Project Title: ADS8350EVM RevA	Sheet Title:
Number: ADS8350EVM Rev. A	Assembly Variant: Variant name not interpreted
SVN Rev.: Not in version control	Sheet: 1 of 1
Drawn By: Luis Chioye	File: Main_ADS8350EVM_RevA_SchDoc
Engineer: Luis Chioye	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>

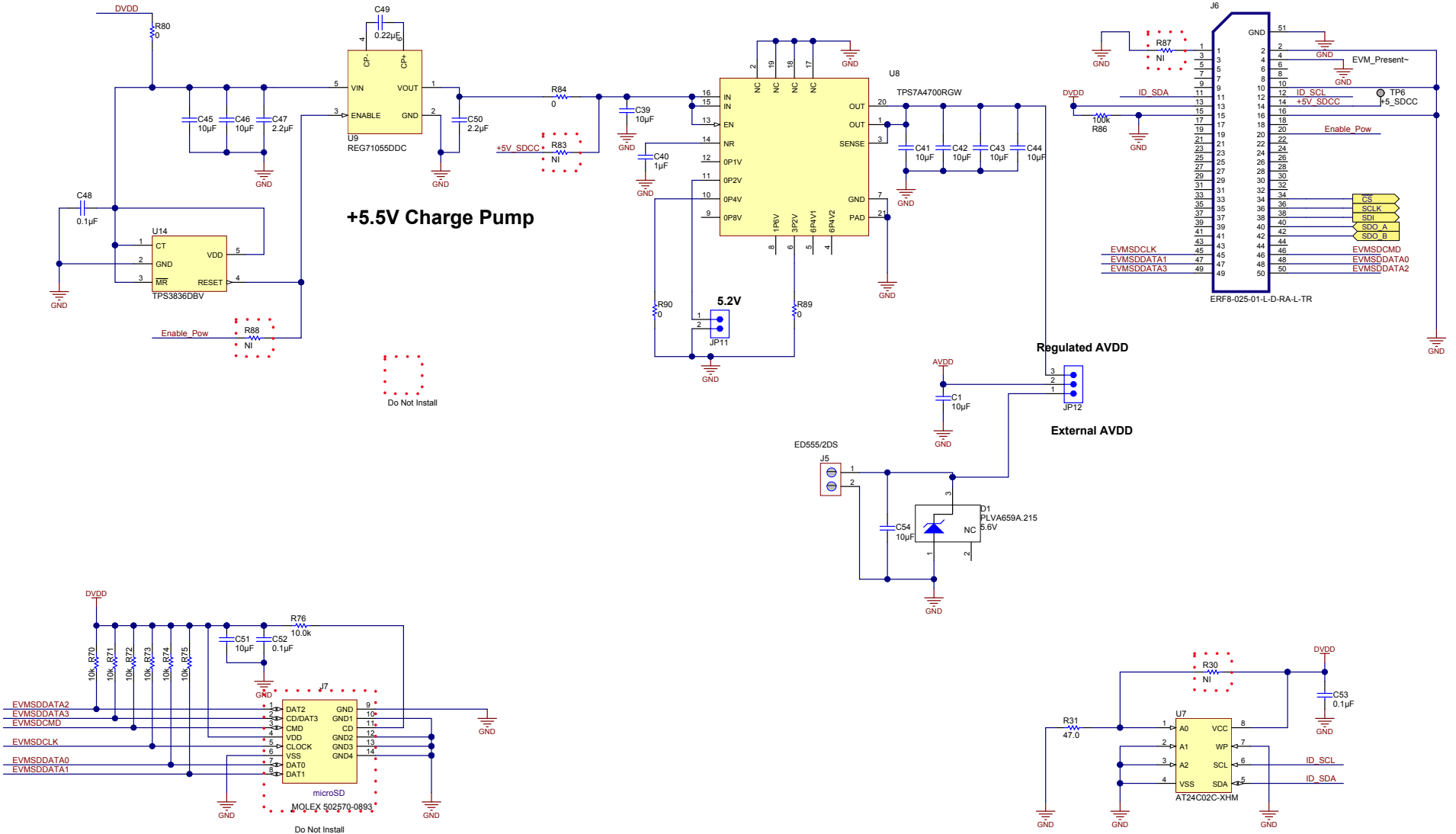


# +3.3V SDCC Digital Supply

# +5.5V Charge Pump

# Regulated AVDD

# External AVDD



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Number: ADS8350EVM Rev. A	Designed for: Public Release	Mod. Date: 11/11/2013
SVN Rev.: Not in version control	Project Title: ADS8350EVM RevA	
Drawn By: Luis Chioye	Sheet Title: Assembly Variant: Variant name not interpreted	Sheet: 1 of 1
Engineer: Luis Chioye	File: Connector_ADS8350EVM_RevA.SchDoc	Size: B
	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

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11. User shall employ reasonable safeguards to ensure that user's use of EVMs will not result in any property damage, injury or death, even if EVMs should fail to perform as described or expected.
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**Agreement to Defend, Indemnify and Hold Harmless.** User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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### **General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations:* For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

### **U.S. Federal Communications Commission Compliance**

#### **For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

##### **Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

##### **FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

##### **FCC Interference Statement for Class B EVM devices**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

##### **Industry Canada Compliance (English)**

#### **For EVMs Annotated as IC – INDUSTRY CANADA Compliant:**

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

##### **Concerning EVMs Including Radio Transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

##### **Concerning EVMs Including Detachable Antennas**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

##### **Canada Industry Canada Compliance (French)**

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

#### Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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#### EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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