1.0 Purpose

This document is intended to provide information on Heatsink Small Outline Package (HSOP) and its process. The package related information includes: Component and board level reliability, electrical parasitic and thermal resistance data.

2.0 Scope

This application note is written generically, and device specific information is not provided. This document serves only as a guideline to help develop user-specific solutions. Actual experience and development efforts are still required to optimize the process per individual device requirements and practices.

Contents

1.0 Purpose ................................................. 1
2.0 Scope ................................................... 1
3.0 HSOP Package Information ....................... 2
3.1 Package Description ............................... 2
3.2 Package Dimensions ............................... 2
4.0 Package Configuration .............................. 4
4.1 Process Flow ......................................... 4
5.0 1st Level Reliability ................................. 4
6.0 2nd Level Reliability ................................. 5
7.0 Printed Circuit Board (PCB) Layout Guidelines ............... 5
8.0 Package Thermal Resistances ..................... 6
9.0 Electrical Performance .............................. 7
10.0 Reference .............................................. 9
3.0 HSOP Package Information

3.1 Package Description

HSOP is a surface mount package with “gull wing” lead form (See Figure 1). This package has a mechanically attached thick Copper (Cu) heat slug to improve the thermal performance. The exposed heat slug provides a direct path for heat conduction away from an IC and into a solder attached Printed Circuit Board (PCB).

3.2 Package Dimensions

Three HSOP packages are available, all with the same body size of 15.90mm (L) x 11.00mm (W) but with different lead counts and pitch. There are 20ld, 30ld and 44ld HSOP packages with lead pitch of 1.27mm, 0.80mm, and 0.65mm, respectively. A few nominal dimensions for all three HSOP packages are provided in Figure 2 and Table 1.

Freescale’s HSOP package is a non-JEDEC package. The exposed pad region, referenced as dimensions E3 and D1 in Figure 2, was widened for better thermal resistance performance compared to the JEDEC MO-166 package [See reference (1)].

The bottom side of the 20ld HSOP is slightly different than the 30 and 44ld HSOP packages. The corners of the exposed pad region are not chamfered on the 20ld HSOP package.

Freescale also carries the 36ld HSOP package. This lead count is considered custom and therefore, will not be covered in this document. Please contact the Product Package Engineer for additional information on the 36ld HSOP package.
### Table 1. Nominal Package Dimensions (in mm)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>20ld HSOP</th>
<th>30ld HSOP</th>
<th>44ld HSOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
</tr>
<tr>
<td>A2</td>
<td>3.00</td>
<td>3.00</td>
<td>3.00</td>
</tr>
<tr>
<td>b</td>
<td>0.46</td>
<td>0.41</td>
<td>0.29</td>
</tr>
<tr>
<td>c</td>
<td>0.28</td>
<td>0.28</td>
<td>0.28</td>
</tr>
<tr>
<td>D</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
</tr>
<tr>
<td>D1</td>
<td>12.15</td>
<td>12.15</td>
<td>12.15</td>
</tr>
<tr>
<td>e</td>
<td>1.27</td>
<td>0.80</td>
<td>0.65</td>
</tr>
<tr>
<td>E</td>
<td>14.20</td>
<td>14.20</td>
<td>14.20</td>
</tr>
<tr>
<td>E1</td>
<td>11.00</td>
<td>11.00</td>
<td>11.00</td>
</tr>
<tr>
<td>E3</td>
<td>6.80</td>
<td>6.85</td>
<td>6.85</td>
</tr>
<tr>
<td>L</td>
<td>0.97</td>
<td>0.97</td>
<td>0.97</td>
</tr>
<tr>
<td>A</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
</tr>
</tbody>
</table>
4.0 Package Configuration

The HSOP package is able to accommodate both single and multiple die. The single die configuration utilizes the multi-strand leadframe, whereas the multi-die configuration is currently limited to the single-strand leadframe. The multi-die leadframe is more cost effective.

The current single-strand leadframe is NiPd with Ag spot plating on the heat slug with Au and larger diameter Al wires. The multi-strand leadframe is also NiPd preplated, but with bare Cu (with no Ag spot plating) heat slug and uses 2mil Cu wire. See Figure 3 to view a cross section of the HSOP package. Both solder and epoxy can be used for the die attach material.

4.1 Process Flow

See Figure 4 for the HSOP process flow map.

5.0 1st Level Reliability

All of the HSOP packages are rated at Moisture Sensitivity Level (MSL)1 @ 220°C. The three packages were internally qualified using JEDEC standard, JEDEC-STD-020. These units were preconditioned to level 1 and passed the following tests: a) Temperature/Humidity/Bias (THB) of 85°C with 85% RH for 96 hours and b) temperature cycled at -55°C to 125°C range for 1000 cycles. The packages also passed the high temperature storage of 150°C for 1000 hours.
The 20ld HSOP package has been qualified at MSL3 @ 240°C, but qualification at this level will be considered in a case-by-case basis.

6.0 2nd Level Reliability

The 2nd level reliability is board level reliability expressed in terms of solder joint life. In almost all cases, customers are interested in knowing the Time to First Failure (TFF) and Mean Time to Failure (MTTF). The HSOP package, like all leaded package, has a high 2nd level reliability. The 30ld HSOP at temperature range of –40 to 125°C has a TTF value of approximately 15,000 cycles and MTTF of approximately 20,000 cycles. The Weibull plot of 30ld HSOP is provided in Figure 5 The temperature cycle for the same package at a temperature range of 0 to 100°C was stopped after no failures at 45499 cycles. The board level reliability study hasn't been performed on the 20ld and 44ld HSOP packages but similar results are expected.

![Weibull Plot of 30ld HSOP](image)

Figure 5. Weibull Plot of 30ld HSOP

7.0 Printed Circuit Board (PCB) Layout Guidelines

The leaded surface mount packages have been widely used in the industry for some time. The assembly sites should already have internal guidelines on PCB pad dimensions. This section will only reference the pad dimensions used to obtain the board level reliability (Section 6.0 2nd Level Reliability) for the 30ld HSOP package. Note that the lead widths are different between the 20ld, 30ld and the 44ld HSOP packages. The PCB pad dimensions would need to be adjusted appropriately to avoid solder shorts. The lead pad dimension for the 30ld HSOP was 0.5mm (w) x 2.0mm (l). The dimensions for the exposed pad region are provided in Figure 6 This exposed pad region can remain the same for all three HSOP packages.
8.0 Package Thermal Resistances

The thermal performance of the HSOP package is characterized using two thermal board types and three boundary conditions. Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2 [5]) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment near the package. The heat that is generated on the die surface reaches the immediate environment along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the test board followed by convection and radiation off the exposed board surfaces. $R_{\theta JA}$ measures the thermal performance of the package in a low conductivity test board (single signal layer – 1s) in a natural convection environment. The 1s test board is designed per JEDEC JESD51-3 [6] and JEDEC JESD51-5 [7]. Another thermal resistance that is commonly reported is Theta-JMA or $R_{\theta JMA}$ on a board with two signal layers and two internal planes (2s2p). The 2s2p test board is designed per JEDEC JESD51-5 [7] and JEDEC JESD51-7 [8]. $R_{\theta JA}$ and $R_{\theta JMA}$ help bound the thermal performance of the HSOP package in a customer’s application. $R_{\theta JA}$ helps estimate the thermal performance of the HSOP package when it is mounted in two distinct configurations: (1) a board with no internal thermal planes (i.e. low conductivity board) or (2) when a multi-layer board is tightly populated with similar components. $R_{\theta JMA}$ provides the thermal performance of the HSOP when there are no nearby components dissipating significant amounts of heat on a multi-layer board. Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC EIA/JESD51-8 [9]) is also provided for the HSOP package. $R_{\theta JB}$ measures the horizontal spreading of heat between the junction and the board. The board temperature is taken near the board surface on one of the package center leads. Another thermal resistance that is provided is junction-to-case thermal resistance (Theta-JC or $R_{\theta JC}$). The case is defined at the exposed pad surface. $R_{\theta JC}$ can be used to estimate the thermal performance of the HSOP package when the board is adhered to a metal housing or heat sink and a complete thermal analysis is done. These thermal resistances help bound the thermal problem under distinct environments.

Table 2 has some thermal information for certain HSOP packages. All of the data was generated using Silicon (Si) die with the die size of 5.54 x 4.19mm.
9.0 Electrical Performance

For a leaded package, the series inductance and capacitance contributed by the HSOP leads are higher than those of the leadless package such as the QFN, but in general lower than those of the BGA packages (due to the parasitic effects contributed by the substrate traces). It is important to note, however, that the RLC (RLC stands for resistance, inductance and capacitance) performance comprises contributions of both the terminal and bonding wire. In cases of small die to flag size ratio, longer bonding wires may be required for the same device in the BGA package. In these cases, the RLC performance may be poorer.

A field solver was used to simulate the RLC performance of the 20ld, 30ld, and 44ld HSOP packages. The results were graphed and provided in Figure 7, Figure 8, and Figure 9.
Figure 7. 20ld HSOP RLC Graphs

Figure 8. 30ld HSOP RLC Graphs
10.0 Reference

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+49 89 92103 559 (German)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc., 2002, 2005. All rights reserved.