Freescale Semiconductor
Application Note

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Heatsink Small Outline Package (HSOP)

1.0 Purpose

This document is intended to provide information on Heatsink Small Outline Package (HSOP) and it's process. The package related information includes: Component and board level reliability, electrical parasitic and thermal resistance data.

2.0 Scope

This application note is written generically, and device specific information is not provided. This document serves only as a guideline to help develop user-specific solutions. Actual experience and development efforts are still required to optimize the process per individual device requirements and practices.

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3.0 HSOP Package Information

Figure 1. HSOP Package Family

3.1 Package Description

HSOP is a surface mount package with “gull wing” lead form (See **Figure 1**). This package has a mechanically attached thick Copper (Cu) heat slug to improve the thermal performance. The exposed heat slug provides a direct path for heat conduction away from an IC and into a solder attached Printed Circuit Board (PCB).

3.2 Package Dimensions

Three HSOP packages are available, all with the same body size of 15.90mm (L) x 11.00mm (W) but with different lead counts and pitch. There are 20ld, 30ld and 44ld HSOP packages with lead pitch of 1.27mm, 0.80mm, and 0.65mm, respectively. A few nominal dimensions for all three HSOP packages are provided in **Figure 2** and **Table 1**.

Freescale’s HSOP package is a non-JEDEC package. The exposed pad region, referenced as dimensions E3 and D1 in **Figure 2**, was widened for better thermal resistance performance compared to the JEDEC MO-166 package [See reference (1)].

The bottom side of the 20ld HSOP is slightly different than the 30 and 44ld HSOP packages. The corners of the exposed pad region are not chamfered on the 20ld HSOP package.

Freescale also carries the 36ld HSOP package. This lead count is considered custom and therefore, will not be covered in this document. Please contact the Product Package Engineer for additional information on the 36ld HSOP package.

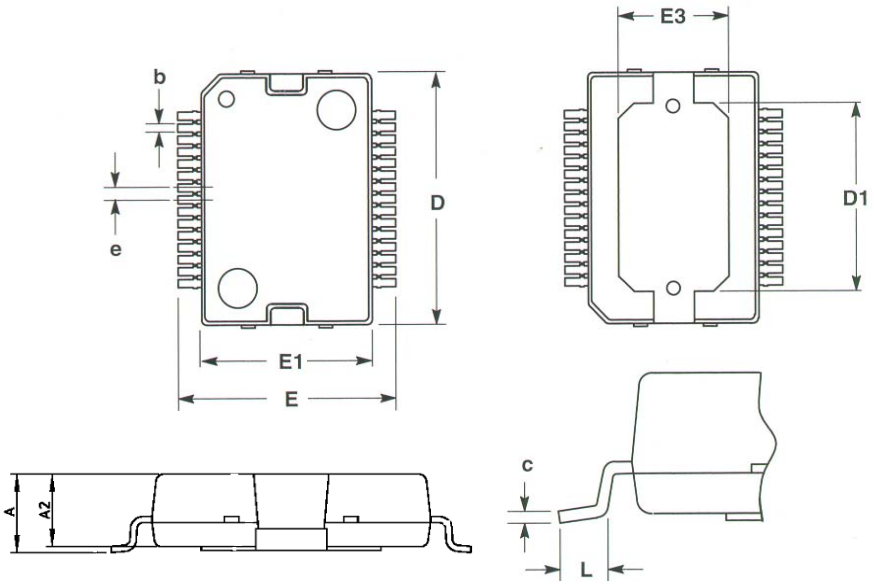

Figure 2. 30ld HSOP Case Outline Drawing

Table 1. Nominal Package Dimensions (in mm)

Dimension	20ld HSOP	30ld HSOP	44ld HSOP
A	3.20	3.20	3.20
A2	3.00	3.00	3.00
b	0.46	0.41	0.29
c	0.28	0.28	0.28
D	15.90	15.90	15.90
D1	12.15	12.15	12.15
e	1.27	0.80	0.65
E	14.20	14.20	14.20
E1	11.00	11.00	11.00
E3	6.80	6.85	6.85
L	0.97	0.97	0.97
A	3.20	3.20	3.20

4.0 Package Configuration

The HSOP package is able to accommodate both single and multiple die. The single die configuration utilizes the multi-strand leadframe, whereas the multi-die configuration is currently limited to the single-strand leadframe. The multi-die leadframe is more cost effective.

The current single-strand leadframe is NiPd with Ag spot plating on the heat slug with Au and larger diameter Al wires. The multi-strand leadframe is also NiPd preplated, but with bare Cu (with no Ag splot plating) heat slug and uses 2mil Cu wire. See **Figure 3** to view a cross section of the HSOP package. Both solder and epoxy can be used for the die attach material.

4.1 Process Flow

See **Figure 4** for the HSOP process flow map.

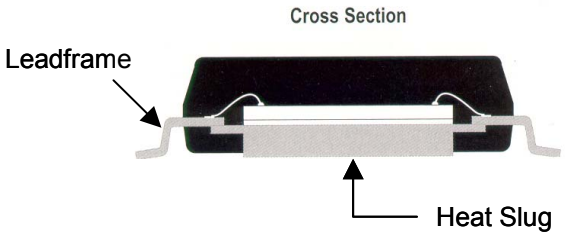

Figure 3. Cross section of HSOP Package

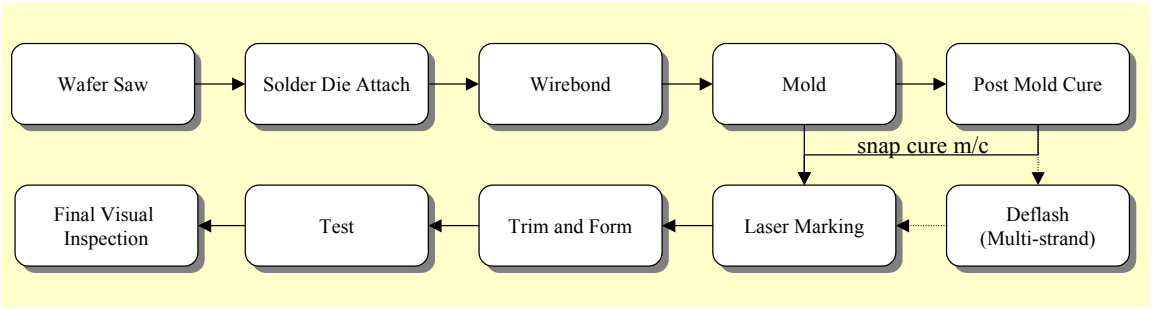

Figure 4. HSOP Process Flow Map

5.0 1st Level Reliability

All of the HSOP packages are rated at Moisture Sensitivity Level (MSL)1 @ 220°C. The three packages were internally qualified using JEDEC standard, JEDEC-STD-020. These units were preconditioned to level 1 and passed the following tests: a) Temperature/Humidity/Bias (THB) of 85°C with 85% RH for 96 hours and b) temperature cycled at -55°C to 125°C range for 1000 cycles. The packages also passed the high temperature storage of 150°C for 1000 hours.

The 20ld HSOP package has been qualified at MSL3 @ 240°C, but qualification at this level will be considered in a case-by-case basis.

6.0 2nd Level Reliability

The 2nd level reliability is board level reliability expressed in terms of solder joint life. In almost all cases, customers are interested in knowing the Time to First Failure (TFF) and Mean Time to Failure (MTTF). The HSOP package, like all leaded package, has a high 2nd level reliability. The 30ld HSOP at temperature range of –40 to 125°C has a TTF value of approximately 15,000 cycles and MTTF of approximately 20,000 cycles. The Weibull plot of 30ld HSOP is provided in **Figure 5** The temperature cycle for the same package at a temperature range of 0 to 100°C was stopped after no failures at 45499 cycles. The board level reliability study hasn't been performed on the 20ld and 44ld HSOP packages but similar results are expected.

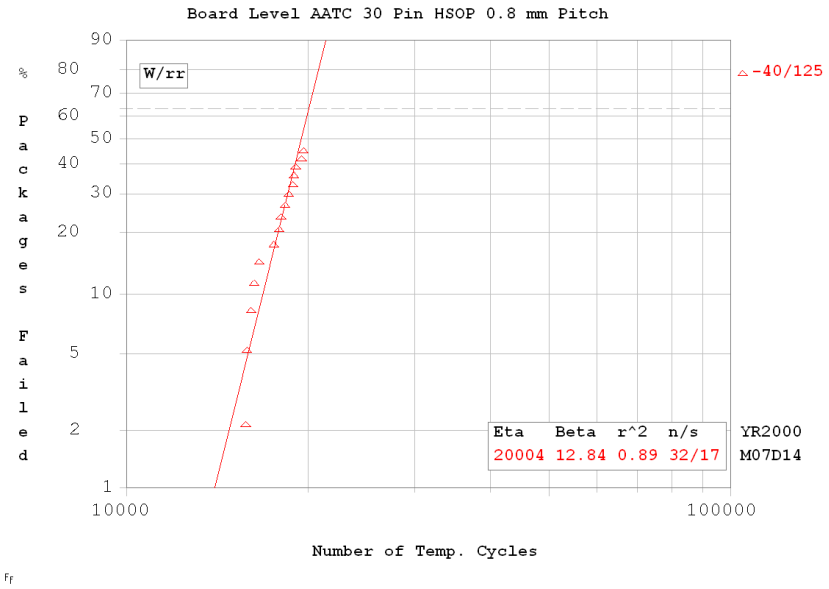

Figure 5. Weibull Plot of 30ld HSOP

7.0 Printed Circuit Board (PCB) Layout Guidelines

The leaded surface mount packages have been widely used in the industry for some time. The assembly sites should already have internal guidelines on PCB pad dimensions. This section will only reference the pad dimensions used to obtain the board level reliability (**Section 6.0 2nd Level Reliability**) for the 30ld HSOP package. Note that the lead widths are different between the 20ld, 30ld and the 44ld HSOP packages. The PCB pad dimensions would need to be adjusted appropriately to avoid solder shorts. The lead pad dimension for the 30ld HSOP was 0.5mm (w) x 2.0mm (l). The dimensions for the exposed pad region are provided in **Figure 6** This exposed pad region can remain the same for all three HSOP packages.

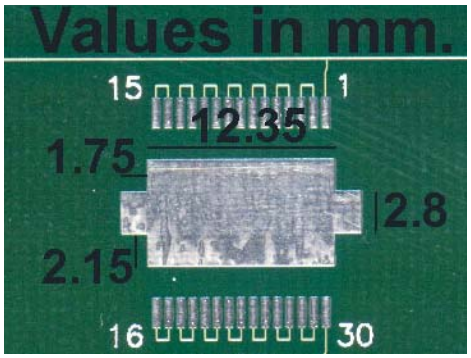

Figure 6. 30ld HSOP Exposed Pad Dimensions

8.0 Package Thermal Resistances

The thermal performance of the HSOP package is characterized using two thermal board types and three boundary conditions. Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2 [5]) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment near the package. The heat that is generated on the die surface reaches the immediate environment along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the test board followed by convection and radiation off the exposed board surfaces. $R_{\theta JA}$ measures the thermal performance of the package in a low conductivity test board (single signal layer – 1s) in a natural convection environment. The 1s test board is designed per JEDEC JESD51-3 [6] and JEDEC JESD51-5 [7]. Another thermal resistance that is commonly reported is Theta-JMA or $R_{\theta JMA}$ on a board with two signal layers and two internal planes (2s2p). The 2s2p test board is designed per JEDEC JESD51-5 [7] and JEDEC JESD51-7 [8]. $R_{\theta JA}$ and $R_{\theta JMA}$ help bound the thermal performance of the HSOP package in a customer's application. $R_{\theta JA}$ helps estimate the thermal performance of the HSOP package when it is mounted in two distinct configurations: (1) a board with no internal thermal planes (i.e. low conductivity board) or (2) when a multi-layer board is tightly populated with similar components. $R_{\theta JMA}$ provides the thermal performance of the HSOP when there are no nearby components dissipating significant amounts of heat on a multi-layer board. Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC EIA/JESD51-8 [9]) is also provided for the HSOP package. $R_{\theta JB}$ measures the horizontal spreading of heat between the junction and the board. The board temperature is taken near the board surface on one of the package center leads. Another thermal resistance that is provided is junction-to-case thermal resistance (Theta-JC or $R_{\theta JC}$). The case is defined at the exposed pad surface. $R_{\theta JC}$ can be used to estimate the thermal performance of the HSOP package when the board is adhered to a metal housing or heat sink and a complete thermal analysis is done. These thermal resistances help bound the thermal problem under distinct environments.

Table 2 has some thermal information for certain HSOP packages. All of the data was generated using Silicon (Si) die with the die size of 5.54 x 4.19mm.

Table 2. Thermal Resistance Data

Rating			20ld	30ld	44ld	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s)	RθJA	52	49	44	°C/W	1,2
Junction to Ambient Natural Convection	Four layer board (2s2p)	RθJMA	19	19	19	°C/W	1,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	RθJMA	40	38	33	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	RθJMA	15	14	14	°C/W	1,3
Junction to Board		RθJB	3	3	3	°C/W	4
Junction to Case	Bottom of Package	RθJC	0.2	0.2	0.2	°C/W	5
Junction to Package Top	Natural Convection	ΨJT	5	5	5	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal. Single layer board is designed per JEDEC JESD51-3 and JEDEC JESD51-5.
3. Per JEDEC JESD51-6 with the board horizontal. 2s2p board is designed per JEDEC EIA/JESD51-5 and JEDEC JESD51-7.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package. 2s2p board is designed per JEDEC JESD51-5 and JEDEC JESD51-7.
5. Thermal resistance between the die and the exposed pad.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9.0 Electrical Performance

For a leaded package, the series inductance and capacitance contributed by the HSOP leads are higher than those of the leadless package such as the QFN, but in general lower than those of the BGA packages (due to the parasitic effects contributed by the substrate traces). It is important to note, however, that the RLC (RLC stands for resistance, inductance and capacitance) performance comprises contributions of both the terminal and bonding wire. In cases of small die to flag size ratio, longer bonding wires may be required for the same device in the BGA package. In these cases, the RLC performance may be poorer.

A field solver was used to simulate the RLC performance of the 20ld, 30ld, and 44ld HSOP packages. The results were graphed and provided in **Figure 7**, **Figure 8**, and **Figure 9**.

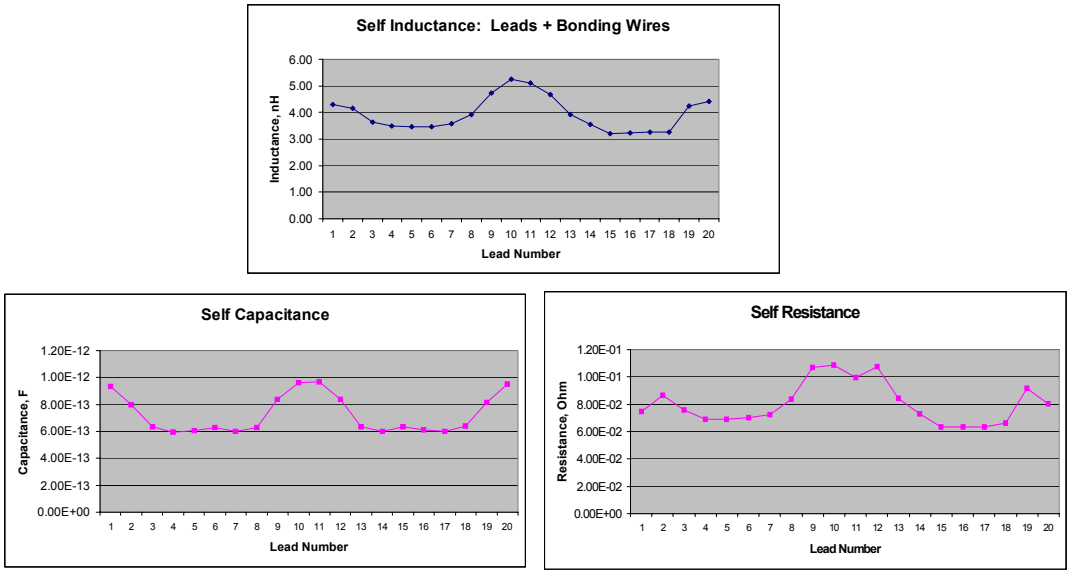

Figure 7. 20ld HSOP RLC Graphs

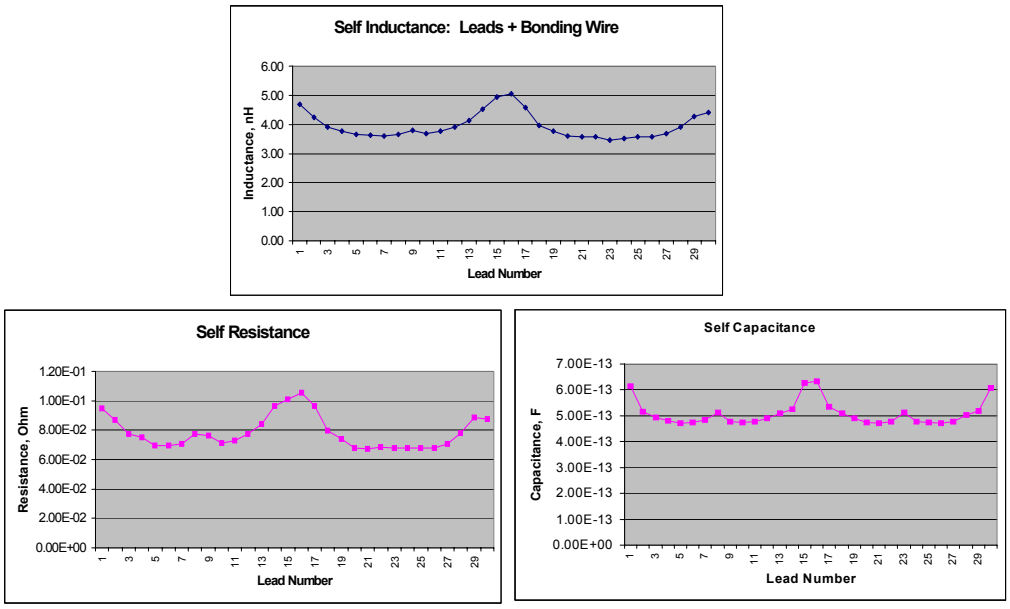

Figure 8. 30ld HSOP RLC Graphs

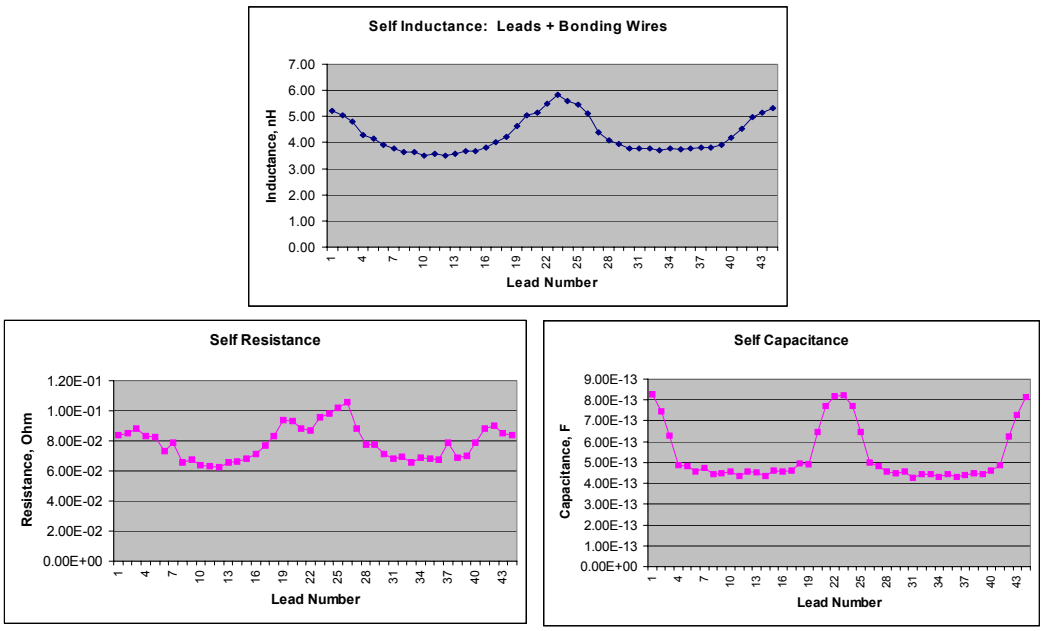

Figure 9. 44ld HSOP RLC Graphs

10.0 Reference

(1) "Plastic Small Outline Heatslug Package", MO-166, JEDEC Solid State Product Outline.

(2) Montes De Oca, Tony, "30ld HSOP Thermal Simulation Report", Motorola Internal

(3) Montes De Oca, Tony, "44ld HSOP Thermal Simulation Report", Motorola Internal Report, Sept 17, 2002.

(4) Zhou, Yaping, "20ld, 30ld, and 44ld HSOP Electrical Parasitic Extraction Report", Motorola Internal Report, Sept 24, 2002.

(5) EIA/JESD51-2, "Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)", December 1995.

(6) EIA/JESD51-3, "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages," August 1996.

(7) EIA/JESD51-5, "Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms," February 1999.

(8) EIA/JESD51-7, "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages," February 1999.

(9) EIA/JESD51-8, "Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board", October 1999.

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