Freescale Semiconductor
Application Note

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Battery Management for the MC13783

by: Power Management and Audio Application Team

1 Introduction

The purpose of this application note is show the battery management and charging of the MC13783.

2 Charging Path

The MC13783 supports up to three types of charge path: dual, single and separate path and two kinds of input configuration: common and separate input. The configuration choice is performed by connecting or not connecting the CHRGMOD pins of the MC13783 as described in the Table 1, on page 3 to ground or to VATLAS; and by the presence of external transistors used for current regulation and trickle charging.

2.1 Single Path Configuration

In this configuration, which is the simplest one (i.e., the most cost effective solution), the entire chipset is always supplied from the battery. The battery always has to be present and charged to be able to run the application. In this configuration, the charge current is also used to supply the phone, so the battery charge algorithm has to

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measure the real battery charge current. The standalone trickle charge is activated for a depleted battery (wall charger and USB). Figure 1 shows the single path configuration.

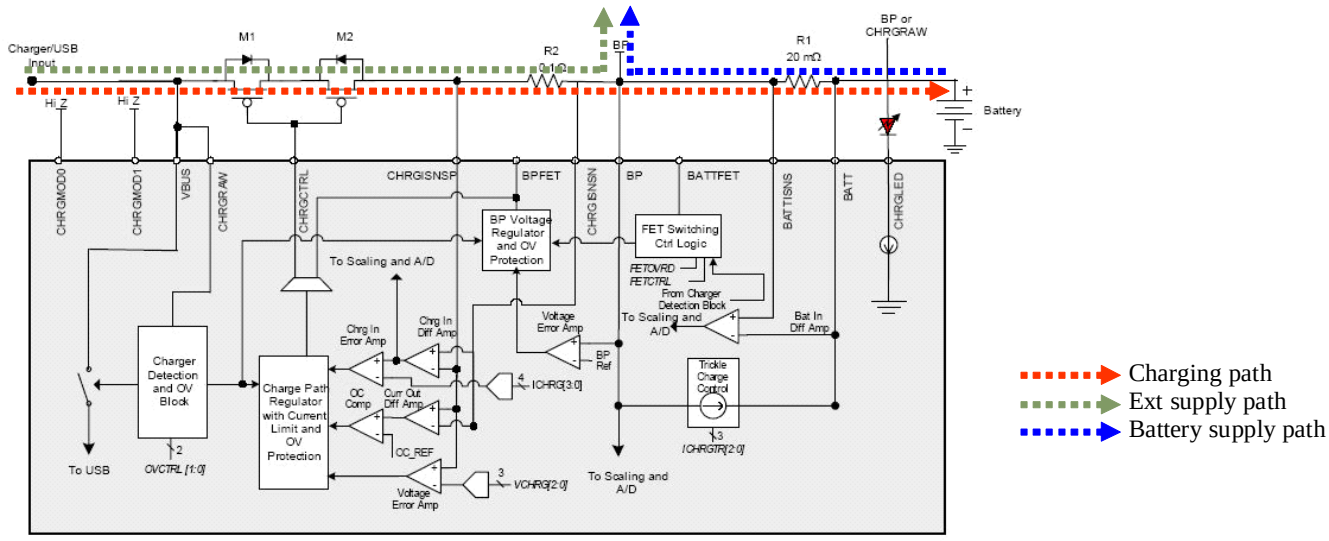

Figure 1. Single Path Configuration

2.2 Serial Path Configuration

In this configuration a power switch, M3, is added to allow the chipset to be supplied by the charger even if the battery is completely discharged (dead battery operation). The charge current is still shared between the battery and the application (complex battery charging algorithm). The standalone trickle charge is activated for USB charging only. Figure 2 shows the serial path configuration.

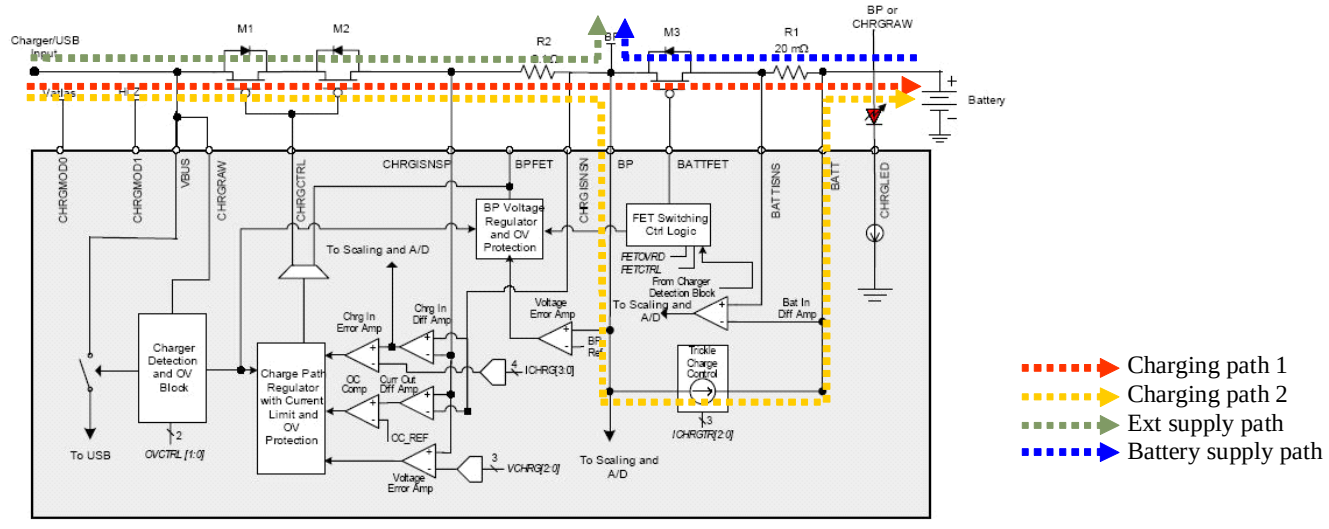

Figure 2. Serial Path Configuration

2.3 Dual Path Configuration

In this configuration, a second power MOS (M4) is added and acts as an independent power voltage regulator to supply the application. The charging current is fully used to charge the battery pack to simplify the charging algorithm. The standalone trickle charge is activated for USB charging only. Figure 3 shows the dual path configuration.

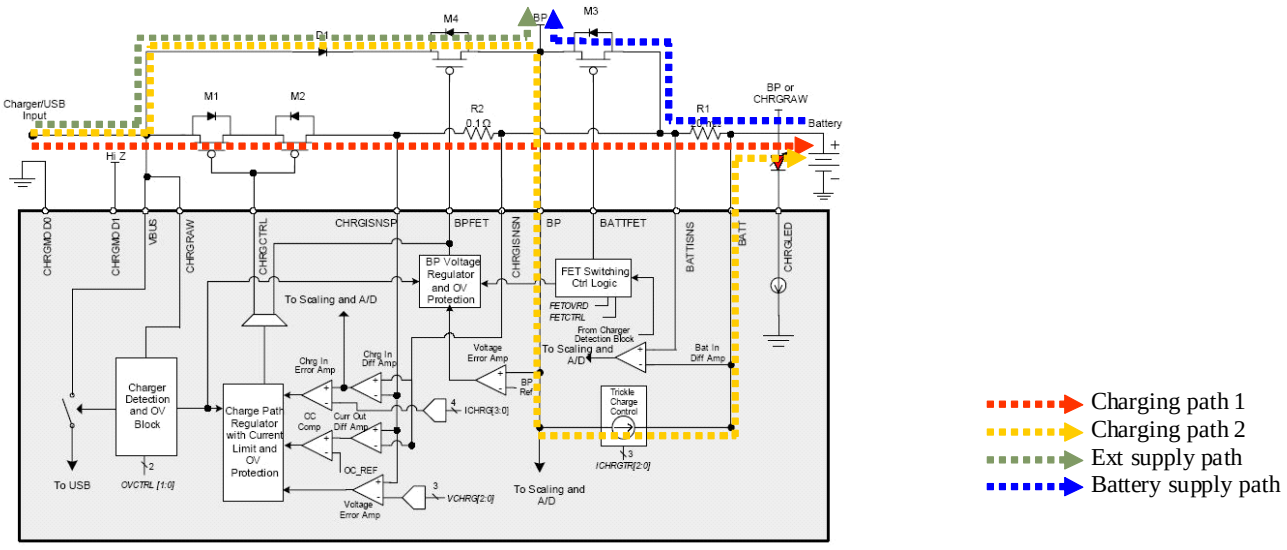

Figure 3. Dual Path Configuration

Table 1 shows the configuration choice that is performed by connecting or not connecting the CHRGMOD pins of the MC13783 to ground or to VATLAS; and by the presence of external transistors used for current regulation and trickle charging.

Table 1. Charge Mode Settings

CHRGMOD1	CHRGMOD0	Charge Mode	Pros	Cons
Hi Z	GND	Common input-Dual Path	• Simpler charge algorithm • Dead battery supported	• Most expansive solution: 4 MOS FET
Hi Z	Hi Z	Common input-Single Path	• Simplest one • Cost effective	• Dead battery not supported • Battery charge algorithm has to monitor the real battery charge current
Hi Z	VATLAS	Common input-Serial Path	• Dead battery supported	• Additional power switch M3 • Complex charge algorithm
VATLAS	GND	Separate input-Dual Path		• Does not support USB charging except with an external circuitry controlled by a GPIO of the processor
VATLAS	Hi Z	Separate input-Single Path		
VATLAS	VATLAS	Separate input-Serial Path		

Table 1. Charge Mode Settings (continued)

CHRGMOD1	CHRGMOD0	Charge Mode	Pros	Cons
GND	GND	Reserved		
GND	Hi Z			
GND	VATLAS			

3 Charger Detection

The application of a charger or USB host will cause the CHGDETI and USBI interrupts to go high. In addition, if a charger is attached, the SE1I will also go high. These interrupts can be used to detect the application of a charger in the system by looking at the CHRGDETS, USB4V4S, and SE1S bits.

In addition, when the charge path regulator is enabled, the charge current is sensed across the R2 resistor to generate the CHGCURRI and CHGCURRS bits.

NOTE

If the charge current falls below the CHGCURR threshold, the CHGCURRS bit goes low.

The CHGCURRS bit is set to 1 whenever the charge path regulator is disabled. If the charger is removed while the charge path regulator is enabled, the software removal detection of the charger can be determined by a combination of the CHRGCURRS, CHGDETS, and USB4V4S bits.

When in separate input charging configuration, the hardware detection of removal of a charger is based on CHRGDETSEP and CHGCURR thresholds. When in common input charging configuration, the hardware detection of removal of a charger is based on CHRGDET and CHGCURR thresholds.

NOTE

The hardware detection of the charger removal with clear ICHRG[3:0] bits causes the charger path regulator to shut off.

4 Charger Control Logic

It should be noted that in the MC13783, the charger is controlled through combinatory logic. Table 2, on page 5 through Table 7, on page 8 define the behavior of the MC13783 autonomous charger. When SPI bits are noted, this means it should be programmed by the processor.

Table 2. Dual Path Logic Table

CHRGRAW	ID	RESETB	DP	DM	FET OVRD	FET CTRL	BATT	BP Regulator	BATTFET	Charge Path Regulator	Trickle Charger	Charger Turn On
H	<3 V	L	L	L	X	X	<BATTON	OFF	H	TRICKLEL	OFF	L
			L	H								
			H	L								
			L	L	X	X	>BATTON	OFF	L	TRICKLEL	OFF	H
			L	H								
			H	L								
			H	H	X	X	X	ON	H	OFF	OFF	H
		H	L	L	0	X	X	OFF	L	ICHRG [3:0]	NA	H
			L	H								
			H	L								
			H	H	0	X	X	ON	H	ICHRG [3:0]	ICHRGTR [2:0]	H
			X	X	1	0	X	ON	H	ICHRG [3:0]	ICHRGTR [2:0]	H
			X	X	1	1	X	OFF	L	ICHRG [3:0]	NA	H
	>3 V	X	X	X	X	X	X	ON	H	ICHRG [3:0]	ICHRGTR [2:0]	H
L	X	X	X	X	X	X	X	OFF	L	OFF	OFF	L

Table 3. Serial Path Logic Table

CHRGRAW	ID	RESETB	DP	DM	FETOVRD	FETCTRL	BATT	BATTFET	Charge Path Regulator	Trickle Charger	Charger Turn On
H	<3V	L	L	L	X	X	<BATTON	L	TRICKLEL	OFF	L
			L	H							
			H	L							
			L	L	X	X	>BATTON	L	TRICKLEL	OFF	H
			L	H							
			H	L							
			H	H	X	X	X	H	Full Rate	OFF	H
		H	L	L	0	X	X	L	ICHRG[3:0]	NA	H
			L	H							
			H	L							
			H	H	0	X	X	* H	Full Rate	OFF	H
								* L	ICHRG[3:0]	ICHRGTR [2:0]	H
			X	X	1	0	X	H	ICHRG[3:0]	ICHRGTR [2:0]	H
			X	X	1	1	X	L	ICHRG[3:0]	NA	H
	>3V	X	X	X	X	X	X	H	Full Rate	ICHRGTR [2:0]	H
L	X	X	X	X	X	X	X	L	OFF	OFF	L
(*) ‘H / Full Rate / OFF / H’ if already Full Rate before entering this mode, ‘L / ICHRG[3:0] / ICHRGTR[2:0] / H’ in the other cases.											

Table 4. Single Path Logic Table

CHRGRAW	ID	RESETB	DP	DM	FET OVRD	FET CTRL	BATT	Charge Path Regulator	Charger Turn On
H	<3V	L	L	L	X	X	<BATTON	TRICKLEL	L
			L	H					
			H	L					
			L	L	X	X	>BATTON	TRICKLEL	H
			L	H					
			H	L					
			H	H	X	X	<BATTON	**TRICKLEL / TRICKLEM	L
			H	H	X	X	>BATTON	TRICKLEM	H
		H	L	L	0	X	X	ICHRG[3:0]	H
			L	H					
			H	L					
			H	H	0	X	X	ICHRG[3:0]	H
			X	X	1	0	X	ICHRG[3:0]	H
			X	X	1	1	X	ICHRG[3:0]	H
	>3V	X	X	X	X	X	<BATTON	** TRICKLEL / TRICKLEM	L
		X	X	X	X	X	>BATTON	** TRICKLEM / TRICKLEH	H
L	X	X	X	X	X	X	X	OFF	L
(**) TRICKLEL, TRICKLEM or TRICKLEH level is used based on BATT voltage.									

Table 5. Separate Input Dual Path Logic Table

CHRGRAW	RESETB	FET OVRD	FET CTRL	BP Regulator	BATTFET	Charge Path Regulator	Trickle Charger	Charger Turn On
H	L	X	X	ON	H	OFF	OFF	H
H	H	0	X	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	0	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	1	OFF	L	ICHRG[3:0]	NA	H
L	X	X	X	OFF	L	OFF	OFF	L

Table 6. Separate Input Serial Path Logic Table

CHRGRAW	RESETB	FET OVRD	FET CTRL	BATTFET	Charge Path Regulator	Trickle Charger	Charger Turn On
H	L	X	X	H	Full Rate	OFF	H
H	H	0	X	* H	Full Rate	OFF	H
				* L	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	0	H	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	1	L	ICHRG[3:0]	NA	H
L	X	X	X	L	OFF	OFF	L
(*) 'H / Full Rate / OFF / H' if already Full Rate before entering this mode, 'L / ICHRG[3:0] / ICHRGTR[2:0] / H' in the other cases.							

Table 7. Separate Input Single Path Logic Table

CHRGRAW	RESETB	FETOVRD	FETCTRL	BATT	Charge Path Regulator	Charger Turn On
H	L	X	X	<BATTON	**TRICKLEL / TRICKLEM	L
H	L	X	X	>BATTON	TRICKLEM	H
H	H	0	X	X	ICHRG[3:0]	H
H	H	1	0	X	ICHRG[3:0]	H
H	H	1	1	X	ICHRG[3:0]	H
L	X	X	X	X	OFF	L
(**) TRICKLEL or TRICKLEM level is used based on BATT voltage						

5 Charger SPI Tables

Charger SPI tables are shown Table 8 and Table 9.

Table 8. Charger Programming Table

Bit #	Bit Name	Reset Signal	Reset State	Type	Description
0	VCHRG0	RESETB	0	R/W	Sets the output voltage of charge regulator.
1	VCHRG1	RESETB	0	R/W	
2	VCHRG2	RESETB	0	R/W	
3	ICHRG0	RESETB	0	R/W	Sets the current of the main charger DAC.
4	ICHRG1	RESETB	0	R/W	
5	ICHRG2	RESETB	0	R/W	
6	ICHRG3	RESETB	0	R/W	
7	ICHRGTR0	RESETB	0	R/W	Sets the current of the trickle charger.
8	ICHRGTR1	RESETB	0	R/W	
9	ICHRGTR2	RESETB	0	R/W	
10	FETOVRD	RESETB	0	R/W	0 = BATTFET and BPFET outputs are controlled by hardware. 1 = BATTFET and BPFET are controlled by the state of the FETCTRL bit.
11	FETCTRL	RESETB	0	R/W	0 = BPFET is driven low, BATTFET is driven high if FETOVRD is set. 1 = BPFET is driven high, BATTFET is driven low if FETOVRD is set.
12	Reserved	RESETB	0	R/W	For future use.
13	RVRSMODE	RESETB	0	R/W	0 = Reverse mode disabled. 1 = Reverse mode enabled.
14	Reserved	RESETB	0	R/W	For future use.
15	OVCTRL0	RESETB	0	R/W	Overvoltage threshold select bit.
16	OVCTRL1	RESETB	0	R/W	
17	UCHEN	RESETB	0	R/W	Unregulated charge enable bit.
18	CHRGLEDEN	RESETB	0	R/W	0 = CHRGLED disabled. 1 = CHRGLED enabled.
19	CHRGRAWPDEN	RESETB	0	R/W	Enables a 5K pull down at CHRGRAW. To be used in the dual path charging configuration.
20	Reserved	RESETB	0	R/W	For future use.
21	Reserved	RESETB	0	R/W	For future use.
22	Unused		0	R	Not available.
23	Unused		0	R	Not available.

Table 9. Charger Related Interrupts

Interrupt bit	Mask bit	Sense bit	Description
CHGDETI	CHGDETM	CHGDETS	Charger detection interrupt, dual edge, debounce 32 msec
CHGOVI	CHGOVM	CHGOVS	Charger overvoltage detection interrupt, dual edge, 7.8 msec rising edge debounce
CHGREVI	CHGREVM	CHGREVS	Charger path reverse current interrupt, rising edge, 2.9 msec debounce
CHGSHORTI	CHGSHORTM	CHGSHORTS	Charger path short circuit in reverse supply mode interrupt, rising edge, 150 μs or 2.9 msec debounce depending on threshold
CCCVI	CCCVM	CCCVS	CCCV interrupt logic high indicates that the charger has switched its mode from CC to CV or from CV to CC. CCVS = 0 for constant current charging, CCCVS = 1 for constant voltage charging. Write a "1" to this location to clear the interrupt. Dual Edge, 2 sec debounce.
CHGCURRI	CHGCURRM	CHGCURRS	CHGCURR interrupt logic high indicates that the charge current has dropped below its threshold. Falling edge, debounce 16 msec.

6 Example of Charging Flow Diagram to the Baseband

Figure 4 is an example of the MC13783 charging flow to the baseband.

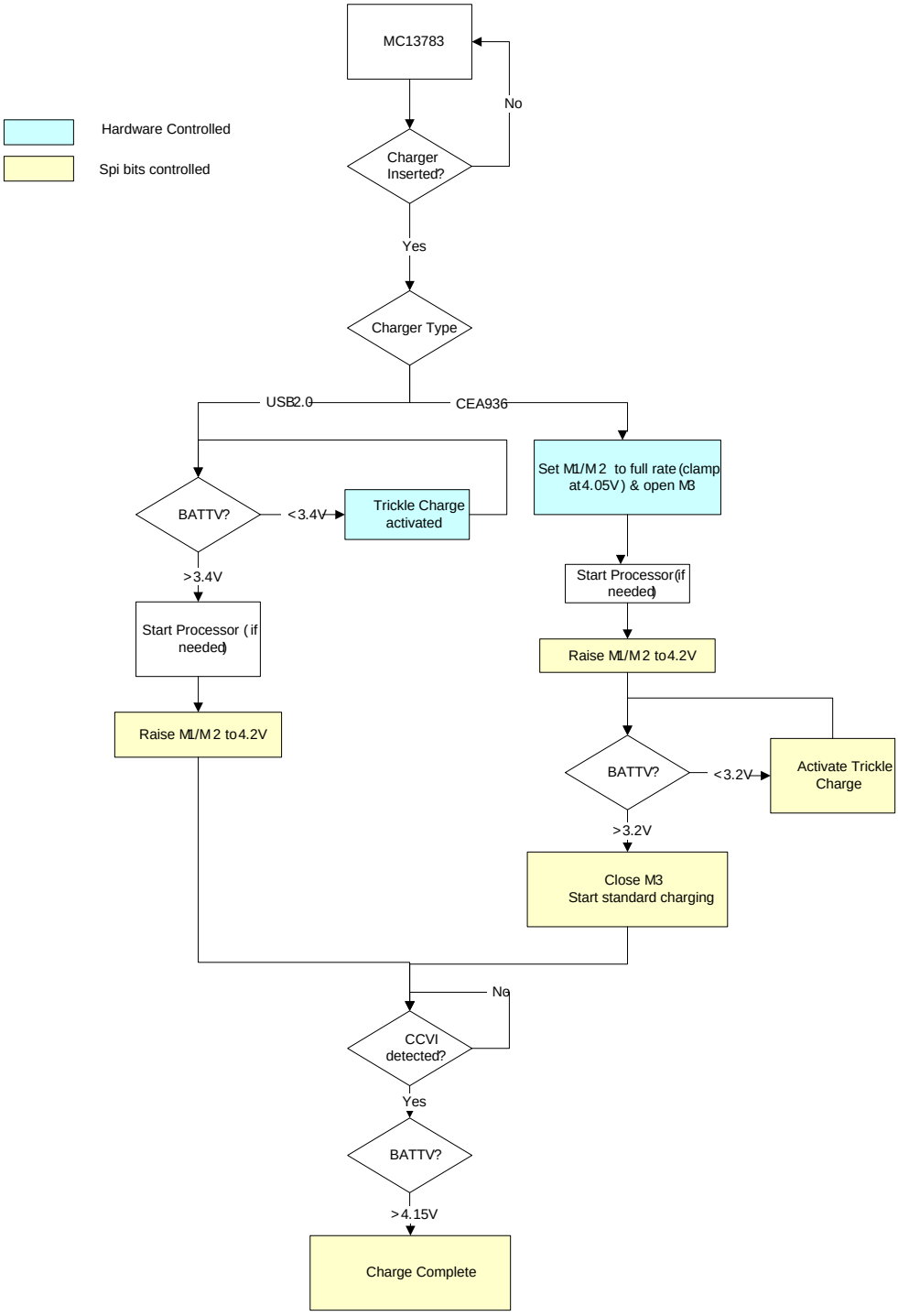

Figure 4. Example of the MC13783 Charging Flow to the Baseband

6.1 Example of CEA936 Charging

If the MC13783 detects the CEA936, then the battery FET (M3) is opened, the charge register VCHRG[3:0] is set to the desired value and the processor powers. Upon powering, the processor determines the state of the battery. If less than 3.4 V, it activates the internal trickle charger (processor must program this rate). If greater than 3.4 V, the processor closes the M3 and sets for a higher charge rate between 0.5 and 1C and it also reprograms VCHRG[3:0] to 4.2 V. With high rate charging, current rate will vary in order to maintain the power dissipation rate of M1 somewhere below the maximum dissipation rate of the M1 FET over the acceptable ambient temperature range for charging (typically 1W). It depends on the type of M1 FET chosen, the layout and the ambient temperature range whereby charging is allowed. Figure 5 shows the CEA936 charging curve.

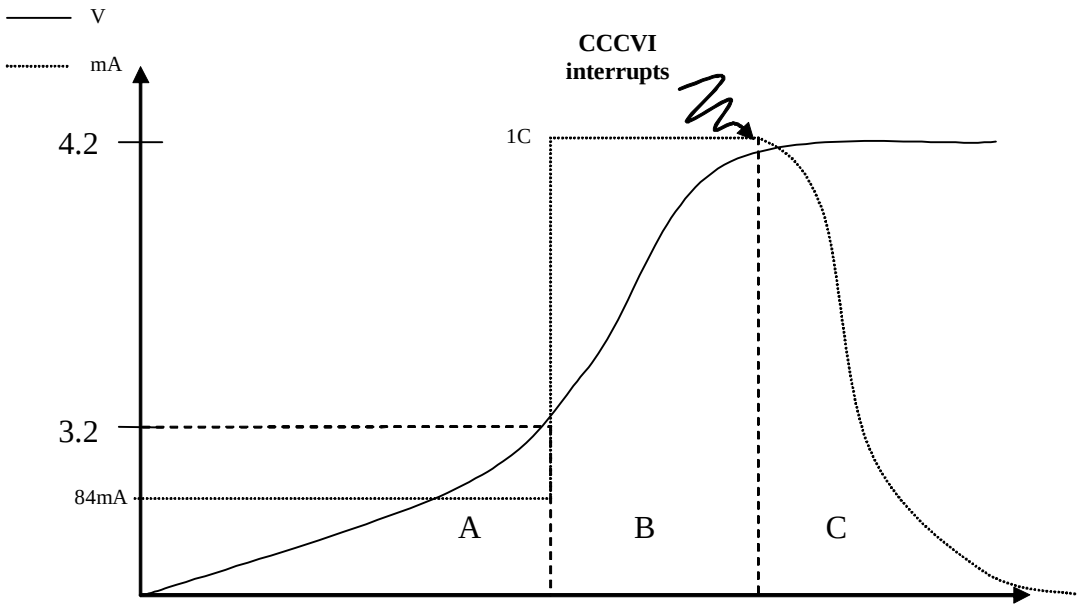

Figure 5. CEA936 Charging Curve

- Step A (small charge): If the battery is dead, the processor programs trickle charge circuitry to a small current (e.g., 84 mA through ICHRGTR[2:0] register).

NOTE

The processor must poll battery voltage to go to step B.

- Step B (fast charge): The charge is set to 1C (e.g., 900 mA in the case of a 900 mA charger) through ICHRG[3:0].
- Step C: The processor doesn't reprogram ICHRG[3:0] to reduce current, it is automatically done in the hardware by the MC13783 because current regulation is automatic when battery voltage approaches 4.2 V. During this step, if the processor checks a voltage less than 4.15 V, it should wait for another CCCVI interrupt. As a safety reason, the processor should also ensure that the battery voltage doesn't exceed 4.2 V.

6.2 Example of USB 2.0 Charging - 100 and 500 mA Profile

If USB 2.0 is detected, the charge rate is set to 70 mA and the 90 minute timer starts. With USB 2.0, charging will always be 100 mA maximum and the processor will turn on when BATT = 3.4 V and not 3.2 V to avoid oscillation around 3.2 V because when the processor starts, it will consume more power than the USB can provide. When the processor starts, it can take over charging and change the termination method, but the charger will only deliver 100 mA maximum. If the processor does not take control, charging will stop either when the 90 minute timer expires or BATT = 4.05. Figure 6 shows the USB 2.0 charging curve with the100 mA profile and Figure 7 shows the USB 2.0 charging curve with 500 mA profile.

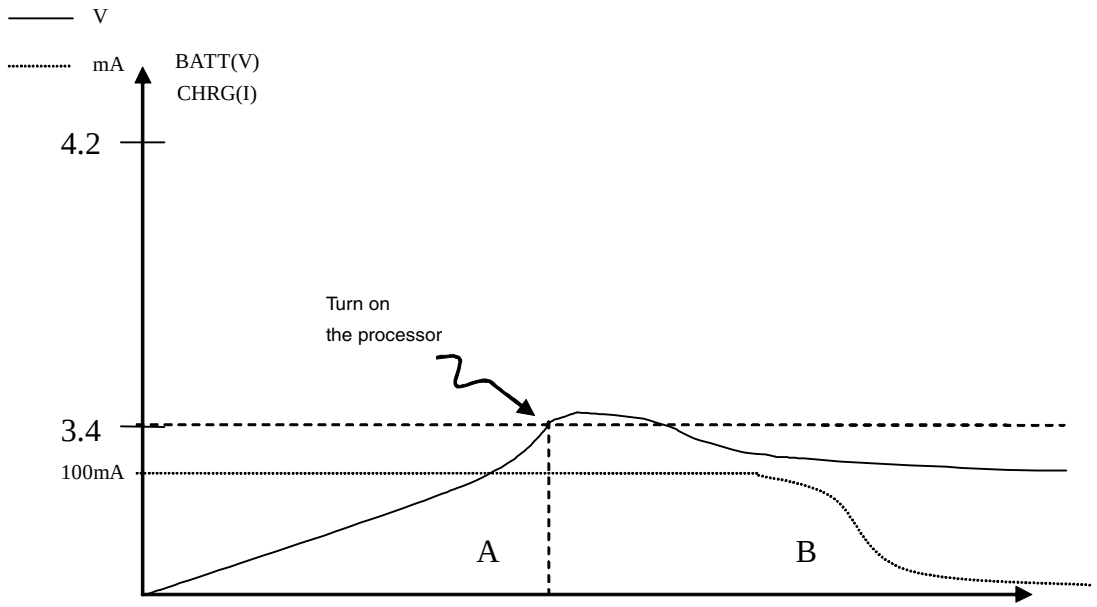

Figure 6. USB 2.0 Charging Curve with the 100 mA Profile

- Step A: The maximum charger available current passes through M1/M2 (100 mA).
- Step B: The processor doesn't reprogram ICHRG[3:0] to reduce current. It is automatically done in the hardware by the MC13783 because current regulation is automatic when battery voltage approaches 4.2 V.

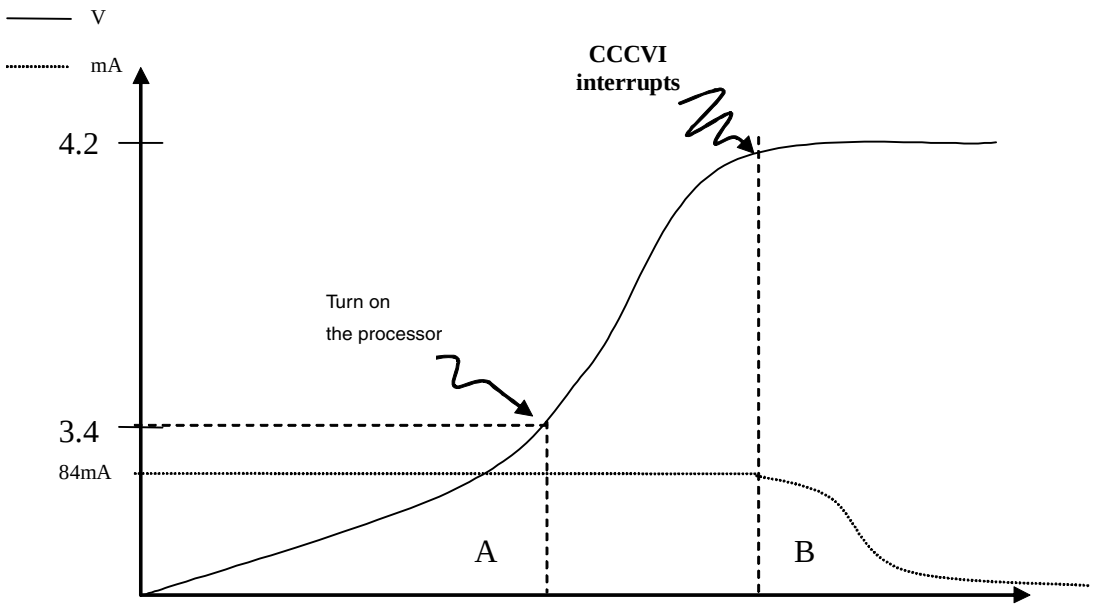

Figure 7. USB 2.0 Charging Curve with 500 mA Profile

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