

Design Checklist for PowerQUICC II Pro MPC8309 Processor

This application note describes the generally recommended connections for new designs based on Freescale's MPC8309 processor. The design checklist may also apply to future bus or footprint-compatible processors. It can also serve as a useful guide for debugging a newly-designed system, by highlighting those areas of a design that merit special attention during initial system startup.

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1 MPC8309 Background

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC II Pro device, the designer must be familiar with the available documentation, software, models, and tools.

1.1 References

Some references listed here may be available only under a nondisclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
 - *MPC8309 PowerQUICC II Pro Integrated Host Processor Reference Manual*
 - *MPC8309 PowerQUICC II Pro Integrated Host Processor Chip Errata*
 - *MPC8309 PowerQUICC II Pro Integrated Host Processor Hardware Specifications*
- Models
 - IBIS
 - BSDL

1.2 Device Errata

The device errata document describes the latest fixes and workarounds for the PowerQUICC II Pro family of devices. Carefully study these documents before starting a design with the respective PowerQUICC II Pro device.

1.3 Product Revisions

[Table 1](#) provides the product revision, package, SVR, and PVR details.

Table 1. PowerQUICC II Pro MPC8309 Product Revision

	Device	Package	SVR	PVR
Rev 1.1	MPC8309	489 I/O MAPBGA	0x8110_0011	0x8085_0020
Rev 1.0	MPC8309	489 I/O MAPBGA	0x8110_0010	0x8085_0020

2 Power

This section provides design considerations for the MPC8309 power supplies, as well as power sequencing. For information on MPC8309 AC and DC electrical specifications and thermal characteristics, refer to Hardware Specifications. For power sequencing recommendations, see [Section 2.3, “Power Sequencing.”](#)

2.1 Power Supply

The Hardware Specifications Sheet lists the recommended range for each power supply listed in [Table 2](#). External signals on the MPC8309 are not 5-V-tolerant. Note that absolute maximum ratings are stress

ratings only and functional operation beyond the recommended operating conditions is not guaranteed. Stresses beyond those listed under absolute maximum ratings may affect device reliability or permanently damage the device.

2.2 Power Consumption

The hardware specification document provides the power dissipation of V_{DD} for various configurations of the coherent system bus (CSB) and the e300 core frequencies. The document also estimates power dissipation for all the I/O power rails. I/O power highly depends on the application and is an estimate. A full analysis of your board implementation is required to define your I/O power supply needs. The typical V_{DD} power plus I/O power must be used for the thermal solution design. The junction temperature must not exceed the maximum specified value. The maximum V_{DD} power is the worst case power consumption and must be used for the core power supply design.

2.3 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. These rates depend on the power supply, the type of load on each power supply, and the manner in which different voltages are derived. However, advances in the PowerQUICC II Pro ESD design allows flexibility in the order in which power rails ramp up, as long as the supplies do not exceed absolute maximum ratings (as defined in the hardware specifications).

NOTE

From a system standpoint, if I/O power supplies ramp up before the V_{DD} core supply stabilizes there may be a period of time when the I/O pins are driven to a logic one or logic zero state. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most IP pins are three-stated. To minimize the time that I/O pins are actively driven, apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

Figure 1 shows a power sequencing example.

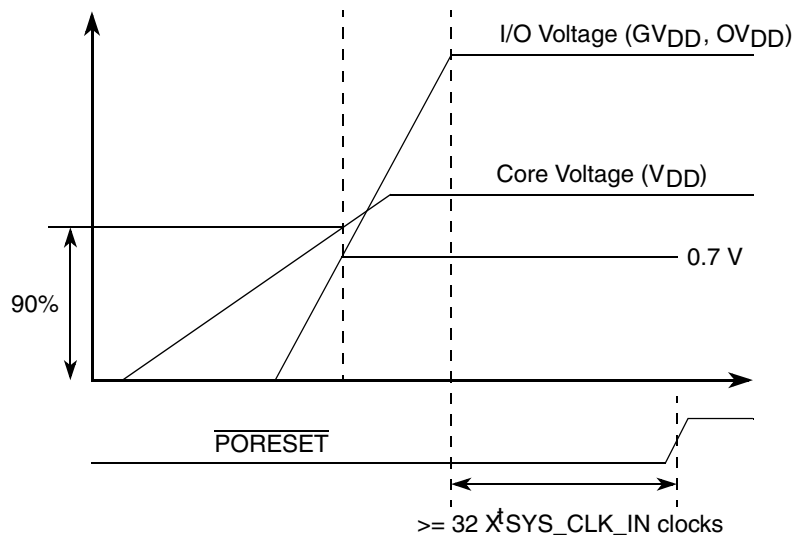


Figure 1. Power Sequencing Example

2.4 Power Planes

Each V_{DD} pin of the MPC8309 must be provided with a low-impedance path to the board power supply. Similarly, each ground pin must be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and ground must be kept to less than half an inch per capacitor lead.

2.5 Decoupling

Due to large address and data buses and high operating frequencies, the MPC8309 can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and it requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, GV_{DD} and OV_{DD} pin. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Other capacitors can surround the part. These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic surface mount technology (SMT) capacitors must be used to minimize lead inductance.

Additionally, several bulk storage capacitors must be distributed around the PCB, feeding the V_{DD}, GV_{DD}, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure quick response time. They should also connect to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–300 μF . Use simulation to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.6 PLL Power Supply Filtering

Each PowerQUICC II Pro PLL gets power through independent power supply pins (AV_{DD1} , AV_{DD2} , and AV_{DD3}). The AV_{DD} level should always equal V_{DD} , and preferably be derived directly from V_{DD} through a low pass filter scheme.

There are several reliable ways to provide power to the PLLs, but the recommended solution is to use independent filter circuits as illustrated in Figure 2, one to each of the three AV_{DD} pins, thus reducing noise injection from one PLL to the other.

This circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It must be built with SMT capacitors with a minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended instead of a single large value capacitor.

Place each circuit as closely as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin without the inductance of vias.

Figure 2 shows the PLL power supply filter circuit for System PLL(AV_{DD1}), QE PLL(AV_{DD2}), and Core PLL (AV_{DD3}).

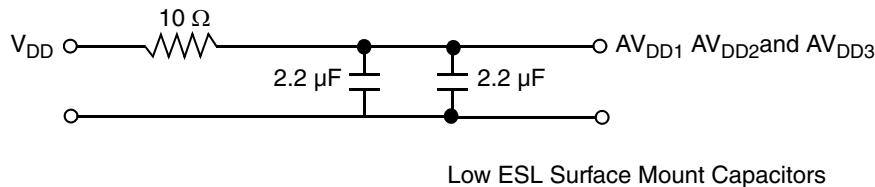


Figure 2. PLL Power Supply Filter Circuit

3 Pin Listing and Connections

Table 2 summarizes the power signal pins.

Table 2. Power Signal Pin Listing

Signal	Connection	Notes
AV_{DD1}	1.0 V \pm 50 mV	Analog power for e300 core PLL
AV_{DD2}	1.0 V \pm 50 mV	Analog power for system PLL
AV_{DD3}	1.0 V \pm 50 mV	Analog power for QE PLL
GV_{DD}	1.8 V \pm 100 mV	DDR2 I/O voltage
MVREF	0.49x GV_{DD} to 0.51 x GV_{DD}	DDR reference voltage

Table 2. Power Signal Pin Listing (continued)

Signal	Connection	Notes
V_{DD}	1.0 V \pm 50 mV	Core supply voltage
OV_{DD}	3.3 V \pm 300 mV	Standard I/O voltage

NOTE

All the power pins need to be tied to their corresponding voltages irrespective of the fact that a module is used or not in the system.

4 Clocking

Figure 3 shows the internal distribution of clocks within the MPC8309.

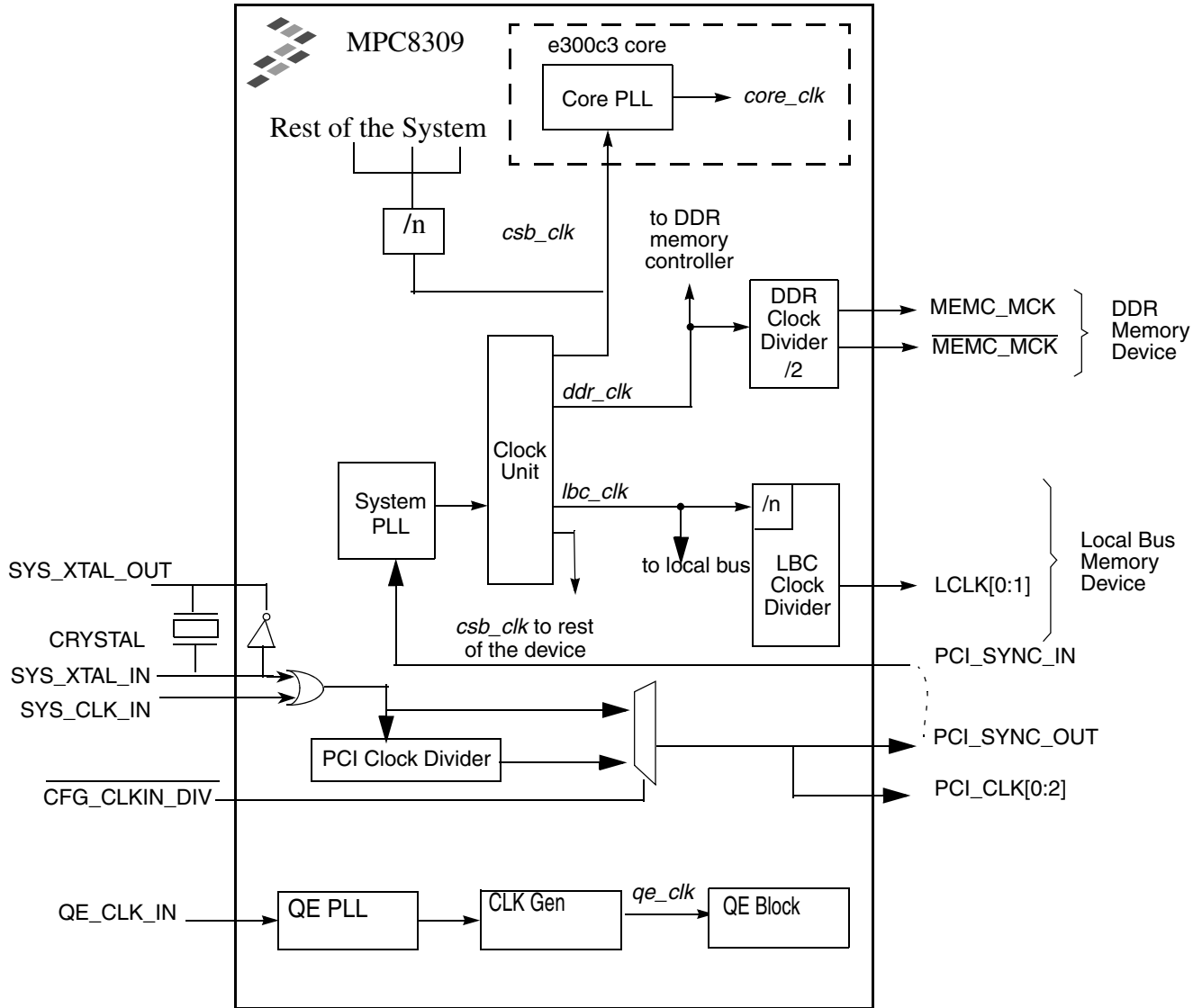


Figure 3. Clock Subsystem Block Diagram for MPC8309

The primary clock source for MPC8309 can be one of three inputs, Crystal (SYS_XTAL_IN), SYS_CLK_IN and PCI_SYNC_IN. The clock for QUICC Engine is derived from QE_CLK_IN. Table 3 lists the clock signal pins.

Table 3. Clock Signal Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
PCI_CLK[0:2]	O	As needed	Open, Should use OCCR to disable the output clock	<ul style="list-style-type: none"> • Device as PCI host: Functions as PCI output clock banks. OCCR register determines whether clocks are set as SYS_CLK_IN or SYS_CLK_IN÷2. • Device as PCI agent: These signals are not used.
PCI_SYNC_IN	I	Connect to PCI_SYNC_OUT or 25–66 MHz clock signals	Not applicable. This pin should always be connected	<ul style="list-style-type: none"> • Device as PCI host: Functions as PCI_SYNC_IN. Connect externally to PCI_SYNC_OUT. • Device as PCI agent: A valid 25–66.67 MHz clock signal (at OV_{DD} level) must be applied to this signal.
PCI_SYNC_OUT	O	Connect to PCI_SYNC_IN	Open, Should use OCCR to disable the output clock	<ul style="list-style-type: none"> • Device as PCI host: Connect externally to PCI_SYNC_IN signal for de-skewing of external PCI clock routing. Loop trace should match with PCI_CLKx signal traces. • Device as PCI agent: This signal is not used.
SYS_CLK_IN/ SYS_XTAL_IN and SYS_XTAL_OUT	I	Connect to 24–66.67 MHz clock signal	1 - 4.7kΩ to GND	Clock input. A valid 25–66.67 MHz clock signal (at OV _{DD} level) must be applied to this input. When an oscillator is used to feed SYS_CLK_IN, tie the SYS_XTAL_IN pin to GND and leave SYS_XTAL_OUT unconnected. When Crystal is connected across SYS_XTAL_IN and SYS_XTAL_OUT, tie SYS_CLK_IN to GND.
QE_CLK_IN	I	Connect to 24–66.67 MHz clock signal	1.5 kΩ to GND	QE Clock input. A valid 25–66.67 MHz clock signal (at OV _{DD} level) must be applied to this input when used.

4.1 System Clock in PCI Host Mode

When the MPC8309 is configured as a PCI host device (RCWH[PCIHOST] = 1), SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2), the PCI_SYNC_OUT and PCI_CLK multiplexers. PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal PCI controller clock to synchronize with the external PCI agent clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

PCI_CLK[0:2] output buffers are enabled by RCWH[PCICKDRV]. The individual PCI_CLK[0:2] can be disabled by clearing the OCCR[PCICOEn] bit. For example, if only one PCI clock is needed, then set RCWH[PCICKDRV] and configure OCCR[0:2] = 3'b100.

$\overline{\text{CFG_CLKIN_DIV}}$ selects whether SYS_CLK_IN or $\text{SYS_CLK_IN} \div 2$ is driven out on the PCI_SYNC_OUT and PCI_CLK[0:2] signals. If $\overline{\text{CFG_CLKIN_DIV}} = 0$, then the PCI interface runs at half the SYS_CLK_IN speed.

4.2 System Clock in PCI Agent Mode

In agent mode, the SYS_CLK_IN signal can be tied to GND. PCI_CLK n and PCI_SYNC_OUT are not used. When the device is configured as a PCI agent mode, the $\overline{\text{CFG_CLKIN_DIV}}$ configurations input can be used to double the internal clock frequencies, if sampled as '0' during power-on reset assertion. This feature is useful if a fixed internal frequency is desired regardless of whether the PCI clock is running at 33 or 66 MHz. PCI specification requires the PCI clock frequency information to be provided by the M66EN signal.

NOTE

M66EN is an input pin in the PCI interface that determines the frequency of PCI bus operation.

4.3 System Clock If PCI Is Disabled

If the PCI interface is not used, and PCI_SYNC_IN is the primary input clock, SYS_CLK_IN and CFG_CLKIN_DIV can be tied to GND. If a valid clock is connected to SYS_CLK_IN (as described in [Table 3.](#)), PCI_SYNC_OUT must be shorted to PCI_SYNC_IN. CFG_CLKIN_DIV has no effect on the output of the clock unit.

5 Power-On Reset and Reset Configurations

A detailed power-on reset flow is as follows:

1. Power to the device is applied.
2. The system asserts $\overline{\text{PORESET}}$ (and optionally $\overline{\text{HRESET}}$) and $\overline{\text{TRST}}$ initializing all registers to their default states.
3. The system applies a stable SYS_CLK_IN signal and stable reset configuration inputs (CFG_RESET_SOURCE).
4. The system negates $\overline{\text{PORESET}}$ after at least 32 stable SYS_CLK_IN clock cycles.
5. The device samples the reset configuration input signals to determine the reset configuration words source.
6. The device starts loading the reset configuration words. When the reset configuration word low is loaded, the system PLL and QE PLL begin to lock. When the system PLL is locked, the *csb_clk* is supplied to the e300 PLL. QE PLL takes approximately same time as System PLL to lock.
7. The e300 PLL begins to lock.

8. The device drives $\overline{\text{HRESET}}$ asserted until the e300 PLL is locked and until the reset configuration words are loaded.
9. If enabled, the boot sequencer loads configuration data from the serial EEPROM as described in the *MPC8309 PowerQUICC II Pro Integrated Host Processor Reference Manual*.

5.1 Reset Configuration Signals

Various device functions of the PowerQUICC II Pro are initialized by sampling certain signals during the assertion of the $\overline{\text{PORESET}}$ signal after a stable clock is supplied. These inputs are either pulled high or low. Although these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{PORESET}}$ is asserted. See Table 4 for termination recommendations for the reset configuration pins.

Table 4. Reset Configuration Pin Listing

Signal	Pin Type	Termination
$\overline{\text{PORESET}}$	I	Driven actively by the external reset logic
$\overline{\text{HRESET}}$	I/O	Pullup with 1.5 k Ω to OV_{DD}
HDLC1_TXD / GPIO[2] / TDM1_TD / CFG_RESET_SOURCE[0]	I/O	Pull up with 4.7 k Ω OV_{DD} or pulldown with 1 k Ω to GND as desired. OR Drive as needed during $\overline{\text{PORESET}}$ assertion and tri-state after $\overline{\text{PORESET}}$ negation
$\overline{\text{HDLC1_RTS}}$ / GPIO[6] / $\overline{\text{TDM1_STROBE}}$ / CFG_RESET_SOURCE[1]	I/O	
HDLC2_TXD / GPIO[18] / TDM2_TD / CFG_RESET_SOURCE[2]	I/O	The length of the stubs introduced by connecting the resistors or any other active device must be kept minimum. Failing to do so may distort the HDLC/TDM signals.
$\overline{\text{HDLC2_RTS}}$ / GPIO[22] / $\overline{\text{TDM2_STROBE}}$ / CFG_RESET_SOURCE[3]	I/O	

For the USBDR_PCTL[0]/UART2_SOUT[1]/LB_POR_CFG_BOOT_ECC signal, Figure 4 shows the circuit to disable ECC checking during boot-up.

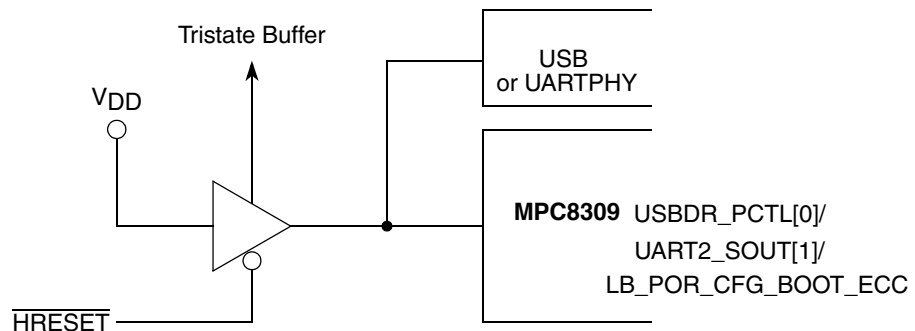


Figure 4. Recommended Circuit for Disabling ECC Checking during Boot-Up

The CFG_RESET_SOURCE[0:3] input signals are sampled during the assertion of $\overline{\text{PORESET}}$ to select the interface to load the reset configurations words:

- I²C interface
- A device (that is, CPLD, EEPROM, or Flash) on the local bus
- From an internally-defined Reset Configuration Word. See [Table 5](#).

Table 5. Reset Configuration Word Source

Reset Configuration Signal Name	Value (Binary)	Meaning
CFG_RESET_SOURCE[0:3]	0000	NOR FLASH
	0001	NAND Flash 8 bit small page
	0010	Reserved
	0011	Reserved
	0100	I ² C EEPROM
	0101	NAND Flash 8 bit large page
	0110	Reserved
	0111	Reserved
	1000	Hard coded option 0
	1001	Hard coded option 1
	1010	Hard coded option 2
	1011	NOR Flash
	1100	Hard coded option 4
	1101	Hard-coded Reset configuration word for eSDHC boot
	1110	Hard-coded Reset configuration word for eSDHC boot
	1111	Hard-coded Reset configuration word for SPI boot

5.2 Reset Configuration Words

The reset configuration words control the clock ratios and other basic device functions such as boot location and endian mode. The reset configuration words are loaded from the local bus or from the I²C interface during the power-on or hard reset flows.

For more details, refer to *MPC8309 PowerQUICC II Pro Integrated Host Processor Reference Manual*.

5.3 Useful System POR Debug Registers

The hardware reset configuration settings can be read in the reset configuration word low register (RCWLR), the reset configuration word high register (RCWHR), the reset status register (RSR), and the system PLL mode register (SPMR). For more information, see the *MPC8309 PowerQUICC II Pro Integrated Host Processor Reference Manual*. Note that all of these registers are read-only, except RSR.

5.4 Boot Sequencer

The boot sequencer provides the means to load the hardware reset configuration word and to configure any memory-mapped register before the boot-up code runs. Reset configuration loading mode is selected based on the settings of the CFG_RESET_SOURCE pins during the power-on reset sequence. The I²C interface loads the reset configuration words from an EEPROM at a specific calling address while the rest of the device is in the reset state. When the reset configuration words are latched inside the device, I²C is reset until $\overline{\text{HRESET}}$ is negated. Then the device is initialized using boot sequencer mode.

Boot sequencer mode is selected at power-on reset by the BOOTSEQ field in the reset configuration word high register (RCWH). If the boot sequencer mode is selected, the I²C module communicates with one or more EEPROM through the I²C interface to initialize one or more configuration register of the MPC8309. For the complete data format for programming the I²C EEPROM, refer to *MPC8309 PowerQUICC II Pro Integrated Host Processor Reference Manual*.

The boot sequencer contains a basic level of error detection. If the I²C boot sequencer fails while loading the reset configuration words are loaded, the RSR[BSF] bit is set. If a preamble or CRC fail is detected in boot sequencer mode, there is no internal or external indication that the boot sequencer operation failed. Use one of the GPIO pins for that purpose.

5.5 HRESET

The $\overline{\text{HRESET}}$ signal is not a pure input signal. It is an open-drain signal that the MPC8309 processor can drive low. The connection on the left side of Figure 5 causes signal contention and must not be used.

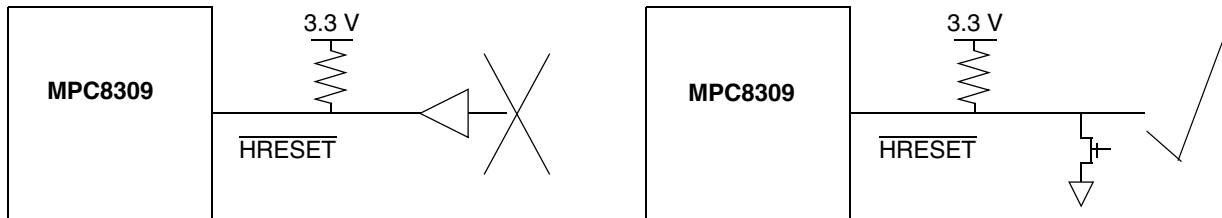


Figure 5. $\overline{\text{HRESET}}$ Connection

6 JTAG and Debug

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 7. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior, and spurious assertion give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE® Std 1149.1 specification, but it is provided on all processors that implement the Power Architecture®. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the

power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not recommended if JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to control the processor fully. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 7](#) allows the COP port to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in [Figure 6](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 6](#) is common to all known emulators.

If the JTAG interface and COP header are not used, Freescale recommends all of the following connections:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{PORESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 7](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- There are on-chip pull-up resistors for TDI, TMS, and TRST_B.

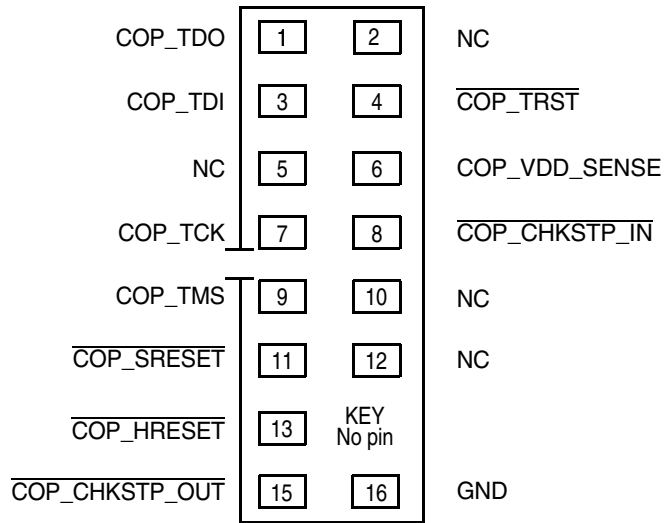


Figure 6. COP Connector Physical Pinout

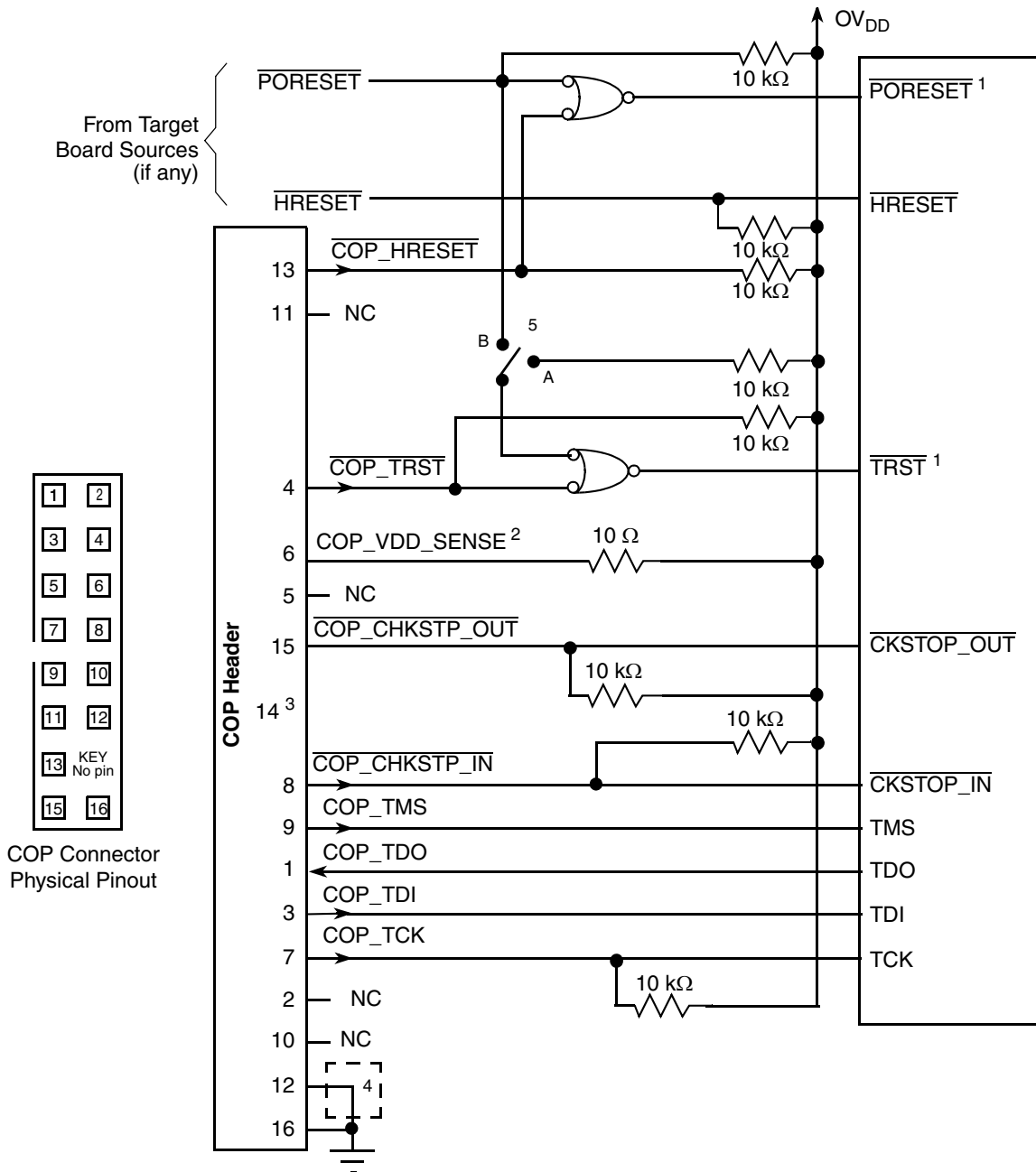


Figure 7. JTAG Interface Connection

Notes:

1. The COP port and target board must be able to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to the processor to control the processor fully as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.

Table 6 details the termination recommendations for the JTAG, TEST, PMC, and thermal management pins.

Table 6. JTAG and TEST Pin Listing

Signal	Pin Type	Termination		Notes
		If used	If not used	
TCK	I	As needed + 10 k Ω to OV _{DD}	10 k Ω to OV _{DD}	Commonly used for boundary scan testing. If this pin is truly not used, it can be tied directly to GND.
TDI	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
TDO	O	As needed	Open	Actively driven during RESET
TMS	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
$\overline{\text{TRST}}$	I	Tie to the output of a Negative OR gate	Tie to $\overline{\text{PORESET}}$ through a 0 k Ω	This JTAG pin has a weak internal pull-up P-FET that is always enabled. If an In-Circuit Emulator is used in the design, $\overline{\text{TRST}}$ must be tied to the output of a Negative OR gate logic. The inputs to the Negative OR gate logic must be any external $\overline{\text{TRST}}$ source and the $\overline{\text{PORESET}}$ signal
Test				
TEST_MODE	I	Tie directly to GND		—
DEBUG				
$\overline{\text{QUIESCE}}$	O	As needed	Open	—
Thermal Management				
THERM0	I	As needed	Tie to GND	Thermal sensitive resistor

7 Functional Blocks

This section presents the recommendations and guidelines for designing with various functional blocks on the MPC8309.

7.1 DDR2 SDRAM

For details on layout consideration and DDR programming guidelines, refer to the following application notes:

- AN2910: *Hardware and Layout Design Considerations for DDR2 Memory Interfaces*, for signal integrity and layout considerations.
- AN3369: *PowerQUICC™ III DDR2 SDRAM Controller Register Setting Considerations*, for DDR programming guidelines.

Table 7 summarizes the DDR SDRAM pins.

Table 7. DDR SDRAM Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
MEMC_MDQ[0:31]	I/O	As needed	Open	When in use, proper signal integrity analysis must be performed using the respective device IBIS model. Parallel termination is optional for DDR signals and must be simulated to verify necessity.
MEMC_MECC[0:7]	I/O	As needed	open	When in use, proper signal integrity analysis must be performed using the respective device IBIS model. Parallel termination is optional for DDR signals and must be simulated to verify necessity.
MEMC_MDM[0:3]	O	As needed	Open	—
MEMC_MDQS[0:3]	I/O	As needed	Open	—
MEMC_MBA[0:2]	O	As needed	Open	—
MEMC_MA[0:13]	O	As needed	Open	—
$\overline{\text{MEMC_MWE}}$	O	As needed	Open	—
$\overline{\text{MEMC_MRAS}}$	O	As needed	Open	—
$\overline{\text{MEMC_MCAS}}$	O	As needed	Open	—
$\overline{\text{MEMC_MCS}}[0:1]$	O	As needed	Open	—
MEMC_MCKE	O	As needed	Open	This output is actively driven during reset rather than being three-stated during reset.
MEMC_MCK[0:1]	O	As needed	Open	—
$\overline{\text{MEMC_MCK}}[0:1]$	O	As needed	Open	—
MEMC_MODT[0:1]	O	As needed	Open	—

7.2 Enhanced Local Bus Controller

The eLBC provides one GPCM, one FCM, and three UPMs for the local bus, with no restriction on how many of the eight banks (chip selects) can be programmed to operate with any given machine. When a memory transaction is dispatched to the eLBC, the memory address is compared with the address information of each bank. The corresponding machine assigned to that bank (GPCM, FCM or UPM) then takes ownership of the external signals that control the access and maintains control until the transaction ends. Thus, with the eLBC in GPCM, FCM, or UPM mode, only one of the eight chip selects is active at any time for the duration of the transaction.

The local bus clock is not configured while it is executing from the local bus, but rather by executing code from the DDR. The PowerQUICC II Pro local bus features a multiplexed address and data bus, LAD[0:15]. An external latch is required to de-multiplex these signals to the connecting device.

7.2.1 Local Bus Address

Figure 8 shows the correct way to make the address for the local bus.

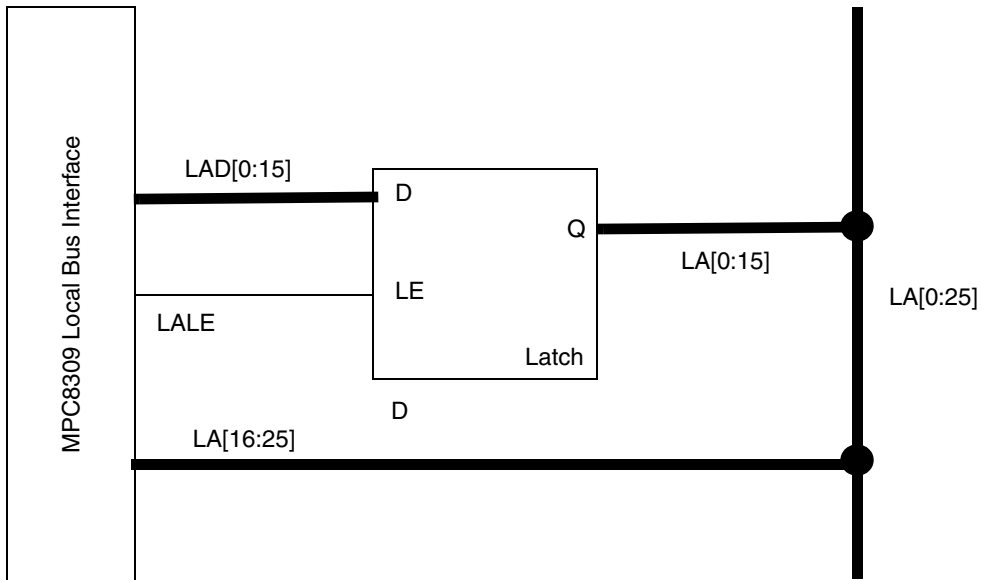


Figure 8. Local Bus Address

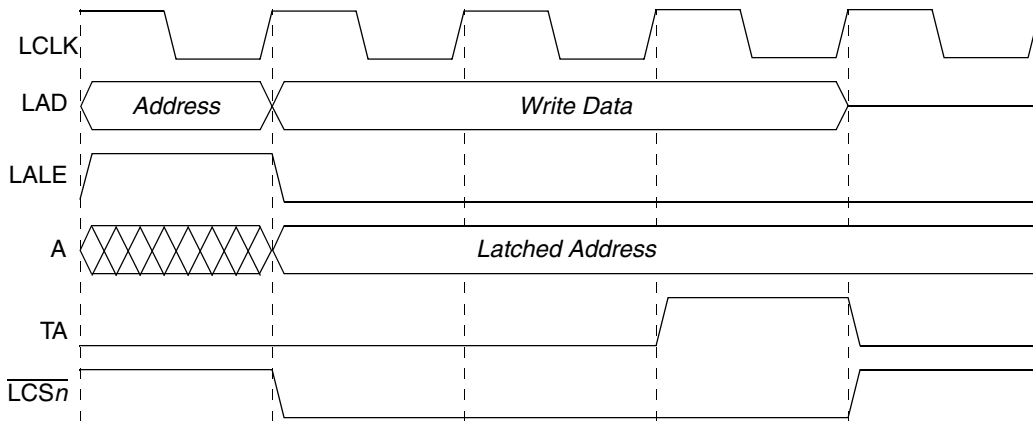


Figure 9. LALE Timing

For every assertion of $\overline{\text{LCSn}}$, LALE is asserted first. While LALE is asserted, all other control signals are negated. The duration of LALE can be programmed to 1–4 cycles in LCRR[EADC]. The default is 4 cycles. The timing of LALE negation is important to ensure that the correct address is latched.

Table 8 lists guidelines for connecting to 8-bit, and 16-bit devices. LAD[0] is the most significant address and data bit, and LAD[15] is the least significant address and data bit. Note that for a 16-bit port

connection, the address LA[25] is normally not required because byte lane control is achieved through signals as outlined in [Table 8](#).

Table 8. Local Bus Byte Lane Control

Device Data Width	Address	Data	Byte Lane Control		
			GPCM	FCM	UPM
8-bit	LA[0:25]	LAD[0:7]	$\overline{\text{LWE}}[0]$	LFWE	$\overline{\text{LBS}}[0]$
16-bit	LA[0:24]	LAD[0:15]	$\overline{\text{LWE}}[0:1]$	—	$\overline{\text{LBS}}[0:1]$

7.2.2 NAND Flash Interface

The FCM provides a glueless interface to parallel-bus NAND flash EEPROM devices. The [Figure 10](#) shows a simple connection between an 8-bit port size NAND Flash EEPROM and the eLBC in FCM mode. Commands, address bytes and data are all transferred on LAD[0:7].

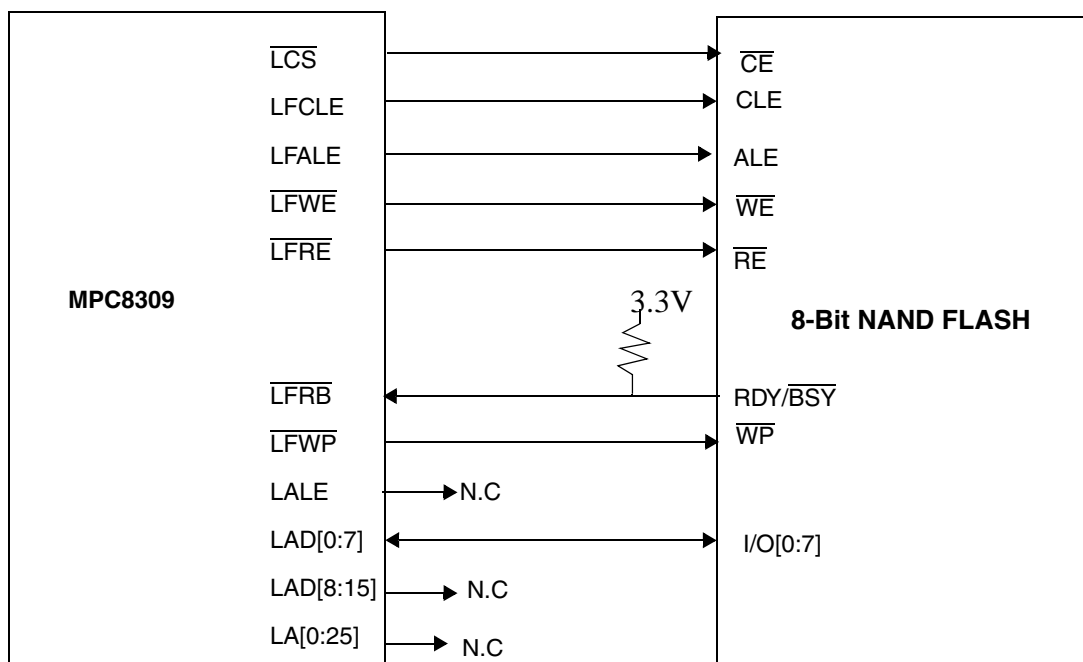


Figure 10. NAND Flash Connection Diagram

Table 9 summarizes the local bus pins.

Table 9. Local Bus Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
LAD[0:15]	I/O	As needed	Open	—
LA[16:25]	O	As needed	Open	—
$\overline{\text{LCS}}[0:3]$	O	As needed	Open	—
$\overline{\text{LWE}}/\overline{\text{LFW}}/\overline{\text{LBS}}$	O	As needed	Open	—
LBCTL	O	As needed	Open	—
LALE	O	As needed	Open	—
LGPL0/LFCLE	O	As needed	Open	—
LGPL1/LFALE	O	As needed	Open	—
LGPL2/ $\overline{\text{LFRE}}/\overline{\text{LOE}}$	O	As needed	Open	—
LGPL3/ $\overline{\text{LFWP}}$	O	As needed	Open	—
LGPL4/ $\overline{\text{LGTA}}/\overline{\text{LUPWAIT}}/\overline{\text{LFRB}}$	I/O	As needed	4.7k Ω – 10k Ω to OVDD	Output when configured as LGPL4.
LGPL5	O	As needed	Open	—
LCLK[0:1]	O	As needed	Open	—

Note: Refer to Table 13 for $\overline{\text{LCS}}[4:7]$.

7.3 PCI Bus Interface

The reset configuration word high controls the hardware configuration of the PCI blocks as follows:

- RCWH[PCIHOST]— Host/agent mode for PCI
- RCWH[PCIARB]—PCI internal/external arbiter mode select.

As Table 10. shows, signals of the PCI interface are multiplexed with the CompactPCI Hot Swap pins. Either PCI or Hot Swap functionality is selected by the RCWH[PCIARB] bit setting. When an external arbiter is selected (RCWH[PCIARB] = 0), the CompactPCI Hot Swap pins function. When an internal arbiter is selected (RCWH[PCIARB] = 1), the $\overline{\text{GNT}}_x/\overline{\text{REQ}}_x$ pins function. Refer to the *MPC8309 PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for details on the reset configuration word high settings.

Table 10. PCI Bus Interface Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
PCI_INTA	O	2 k–10 k Ω to OV _{DD}	Open	Open drain signal. In agent mode, $\overline{\text{INTA}}$ typically connects to a central interrupt controller.
PCI_RESET_OUT	O	As needed	Open	This signal is used only in host mode. It must be left unconnected in agent mode.
PCI_AD[31:0]	I/O	As needed	2 k–10 k Ω to OV _{DD} or Open	If the PCI port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCIARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1
PCI_C / $\overline{\text{BE}}$ [3:0]	I/O	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD} or Open	If the PCI port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCIARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1
PCI_PAR	I/O	As needed	2 k–10 k Ω to OV _{DD}	If the PCI port is not used, this signal must be pulled up.
PCI_FRAME	I/O	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI}}_{\text{TRDY}}$	I/O	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	PCI specification requires a weak pullup.
PCI_IRDY	I/O	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	PCI specification requires a weak pullup.

Table 10. PCI Bus Interface Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{PCI_STOP}}$	I/O	As needed + 2 k–10 k Ω to OV_{DD}	2 k–10 k Ω to OV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI_DEVSEL}}$	I/O	As needed + 2 k–10 k Ω to OV_{DD}	2 k–10 k Ω to OV_{DD}	PCI specification requires a weak pullup.
PCI_IDSEL	I	PCI host: Tie to GND PCI agent: One of PCI_AD[31:0]	Tie to GND using 4.7K	IDSEL must be connected to GND for host systems and to one address line for agent systems. If the PCI port is not used, it must be grounded. <ul style="list-style-type: none"> • PCI host is selected by RCWH[PCIHOST] = 1. • PCI agent is selected by RCWH[PCIHOST] = 0.
$\overline{\text{PCI_SERR}}$	I/O	As needed + 2 k–10 k Ω to OV_{DD}	2 k–10 k Ω to OV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI_PERR}}$	I/O	As needed + 2 k–10 k Ω to OV_{DD}	2 k–10 k Ω to OV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI_REQ0}}$	I/O	External arbiter: As needed Internal arbiter: As needed + 2 k–10 k Ω to OV_{DD}	External arbiter: Open Internal arbiter: 2 k–10 k Ω to OV_{DD}	If an external arbiter is used, $\overline{\text{REQ0}}$ becomes an <i>output</i> signal and does not need to be terminated. <ul style="list-style-type: none"> • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI_REQ1}}$ / CPCI_HS_ES	I	External arbiter: As needed Internal arbiter: As needed + 2 k–10 k Ω to OV_{DD}	2 k–10 k Ω to OV_{DD}	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. <ul style="list-style-type: none"> • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI_REQ2}}$	I	As needed + 2 k–10 k Ω to OV_{DD}	2 k–10 k Ω to OV_{DD}	—

Table 10. PCI Bus Interface Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{PCI_GNT}}[0]$	I/O	External arbiter: As needed + 2 k–10 k Ω to OV_{DD} Internal arbiter: As needed	External arbiter: 2 k–10 k Ω to OV_{DD} Internal arbiter: Open	If an external arbiter is used, $\overline{\text{GNT}}0$ becomes an <i>input</i> signal and must be pulled up with 2 k–10 k Ω to OV_{DD} . <ul style="list-style-type: none"> External arbiter selected by $\text{RCWH}[\text{PCIARB}] = 0$. Internal arbiter selected by $\text{RCWH}[\text{PCIARB}] = 1$.
$\overline{\text{PCI_GNT}}[1]/$ CPCI_HS_LED	O	As needed	Open	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. <ul style="list-style-type: none"> External arbiter selected by $\text{RCWH}[\text{PCIARB}] = 0$. Internal arbiter selected by $\text{RCWH}[\text{PCIARB}] = 1$.
$\overline{\text{PCI_GNT}}[2]/$ CPCI_HS_ENUM	O	External arbiter: As needed + 2 k–10 k Ω to OV_{DD} Internal arbiter: As needed	External arbiter: Open Internal arbiter: Open	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. <ul style="list-style-type: none"> If CompactPCI Hot Swap function is used, a weak pullup is required (2 k–10 kΩ to OV_{DD}). External arbiter selected by $\text{RCWH}[\text{PCIARB}] = 0$. Internal arbiter selected by $\text{RCWH}[\text{PCIARB}] = 1$.
$\overline{\text{PCI_PME}}$	O	As needed 2 k–10 k Ω to OV_{DD}	Open	Open-drain signal. No role if PCI is not used.
M66EN	I	As needed	5 k Ω to OV_{DD} or 1 k Ω to GND	Open-drain signal. No role if PCI is not used.

7.4 Universal Serial Bus

Figure 11 shows the USB interface block diagram.

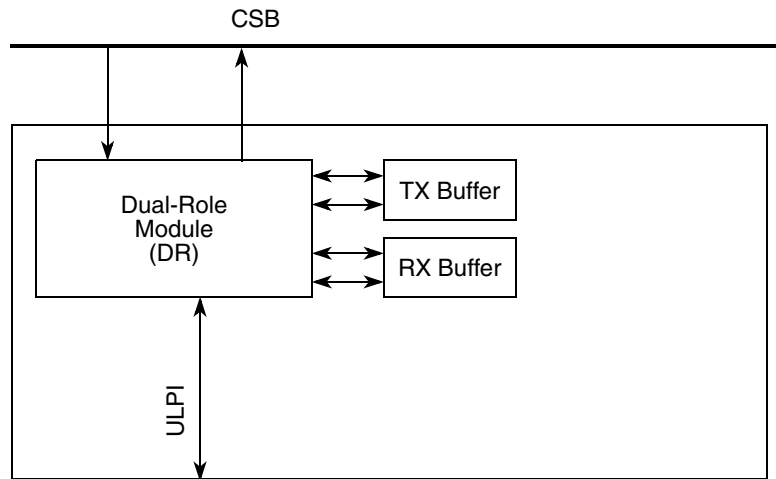


Figure 11. USB Interface Block Diagram

The USB DR module is a USB 2.0-compliant serial interface engine for implementing a USB interface. The DR controller can act as a device or host controller. Interfaces to negotiate the host or device role on the bus in compliance with the on-the-go (OTG) supplement to the USB specification are also provided. The DR module supports the required signaling for UTMI low pin count interface (ULPI) transceivers (PHYs). The PHY interfacing to the ULPI is an external PHY.

The USB DR module has three basic operating modes—host, device, and OTG. Table 11 lists the ULPI pins.

Table 11. ULPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_TXDRXD[0] / GPIO[32]	I/O	As needed	Open	Pin functionality determined by SICR_2[12-13] bit setting
USBDR_TXDRXD[1] / GPIO[33]	I/O	As needed	Open/ 2 k–10 kΩ to OV _{DD}	Can be left open if USB function is chosen for this pin and it is unused. Pull up required if QE function is chosen for this pin and it is unused. Pin functionality determined by SICR_2[12-13] bit setting
USBDR_TXDRXD[2] / GPIO[34] / QE_BRG[1]	I/O	As needed	Open	Pin functionality determined by SICR_2[12-13] bit setting

Table 11. ULPI Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_TXDRXD[3]/ GPIO[35] / QE_BRG[2]	I/O	As needed	Open/ 2 k–10 kΩ to OV _{DD} /	Can be left open if USB/QE function is chosen for this pin and it is unused. Pin functionality determined by SICR_2[12-13] bit setting
USBDR_TXDRXD[4]/ GPIO[36] / QE_BRG[3]	I/O	As needed	Open	Pin functionality determined by SICR_2[12-13] bit setting
USBDR_TXDRXD[5]/ GPIO[37] / QE_BRG[4]	I/O	As needed	Open	Pin functionality determined by SICR_2[12-13] bit setting
USBDR_TXDRXD[6]/ GPIO[38] / QE_BRG[9]	I/O	As needed	Open	The USB interface cannot be enabled on designs that require BRG9 to be driven by 8309. For example, while interfacing the TDM_2 controller with a voice SLIC device, a Frame Sync signal must be driven by 8309 on BRG9. Pin functionality determined by SICR_2[12-13] bit setting
USBDR_TXDRXD[7] / GPIO[39] / QE_BRG[11]	I/O	As needed	Open	Pin functionality determined by SICR_2[12-13] bit setting
USBDR_CLK/ UART2_SIN[2]/ UART2_CTS[1]	I	As needed	2 k–10 kΩ to OV _{DD} /	Pin functionality determined by SICR_1[24-25] bit setting.
USBDR_NXT/ UART2_SIN[1]/ UC1_URM/ QE_EXT_REQ_4	I/O	As needed	2 k–10 kΩ to OV _{DD} /	Pin functionality determined by SICR_1[22-23] bit setting
USBDR_DIR / URM_TRIG	I/O	As needed	2 k–10 kΩ to OV _{DD}	Pin functionality determined by SICR_1[26-27] bit setting
USBDR_STP / UC3_URM / QE_EXT_REQ_2	I/O	As needed	Open / 2 k–10 kΩ to OV _{DD}	Can be left open if USB function is chosen for this pin and it is unused. Pull up required if QE function is chosen for this pin and it is unused. Pin functionality determined by SICR_1[26-27] bit setting
USBDR_PWRFAULT / CE_PIO[1]	I	As needed	1 kΩ to GND/ Open	Pull down to be used if USB function is chosen for this pin and it is unused. Can be left open if CE_PIO_1 function is chosen for this pin and it is unused. Pin functionality determined by SICR_1[26-27] bit setting

Table 11. ULPI Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDP_PCTL[0] / UART2_SOUT[1] / UC2_URM / LB_POR_CFG_BOOT_E CC	I/O	As needed	Open	Can be left open if USB/UART function is chosen for this pin and it is unused. When used as LB_POR_CFG_BOOT_ECC: Pull up with 1.5k Ω to OV _{DD} ; no pull down resistor required when logic 0 needs to be driven as the internal pull down is implemented in SOC OR Driven as needed during $\overline{\text{HRESET}}$ assertion and tri-state after $\overline{\text{HRESET}}$ negation. Pin functionality determined by SICR_1[22-23] bit setting
USBDP_PCTL[1] / UART2_SOUT[2] / UART2_RTS[1] / LB_POR_BOOT_ERR	O	As needed	Open	Pin functionality determined by SICR_1[24-25] bit setting

7.5 Integrated Programmable Interrupt Controller

The integrated programmable interrupt controller (IPIC) provides interrupt management for receiving hardware-generated interrupts from internal and external sources. It also prioritizes and delivers the interrupts to the CPU for servicing. The $\overline{\text{IRQ}}$ lines are multiplexed with signals CKSTOP_IN and CKSTOP_OUT interface pins. The configuration of each $\overline{\text{IRQ}}$ pin is programmed using the system I/O configuration register 2 (SICR_2).

Table 12 summarizes the programmable interrupt controller pins.

Table 12. Programmable Interrupt Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{IRQ}}[0]/\overline{\text{MCP_IN}}$	I	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	—
$\overline{\text{IRQ}}[1]/\overline{\text{MCP_OUT}}$	I/O	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	—
$\overline{\text{IRQ}}[2]/$ CKSTOP_IN	I/O	As needed + 2k–10k to OV _{DD}	2k–10k to OV _{DD}	—
$\overline{\text{IRQ}}[3]/$ CKSTOP_OUT	I	As needed + 2k–10k to OV _{DD}	2k–10k to OV _{DD}	—

7.6 DUART

Table 13 lists the dual UART pins.

Table 13. Dual UART Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
UART1_SOUT[1]/ $\overline{\text{LCS}}[4]$	O	As needed	Open	—
UART1_SIN[1]/ $\overline{\text{LCS}}[5]$	I/O	As needed	2 k–10 k Ω to OV _{DD} / Open	Pull up required if UART function is chosen for this pin and it is unused. Can be left open if $\overline{\text{LCS}}$ function is chosen for this pin and it is unused.
UART1_SOUT[2]/ $\overline{\text{UART1_RTS}}[1]/$ $\overline{\text{LCS}}[6]$	O	As needed	Open	—
$\overline{\text{UART1_SIN}}[2]/$ $\overline{\text{UART1_CTS}}[1]/$ $\overline{\text{LCS}}[7]$	I/O	As needed	2 k–10 k Ω to OV _{DD} / Open	Pull up required if UART function is chosen for this pin and it is unused. Can be left open if $\overline{\text{LCS}}$ function is chosen for this pin and it is unused.
USBDR_PCTL[0] / UART2_SOUT[1] / LB_POR_CF G_BOOT_ECC	O	As needed	Open	—
USBDR_NXT / UART2_SIN[1] / QE_EXT_REQ_4	I/O	As needed	2 k–10 k Ω to OV _{DD} / Open	Pull up required if UART function is chosen for this pin and it is unused. Can be left open if $\overline{\text{LCS}}$ function is chosen for this pin and it is unused.
USBDR_PCTL[1] / $\overline{\text{UART2_SOUT}}[2] /$ $\overline{\text{UART2_RTS}}[1] /$ LB_POR_BOOT_E RR	O	As needed	Open	—
USBDR_CLK / UART2_SIN[2] / $\overline{\text{UART2_CTS}}[1]$	I/O	As needed	2 k–10 k Ω to OV _{DD} / Open	Pull up required if UART function is chosen for this pin and it is unused. Can be left open if $\overline{\text{LCS}}$ function is chosen for this pin and it is unused.

7.7 I²C Interface

There are two I²C ports. Table 14 lists the I²C1 pins.

Table 14. I²C Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
IIC_SCL1	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	Open-drain signal
IIC_SDA1	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	Open-drain signal
IIC_SCL2	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	Open-drain signal
IIC_SDA2	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	Open-drain signal

7.8 SPI

Table 15 lists the SPI pins.

Table 15. SPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SPI MOSI	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	—
SPI MISO	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	—
SPI CLK	I/O	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	—
SPI SEL	I	As needed + 2 k–10 kΩ to OV _{DD}	2 k–10 kΩ to OV _{DD}	Must be used when SPI is configured as slave
$\overline{\text{SPI SEL_BOOT}}$	I/O	As needed + 2 k–10 kΩ to OV _{DD}	Open/ 2 k–10 kΩ to OV _{DD}	Pull up required if IIC_SDA2 function is chosen for this pin and it is unused. Can be left open if $\overline{\text{SPI SEL_BOOT}}$ or $\overline{\text{CKSTOP_OUT}}$ function is chosen for this pin and it is unused.

7.9 QUICC Engine Communication Interfaces

The QUICC Engine Communication interfaces include three Fast Ethernet Controllers (FEC) and HDLC/TDM ports.

7.9.1 Fast Ethernet Controller

QEULite supports three FECs on UCC1, UCC2, and UCC3. The FECs support the following interfaces:

- Media Independent Interface (MII)
- Reduced Media Independent Interface (RMII)

A dedicated set of Ethernet Management signals (FEC_MDC and FEC_MDIO) is available for management of external devices connected on these interfaces.

Table 16 lists the FEC pins.

Table 16. FEC Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
FEC_MDC	O	As needed	Open	—
FEC_MDIO	I/O	As needed + 2 k–10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	Open drain signal
FEC1_COL/ GTM1_TIN[1]/ GPIO[16]	I/O	As needed	1 k Ω to GND	—
FEC1_CRS/ GTM1_TGATE[1]/ GPIO[17]	I/O	As needed	1 k Ω to GND	—
FEC1_RX_CLK/ GPIO[18]	I/O	As needed	1 k Ω to GND	—
FEC1_RX_DV/ GTM1_TIN[2]/ GPIO[19]	I/O	As needed	1 k Ω to GND	—
FEC1_RX_ER/ GTM1_TGATE[2]/ GPIO[20]	I/O	As needed	1 k Ω to GND	—
FEC1_RXD[0]/ GPIO[21]	I/O	As needed	1 k Ω to GND	—
FEC1_RXD[1]/ GTM1_TIN[3]/ GPIO[22]	I/O	As needed	1 k Ω to GND	—
FEC1_RXD[2]/ GTM1_TGATE[3]/ GPIO[23]	I/O	As needed	1 k Ω to GND	—
FEC1_RXD[3]/ GPIO[24]	I/O	As needed	1 k Ω to GND	—

Table 16. FEC Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
FEC1_TX_CLK/ GTM1_TIN[4]/ GPIO[25]	I/O	As needed	1 k Ω to GND	—
FEC1_TX_EN/ GTM1_TGATE[4]/ GPIO[26]	I/O	As needed	Open/ 2 k–10 k Ω to OV _{DD}	Can be left open if FEC1_TX_EN/GPIO_26 function is chosen for this pin and it is unused. Pull up required if GTM1_TGATE4 is chosen for this pin and it is unused.
FEC1_TX_ER/ GTM1_TOUT[4]/ GPIO[27]	I/O	As needed	Open	—
FEC1_TXD[0]/ GTM1_TOUT[1]/ GPIO[28]	I/O	As needed	Open	—
FEC1_TXD[1]/ GTM1_TOUT[2]/ GPIO[29]	I/O	As needed	Open	—
FEC1_TXD[2]/ GTM1_TOUT[3]/ GPIO[30]	I/O	As needed	Open	—
FEC1_TXD[3]/ GPIO[28]	I/O	As needed	Open	—
FEC2_COL/ GPIO[32]	I/O	As needed	1 k Ω to GND	—
FEC1_CRS / GPIO[33]	I/O	As needed	1 k Ω to GND	—
FEC2_RX_CLK/ GPIO[34]	I/O	As needed	1 k Ω to GND	—
FEC2_RX_DV/ GPIO[35]	I/O	As needed	1 k Ω to GND	—
FEC2_RX_ER/ GPIO[36]	I/O	As needed	1 k Ω to GND	—
FEC2_RXD[0] / GPIO[37]	I/O	As needed	1 k Ω to GND	—
FEC2_RXD[1] / GPIO[38]	I/O	As needed	1 k Ω to GND	—
FEC2_RXD[2] / GPIO[39]	I/O	As needed	1 k Ω to GND	—

Table 16. FEC Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
FEC2_RXD[3] / GPIO[40]	I/O	As needed	1 k Ω to GND	—
FEC2_TX_CLK/ GPIO[41]	I/O	As needed	1 k Ω to GND	—
FEC2_TX_EN / GPIO[42]	I/O	As needed	Open	—
FEC2_TX_ER / GPIO[43]	I/O	As needed	Open	—
FEC2_TXD[0] / GPIO[44]	I/O	As needed	Open	—
FEC2_TXD[1]/ GPIO[45]	I/O	As needed	Open	—
FEC2_TXD[2] / GPIO[46]	I/O	As needed	Open	—
FEC2_TXD[3] / GPIO[47]	I/O	As needed	Open	—
FEC3_COL / GPIO[48]	I/O	As needed	1 k Ω to GND	—
FEC3_CRS / GPIO[49]	I/O	As needed	1 k Ω to GND	—
FEC3_RX_CLK/ GPIO[50]	I/O	As needed	1 k Ω to GND	—
FEC3_RX_DV / GPIO[51]	I/O	As needed	1 k Ω to GND	—
FEC3_RX_ER / GPIO[52]	I/O	As needed	1 k Ω to GND	—
FEC3_RXD[0] / GPIO[53]	I/O	As needed	1 k Ω to GND	—
FEC3_RXD[1] / GPIO[54]	I/O	As needed	1 k Ω to GND	—
FEC2_RXD[2] / GPIO[55]	I/O	As needed	1 k Ω to GND	—
FEC2_RXD[3] / GPIO[56]	I/O	As needed	1 k Ω to GND	—
FEC3_TX_CLK/ GPIO[57]	I/O	As needed	1 k Ω to GND	—
FEC3_TX_EN / GPIO[58]	I/O	As needed	Open	—

Table 16. FEC Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
FEC3_TX_ER / GPIO[59]	I/O	As needed	Open	—
FEC3_TXD[0]/ GPIO[60]	I/O	As needed	Open	—
FEC3_TXD[1] / GPIO[61]	I/O	As needed	Open	—
FEC3_TXD[2] / GPIO[62]	I/O	As needed	Open	—
FEC3_TXD[3] / GPIO[63]	I/O	As needed	Open	—

7.9.2 HDLC/TDM Ports

The QUICC Engine supports two HDLC/TDM ports.

Table 17 lists the HDLC/TDM port signals.

Table 17. HDLC/TDM Port Signals

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
HDLC1_RXCLK/ TDM1_RCK/ GPIO[1]	I/O	As needed	Open	If unused and left open, configure this pin as output
HDLC1_RXD/ TDM1_RD/ GPIO[3]	I/O	As needed	1 k Ω to GND	—
HDLC1_TXCLK/ TDM1_TCK/ GPIO[0]	I/O	As needed	Open	If unused and left open, configure this pin as output
$\overline{\text{HDLC1_CD}}$ / TDM1_TFS/ GPIO[4]	I/O	As needed	2 k–10 k Ω to OV _{DD}	—
$\overline{\text{HDLC1_CTS}}$ / TDM1_RFS/ GPIO[5]	I/O	As needed	2 k–10 k Ω to OV _{DD}	—
HDLC2_TXCLK/ TDM2_TCK/ GPIO[16]	I/O	As needed	Open	If unused and left open, configure this pin as output
HDLC2_RXCLK/ TDM2_RCK/ GPIO[17]	I/O	As needed	Open	If unused and left open, configure this pin as output
HDLC2_RXD/ TDM2_RD/ GPIO[19]	I/O	As needed	1 k Ω to GND	—
$\overline{\text{HDLC2_CD}}$ / TDM2_TFS/ GPIO[20]	I/O	As needed	2 k–10 k Ω to OV _{DD}	—
$\overline{\text{HDLC2_CTS}}$ / TDM2_RFS/ GPIO[21]	I/O	As needed	2 k–10 k Ω to OV _{DD}	—

7.10 eSDHC

Table 18 lists the eSDHC interface pins.

Table 18. eSDHC Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SD_CLK	O	33 Ω serial resistor must be provided for SD_CLK and placed close to MPC8309 device.	Open	Pin functionality determined by SICR_1[10-11] bit setting
SD_CMD	I/O	As needed + 10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	Pin functionality determined by SICRH[10–11] bit setting
SD_DAT3	I/O	As SD_DAT3: 10k Ω to 100k Ω to OV _{DD} As SD_CD: 160k Ω to GND	2 k–10 k Ω to OV _{DD}	Can function as DAT3 line or as card detection pin in 4-bit mode and as card detection pin in 1-bit mode. Pin functionality determined by SICR_1[12–13] bit setting. 10 -100 k Ω to OVDD is required during the normal operating conditions. Board should have a 160 K pull-down resistor if DAT3 is used for an SD card detection. In this case, the pull-up resistor must be disconnected during the identification phase. The pull-up resistor must be connected and the pull-down resistor must be switched out after the identification phase
SD_DAT2	I/O	As needed + 10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	Can function as DAT2 line or as read wait in 4-bit mode and as read wait in 1-bit mode Pin functionality determined by SICR_1[12-13] bit setting
SD_DAT1	I/O	As needed + 10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	Can function as DAT1 line or as interrupt detect in 4-bit mode and as read wait in 1-bit mode Pin functionality determined by SICR_1[10–11] bit setting
SD_DAT0	I/O	As needed + 10 k Ω to OV _{DD}	2 k–10 k Ω to OV _{DD}	Can function as DAT0 line or as interrupt detect Pin functionality determined by SICR_1[10-11] bit setting
$\overline{\text{SD_CD}}$	I	As needed + 100 k Ω to OV _{DD} on the $\overline{\text{SD_CD}}$ signal and a 330 Ω pull down on the common pin of the WP/CD Switch of the SD Card connector	2 k–10 k Ω to OV _{DD}	$\overline{\text{SD_CD}}$ low implies card is present and high implies card is absent. Pin functionality determined by SICR_1[10-11] bit setting
SD_WP	I	As needed + 100 k Ω to OV _{DD} on the SD_WP signal and a 330 Ω pull down on the common pin of the WP/CD Switch of the SD Card connector	2 k–10 k Ω to OV _{DD}	SD_WP high implies write protection is enabled on the SD Card and low implies write protection is disabled on the SD Card Pin functionality determined by SICR_1[10-11] bit setting

7.11 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. Table 19 lists the FlexCAN interface pins.

Table 19. FlexCAN Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
RXCAN1	I	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[14-15] bit setting
TXCAN1	O	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[14-15] bit setting
RXCAN2	I	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[16-17] bit setting
TXCAN2	O	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[16-17] bit setting
RXCAN3	I	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[18-19] bit setting
TXCAN3	O	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[18-19] bit setting
RXCAN4	I	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[20-21] bit setting
TXCAN4	O	As Needed	1 - 4.7kΩ to GND	Pin functionality determined by SICR_1[20-21] bit setting

8 Revision History

Table 20 provides a revision history for this application note.

Table 20. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	06/2014	<ul style="list-style-type: none"> Updated Table 5. In Table 18, "If Used" column for "SD_CLK" signal is updated with "33 Ω serial resistor must be provided for SD_CLK and placed close to MPC8309 device."
1	05/2012	<ul style="list-style-type: none"> In Table 4, "Reset Configuration Pin Listing," replaced $\overline{\text{HRESET}}$ with $\overline{\text{PORESET}}$ in the termination column for CFG_RESET_SOURCE[n]. In Table 9, "Local Bus Pin ListingFor Signals," replaced the "if not used" column value for LGPL4/LGTA_B/LUPWAIT/LFRB_B signal from "Open" to "4.7kΩ – 10kΩ to OVDD". In Table 11, "ULPI Pin Listing," deleted the signals QE_TRB_O and QE_TRB_I . In Table 18, "eSDHC Pin Listing," modified the description of connections "If used", and notes.
0	03/2011	Initial release.

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