Freescale Semiconductor
Application Note

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Power Management Design Guidelines for the i.MX50x Family of Microprocessors

1 Purpose

The present document is intended to teach the reader how to supply the power management to the i.MX50x family of processors using either the Freescale MC13892 or the MC34709 as the main power management device.

2 Introduction

The i.MX50x family of microprocessors requires complex power management distribution along with specific sequencing for proper power up. To supply integrated power management to the i.MX50 processors, Freescale provides two highly integrated PMICs solutions for different specific scenarios. The MC13892, provide a highly integrated solution which provides most of the required voltage rails as well as integrated battery charger, 10 bits ADC and backlight LED drivers. Likewise, the MC34709 is a reduced solution providing as well the majority of the required power rails for applications with less system requirements.

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3 i.MX50 Microprocessor Overview

The i.MX50 Applications Processors (i.MX50) is part of a growing family of multimedia-focused products, offering high performance processing optimized for lowest power consumption.

The i.MX50 is optimized for portable multimedia applications and it features Freescale's advanced implementation of the ARM Cortex-A8™ core, which operates at speed as high as 800 MHz. The i.MX50 provides a powerful display architecture, including a 2D Graphics Processing Unit (GPU) and Pixel Processing Pipeline (ePXP). In addition, i.MX508 includes a complete integration of the electrophoretic display function. The i.MX50 supports DDR2, LPDDR2, and LPDDR1 DRAM at clock rate up to 266 MHz to enable a range of performance and power trade-offs.

The flexibility of the i.MX50 architecture allows it to be used in a variety of applications. As the heart of the application chipset, the i.MX50 provides a rich set of interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays.

i.MX50 power requirements are summarized in Table 1.

Table 1. i.MX50 Power requirements

Voltage Domain		Voltage		Current	
Name	**Description**	**TYP**	**Units**	**Max**	**Units**
VDDGP	400< fARM ≤ 800 MHz	1.05	V	1250	mA
	167< fARM ≤ 400 MHz	0.95	V		
	24< fARM ≤ 167 MHz	0.9	V		
	Stop Mode	0.85	V		
VCC	LPM	0.95	V	400	mA
	RPM	1.05	V		
	HPM	1.225	V		
VDDA	Run Mode	1.2	V	250	mA
	Stop Mode	0.95	V		
VDDAL1	Run Mode	1.2	V		
	Stop Mode	0.95	V		
VDD3P0	Bandgap and 480 MHz PLL supply	3.0	V	10	mA
VDD2P5	Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	2.5	V	150	mA
VDD1P2	PLL digital supplies	1.8	V	10	mA
VDD1P8	PLL analog supplies	1.8	V	10	mA
NVCC_JTAG	GPIO digital power supplies	1.875 or 2.775	V		
NVCC_EMI_DRAM	DDR2/LPDDR1	1.8	V	350	mA
	LPDDR2	1.2	V		

Table 1. i.MX50 Power requirements

Voltage Domain		Voltage		Current	
Name	**Description**	**TYP**	**Units**	**Max**	**Units**
VREF	DRAM Reference Voltage Input	1/2 NVCC_EMI_DRAM	V	0.004	mA
VDDO25	EMI Pad Predriver supply	2.5	V	10	mA
NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_KEYPAD NVCC_EIM NVCC_EPDC NVCC_LCD NVCC_MISC NVCC_SPI NVCC_SSI NVCC_UART	High voltage I/O (HVIO) supplies	HVIO_L=1.875 HVIO_H=3.0	V		
NVCC_SRTC	SRTC core and I/O supply (LVIO)	1.2	V		
NVCC_RESET	LVIO	1.875 or 2.775	V		
USB_H1_VDDA25 USB_OTG_VDDA25	USB_PHY analog supply	2.5	V	50	mA
USB_DDA33 USB_OTG_VDA33	USB PHY I/O analog supply	3.3	V	16	mA

3.1 i.MX50 Power-up/down Sequence

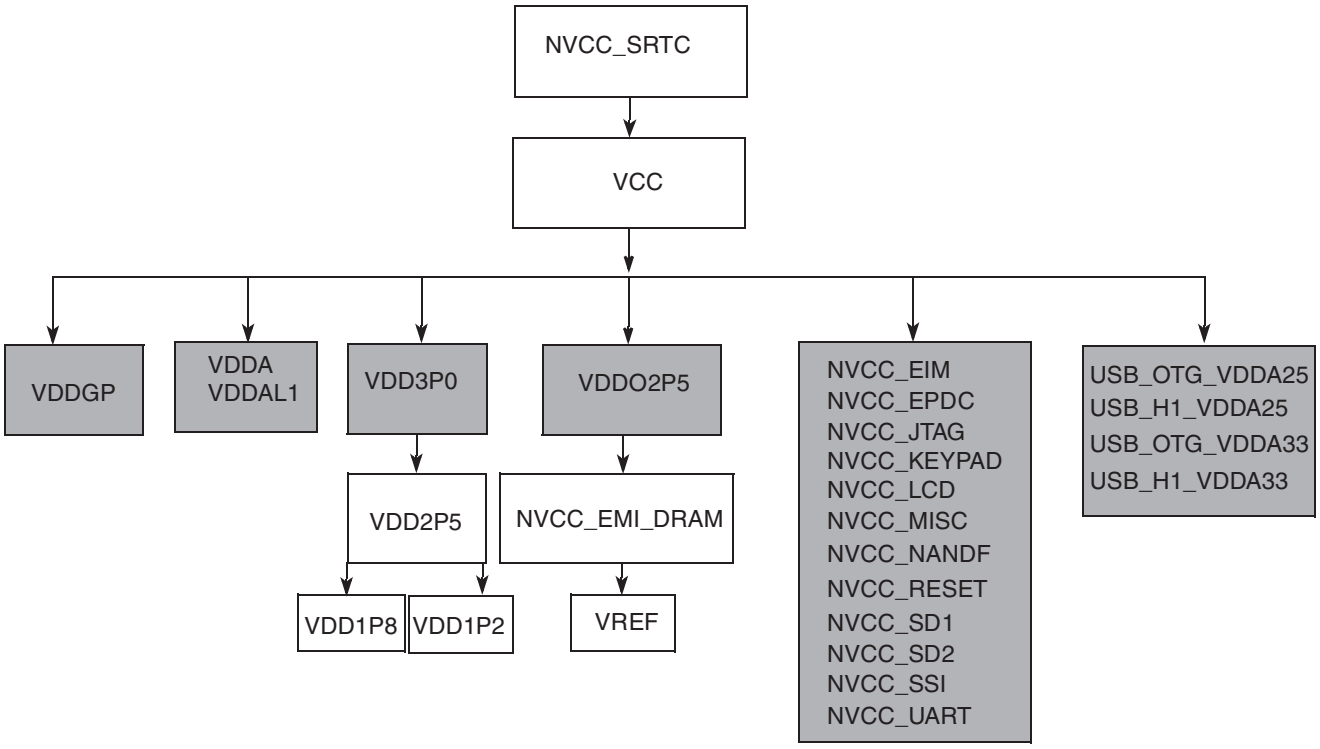

Figure 1. i.MX50 Power up Sequence

NOTE

- The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
- No power-up sequence dependencies exist between the supplies shown shaded in gray.

3.2 Power-Down Sequence

The power-down sequence is recommended to be the opposite of the power-up sequence. In other words, the same power supply constraints exist while powering off as while powering on.

4 i.MX50 Power Management Design with MC13892

The MC13892 is a power management IC that includes the necessary sources to supply the i.MX50. Its main features are:

- Battery charger system for wall charging and USB charging
- 10-bit ADC for monitoring battery and other inputs, plus a coulomb counter support module
- Four adjustable output buck regulators for direct supply of the processor core and memory
- 12 adjustable output LDOs with internal and external pass devices
- Boost regulator for supplying RGB LEDs
- Serial backlight drivers for displays and keypad, plus RGB LED drivers

- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry, with coin cell backup and support for external secure real time clock on a companion system processor IC
- Touch screen interface
- SPI/I2C bus interface for control and register access

4.1 MC13892 Voltage supplies

Table 2. MC13892 Voltage Supplies Summary

Supply	Typical Application	Output Voltage (in V)	Load Capability (in mA)
SW1	Buck regulators for processor core(s)	0.600-1.375	1050
SW2	Buck regulators for processor SOG, etc.	0.600-1.375; 1.100-1.850	800
SW3	Buck regulators for internal processor memory and peripherals	0.600-1.375; 1.100-1.850	800
SW4	Buck regulators for external memory and peripherals	0.600-1.375; 1.100-1.850	800
SWBST	Boost regulator for USB OTG, Tri-color LED drivers	5.0	300
VIOHI	IO and Peripheral supply, eFuse support	2.775	100
VPLL	Quiet Analog supply (PLL, GPS)	1.2/1.25/1.5/1.8	50
VDIG	Low voltage digital (DPLL, GPS)	1.05/1.25/1.65/1.8	50
VSD	SD Card, external PNP	1.8/2.0/2.6/2.7/2.8/2.9/3.0/3.15	250
VUSB2	External USB PHY supply	2.4/2.6/2.7/2.775	50
VVIDEO	TV DAC supply, external PNP	2.5/2.6/2.7/2.775	350
VAUDIO	Audio supply	2.3/2.5/2.775/3.0	150
VCAM	Camera supply, internal PMOS	2.5/2.6/2.75/3.0	65
	Camera supply, external PNP	2.5/2.6/2.75/3.0	250
VGEN1	General peripherals supply #1, external PNP	1.2/1.5/2.775/3.15	200
VGEN2	General peripherals supply #2, external PNP	1.2/1.5/1.6/1.8/2.7/2.8/3.0/3.15	350
VGEN3	General peripherals supply #3, internal PMOS	1.8/2.9	50
	General peripherals supply #3, external PNP	1.8/2.9	250
VUSB	USB Transceiver supply	3.3	100

4.2 MC13892 Power-up Sequence

The Power Up mode Select pins (PUMS1 and 2) are used to configure the startup characteristics of the regulators. Supply enabling and output level options are selected by hardwiring the PUMSx pins for the desired configuration. Tying the PUMSx pins to ground corresponds to 00, open to 01, VCOREDIG to 10, and VCORE to 11.

The recommended power up strategy for end products is to bring up as little of the system as possible at booting, essentially sequestering just the bare essentials, to allow processor startup and software to run. With such a strategy, the startup transients are controlled at lower levels, and the rest of the system power tree can be brought up by software. This allows optimization of supply ordering where specific sequences may be required, as well as supply default values. Software code can load up all of the required programmable options to avoid sneak paths, under/over-voltage issues, startup surges, etc., without any change in hardware. For this reason, the Power Gate drivers are limited to activation by software rather than the sequencer, allowing the core(s) to startup before any peripheral loading is introduced.

The power up defaults Table 3 shows the initial setup for the voltage level of the switching and LDO regulators, and whether they get enabled.

Table 3. Power Up Defaults Table

PUMS1	GND	Open	VCOREDIG	VCORE	GND	Open
PUMS2	**Open**	**Open**	**Open**	**Open**	**GND**	**GND**
SW1 (1)	0.775	1.050	**1.050**	0.775	1.200	1.200
SW2 (1)	1.025	1.225	**1.225**	1.025	1.350	1.450
SW3 (1)	1.200	1.200	**1.200**	1.200	1.800	1.800
SW4 (1)	1.800	1.800	**1.800**	1.800	1.800	1.800
SWBST	Off	Off	**Off**	Off	5.000	5.000
VUSB	3.300 (2)	3.300 (2)	**3.300 (2)**	3.300 (2)	3.300 (4)	3.300 (4)
VUSB2	2.600	2.600	**2.600**	2.600	2.600	2.600
VPLL	1.800	1.800	**1.800**	1.800	1.500	1.500
VDIG	1.250	1.250	**1.250**	1.250	1.250	1.250
VIOHI	2.775	2.775	**2.775**	2.775	2.775	2.775
VGEN2	3.150	Off	**3.150**	Off	3.150	3.150
VSD	Off	Off	**Off**	Off	3.150	3.150
Not initialized during power-up						
VCAM	Off	Off	**Off**	Off	Off	Off
VGEN1	Off	Off	**Off**	Off	Off	Off
VGEN3	Off	Off	**Off**	Off	Off	Off
VVIDEO	Off	Off	**Off**	Off	Off	Off
VAUDIO	Off	Off	**Off**	Off	Off	Off

Notes

1. The SWx regulators are activated in PWM pulse skipping mode, but allowed when enabled by the startup sequencer.
2. USB supply VUSB, is only enabled if 5.0 V is present on UVBUS.
3. The following supplies are not included in the matrix since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO
4. SWBST = 5.0 V powers up and does VUSB regardless of 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

The power up sequence is shown in Table 4. VCOREDIG, VSRTC, and VCORE are brought up in the pre-sequencer startup. Once VCOREDIG is activated (i.e., at the first-time power application), it will be continuously powered as long as a valid coin cell is present.

Table 4. Power Up Sequence

Tap x 2ms	PUMS2 = Open	PUMS2 = GND
0	SW2	SW2
1	SW4	VGEN2
2	VIOHI	SW4
3	VGEN2	VIOHI, VSD
4	SW1	SWBST, VUSB (7)
5	SW3	SW1
6	VPLL	VPLL
7	VDIG	SW3
8	-	VDIG
9	VUSB (6), VUSB2	VUSB2

Notes

5. The following supplies are not included in the matrix since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO. SWBST is not included on the PUMS2 = Open column.
6. USB supply VUSB, is only enabled if 5.0 V is present on UVBUS.
7. SWBST = 5.0 V powers up and so does VUSB regardless of 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

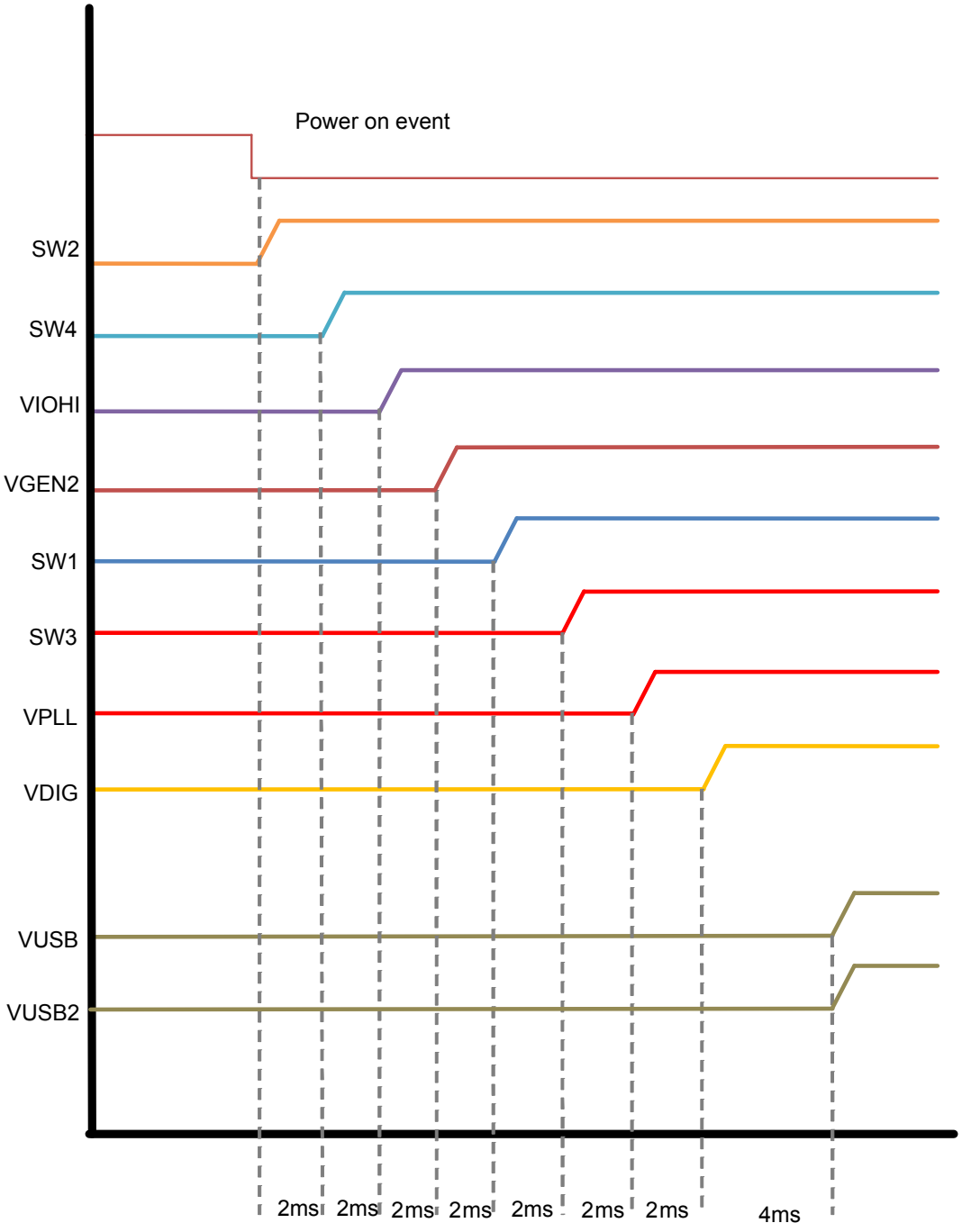

Figure 2. MC13892 Power up Sequence for i.MX50 processors.

4.3 Interfacing the i.MX50 with the MC13892.

Table 5, shows all the i.MX50 voltage rails, their power requirements and their associated MC13892 regulator. Most of the supply domains have flexible voltage and could be adjusted or supplied with a different regulator depending on each application needs

Table 5. i,MX50 voltage domain supplies with the MC13892

I.MX50				MC13892			
Power Rail of i.MX50	**Power Domain**	**TYP**		**Associated Regulator**	**Voltage PUM[4:0]=1110**	**Current (mA)**	**PUS**
NVCCSRTC	32 kHz osc. power (when chip off)	1.2		VSRTC	1.2	0.05	-
VCC	LP Transistor power	1.2		SW2	1.2	800	0
VDDA	Peripheral Memory + L2 Cache power	1.2		SW3	1.2	800	5
VDDAL1	L1 Cache power	1.2		SW3	1.2	800	5
VDDGP	Core and G Transistor power	1		SW1	1	1050	4
VDDO2P5	Predriver for EMI pads	2.5		External LDO	2.5	250	-
VDD2P5	Power to 24 MHz osc, efuse, xtalok, 32 kHz osc. power mux	2.5		External LDO	2.5	250	-
NVCC_EMI_DRAM	Power to EMI pins	1.2		External Buck	1.2	-	-
VREF	DRAM Reference	0.9		Voltage divider 0.5 x NVCC_EMI_DRAM	1.2 * 0.5	250	-
NVCC EIM NVCC JTAG NVCC SPI NVCC SD NVCC NANDF NVCC SSI NVCC MISC NVCC KEYPAD	3.0 V I/Os	3 3 3 3 3		VGEN2	3.0	350	3
ALL 3.3V IO NVCC NVCC EPDC NVCC LCD NVCC UART NVCC_SD2	3.0 V I/Os	 3.15 3.15 3.15 3.15		External Buck VSD	3.15 3.15	5000 250	- -
VDD3P0	VDD2P5 LDO input + power to Bandgap, DCDC predriver, tempsensor, 480 MHz PLL	3		VGEN2	3.0	350	3

Table 5. i,MX50 voltage domain supplies with the MC13892

I.MX50				MC13892			
Power Rail of i.MX50	**Power Domain**	**TYP**		**Associated Regulator**	**Voltage PUM[4:0]=1110**	**Current (mA)**	**PUS**
USB_OTG_VDDA33	Power to USB Host	3.3		VUSB	3.3	100	9
USB_H1_VDDA33	Power to USB OTG	3.3		VUSB	3.3	100	9
All 1.8 IO NVCC VDD DCDCI VDD DCDCO	1.8 V I/Os	1.8 Not used		SW4	1.8	800	1
NVCC_RESET (LVIO)	Power to POR_B,RESET_IN_B, TESTMODE, & BOOTMODE[0:1]	1.875 or 2.775		VPLL	1.8	50	6
USB_OTG_VDDA25	Power to USB Host	2.5		VUSB2	2.5	50	9
USB_H1VDDA25	Power to USB OTG	2.5		VUSB2	2.5	50	9
VDD1P8	Power to all PLLs	1.8		VPLL	1.8	50	6
VDD1P2	Power to all PLL digital, 32 kHz osc. (when chip on), much of analog, digital	1.2		VDIG	1.2	50	7

4.3.1 Interfacing Block Diagram

The following block diagrams show all the power connections needed for the interface, as well as how the communication signals must be connected between the i.MX50 and MC13892.

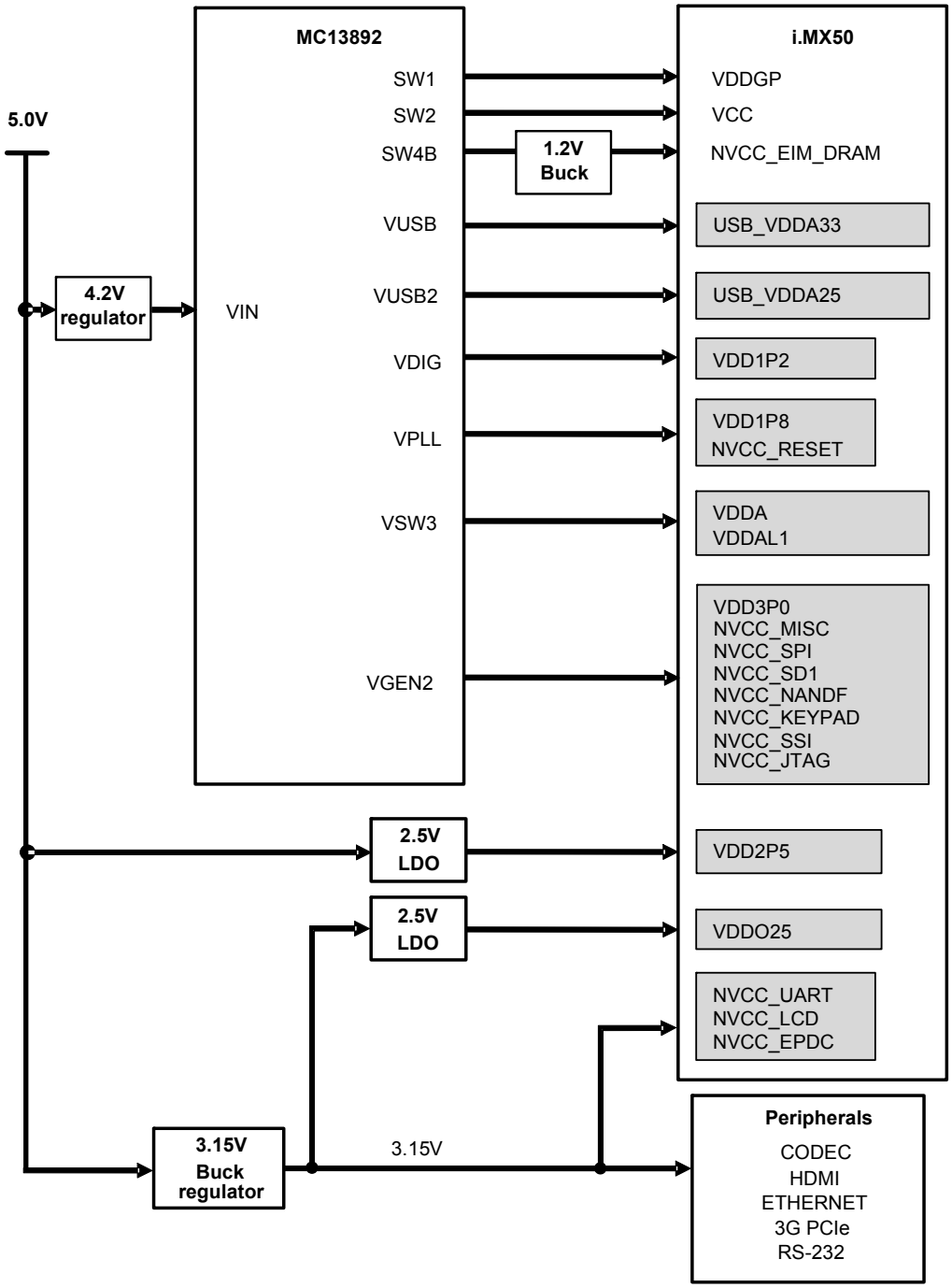

Figure 3. i.MX50 Power Interface with MC13892 Block Diagram

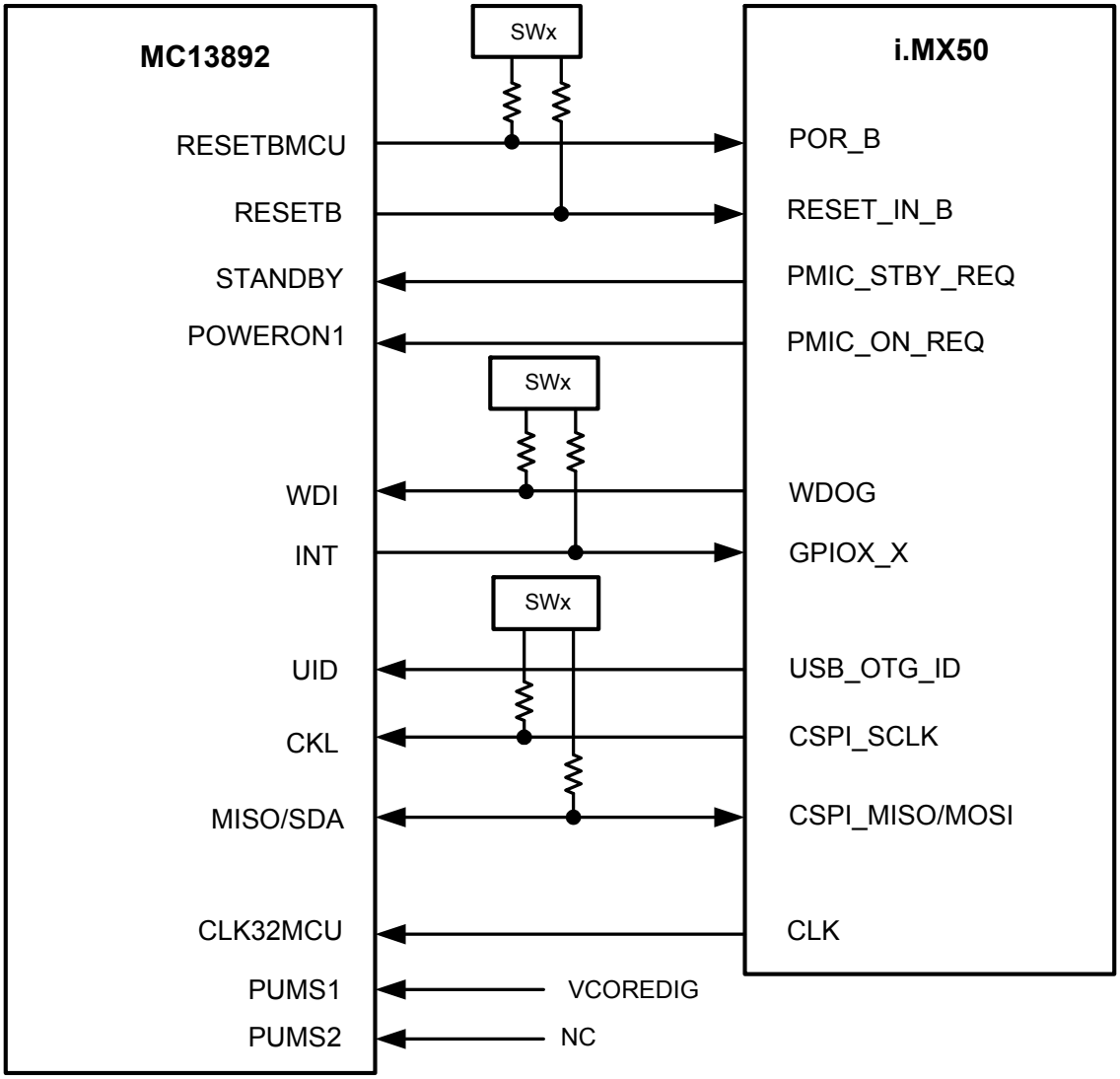

Figure 4. i.MX50 Control Interface with MC34709 Block Diagram

4.3.1.1 3.15 V Buck Regulator

For system stability, it is recommended that you use an extra 3.15 V DCDC power supply to support large current requirements (for example a 3G module or Wi-Fi card). The MC34709 has limited 3.15 V output ability.

4.3.1.2 1.2 V Buck Regulator

A 1.2V Buck regulator is required to provide voltage to the 1.2V LPDDR2 module and the NVCC_EMI_DRAM domain in the i.MX50 processor. Regulator SW4 will supply the input of this regulator at 1.8V and will also be used as the 1.8V supply on the LPDDR2 Module as well.

4.3.1.3 2.5 V LDO Regulators

Due to the Power-up sequence dependency, two 2.5V LDO regulators are required to power up the VDD2P5 and VDDO25 domains in the i.MX processor. The first one is enabled by the SW2 voltage rail, while the second LDO is enabled with the VGEN2 voltage rail. See Figure 3.

4.3.2 Interface Power-up Sequence

The resulting power-up sequence of the interface is shown in the following figure

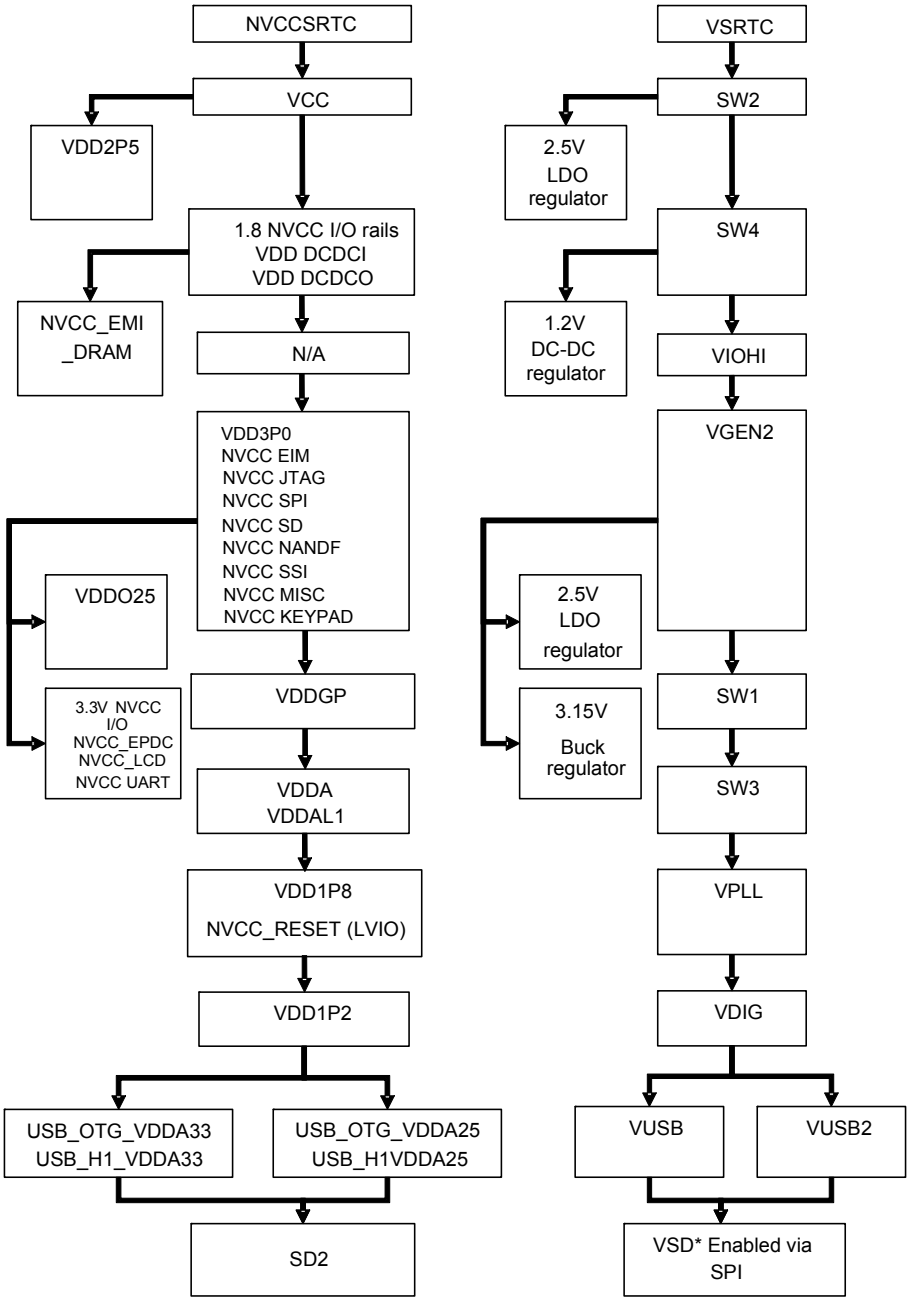

Figure 5. Power up Sequence Flow Chart

4.4 Application Example with the MC13892

The following schematic is simplified application example for interfacing the MC13892 with an i.MX50 processor. note that this schematic only includes the block related to the power section as well as power management controlling signals.

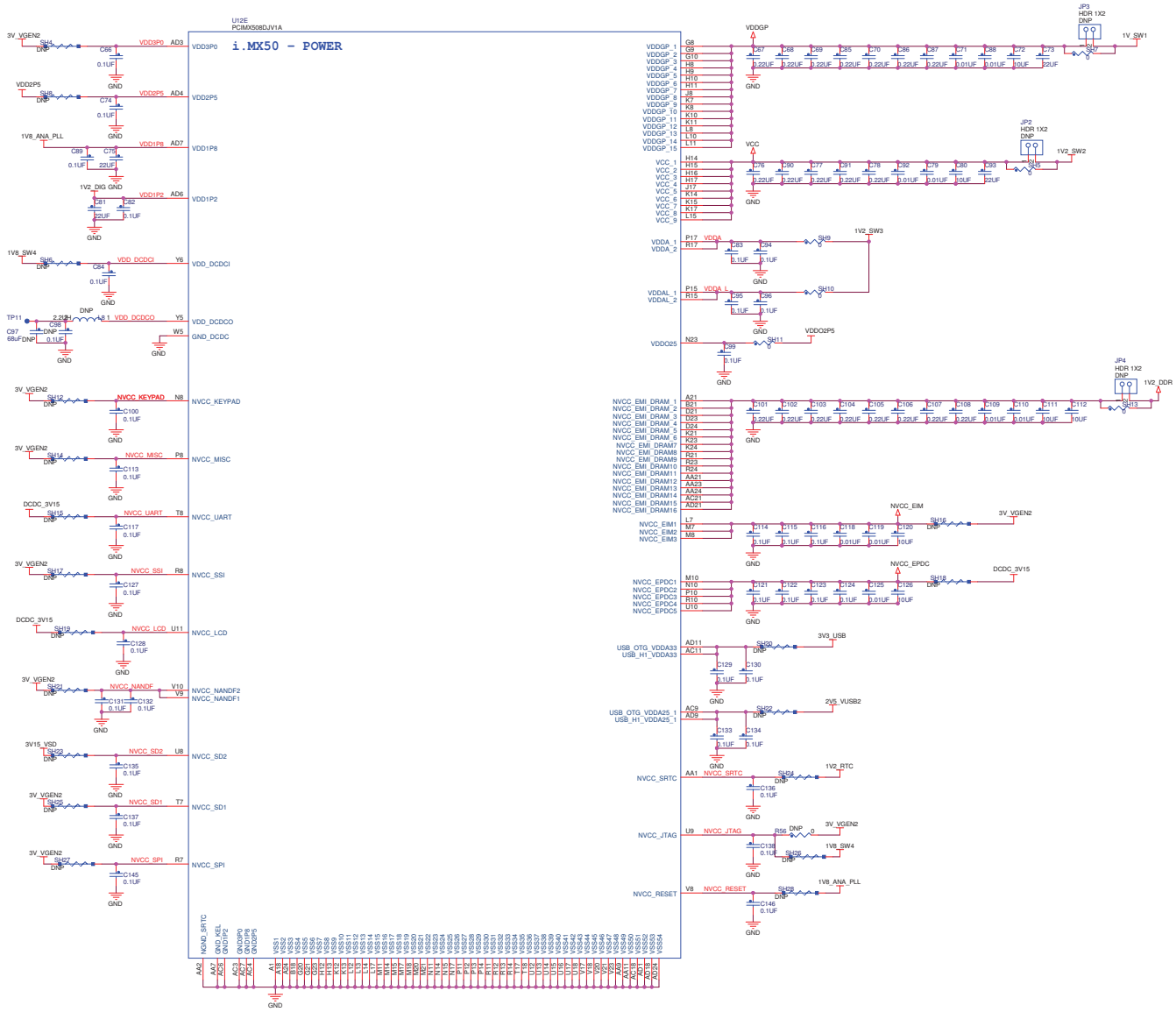

Figure 6. i.MX50 Voltage Domains

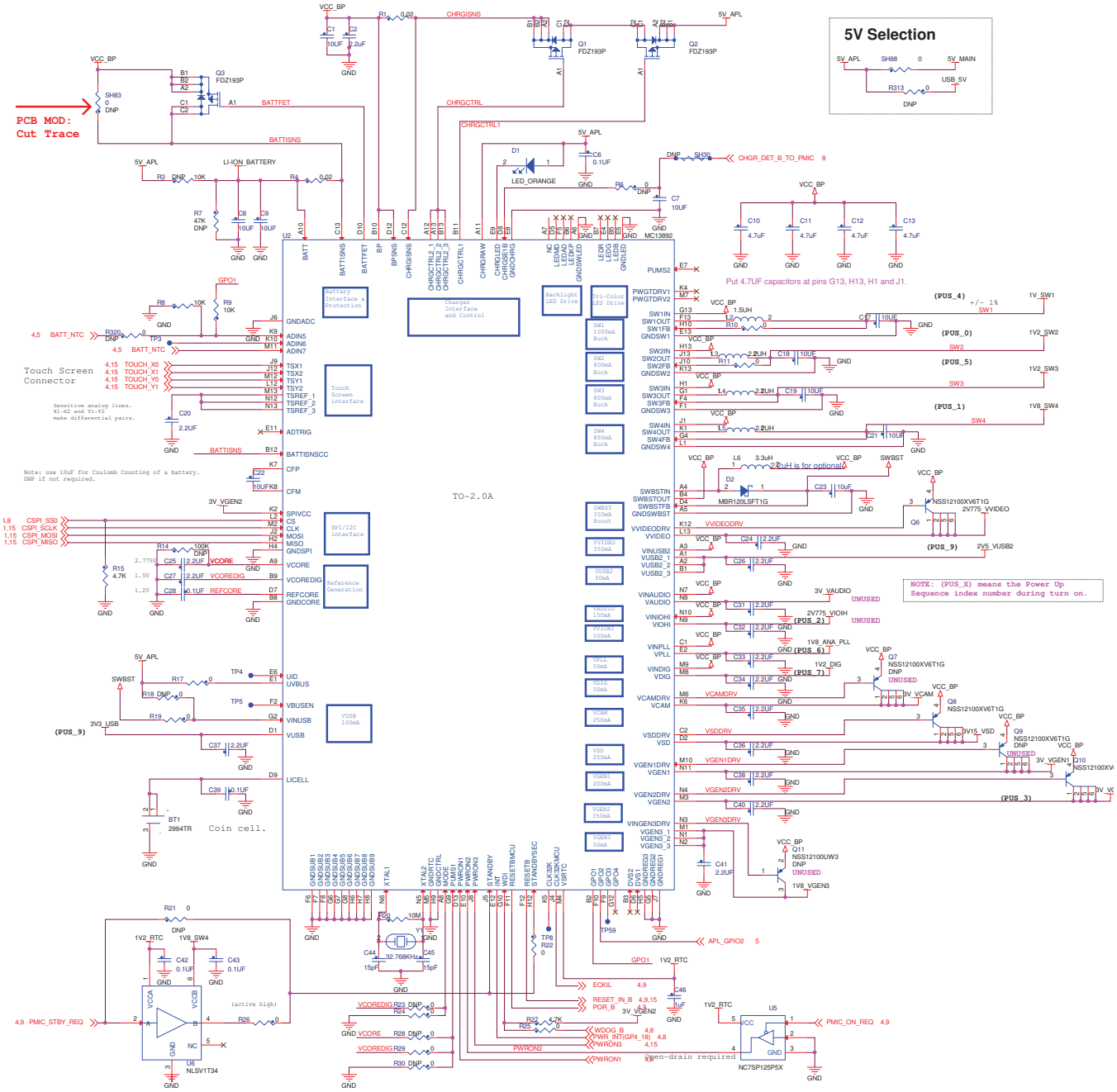

Figure 7. MC13892 Schematic

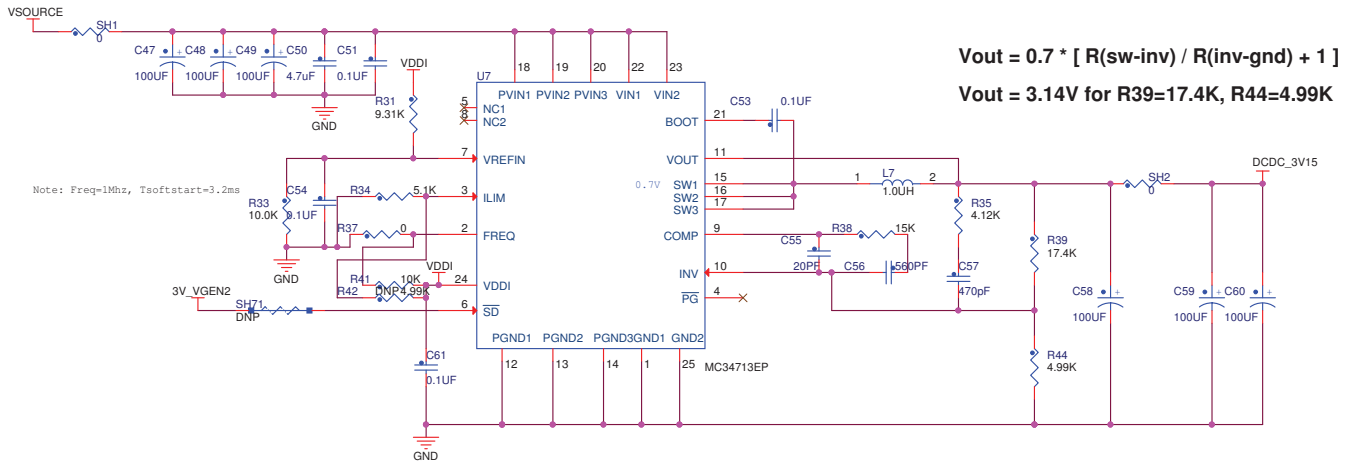

Figure 8. 3.15V Buck Regulator

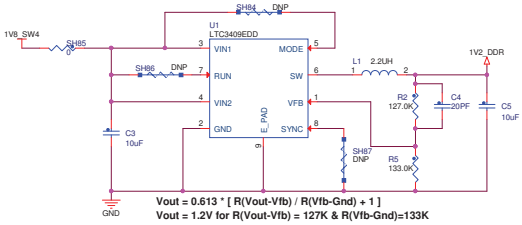

Figure 9. 1.2V Buck Regulator

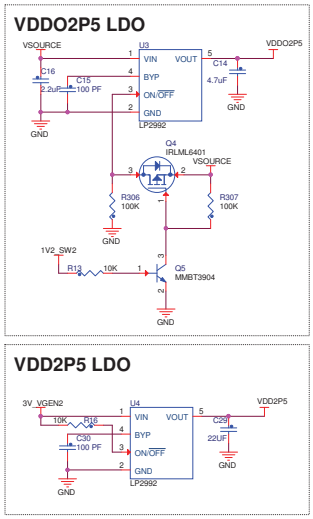

Figure 10. 2.5V LDO Regulators

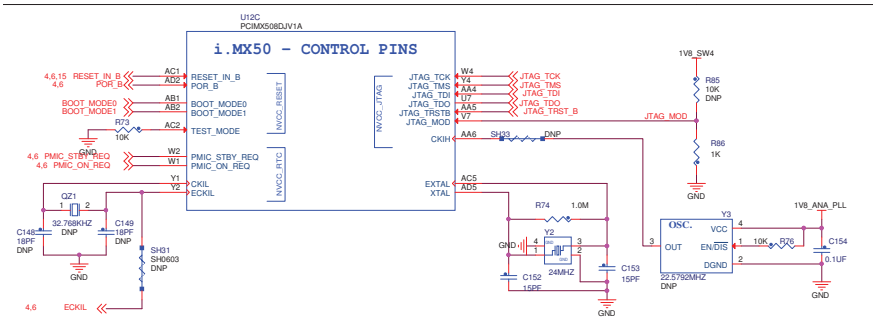

Figure 11. i.MX50 Control Signals

4.5 MC13892 PCB Layout Example

The following example shows the PMIC layout section for a reference design of the i.MX50 using the MC13892 power management. It is design in 10 layers with 4 inner planes (GND and PWR) form layer 4 to layer 7. For simplicity, only top, bottom and Inner signal layers are shown in figures x to y.

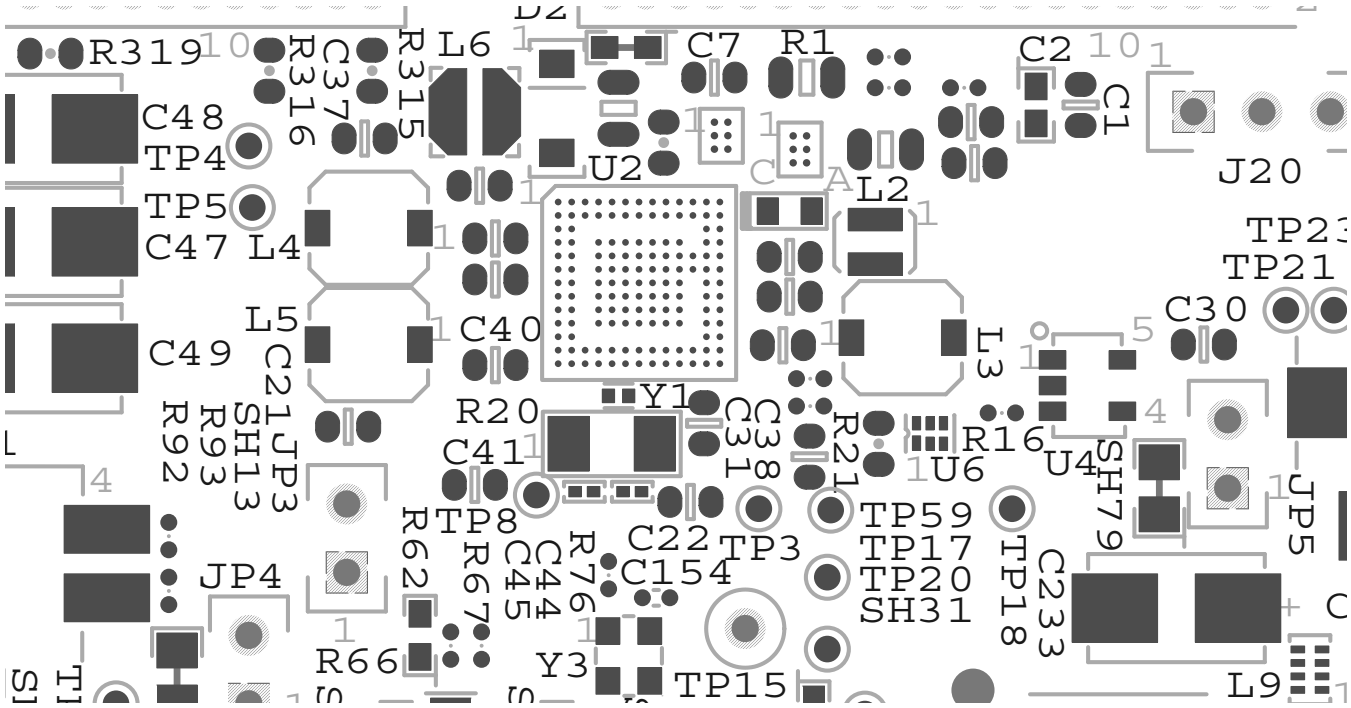

Figure 12. Top Fabrication Drawing

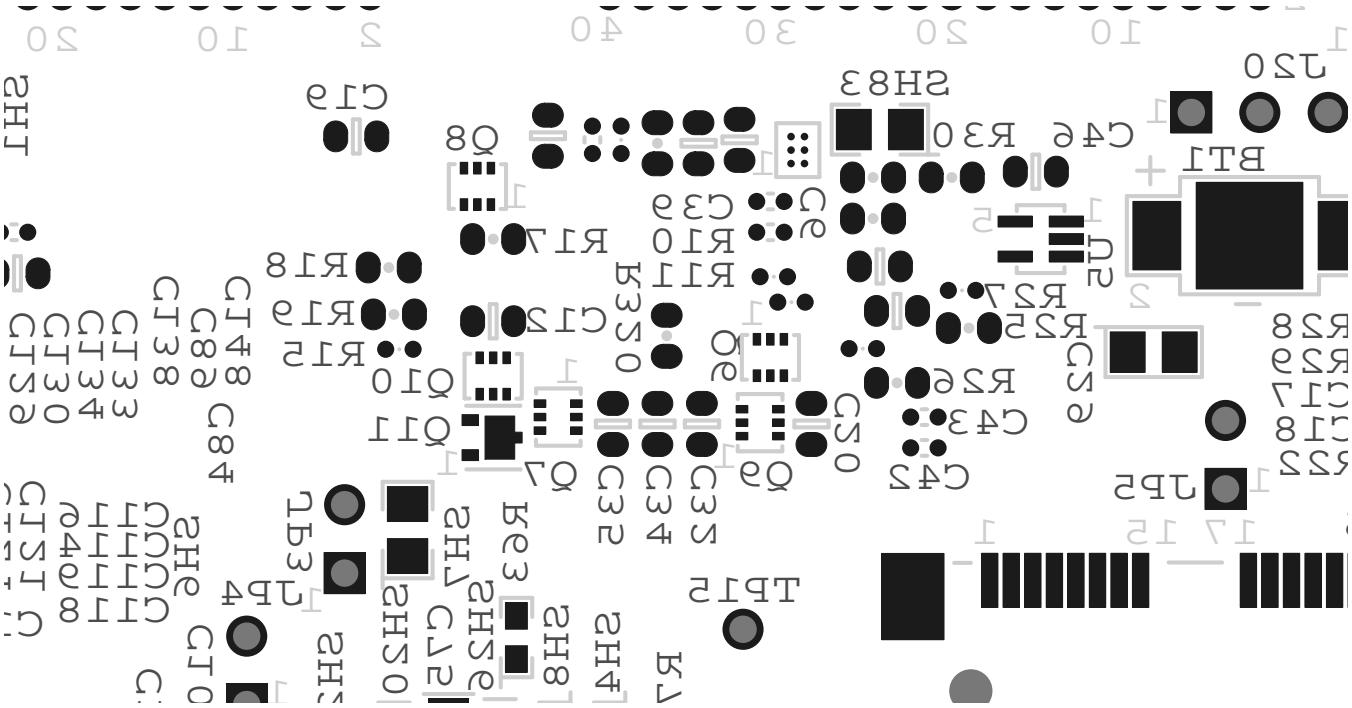

Figure 13. Bottom Fabrication Drawing

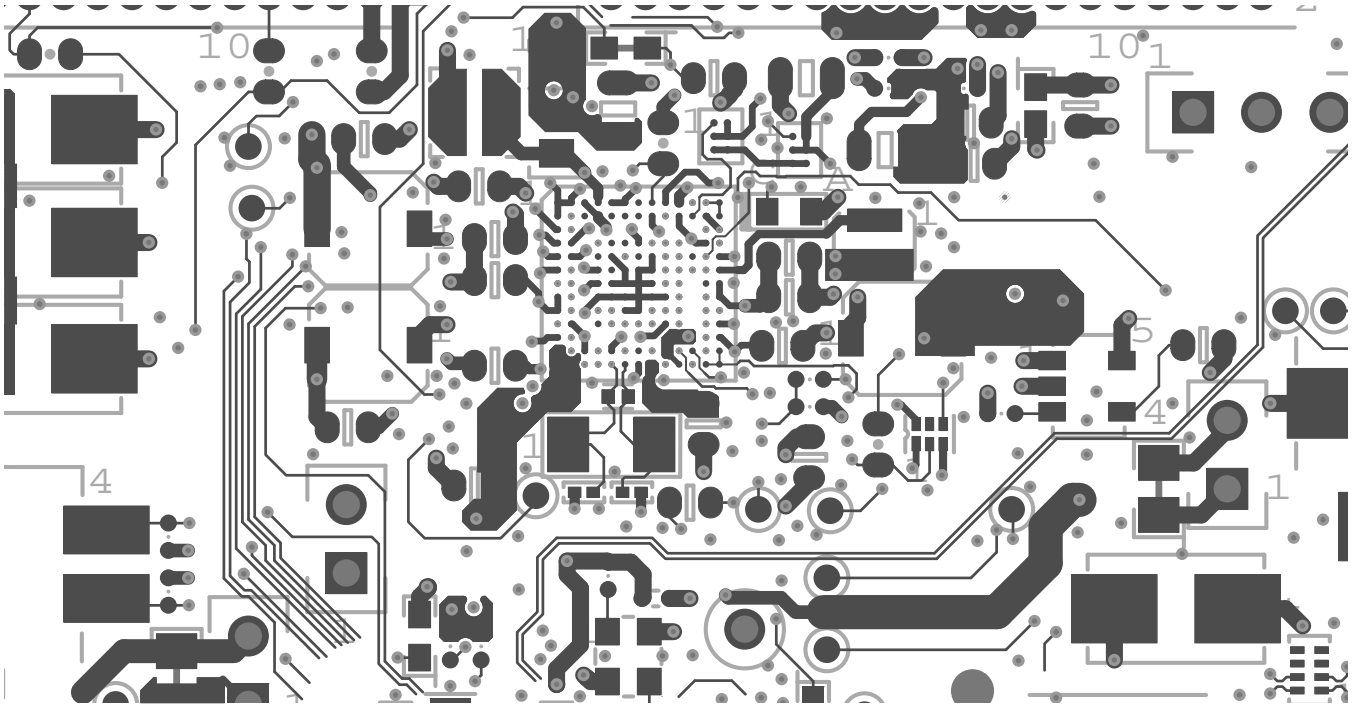

Figure 14. Top Layer

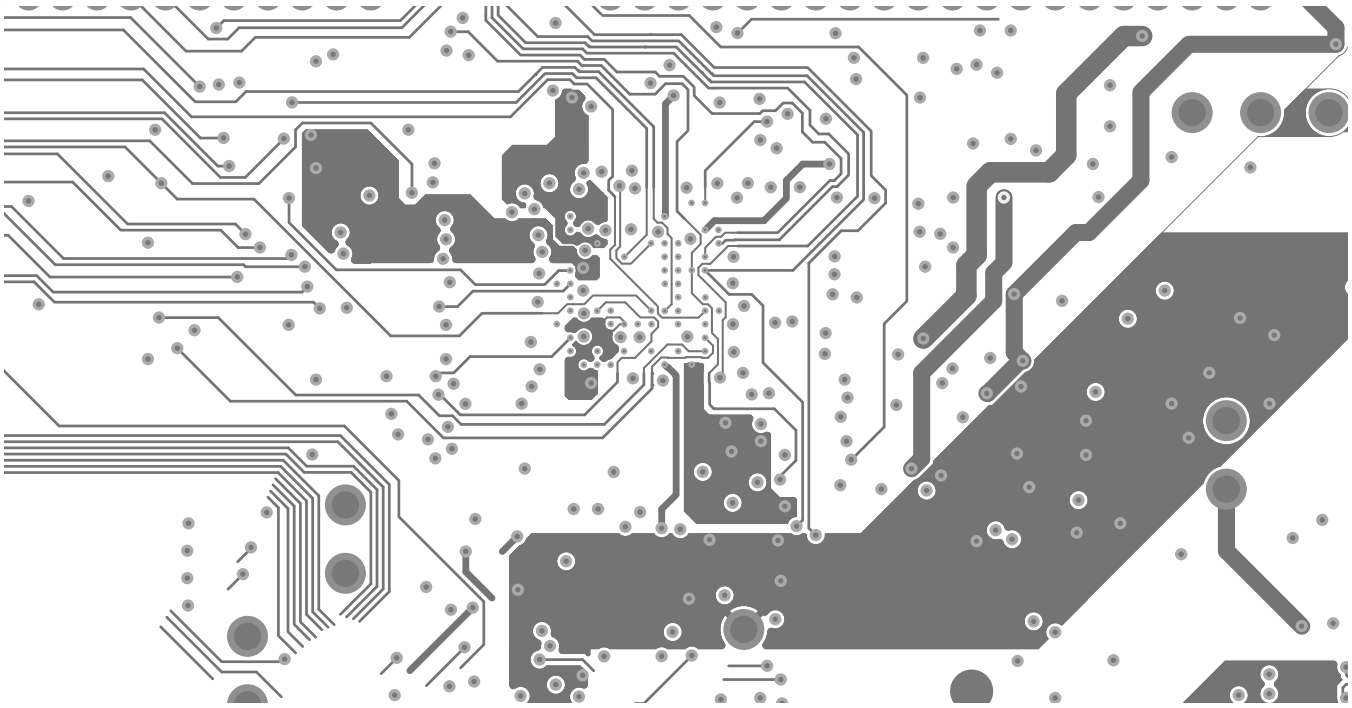

Figure 15. Inner Layer 2 (Signal)

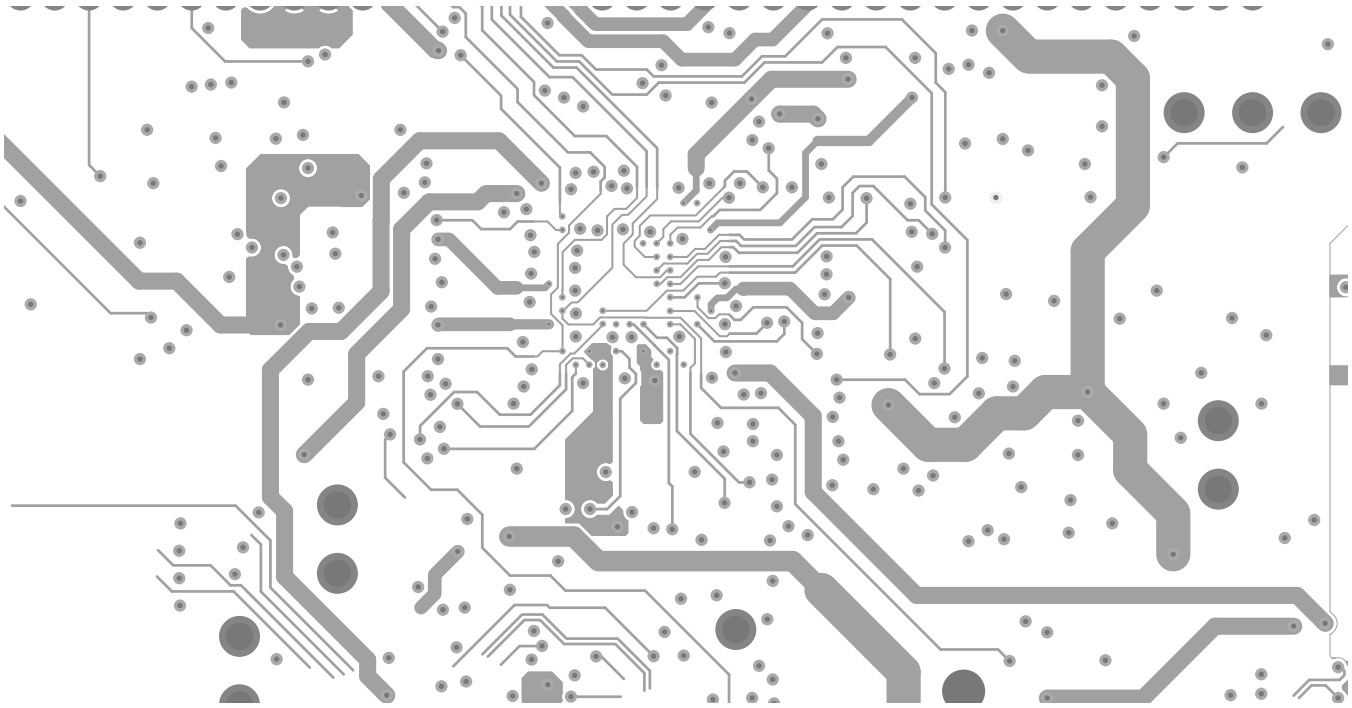

Figure 16. Inner Layer 3 (Signal)

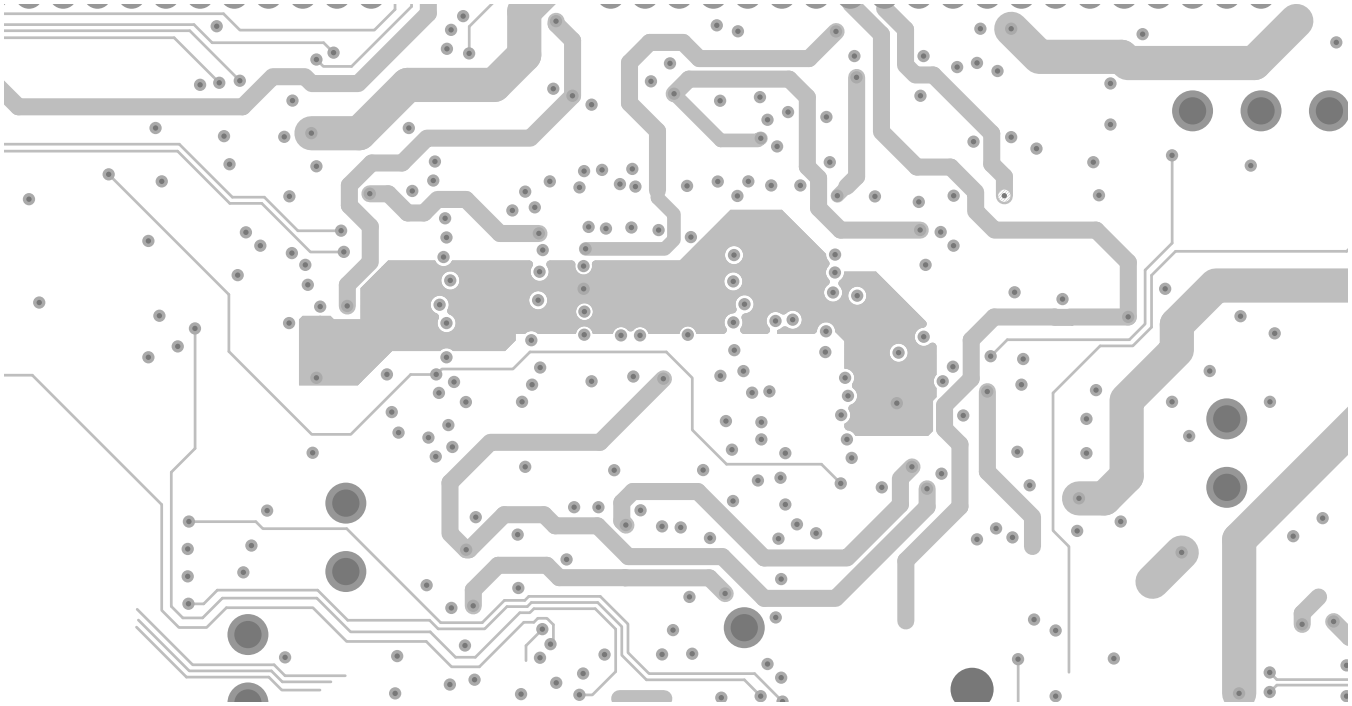

Figure 17. Inner Layer 8 (Signal)

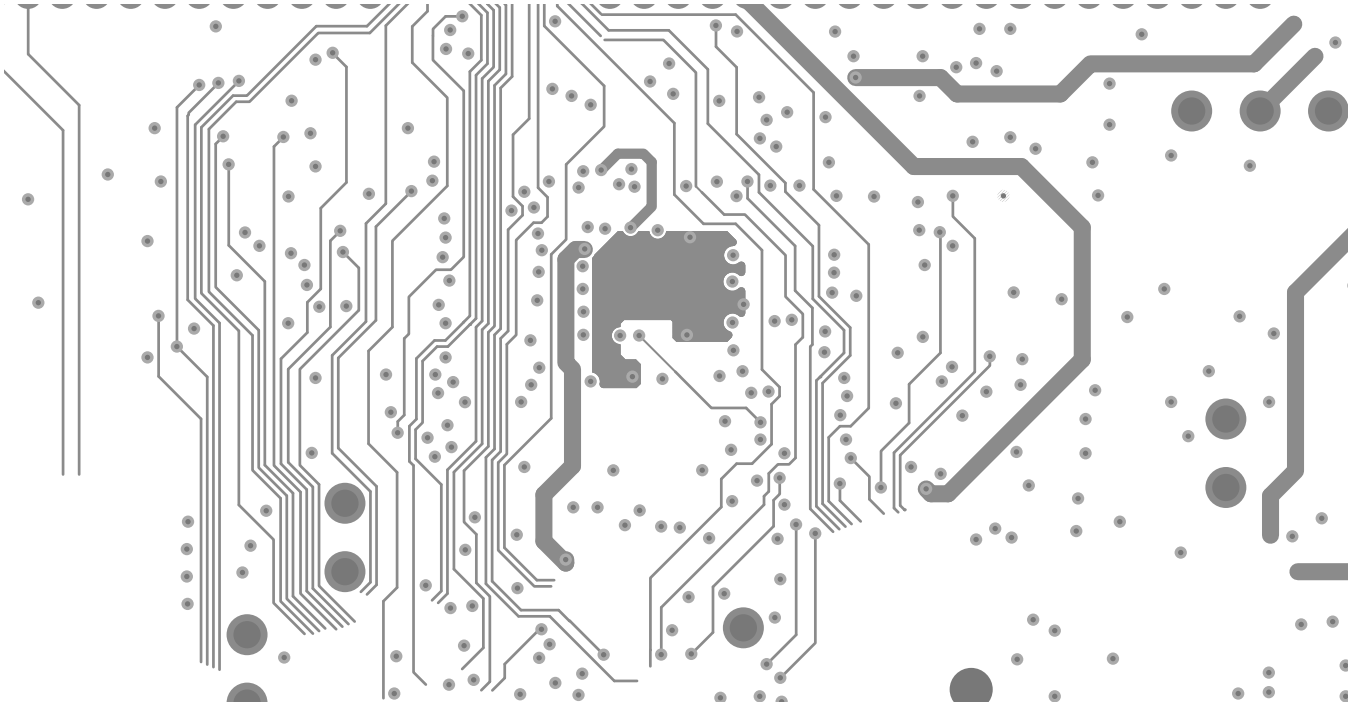

Figure 18. Inner Layer 9 (Signal)

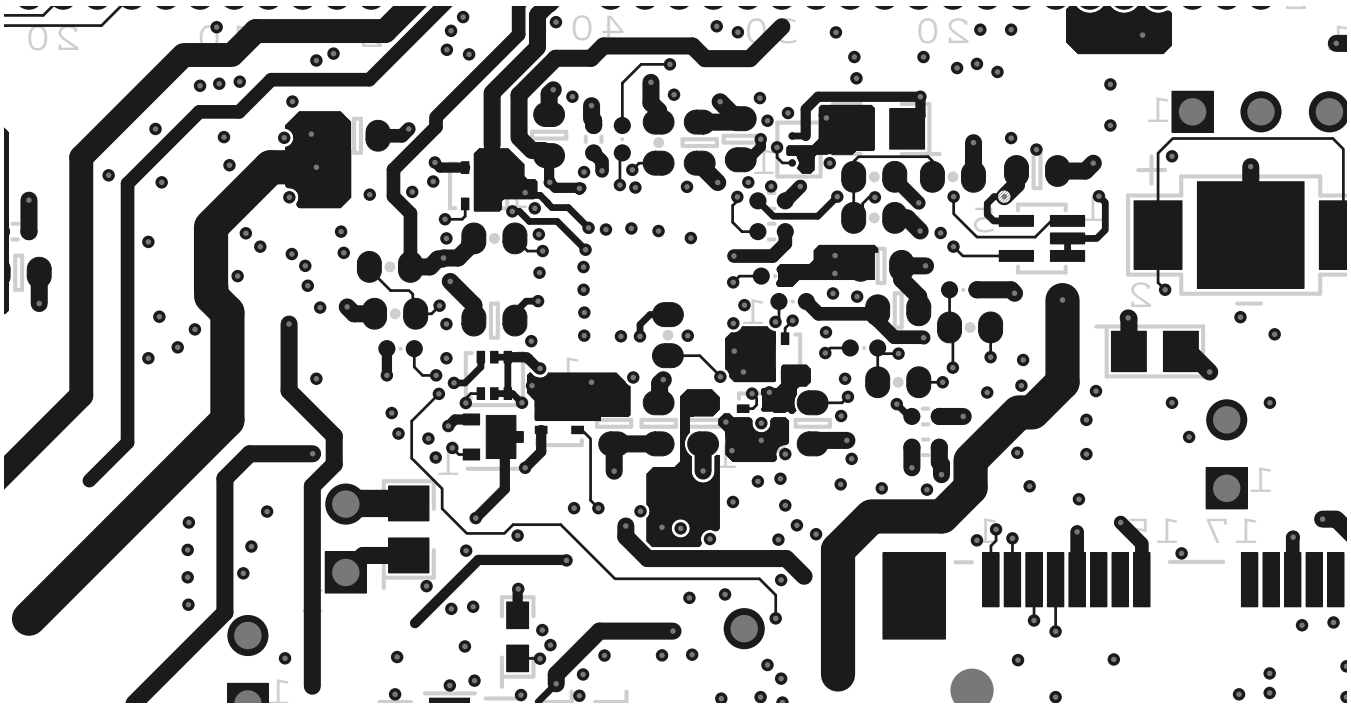

Figure 19. Bottom Layer

5 i.MX50 Power Management Design with the MC34709

The MC34709 is a power management IC that includes the necessary sources to supply the i.MX50. Its main features are:

- Ten-bit ADC for monitoring.
- Four-wire resistive touchscreen interface
- Five buck converters for direct supply of the processor core and memory
- One boost converter for USB OTG support
- Eight LDO Regulators with internal and external pass devices for thermal budget optimization
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry with coin cell backup
- Support for external secure real time clock on a companion system processor IC
- Single SPI/I2C bus for control & register access
- Four general purpose low voltage I/Os with interrupt capability
- Two PWM outputs

5.1 MC34709 Voltage supplies

Table 6. MC34709 Voltage Supplies Summary

Supply	Typical Application	Output Voltage (in V)	Load Capability (in mA)
SW1	Buck regulator for processor VDDGP domain	0.650 - 1.4375	2000
SW2	Buck regulator for processor VCC domain	0.650 - 1.4375	1000
SW3	Buck regulator for processor VDD domain and peripherals	0.650 - 1.425	500
SW4A	Buck regulator for DDR memory and peripherals	1.200 – 1.975: 2.5/3.15/3.3	500
SW4B	Buck regulator for DDR memory and peripherals	1.200 – 1.975: 2.5/3.15/3.3	500
SW5	Buck regulator for I/O domain	1.200 – 1.975	1000
SWBST	Boost regulator for USB OTG	5.00/5.05/5.10/5.15	380
VSRTC	Secure Real Time Clock supply	1.2	0.05
VPLL	Quiet Analog supply	1.2/1.25/1.5/1.8	50
VREFDDR	DDR Ref supply	0.6-0.9V	10
VDAC	TV DAC supply, external PNP	2.5/2.6/2.7/2.775	250
VUSB2	VUSB/peripherals supply, internal PMOS	2.5/2.6/2.75/3.0	65
	VUSB/peripherals external PNP	2.5/2.6/2.75/3.0	350
VGEN1	General peripherals supply #1	1.2/1.25/1.3/1.35/ 1.4/1.45/1.5/1.55	250
VGEN2	General peripherals supply #2, internal PMOS	2.5/2.7/2.8/2.9/3.0/ 3.1/3.15/3.3	50
	General peripherals supply #2, external PNP	2.5/2.7/2.8/2.9/3.0/ 3.1/3.15/3.3	250
VUSB	USB Transceiver supply	3.3	100

5.2 MC34709 Power-up Sequence

The MC34709 has 5 PUMS signals that enable to program the power up sequence as well as the default output voltage for specific rails, making the part suitable to supply DDR2, DDR3, LPDDR2, LVDDR3 memories with the correct power up sequence for many processors of the i.MX family. The following table shows the power up sequence and all possible voltage combinations to supply the i.MX50 in all possible modes.

Table 7. Power-up Defaults

i.MX50	mDDR	LPDDR2	LPDDR2	mDDR	LPDDR2	mDDR
PUMS[4:1]	**1010**	**1011**	**1100**	**1101**	**1110**	**1111**
PUMS5=0 VUSB2/VGEN2	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP
PUMS5=1 VUSB2/VGEN2	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS
SW1A (VDDGP)	1.1	1.1	1.1	1.1	1.1	1.1
SW1B (VDDGP)	1.1	1.1	1.1	1.1	1.1	1.1
SW2[8] (VCC)	1.2	1.2	1.2	1.2	1.2	1.2
SW3[8] (VDDA)	1.2	1.2	1.2	1.2	1.2	1.2
SW4A[8] (DDR/SYS)	1.8	1.2	3.15	3.15	3.15	3.15
SW4B[8] (DDR/SYS)	1.8	1.2	1.2	1.8	1.2	1.8
SW5[8] (I/O)	1.8	1.8	1.8	1.8	1.8	1.8
VUSB[9]	3.3	3.3	3.3	3.3	3.3	3.3
VUSB2	2.5	2.5	2.5	2.5	2.5	2.5
VSRTC	1.2	1.2	1.2	1.2	1.2	1.2
VPLL	1.8	1.8	1.8	1.8	1.8	1.8
VREFDDR	On	On	On	On	On	On
VDAC	2.5	2.5	2.5	2.5	2.5	2.5
VGEN1	1.2	1.2	1.2	1.2	1.2	1.2
VGEN2	3.1	3.1	3.1	3.1	2.5	2.5
Not used on System						
SWBST	Off	Off	Off	Off	Off	Off

Notes
8. The SWx node are activated in APS mode when enabled by the start-up sequencer.
9. VUSB is supplied by SWBST.

Table 8. Power-up Sequence i.MX50

Tap x 2.0 ms	PUMS [4:1] = [0100, 1011, 1100, 1101, 1110, 1111]
0	SW2
1	SW3
2	SW1A/B
3	VDAC
4	SW4A/B, VREFDDR
5	SW5
6	VGEN2, VUSB2
7	VPLL
8	VGEN1
9	VUSB

VCOREDIG, VSRTC, and VCORE, are brought up in the pre-sequencer start-up. See Figure 2

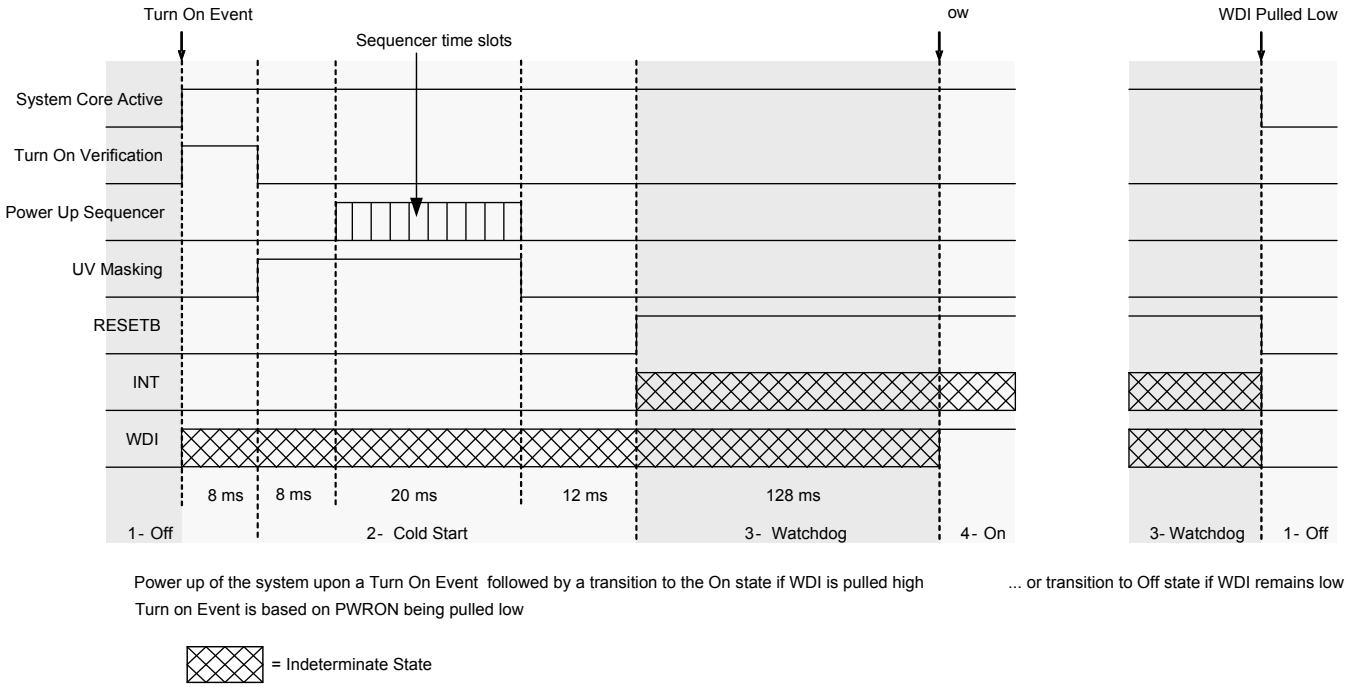

Figure 20. Complete MC34709 Power-up Sequence

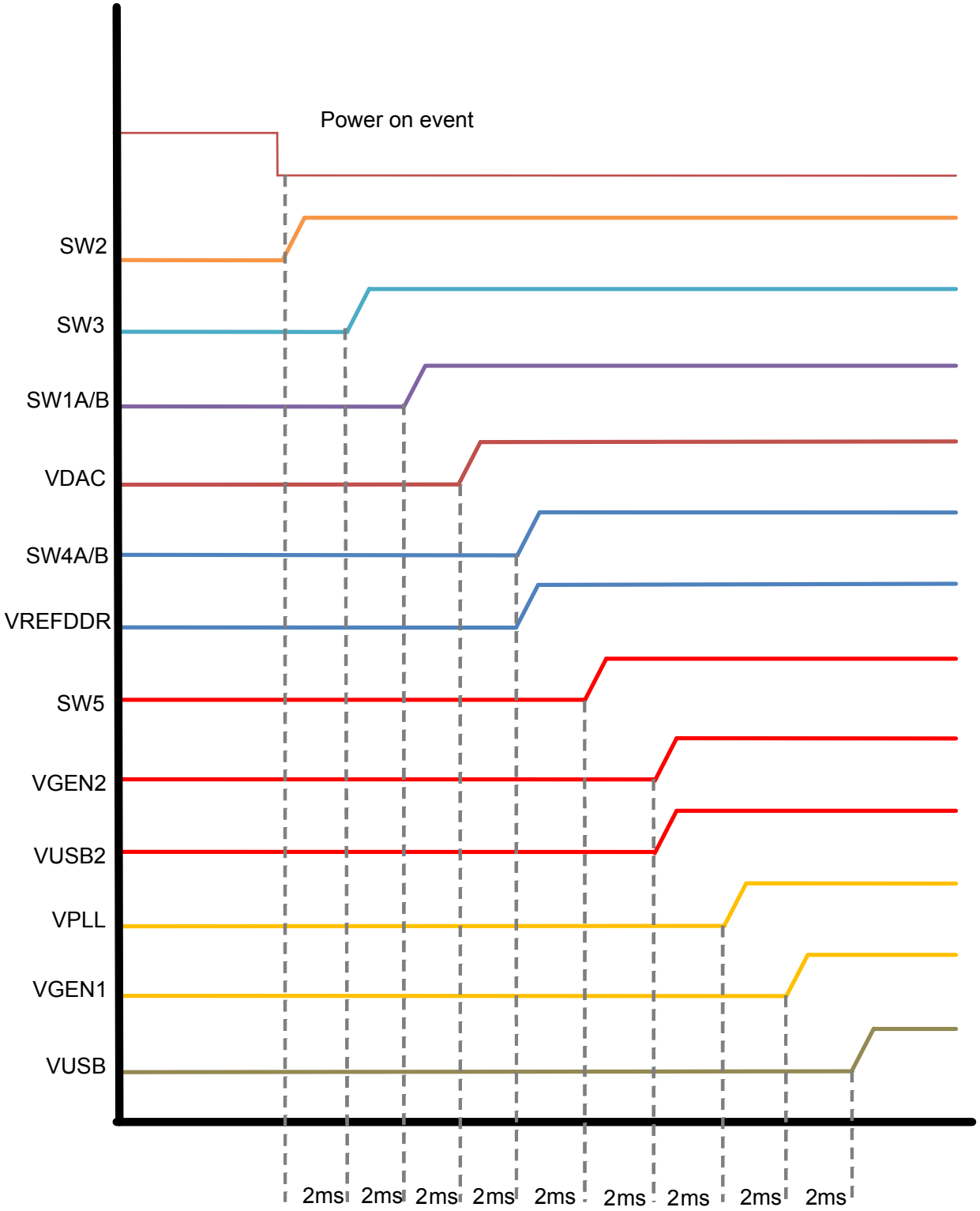

Figure 21. MC3709 Power up Sequence for i.MX50 processors.

5.3 Interfacing the i.MX50 with the MC34709

Table 9, shows all the i.MX voltage rails, their power requirements and their associated MC34709 regulator. Most of the supply domains have flexible voltage and could be adjusted or supplied with a different regulator depending on each application needs

Table 9. i.MX50 voltage domain supplies with the MC34709

I.MX50						MC34709			
Power Rail of i.MX50	**Power Domain**	**MIN**	**TYP**	**MAX**		**Associated Regulator**	**PUM[4:0] =1110**	**Current (mA)**	**PUS**
NVCCSRTC	32 kHz osc. power (when chip off)		1.2			VSRTC	1.2		-
VCC	LP Transistor power		1.2			SW2	1.2	1000	0
VDDA	Peripheral Memory + L2 Cache power		1.2			SW3	1.2	500	1
VDDAL1	L1 Cache power		1.2			SW3	1.2	500	1
VDDGP	Core and G Transistor power		1			SW1A/B	1	1600	2
VDDO2P5	Predriver for EMI pads		2.5			VDAC	2.5	50	3
NVCC_EMI_DRAM	Power to EMI pins		1.2			SW4B	1.2	500	4
VREF	DRAM Reference		0.9						
ALL 3.3V IO NVCC	3.0 V I/Os		-						
VDD3P0	VDD2P5 LDO input + power to Bandgap, DCDC predriver, tempsensor, 480 MHz PLL		3			SW4A	3.15	500	4
USB_OTG_VDDA33	Power to USB Host		3.3			VUSB	3.3	100	9
USB_H1_VDDA33	Power to USB OTG		3.3			VUSB	3.3	100	9
All 1.8 IO NVCC	1.8 V I/Os		-						
NVCC_RESET (LVIO)	Power to POR_B,RESET_IN_B, TESTMODE, & BOOTMODE[0:1]		1.875 or 2.775			SW5	1.8	1000	5

Table 9. i.MX50 voltage domain supplies with the MC34709

I.MX50						MC34709			
Power Rail of i.MX50	Power Domain	MIN	TYP	MAX		Associated Regulator	PUM[4:0] =1110	Current (mA)	PUS
VDD2P5	Power to 24 MHz osc, efuse, xtalok, 32 kHz osc. power mux		2.5			VGEN2	2.5	250	6
USB_OTG_VDDA25	Power to USB Host		2.5			VGEN2	2.5	250	6
USB_H1VDDA25	Power to USB OTG		2.5			VGEN2	2.5	250	6
VDD1P8	Power to all PLLs		1.8			VPLL	1.8	50	7
VDD1P2	Power to all PLL digital, 32 kHz osc. (when chip on), much of analog, digital		1.2			VGEN1	1.2	250	8

5.3.1 Interfacing Block Diagram

The following block diagrams show all the power connections needed for the interface, as well as how the communication signals must be connected between the i.MX50 and MC34709.

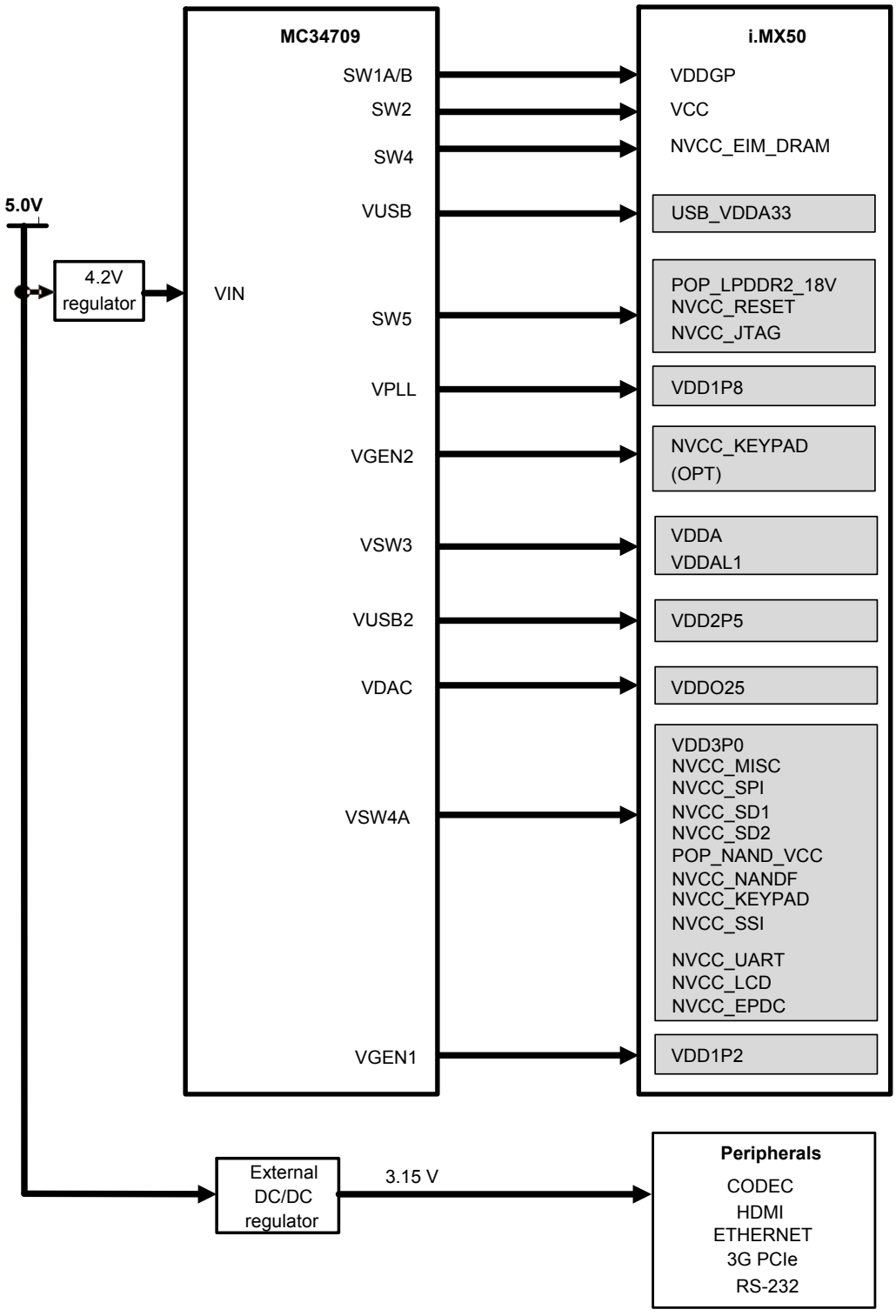

Figure 22. i.MX50 Power Interface with MC34709 Block Diagram

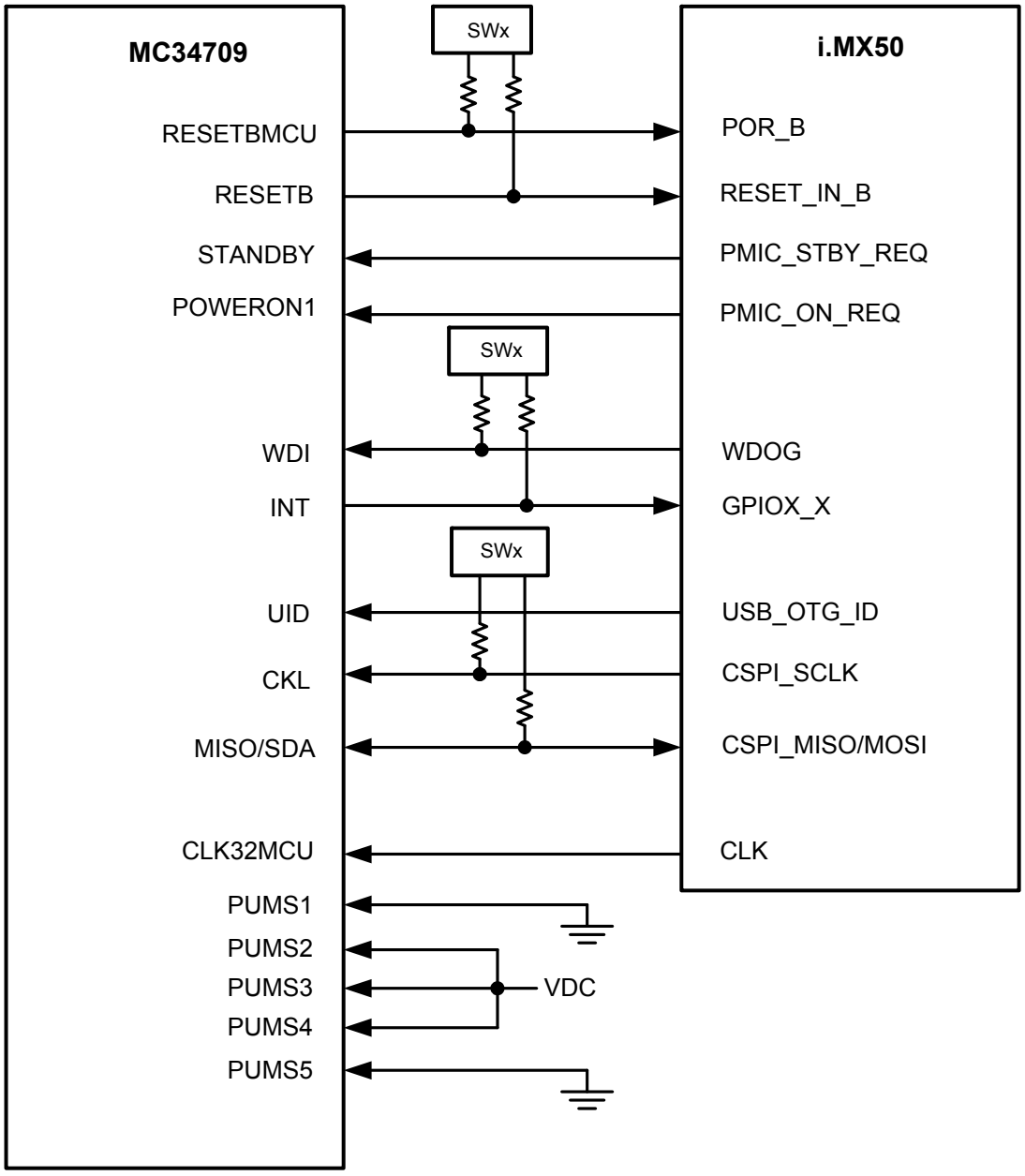

Figure 23. i.MX50 Control Interface with MC34709 Block Diagram

5.3.1.1 3.15 V DC-DC power supply

For system stability, it is recommended that you use an extra 3.15 V DCDC power supply to support large current requirements (for example a 3G module or Wi-fi card). The MC34709 has limited 3.15 V output ability to supply al peripherals, however, in cases where Ethernet, 3G, or Wi-fi are not required, this buck converter may be eliminated from the power three.

5.3.2 Interface Power-up Sequence

The resulting power-up sequence of the interface is shown in the following figure

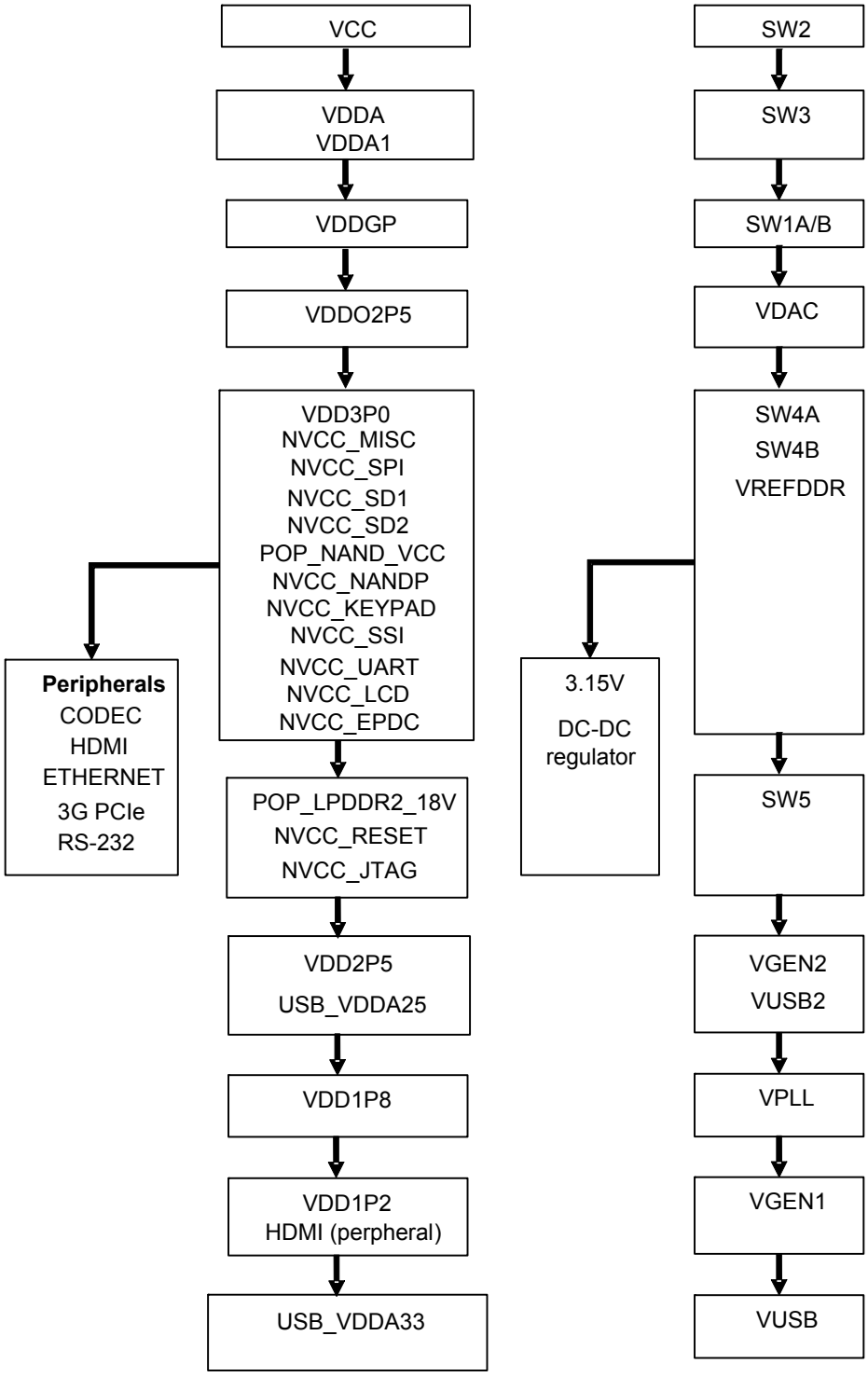

Figure 24. Power up Sequence Flow Chart

5.4 Application Example with the MC34709

The following schematic is simplified application example for interfacing the MC34709 with an i.MX50 processor. note that this schematic only includes the block related to the power section as well as power management controlling signals.

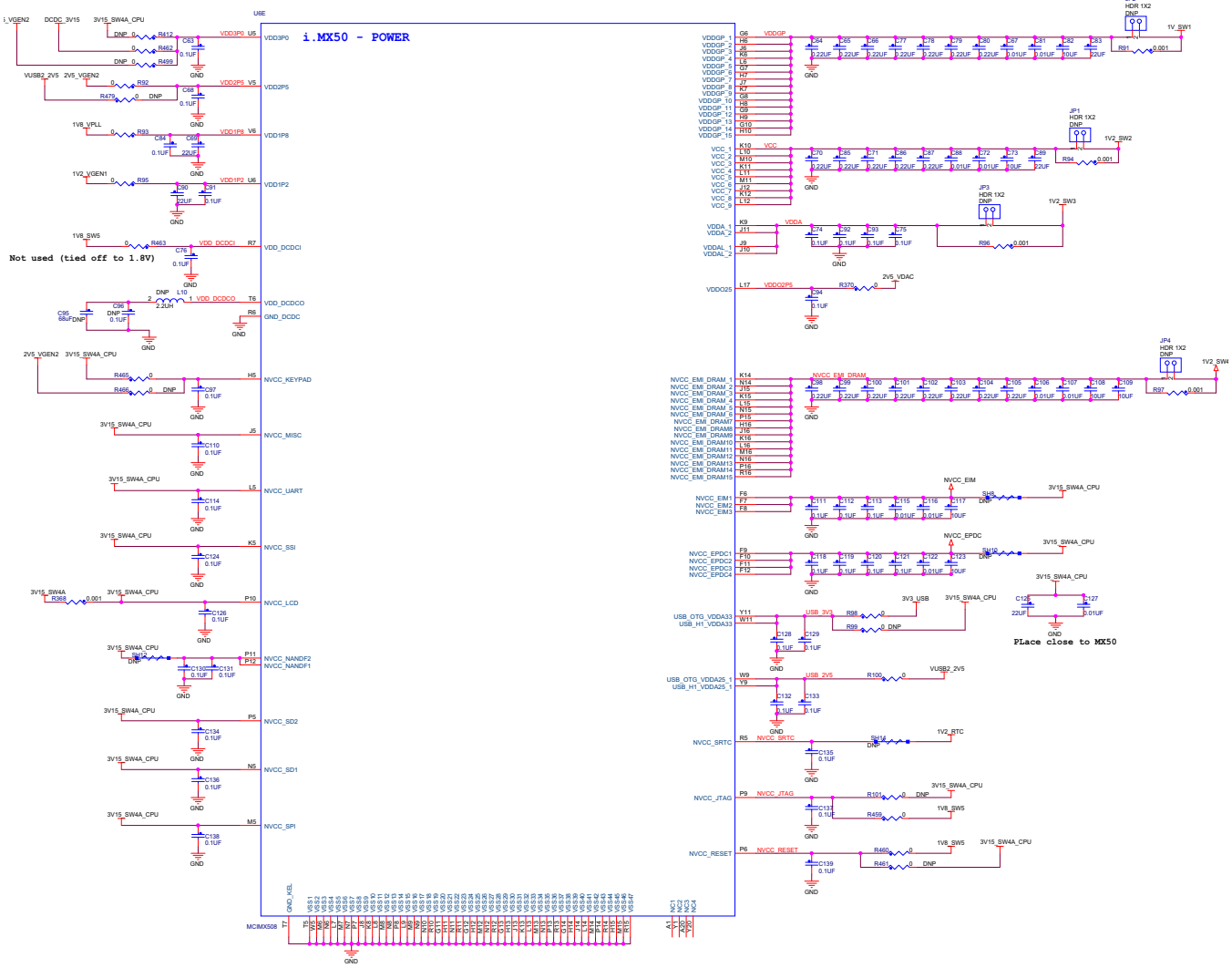

Figure 25. i.MX50 Voltage Domain Distribution

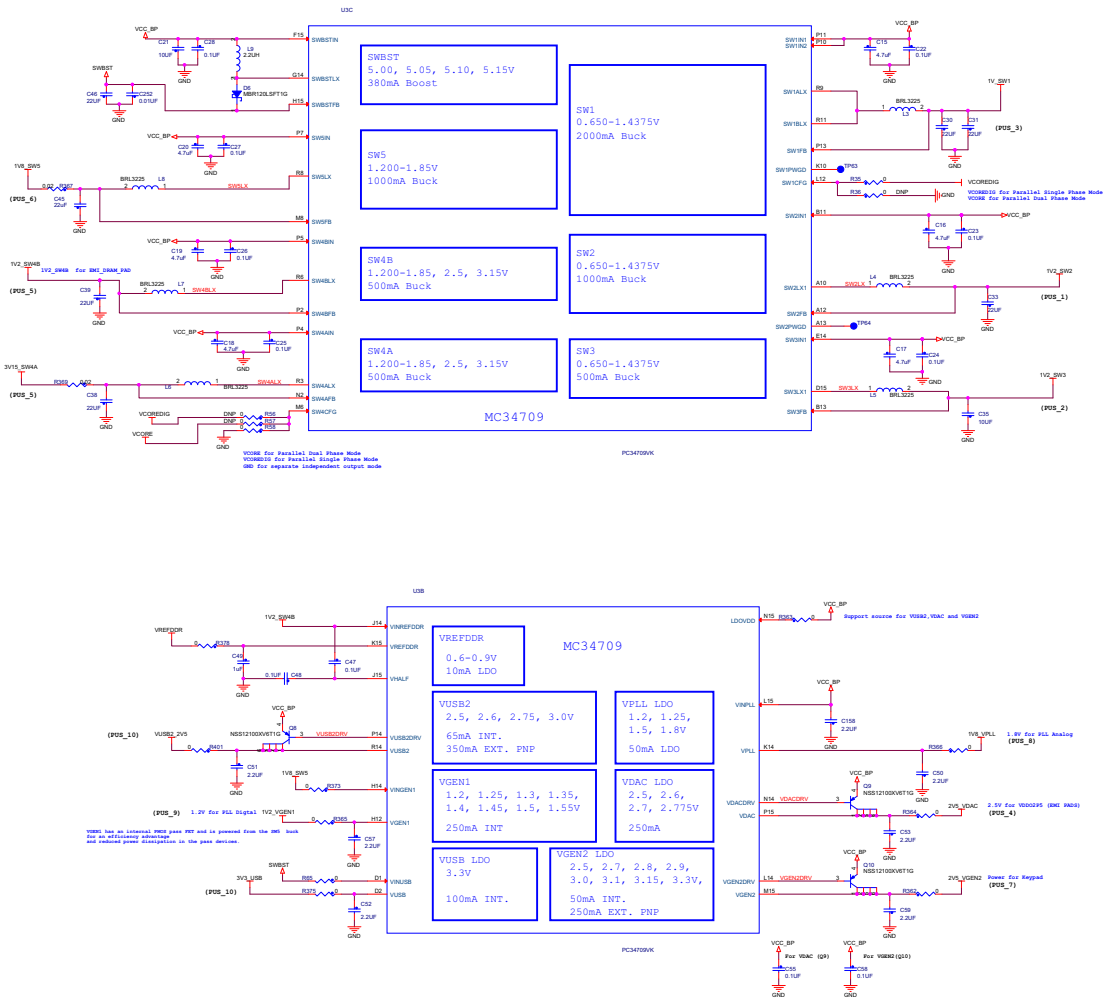

Figure 26. MC34709 Power Supplies Schematic

3.15V/2A Regulator

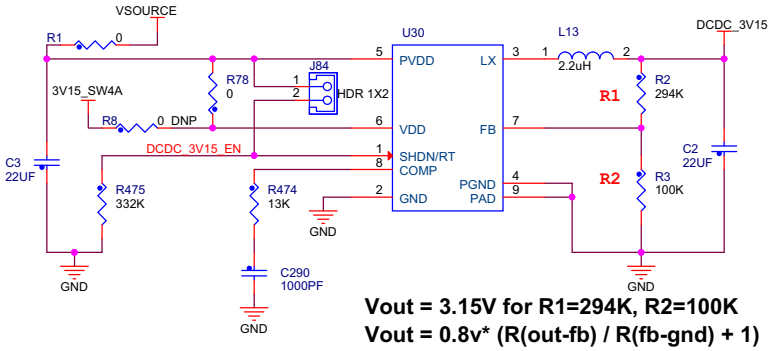

Figure 27. 3.15V DC-DC Regulator

Battery Regulator & Terminals

3-pin connector J2 allows the use of aftermarket Li-ION batteries. Recommended battery capacity is 800 - 1500 mAh.

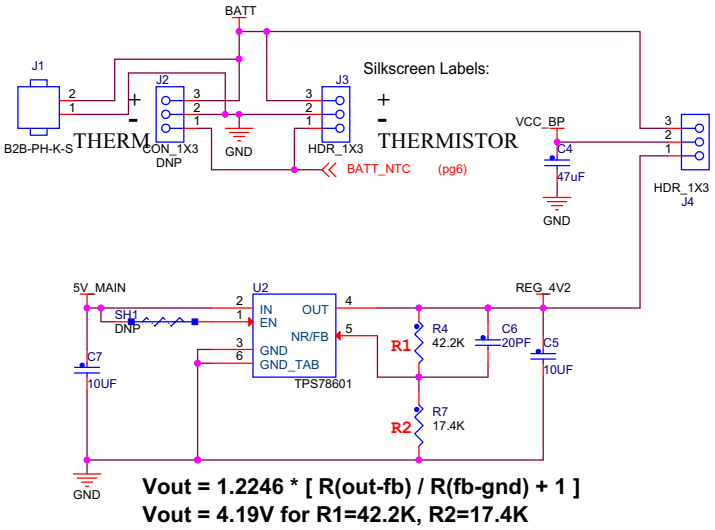

Figure 28. Main BP Supply (Battery or 4.2V)

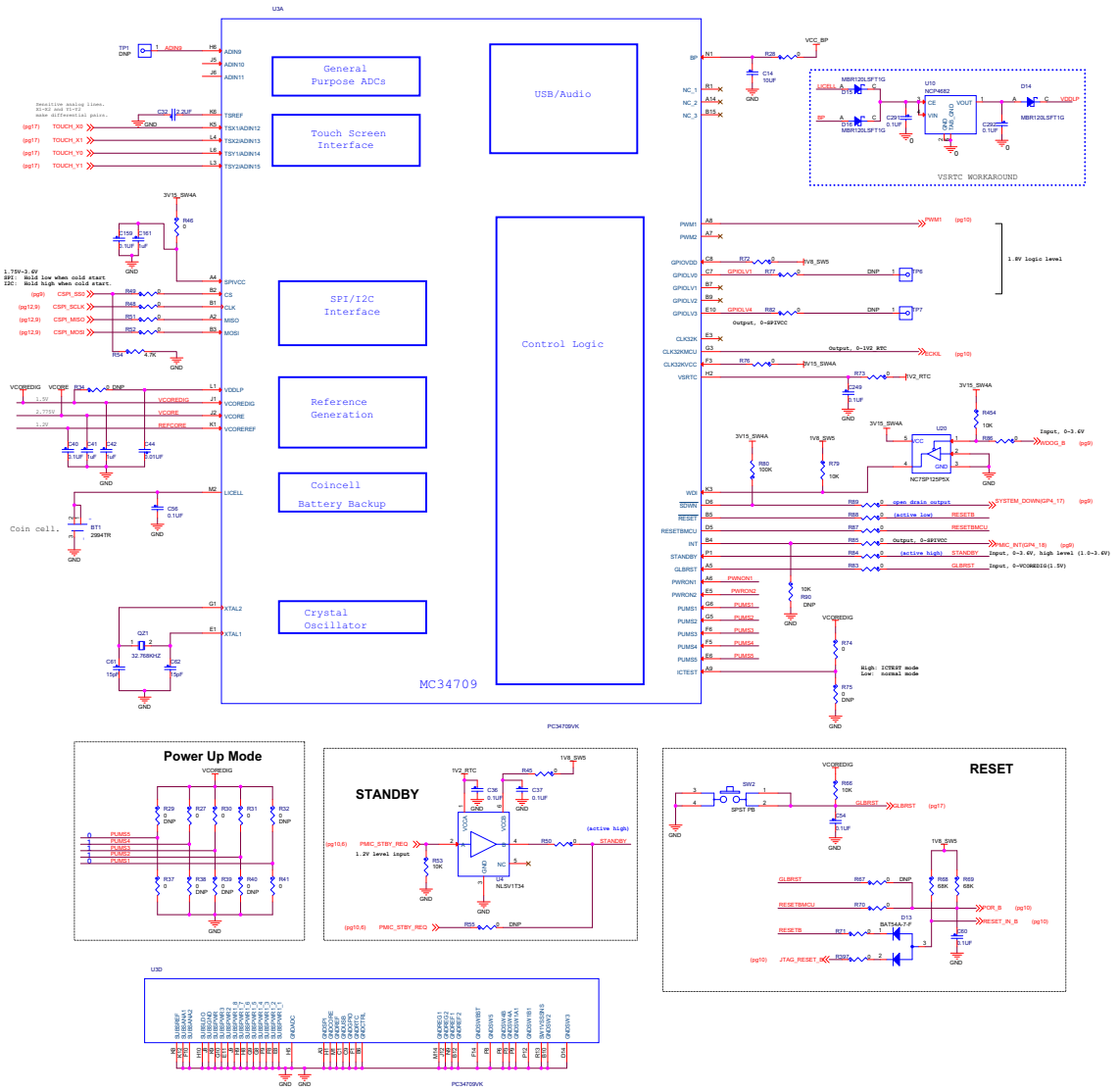

Figure 29. MC34709 System/Control Signals

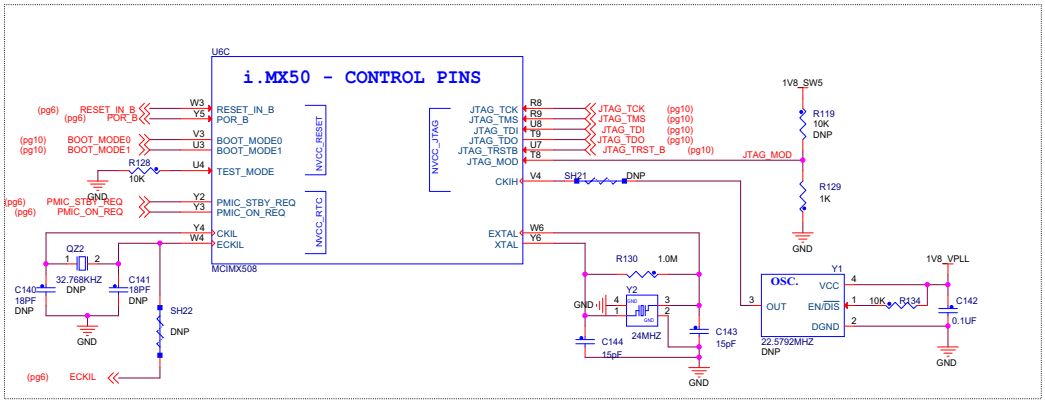

Figure 30. i.MX50 Control Signals

If an external battery charger is required, it is recommended to use a charger with power path management which isolates the battery from the system node while charging. The main system voltage from the charger will be connected directly to the BP node while the external charging voltage and the battery are connected on the charger's end.

5.5 MC34709 layout example

The following is a layout example of the MC34709 implemented on a four layer board with all component on the top layer and using standard 8 mils vias.

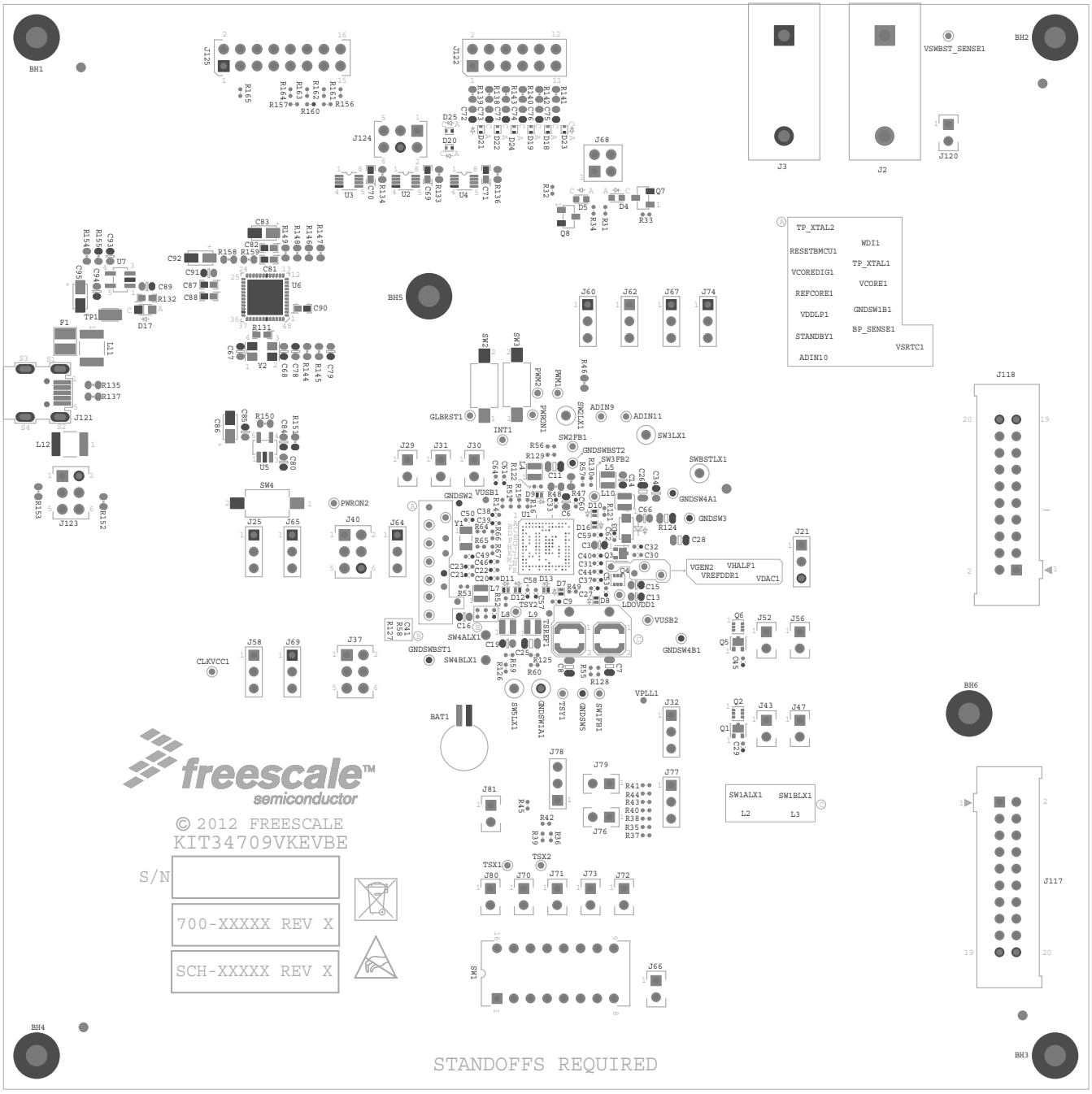

Figure 31. KIT34709VKEVBE FAB Drawing

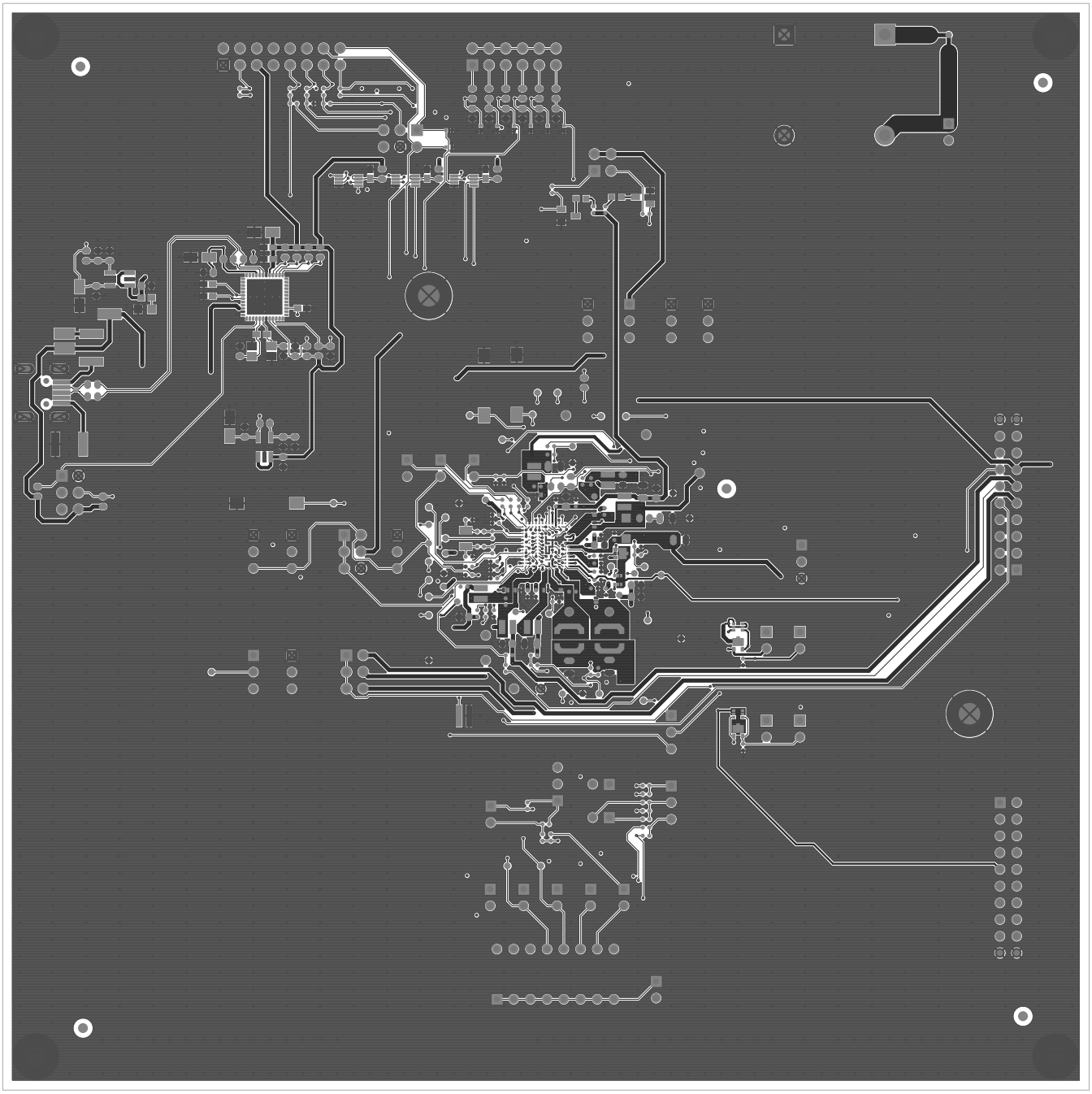

Figure 32. KIT34709VKEVBE Top Layer

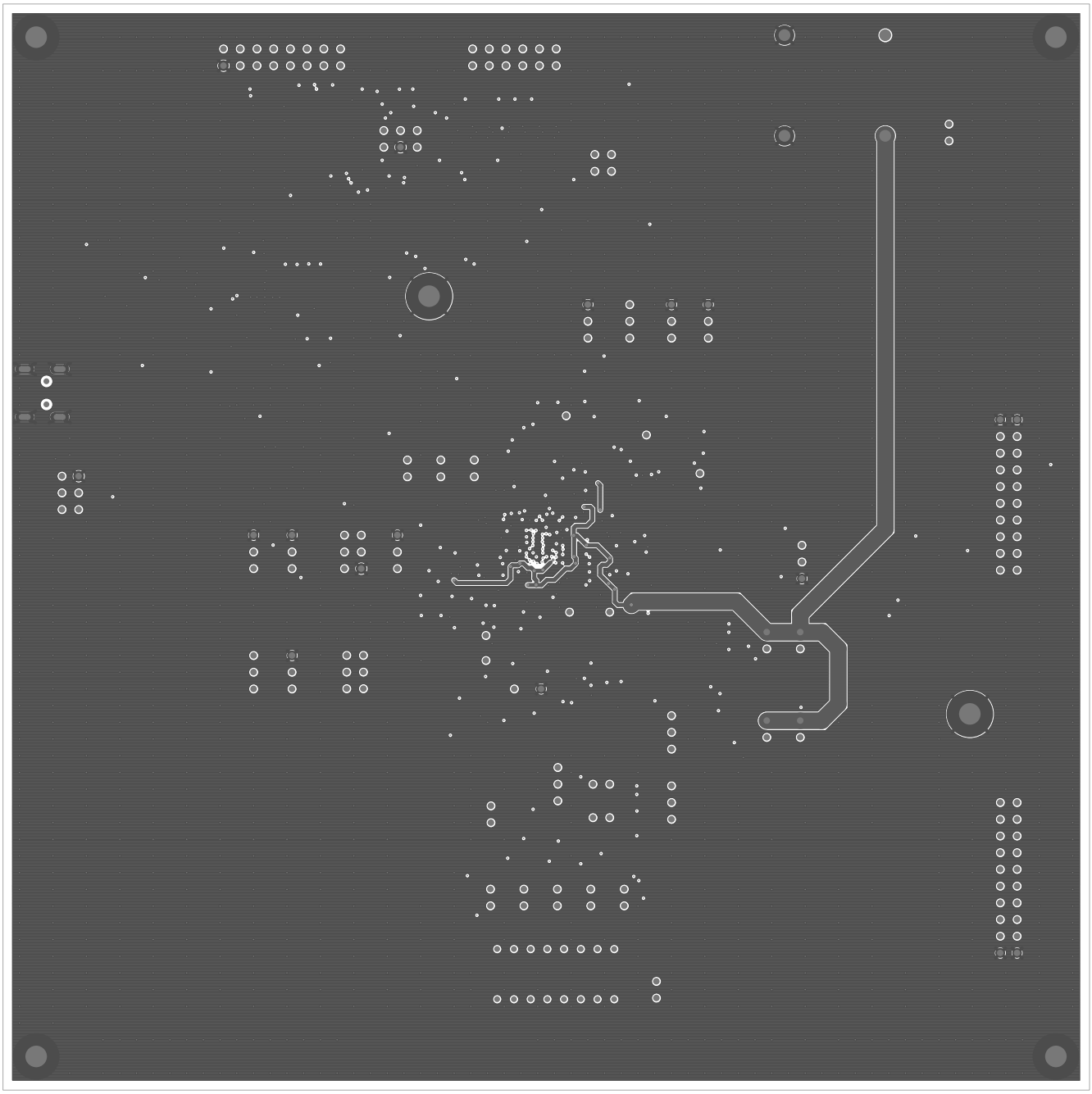

Figure 33. KIT34709VKEVBE Layer 2

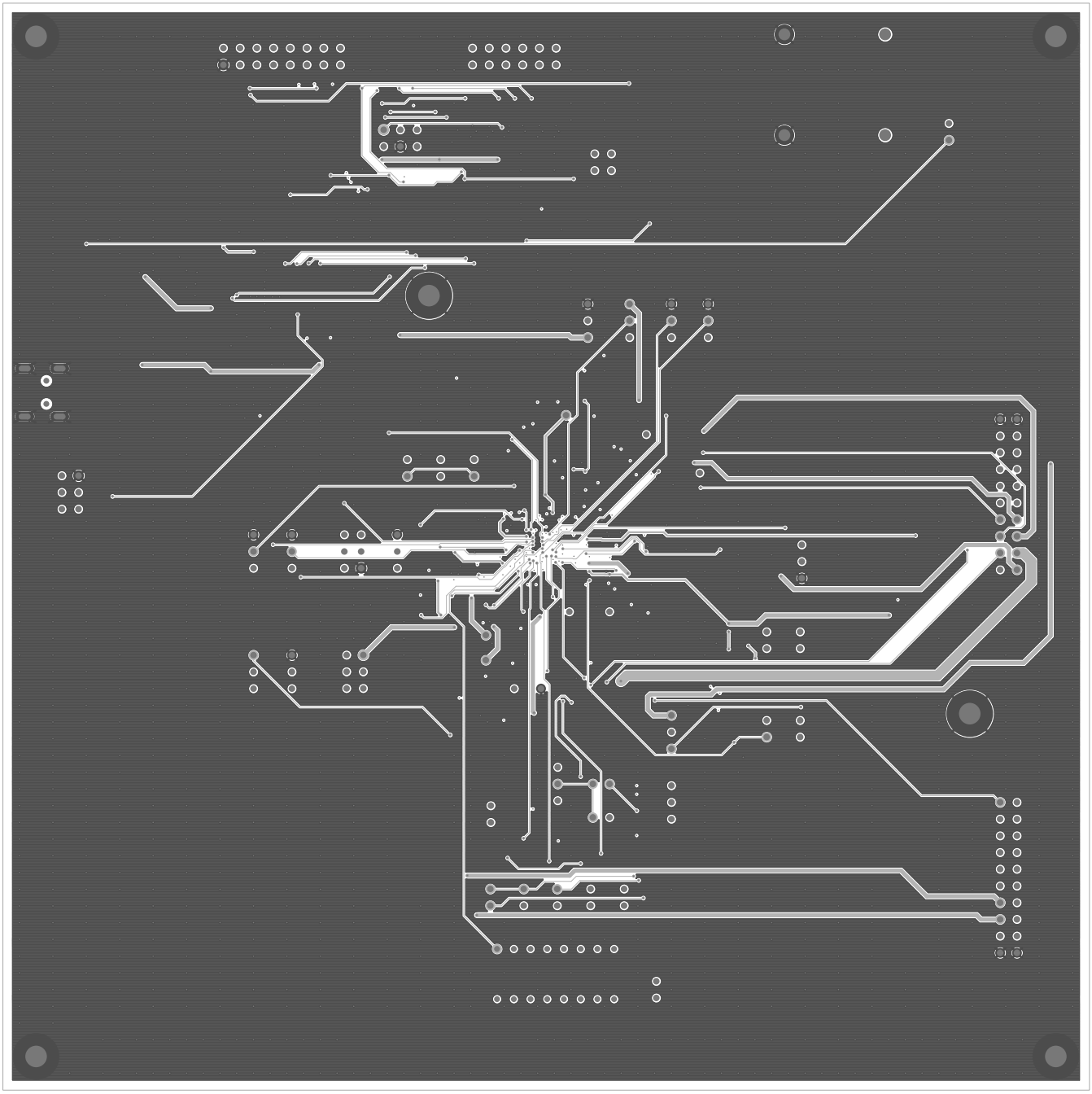

Figure 34. KIT34709VKEVBE Layer 3

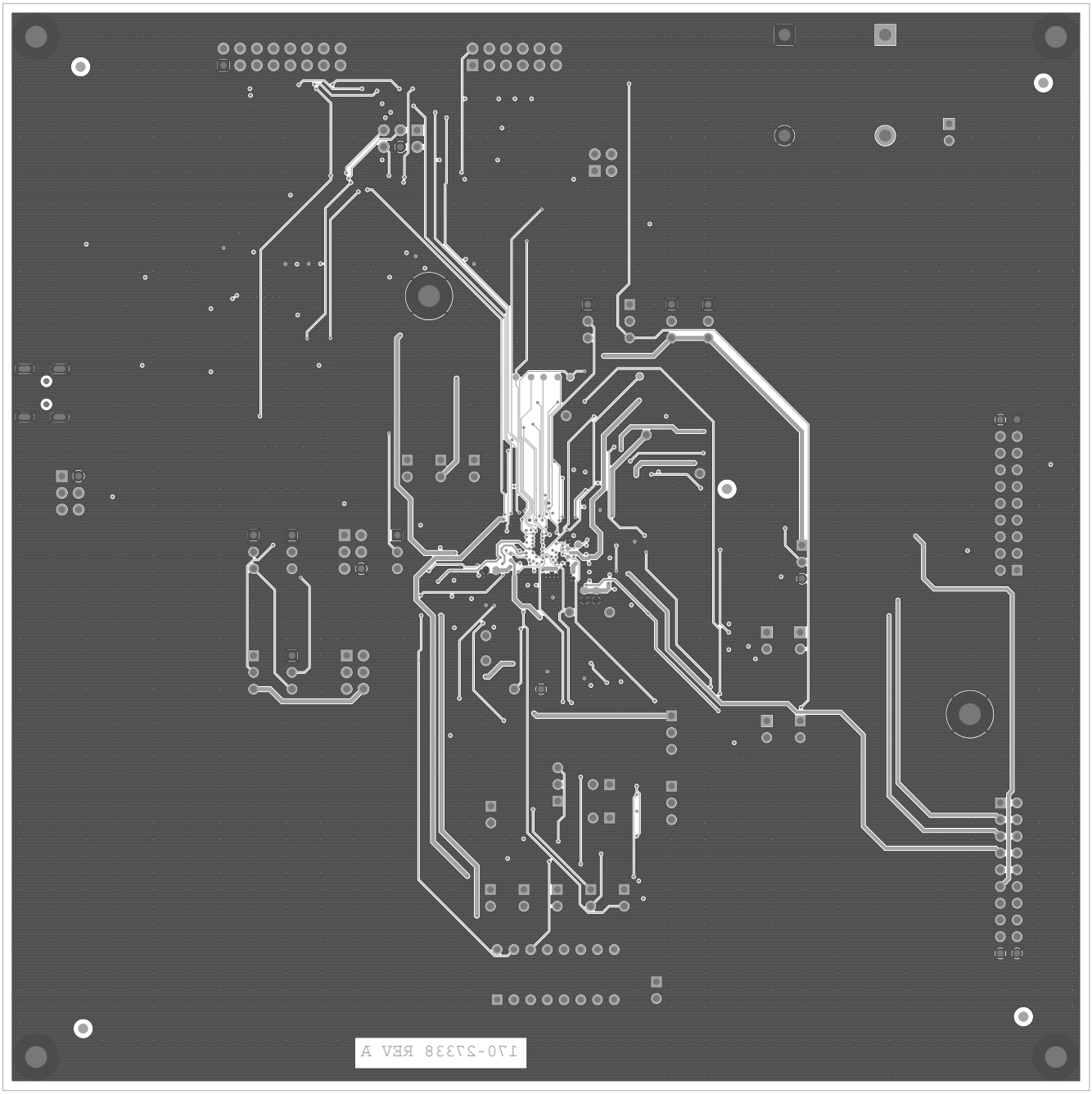

Figure 35. KIT34709VKEVBE Bottom Layer

5.6 Migrating from MC34708 to MC34709

For customers migrating from the MC34708 platform to the MC34709 a very low design effort is required due to the high compatibility system between the to devices. Table 10 shows the main difference between both power management devices.

Table 10. MC34708 and MC34709 difference

Features	MC34708	MC34709
Control Logic		
• Power control logic with processor interface and event detection	Yes	Yes
• Single SPI/I2C bus for control & register access	Yes	Yes
• Real time clock and crystal oscillator circuitry with coin cell backup	Yes	Yes
• Support for external secure real time clock on a companion system processor IC	Yes	Yes
10 bit ADC		
• 4 wire resistive touchscreen interface	Yes	Yes
• 7 External ADC inputs.	Yes	Yes
• Dedicated ADC channel for Battery voltage sensing	Yes	No
• Dedicated ADC channel for battery current sensing	Yes	No
• Dedicated ADC channel for BP voltage	Yes	No
• Dedicated ADC channel for Die temperature	Yes	Yes
• Dedicated ADC channel for VBUS voltage. (USB device detection)	Yes	No
• Dedicated ADC channel for coin cell voltage	Yes	Yes
Power Supplies(10)		
• 5 Buck regulator	Yes	Yes
• 1 Boost regulator	Yes	Yes
• 8 LDO Regulators with internal and external pass devices.	Yes	Yes
Auxiliary Circuits		
• USB/UART/Audio switching for mini-micro USB connector	Yes	No
• Four general purpose low voltage I/Os with interrupt capability	Yes	Yes
• Two PWM outputs	Yes	Yes
• Two General purpose LED drivers	Yes	No
Package		
• 206 MAPBGA - 8.0 x 8.0 mm - 0.5 mm pitch	Yes	No
• 206 MAPBGA - 13 x 13 mm - 0.8 mm pitch	Yes	No
• 130 MAPBGA - 8.0 x 8.0 mm - 0.5 mm Pitch	No	Yes

Notes:

10. All Power supplies have the same voltage and current rating on both devices.

Firmware portability is straights forward, since register maps are bit to bit compatible. However, the MC34709 uses a reduced set of register which eliminate all registers/bits related to the functionality not supported on the MC34709, therefore care must be taken that RESERVED registers/bits are not addressed on the firmware when porting the application to the MC34709.

6 References

Document Number	Description	Description / URL
MC34709	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC34709.pdf?fsrch=1&sr=2
MC13892	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MC13892.pdf?fsrch=1&sr=1
IMX50SDG	Development Guide	http://cache.freescale.com/files/32bit/doc/user_guide/IMX50SDG.pdf?fsrch=1&sr=1
IMX50RM	Reference Manual	http://cache.freescale.com/files/32bit/doc/ref_manual/IMX50RM.pdf?fsrch=1&sr=10
IMX50CEC	Data Sheet	http://cache.freescale.com/files/32bit/doc/data_sheet/IMX50CEC.pdf

7 Revision History

Revision	Date	Description of Changes
1.0	12/2012	• Initial release

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