TI Triple rate SDI module for Xilinx XtremeDSP starter platform

Part No. SDXILEVK/NOPB

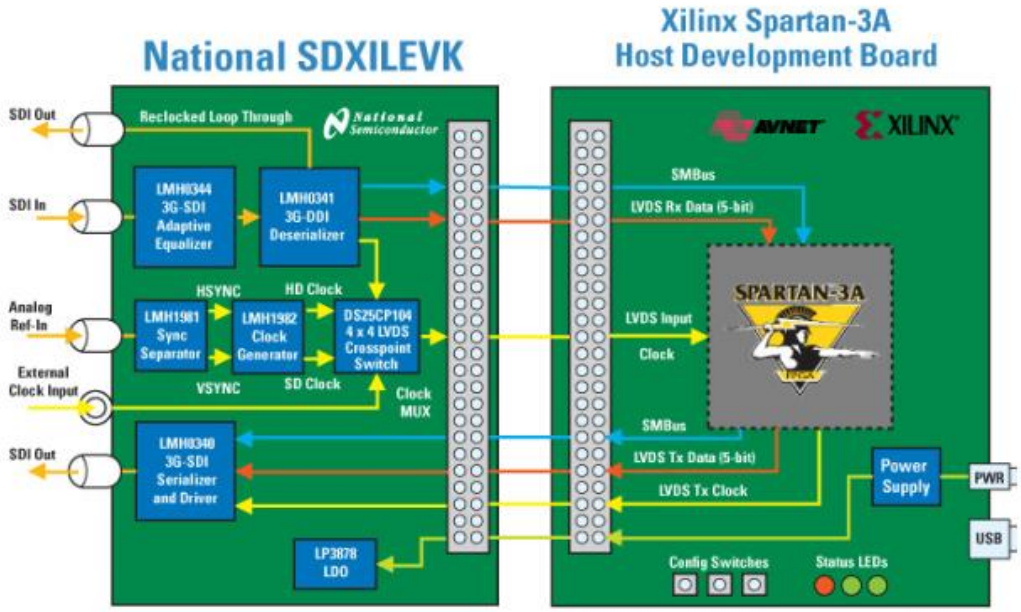
Texas Instruments in collaboration with Xilinx developed a triple-rate SDI and video clocking daughter card for the Xilinx Spartan-3A/3E development kits. The daughter card plugs directly into the Spartan development board through an EXP connector. The combined solution of the daughter card and the development kit provides broadcast video system designers a comprehensive platform for rapid evaluation and prototyping of new designs to reduce time to market.

The daughter card is also referred in the documents below by its internal TI part name SDXILEVK. The TI part name is used for reference only and cannot be used to order the part.

The 3G SDI SerDes evaluation system consists of:

- Xilinx XtremeDSP starter platform Spartan-3A DSP 1800A edition (sold separately by Xilinx)
- TI SDI video and clocking daughter card (SDXILEVK)
- SDXILEVK Schematics, Bill of Materials (BOM)
- FPGA IP (not included in the box)

SDXILEVK Hardware Platform



The SDXILEVK daughter card contains:

- LMH0344 - Triple-rate SDI Adaptive Cable Equalizer
- LMH0340 - Triple-rate SDI Serializer with integrated cable driver
- LMH0341 - Triple-rate SDI deserializer with reclocked loop through
- LMH1981 - Multi-Format Video Sync Separator
- LMH1982 - Multi-Rate Video Clock Generator
- DS25CP104A - 4x4 LVDS Crosspoint Switch
- LP3878-ADJ - Low Noise LDO

The SDXILEVK supports a complete 3G-SDI signal path consisting of adaptive cable equalizer (LMH0344), deserializer with reclocked loop through (LMH0341) and serializer with integrated cable driver (LMH0340). A multi-rate sync separator (LMH1981) and clock generator (LMH1982) deliver ultra-low jitter reference clocks to the host FPGA. A 4x4 LVDS crosspoint switch (DS25CP104A) acts as a reference clock selector to choose between four separate clocking options:

- Recovered clock from LMH0341 deserializer
- Genlock from analog reference, LMH1981 sync separator and LMH1982 clock generator
- Local clock generation from LMH1982 in free-run mode
- External clock via SMA connector

These selectable reference clocks allow designers to compare system performance using different clocking sources. For example, one application may require genlock capability for synchronization while another one leverages the recovered clock from the SDI deserializer. Designers may compare system jitter performance of each clocking solution then make architectural decisions based on system requirements and constraints.

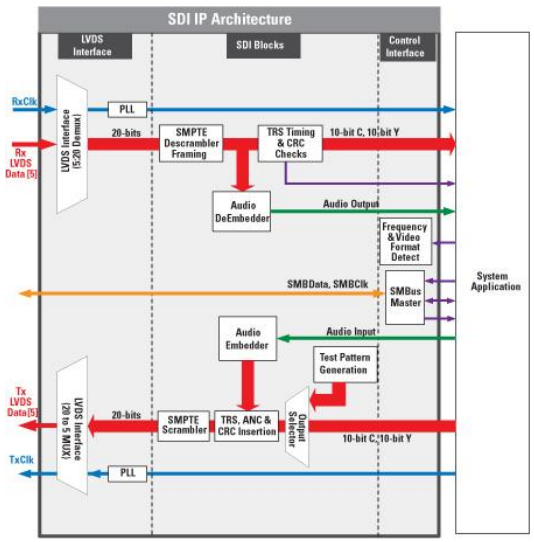
FPGA IP Description

A full set of FPGA firmware is available from TI as source code to enable quick system integration and faster time to market. This IP implements the SMPTE SDI framing and deframing protocols. A reference design using this IP is available for the Xilinx Spartan-3A/3E host development kits and is compatible with other Spartan-3A and Spartan-3E devices.

The IP architecture includes:

- Triple rate SDI support with automatic rate detect
- SMPTE scrambling, descrambling and framing
- Audio embedding and de-embedding
- Test pattern generation for development and validation
- 20:5 output muxing and 5:20 input demuxing to support the 5-bit LVDS interface bus
- SMBus management interface

By providing both the hardware and FPGA firmware, TI enables maximum flexibility to modify system design, quickly adapt to standard changes, add features, and reduce time-to-market. Competing solutions that integrate the protocol blocks locally in the discrete SerDes, constrain system designs to a minimal set of digital functions.



Feature	Benefit
Triple-Rate SDI	Supports SD, HD and 3G-SDI (SMPTE 259M-C, 292M, 424M)
Four Clocking Options	Compare SerDes jitter performance with multiple reference clocks
Verilog or VHDL Source Code	Flexible SMPTE IP allows users to easily customize features and functions
Genlock	Synchronize timing to analog house reference
Audio Embedding / De-embedding	Support up to 8-channels of audio embed / de-embed
Serial Reclocked Loop Through	Enables low-jitter input monitoring or daisy chaining
Two Triple-Rate SDI Outputs	Support Dual-Link SMPTE
High Input Jitter Tolerance	Receive, lock and deserialize noisy signals with accumulated jitter
Ultra-Low Output Alignment Jitter	Transmit ultra-clean output signals well within SMPTE jitter specifications