

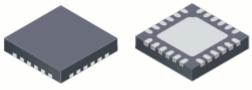


Single LNB Supply and Control Voltage Regulators

Features and Benefits

- Integrated boost MOSFET, current sensing, compensation, and output LDO
- Configurable boost capacitor option:
- A8300: ceramic
- A8300-1: electrolytic
- Sleep mode with shutdown current < 15 μ A (typ)
- Early Power Failure (EPF) warning function
- Backfeed current control
- Robust output pin voltage rating for surge and backfeed protection
- Adjustable LNB output current limit from 300 to 950 mA
- Selectable overcurrent disable timer
- Covers a wide array of application requirements
- Minimizes component sizing to fit each application
- For startup, reconfiguration, and continuous output (maximum value depends on PCB thermal design)
- Boost peak current limit scales with LNB current limit setting
- LNB overcurrent limit protection and TSD can be either latched or auto-restart
- Full DiSEqC[™] compatibility
- Dynamic tone detect amplitude and frequency transmit/receive thresholds
- Diagnostic features: PNG, TDET, and EPF
- Extensive protection features: UVLO, TSD, CPOK, and OCP

Package: 24-contact MLP/QFN with exposed thermal pad (suffix ES)



 $4 \text{ mm} \times 4 \text{ mm} \times 0.75 \text{ mm}$

Description

Intended for analog and digital satellite receivers, these single low noise block converter regulators (LNBR) consist of a monolithic boost converter followed by a low-drop linear regulator. They are specifically designed to provide the power and the interface signals to an LNB down converter via coaxial cable in satellite TV receiver systems.

The A8300 and A8300-1 require few external components, with the boost switch and compensation circuitry integrated inside of the devices. The 563 kHz switching frequency is chosen to minimize the size of the passive filtering components.

For DiSEqC[™] communication the ICs provide an internal 22-kHz tone that is gated with a control pin, or can accept an external 22-kHz through this same pin. In addition, these devices have integrated tone detection capability for full twoway DiSEqC[™] communications, as well as an integrated gate drive for the filter bypass FET.

The I^2C^{TM} -compatible interface provides control capabilities for complex system requirements, as well as diagnostic capabilities for system fault reporting. A sleep pin is also available to maximize power savings and to quickly shut down the device if needed, without using I^2C^{TM} control.

The devices also offer an Early Power Failure (EPF) function, which helps to verify the status of the 12 V rail as well as initiate shutdown routines.

The A8300 and A8300-1 are supplied in a 4 mm × 4 mm, 24-contact, lead (Pb) free QFN package (suffix ES), with 100% matte tin plated leadframe.

Part Number	Package type	Temperature	RoHS Compliant	Part Composition / RoHS Data
A8300SESTR-T	24-lead QFN	-20°C to 85°C	Yes	<u>View Data</u>
A8300SESTR-T-1	24-lead QFN	-20°C to 85°C	Yes	<u>View Data</u>
APEK8300SES-01-MH	DEMO BOARD	-20°C to 85°C	No	
APEK8300SES-01-MH-1	DEMO BOARD	-20°C to 85°C	No	

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