TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6K06FU

High Speed Switching Applications

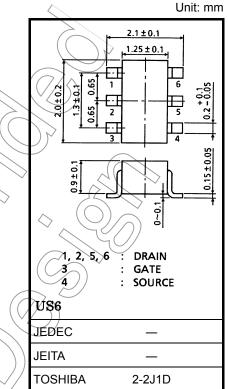
- Small package
- Low ON- resistance: $R_{DS(ON)} = 160 \text{ m}\Omega \text{ max} (@V_{GS} = 4 \text{ V})$

 $R_{\rm DS(ON)} = 210 \text{ m}\Omega \text{ max} (@V_{\rm GS} = 2.5 \text{ V})$

• Low gate threshold voltage

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V _{DS}	20	$(\mathcal{N} \land$	\searrow
Gate-source voltage		V _{GSS}	±12	V V	
Drain current	DC	۱ _D	1.1	\searrow	
	Pulse	I _{DP}	22	~~~	
Drain power dissipation (Ta = 25°C)		PD	300	~ mW	
Drain power dissipation	(14 – 25 C)	(Note 1)	mvv		(
Channel temperature		T _{ch}	150	^°C	
Storage temperature range		T _{stg}	-55 to 150	< ℃	

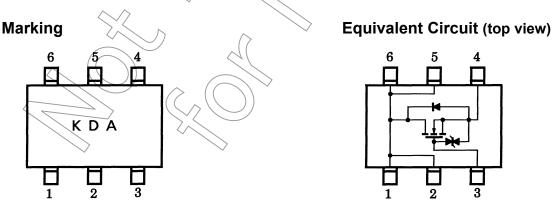


Weight: 6.8 mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (t.e.

operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions")"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board. (25.4 mm \times 25.4 mm \times 1.6 mm, Cu pad: 0.32 mm² \times 6) Figure 1.



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

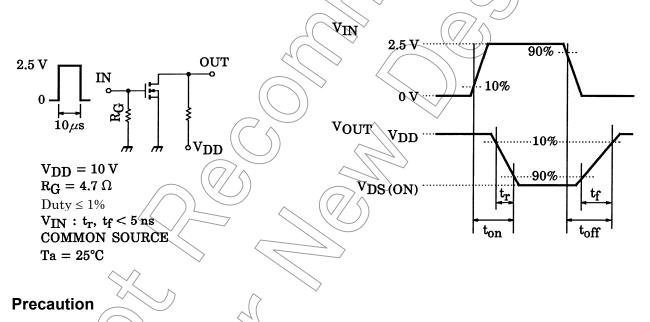
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Electrical Characteristics (Ta = 25°C)

Chara	octeristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage current		I _{GSS}	$V_{GS}=\pm 12~V,~V_{DS}=0$		_	±1	μA	
Drain-source brea	urce breakdown voltage $V_{(BR) DSS}$ $I_D = 1 \text{ mA}, V_{GS} = 0$		20	_	_	V		
Drain cut-off curre	ent	I _{DSS}	$V_{DS} = 20 V, V_{GS} = 0$	\geq	_	1	μA	
Gate threshold vo	ltage	V _{th}	$V_{DS} = 3 \text{ V}, \text{ I}_{D} = 0.1 \text{ mA}$	0.6		1.1	V	
Forward transfer a	admittance	Y _{fs}	$V_{DS} = 3 V, I_D = 0.5 A$ (Note 2)	12)/(S	
Drain-source ON resistance		R _{DS} (ON)	$I_D = 0.5 \text{ A}, V_{GS} = 4 \text{ V}$ (Note 2)	\sum	120	160		
			$I_{D} = 0.5 \text{ A}, V_{GS} = 2.5 \text{ V}$ (Note 2)	\bigcirc	160	210	mΩ	
Input capacitance		C _{iss}	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0, \text{ f} = 1 \text{ MHz}$	_	125		pF	
Reverse transfer	capacitance	C _{rss}	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0, \text{ f} = 1 \text{ MHz}$		30		pF	
Output capacitand	ce	C _{oss}	$V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz$		75		pF	
Switching time	Turn-on time	t _{on}	V _{DD} = 10 V, I _D = 0.5 Å,		42	\searrow	ns	
	Turn-off time	t _{off}	$V_{GS} = 0$ to 2.5 V, $R_{GF} = 4.7 \Omega$	-6	100	> -		

Note 2: Pulse test

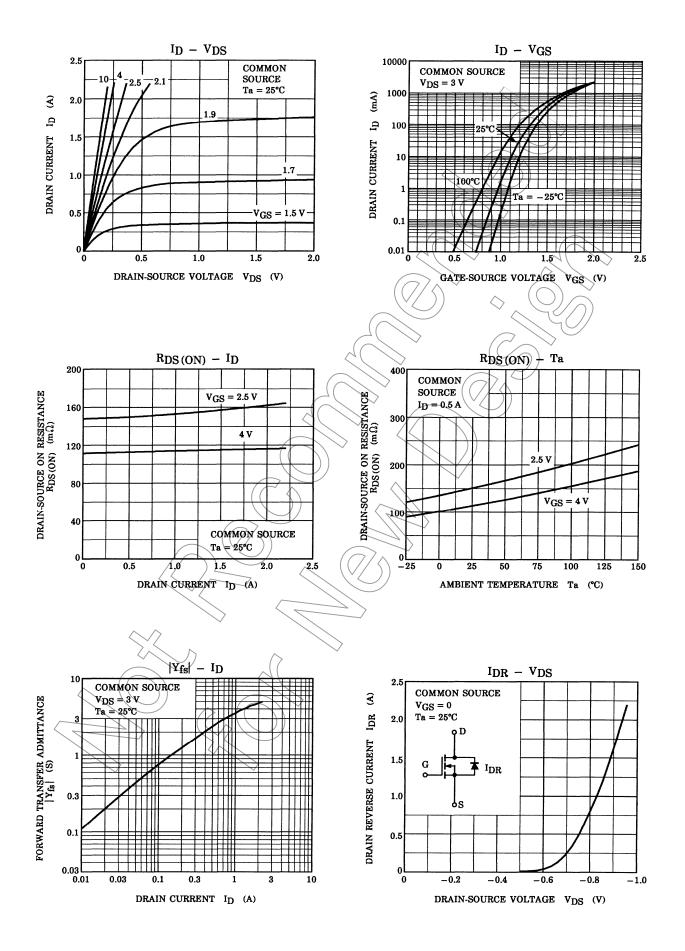
Switching Time Test Circuit



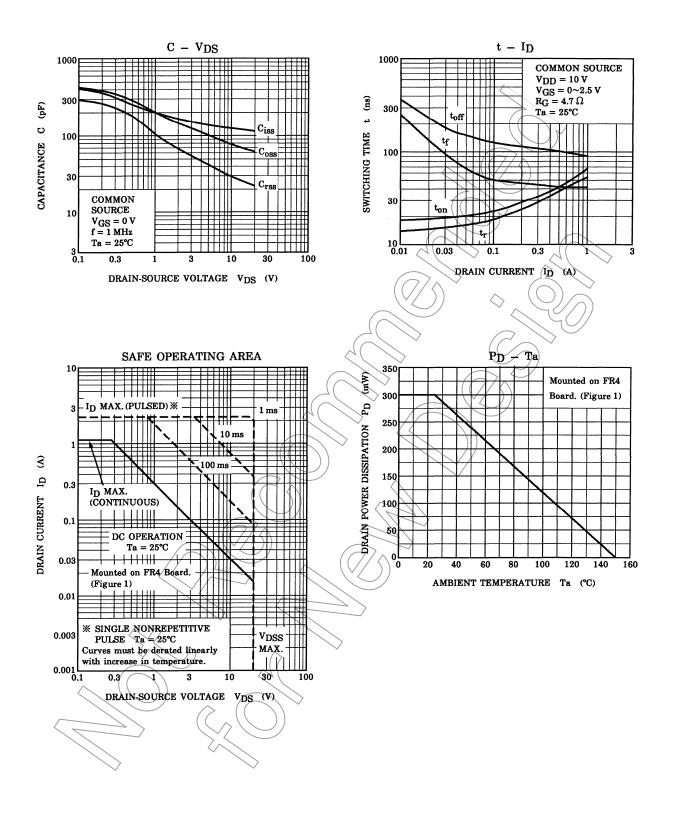
 V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 100 \ \mu A$ for this product. For normal switching operation, VGS (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} .

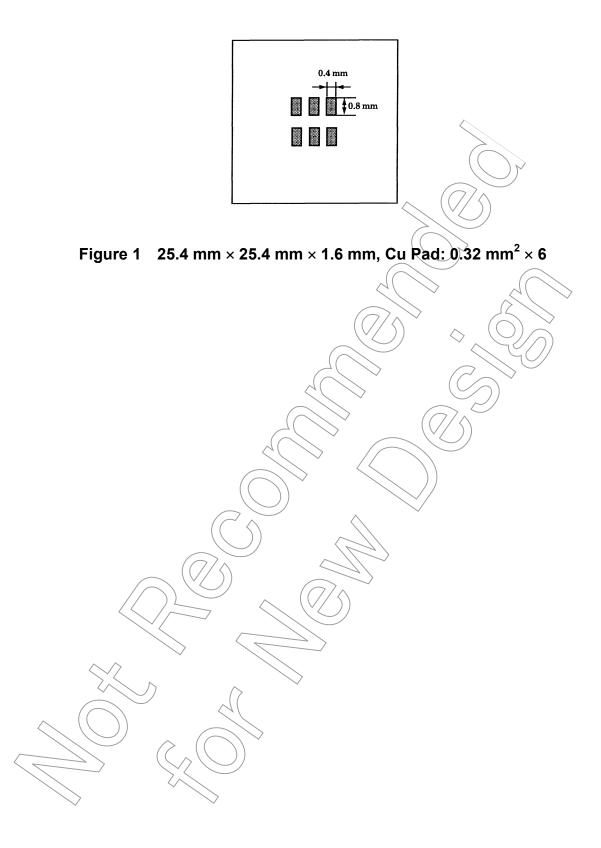
 $\label{eq:GS} \begin{array}{l} \mbox{(Relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on)$)$ Please take this into consideration for using the device. } \end{array}$

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