2.1 ± 0.1 1.25 ± 0.1

0~0.1

_

2-2J1C

4.SOURCE2

5.GATE2 6.DRAIN1

0.65

1.SOURCE1

2.GATE1

3.DRAIN2

2.0±0.2 1.3±0.1

US6

JEDEC

JEITA

TOSHIBA

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N7002FU

High Speed Switching Applications

Analog Switch Applications

- Small package
 - Low ON resistance : $R_{on} = 3.3 \Omega (max) (@V_{GS} = 4.5 V)$
 - : $R_{on} = 3.2 \Omega (max) (@V_{GS} = 5 V)$

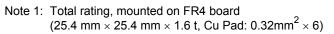
: $R_{on} = 3.0 \ \Omega \ (max) \ (@V_{GS} = 10 \ V)$

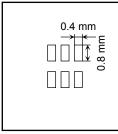
Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

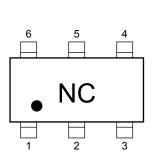
Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V _{DS}	60	V	
Gate-Source voltage		V _{GSS}	± 20	V	
Drain current	DC	۱ _D	200	mA	
	Pulse	I _{DP}	800		
Drain power dissipation (Ta = 25° C)		P _D (Note 1)	300	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the

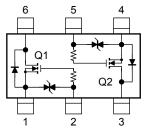
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).







Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production 2002-11

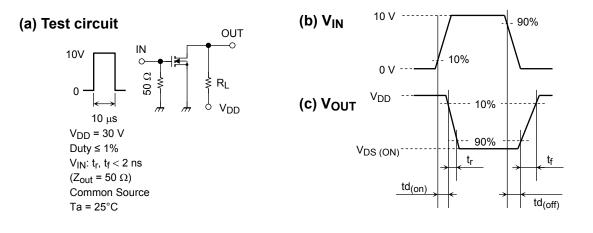
Unit: mm

م

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур	Max	Unit
Gate leakage current		I _{GSS}	V_{GS} = ± 20 V, V_{DS} = 0			± 10	μA
Drain-Source breakdown voltage		V (BR) DSS	I _D = 0.1 mA, V _{GS} = 0	60			V
Drain cut-off current		IDSS	V _{DS} = 60 V, V _{GS} = 0	—		1	μA
Gate threshold vo	Itage	V _{th}	V _{DS} = 10 V, I _D = 0.25 mA	1.0	—	2.5	V
Forward transfer admittance		Y _{fs}	V _{DS} = 10 V, I _D = 200 mA	170	—	_	mS
Drain-Source ON resistance		R _{DS} (ON)	I _D = 500 mA, V _{GS} = 10 V	_	2.0	3.0	Ω
			I _D = 100 mA, V _{GS} = 5 V	_	2.1	3.2	
			I _D = 100 mA, V _{GS} = 4.5 V	_	2.2	3.3	
Input capacitance		C _{iss}	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	_	17		pF
Reverse transfer capacitance		C _{rss}			1.4		pF
Output capacitance		C _{oss}			5.8		pF
Switching time	Turn-on delay time	td _(on)	V _{DD} = 30V, I _D = 200 mA,		2.4	4.0	ns
	Turn-off delay time	td _(off)	$V_{GS} = 0$ to 10V	_	26	40	

Switching Time Test Circuit

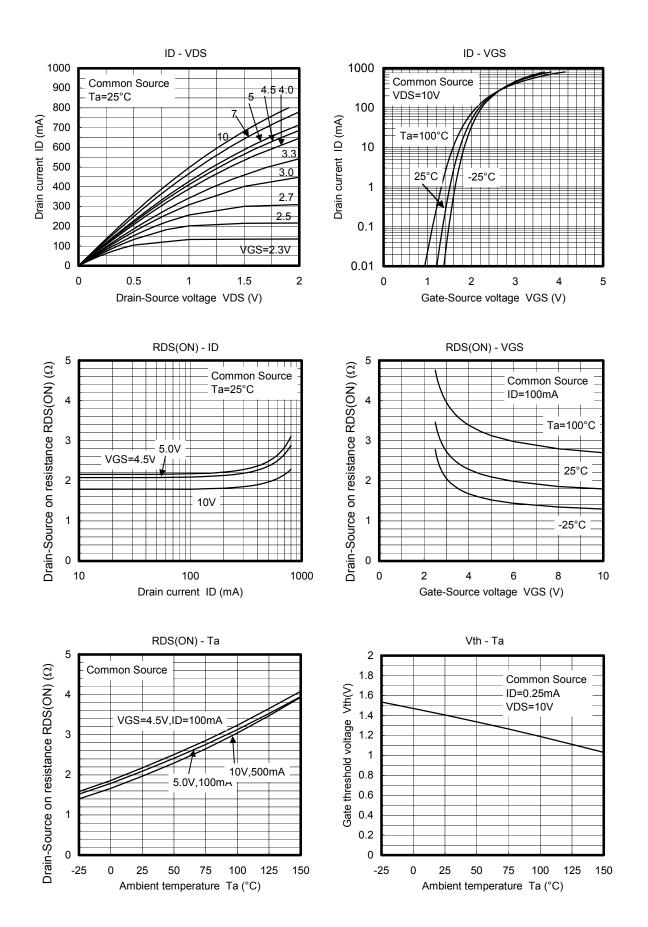


Precaution

 V_{th} can be expressed as voltage between gate and source when low operating current value is I_D =250 μ A for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} . (Relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on))

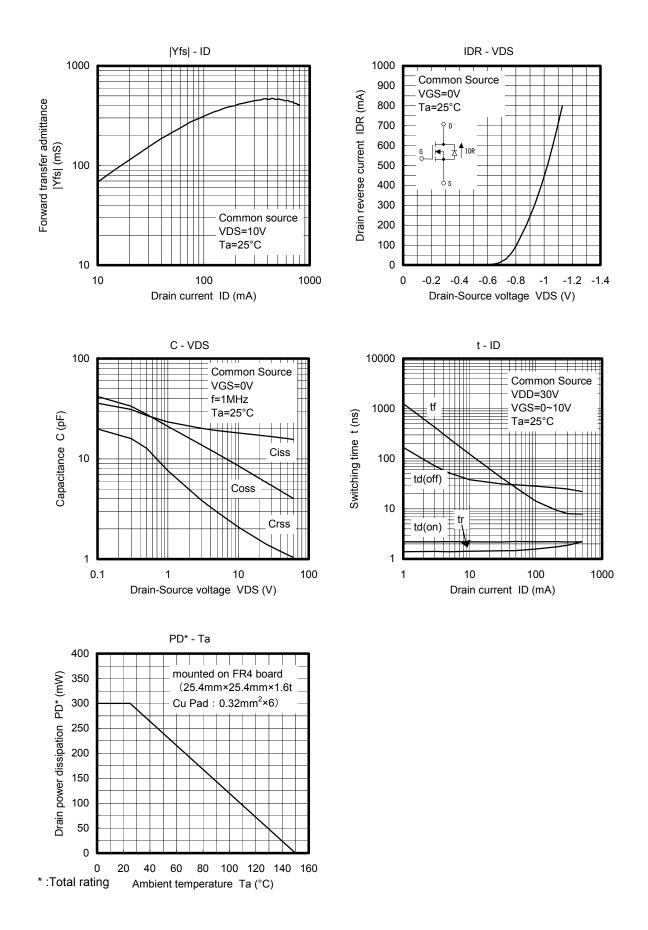
Please take this into consideration for using the device.

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2014-03-01

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