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PRODUCT BULLETIN

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ISSUE DATE: 06-Aug-2014
NOTIFICATION: 16357
TITLE: i.MX 6DualLite/6Solo Errata Document Update
EFFECTIVE DATE: 07-Aug-2014

DEVICE(S)

MPN
MCIMX6S1AVM08AB
MCIMX6S1AVM08ABR
MCIMX6S1AVM08AC
MCIMX6S1AVM08ACR
MCIMX6S1AVM08AD
MCIMX6S4AVM08AB
MCIMX6S4AVM08ABR
MCIMX6S4AVM08AC
MCIMX6S4AVM08ACR
MCIMX6S4AVM08AD
MCIMX6S5DVM10AB
MCIMX6S5DVM10ABR
MCIMX6S5DVM10AC
MCIMX6S5DVM10ACR
MCIMX6S5DVM10AD
MCIMX6S5EVM10AB
MCIMX6S5EVM10ABR
MCIMX6S5EVM10AC
MCIMX6S5EVM10ACR
MCIMX6S5EVM10AD
MCIMX6S6AVM08AB
MCIMX6S6AVM08ABR
MCIMX6S6AVM08AC
MCIMX6S6AVM08ACR
MCIMX6S6AVM08AD
MCIMX6S7CVM08AB

MCIMX6S7CVM08AC
MCIMX6S7CVM08AD
MCIMX6S8DVM10AB
MCIMX6S8DVM10AC
MCIMX6S8DVM10AD
MCIMX6U1AVM08AB
MCIMX6U1AVM08ABR
MCIMX6U1AVM08AC
MCIMX6U1AVM08ACR
MCIMX6U1AVM08AD
MCIMX6U4AVM08AB
MCIMX6U4AVM08ABR
MCIMX6U4AVM08AC
MCIMX6U4AVM08ACR
MCIMX6U4AVM08AD
MCIMX6U5DVM10AB
MCIMX6U5DVM10ABR
MCIMX6U5DVM10AC
MCIMX6U5DVM10ACR
MCIMX6U5DVM10AD
MCIMX6U5EVM10AB
MCIMX6U5EVM10ABR
MCIMX6U5EVM10AC
MCIMX6U5EVM10ACR
MCIMX6U5EVM10AD
MCIMX6U6AVM08AB
MCIMX6U6AVM08ABR
MCIMX6U6AVM08AC
MCIMX6U6AVM08ACR
MCIMX6U6AVM08AD
MCIMX6U7CVM08AB
MCIMX6U7CVM08AC
MCIMX6U7CVM08AD
MCIMX6U8DVM10AB
MCIMX6U8DVM10AC
MCIMX6U8DVM10AD

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AFFECTED CHANGE CATEGORIES

- ERRATA

DESCRIPTION OF CHANGE

The i.MX 6DualLite and i.MX 6Solo silicon errata documentation has been updated to include additional errata that have been identified.

The updated errata documentation is attached and can be found at
http://www.freescale.com/files/32bit/doc/errata/IMX6SDLCE.pdf

Substantive changes in the errata are as follows:
• Deleted the following errata:
– ERR007005: This item was ARM erratum 791420. Access to this information must come directly from ARM.
• Added the following errata:
– ERR007805 “I2C: When the I2C clock speed is configured for 400 kHz, the SCL low period violates the I2C specification"
– ERR008001 “GPMI: GPMI does not support the Set Feature command in Toggle mode”
– ERR008000 “ESAI: ESAI may encounter channel swap when overrun/underrun occurs”
– ERR008057 “MMDC: Skew differences of up to 150 ps observed on SDCLK0, DQS0 and DQS7 differential traces”
– ERR007554 “PCIe: MSI Mask Register Reserved Bits not read-only”
– ERR007926 “ROM: 32 kHz internal oscillator timing inaccuracy may affect SD/MMC, NAND, and OneNAND boot”

Refer to the document revision history for detailed information.

REASON FOR CHANGE

The errata documentation for i.MX 6DualLite and i.MX 6Solo product lines has been updated.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

The errata describe existing conditions identified on current production devices. There are potential hardware and/or software implications to customers.

NOTE:

THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Service Request

For sample inquiries - please go to www.freescale.com

QUAL DATA AVAILABILITY DATE: 25-Jul-2014

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):
External attachment(s) FOR this notification can be viewed AT:
16357_IMX6SDLCE.pdf
