



PRODUCT BULLETIN

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ISSUE DATE: 18-Jun-2014
NOTIFICATION: 16224
TITLE: ERRATA: TBI LINK STATUS / SGMII STAYS UP (REIDL Workaround)
EFFECTIVE DATE: 19-Jun-2014

DEVICE(S)

MPN
BSC9132NSE7KNKB
BSC9132NSE7MNMB
BSC9132NSN7KNKB
BSC9132NSN7MNMB
BSC9132NXE7KNKB
BSC9132NXE7MNMB
BSC9132NXN7KNKB
BSC9132NXN7MNMB
MSC8157ESAG1000A
MSC8157ESVT1000A
MSC8157ETAG1000A
MSC8157ETVT1000A
MSC8157SAG1000A
MSC8157SVT1000A
MSC8157TAG1000A
MSC8157TVT1000A
MSC8157TVT1200A
P2040NSE1FLB
P2040NSE1HLB
P2040NSE1KLB
P2040NSE1MMB
P2040NSE7MMC
P2040NSN1FLB
P2040NSN1HLB
P2040NSN1KLB
P2040NSN1MMB
P2040NSN7FLC

P2040NSN7HLC
P2040NSN7KLC
P2040NSN7MMC
P2040NXE1MMB
P2040NXE7MMC
P2040NXN1FLB
P2040NXN1MMB
P2040NXN7MMC
P2041NSE1MMB
P2041NSE1NNB
P2041NSE1PNB
P2041NSE7MMC
P2041NSE7NNC
P2041NSE7PNAC
P2041NSE7PNC
P2041NSN1MMB
P2041NSN1NNB
P2041NSN1PNB
P2041NSN7MMC
P2041NSN7NNC
P2041NSN7PNAC
P2041NSN7PNC
P2041NXE1MMB
P2041NXE1NNB
P2041NXE1PNB
P2041NXE7MMC
P2041NXE7NNC
P2041NXE7PNC
P2041NXN1MMB
P2041NXN1NNB
P2041NXN1PNB
P2041NXN7MMC
P2041NXN7NNC
P3041NSE1MMB
P3041NSE1NNB
P3041NSE1PNB
P3041NSE7MMC
P3041NSE7NNC
P3041NSE7PNC
P3041NSN1MMB
P3041NSN1NNB

P3041NSN1PNB
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P3041NSN7NNC
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P3041NXE1PNB
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P4040NSN7PNC
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P4040NXN1MMB
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P5010NSE1QMB
P5010NSE1TNB
P5010NSE1VNB
P5010NSE7MMB
P5010NSE7QMB
P5010NSE7TNB
P5010NSE7VNB
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P5010NSN1QMB
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P5010NSN1VNB
P5010NSN7MMB
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P5021NSE7TMC
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P5021NSN12QB
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P5021NSN1VNB
P5021NSN72QC
P5021NSN7TMC
P5021NSN7VNC

P5021NXE7TMC
P5021NXN1TMB
P5021NXN7TMC
P5040NSE12QB
P5040NSE1TMB
P5040NSE1VNB
P5040NSE72QC
P5040NSE7TMC
P5040NSE7VNC
P5040NSN12QB
P5040NSN1TMB
P5040NSN1VNB
P5040NSN72QC
P5040NSN7TMC
P5040NSN7VNC
P5040NXE1TMB
P5040NXE7TMC
P5040NXN1TMB
P5040NXN7TMC
P5040PSE12QA
P5040PSE1TZA
PC8157ESAG1000A
PC8157LAG1000A
PC8157SAG1000A
PC8157TAG1000A
PSC9132PJE7MNMB
PSC9132PLE7MNMB
PSC9132PSE7KNKB
PSC9132PSE7MNMB
PSC9132PXE7KNKB
PSC9132PXE7MNMB

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AFFECTED CHANGE CATEGORIES

- ERRATA

DESCRIPTION OF CHANGE

PLEASE REFER TO DEVICE ERRATUM A-007207 FOR EXACT REGISTER OFFSETS

AND AFFECTED SILICON VERSIONS

The TBI Status Register (SR) contains a link status bit (TBI SR [Link Status]) that represents the current state of the SGMII link. If Auto-Negotiation (AN) is disabled, the TBI link status bit should become a b'1 indicating the link is up after recognizing IDLE sequences, and stay at b'1 as long as valid data is received & the TBI is not reset. TBI link status bit should become a b'0 indicating the link is down after several invalid characters are received or the TBI is reset. If AN is enabled, the TBI link status bit does not become set to b'1 until auto-negotiation is complete (TBI CR [AN DONE]=1), but the same conditions as AN disabled then apply for the TBI link status bit to get cleared to b'0.

An electrical idle (common mode) condition on the SGMII link results in the reception of invalid data, and should cause the TBI link status bit to get cleared. If the transition from active to common mode takes enough time that the Rx is able to recognize at least 4 more K28.5 characters (for IDLE sequences, 70-80 UI), the portion of the design intended to detect the link down condition may shut off before the link down condition is actually reflected in the TBI.

This premature shutdown may cause the TBI link status to remain set to a b'1 indicating the link is up. This 'stuck at 1' condition would persist until valid K28.5 characters are received again.

WORKAROUND:

For affected systems, in addition to examining the TBI link status, examining the SerDes electrical idle state is also necessary. The link is actually down if either the TBI link status is cleared or the SerDes lane receive electrical idle detected. Code modification may be required.

Example pseudo-code:

```
if (SRDS1_B2GCRD1[REIDL] == b'1)
  OR
  (TBI SR[LINK STATUS] == b'0)
{
  LINK is DOWN
}
```

On P2041/P2040/P3041, P5020, P4080, and P5040, SerDes electrical idle detected is BnGCRm1[REIDL]=1 for bank n, lane m.

On P1023 and 8157, SerDes electrical idle detected is LmGCR1[REIDL]=1 for lane m.

On BSC9132, SerDes electrical idle detected is SERDES_LnGCR1[REIDL] for lane n.

REASON FOR CHANGE

If the customer system never enters SGMII electrical idle, or if the transition from active to common mode takes less than 40 UI (~32ns), then there is no impact – the false link up scenario will not occur.

If the customer system can generate an SGMII electrical idle condition as described above, then the TBI status may stay stuck at 1 while the link is down, and would not transition to 0 until valid K28.5 characters are received again.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

NO IMPACT WITH WORKAROUND IMPLEMENTED

NOTE:

THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a [Service Request](#)

For sample inquiries - please go to www.freescale.com

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):

External attachment(s) FOR this notification can be viewed AT:

[16224_SGMII_False_Link_Up_PB16224_1.pdf](#)

[16224_SGMII_False_Link_Up_PB16224_3.pdf](#)

[16224_SGMII_False_Link_Up_PB16224_2.pdf](#)
