**Product data sheet** 

# 1. General description

Planar passivated SCR with sensitive gate in a SOT223 (SC-73) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

### 2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

# 3. Applications

- Adapters
- · Battery powered applications
- Industrial automation

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DRM}$	repetitive peak off- state voltage		[1]	-	-	600	V
$V_{RRM}$	repetitive peak reverse voltage			-	-	600	V
I <sub>TSM</sub>	non-repetitive peak on- state current	half sine wave; $T_{j(init)} = 25 ^{\circ}C$ ; $t_p = 10  \text{ms}$ ; Fig. 4; Fig. 5		-	-	10	Α
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>sp</sub> ≤ 112 °C; <u>Fig. 1</u>		-	-	0.6	A
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_{sp} \le 112 ^{\circ}\text{C}$ ; Fig. 2; Fig. 3		-	-	1	A
Static char	acteristics						
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 9$		-	50	200	μA

<sup>[1]</sup> Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.





SCR

# 5. Pinning information

## Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	4	A <del>D</del> K
2	Α	anode		G sym037
3	G	gate		
4	mb	mb; connected to anode	☐1 ☐2 ☐3 SC-73 (SOT223)	

# 6. Ordering information

### Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT148W-600R	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

# 7. Marking

### Table 4. Marking codes

Type number	Marking code
BT148W-600R	BT148W 60

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		[1]	-	600	V
$V_{RRM}$	repetitive peak reverse voltage			-	600	V
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>sp</sub> ≤ 112 °C; <u>Fig. 1</u>		-	0.6	Α
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_{sp} \le 112 \text{ °C}$ ; Fig. 2; Fig. 3		-	1	А
I <sub>TSM</sub>	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; <u>Fig. 4</u> ; <u>Fig. 5</u>		-	10	A
		half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms		-	11	A
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN		-	0.5	A <sup>2</sup> s
dI <sub>T</sub> /dt	rate of rise of on-state current	$I_T = 4 \text{ A}$ ; $I_G = 0.2 \text{ A}$ ; $dI_G/dt = 0.2 \text{ A/}\mu\text{s}$		-	50	A/µs
I <sub>GM</sub>	peak gate current			-	1	Α
$V_{RGM}$	peak reverse gate voltage			-	5	V
$P_GM$	peak gate power			-	1.2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.12	W
T <sub>stg</sub>	storage temperature			-40	150	°C
Tj	junction temperature		[2]	-	125	°C

<sup>[1]</sup> Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.

<sup>[2]</sup> Operation above 110°C may require the use of a gate to cathode resistor of  $1k\Omega$  or less.

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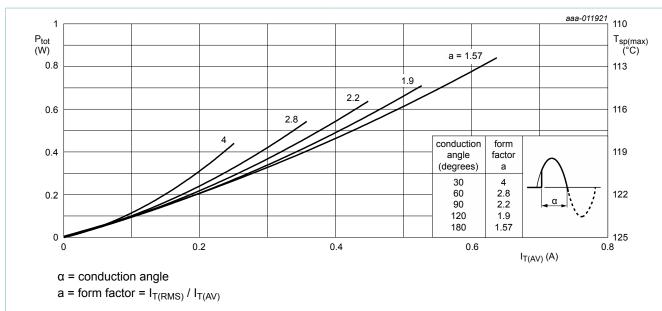


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

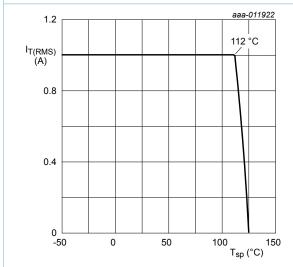
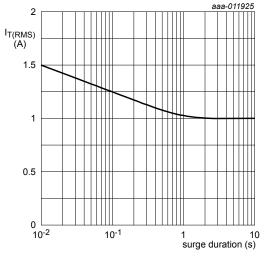


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz;  $T_{sp}$  = 112 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values

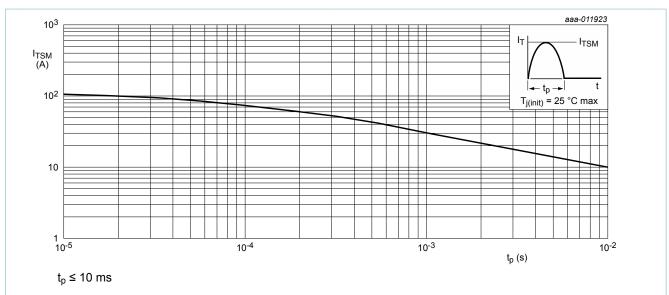


Fig. 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

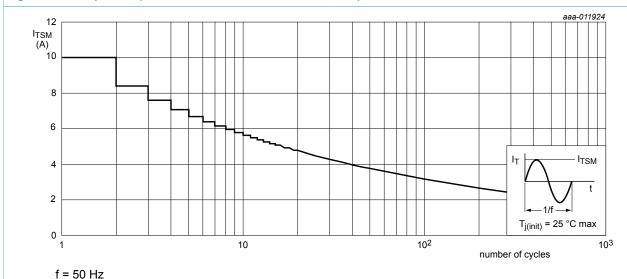


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

SCR

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point	Fig. 6	-	-	15	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	printed circuit board mounted; pad area; Fig. 7	-	70	-	K/W
		printed circuit board mounted; minimum footprint; Fig. 8	-	156	-	K/W

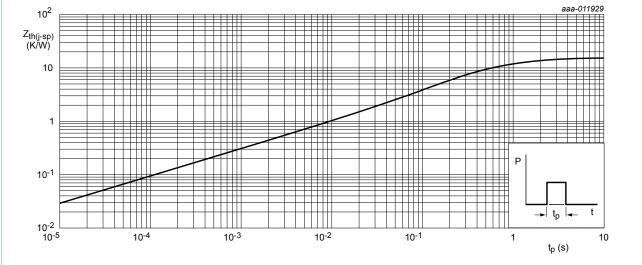
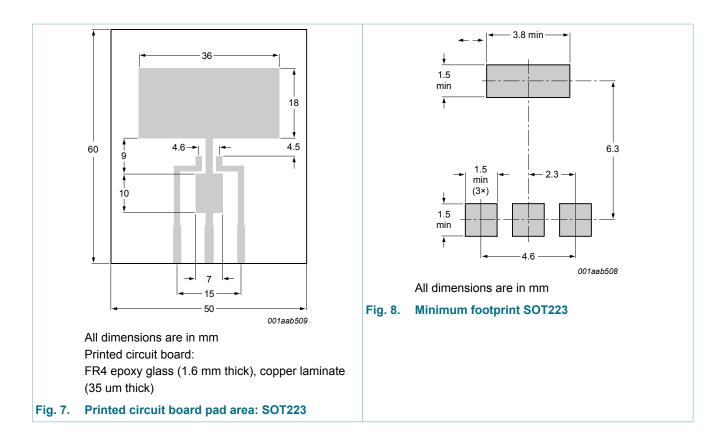


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

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SCR

# 10. Characteristics

### Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	50	200	μA
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 10	-	0.17	10	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	0.1	6	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 2 A; T <sub>j</sub> = 25 °C; <u>Fig. 12</u>	-	1.3	1.5	V
$V_{\text{GT}}$	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 13	-	0.4	1	V
		$V_D = 600 \text{ V}; I_T = 0.1 \text{ A}; T_j = 125 \text{ °C};$ Fig. 13	0.1	0.2	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
I <sub>R</sub>	reverse current	V <sub>R</sub> = 600 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
Dynamic cl	haracteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 125 °C; $R_{GK}$ = 100 Ω; $(V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; Fig. 14	-	50	-	V/µs
t <sub>gt</sub>	gate-controlled turn-on time	$I_{TM}$ = 4 A; $V_D$ = 600 V; $I_G$ = 5 mA; $dI_G/$ dt = 0.2 A/µs; $T_j$ = 25 °C	-	2	-	μs
t <sub>q</sub>	commutated turn-off time	$\begin{split} &V_{DM} = 402 \text{ V; } T_j = 125 \text{ °C; } I_{TM} = 4 \text{ A;} \\ &V_R = 35 \text{ V; } (dI_T/dt)_M = 30 \text{ A/µs; } dV_D/\\ &dt = 2 \text{ V/µs; } R_{GK} = 1 \text{ k}\Omega; \text{ ($V_{DM}$ = 67\% of $V_{DRM}$)} \end{split}$	-	100	-	μs

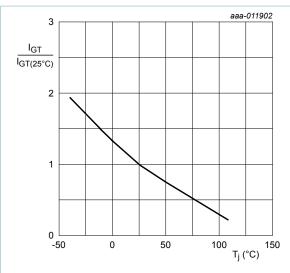


Fig. 9. Normalized gate trigger current as a function of junction temperature

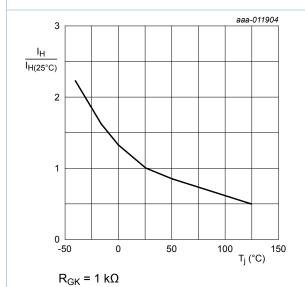
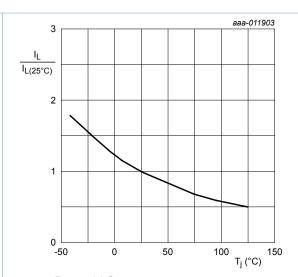
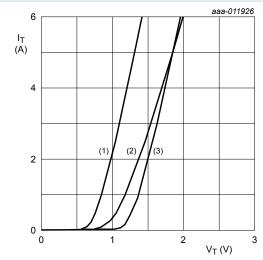


Fig. 11. Normalized holding current as a function of junction temperature



 $R_{GK} = 1 k\Omega$ 

Fig. 10. Normalized latching current as a function of junction temperature



 $V_o = 1.107 \text{ V}; R_s = 0.14 \Omega$ 

(1) T<sub>j</sub> = 125 °C; typical values

(2) T<sub>i</sub> = 125 °C; maximum values

(3) T<sub>i</sub> = 25 °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

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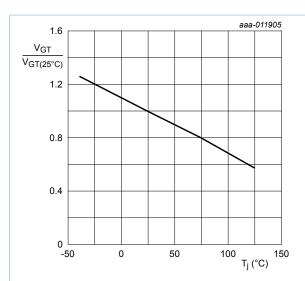


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

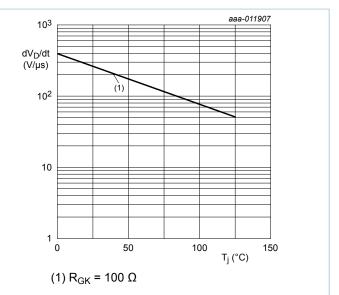
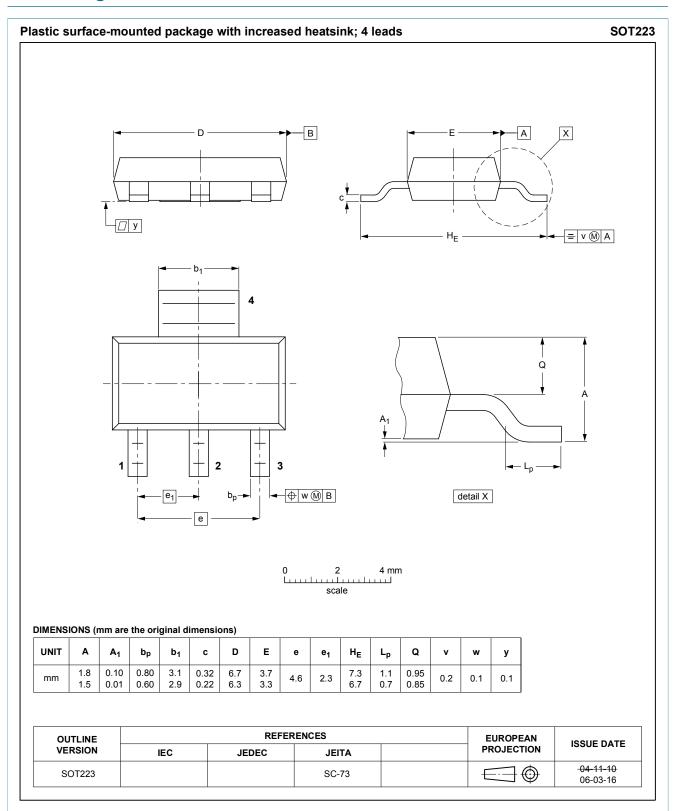


Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

# 11. Package outline



## 12. Legal information

#### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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## 13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	3
9	Thermal characteristics	6
10	Characteristics	8
11	Package outline	11
12	Legal information	12
12.1	Data sheet status	12
12.2	Definitions	12
12.3	Disclaimers	12
12.4	Trademarks	13

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