MIC4606

85V Full-Bridge MOSFET Drivers with Adaptive Dead Time and Shoot-Through Protection

General Description

The MIC4606 is an 85V full-bridge MOSFET driver that features adaptive dead time and shoot-through protection. The adaptive dead time circuitry actively monitors both sides of the full-bridge to minimize the time between high-side and low-side MOSFET transitions, thus maximizing power efficiency. Antishoot-through circuitry prevents erroneous inputs and noise from turning both MOSFETs of each side of the bridge on at the same time.

The MIC4606 also offers a wide 5.5V to 16V operating supply range to maximize system efficiency. The low 5.5V operating voltage allows longer run times in battery-powered applications. Additionally, the MIC4606's adjustable gate drive sets the gate drive voltage to V_{DD} for optimal MOSFET $R_{DS(ON)}$, which minimizes power loss due to the MOSFET's $R_{DS(ON)}$.

The MC4606-1 features four independent inputs while the MIC4606-2 utilizes two PWM inputs, one for each side of the H-bridge. The MIC4606-1 and MIC4606-2 are available in a 16 pin 4 x 4 QFN package with an operating temperature range of -40°C to 125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

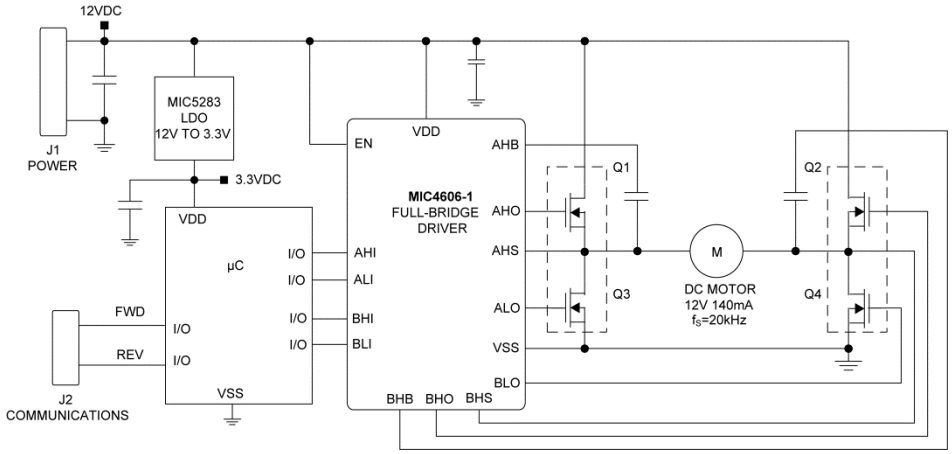
Features

- 5.5V to 16V gate drive supply voltage range
- Advanced adaptive dead time
- Intelligent shoot-through protection
  - MIC4606-1: 4 Independent TTL inputs
  - MIC4606-2: 2 PWM inputs
- Enable input for on/off control
- On-chip bootstrap diodes
- Fast 35ns propagation times
- Drives 1000pF load with 20ns rise and fall times
- Low power consumption: 235µA total quiescent current
- Separate high- and low-side undervoltage protection
- –40°C to +125°C junction temperature range

Applications

- Full-bridge motor drives
- Power inverters
- High Voltage step-down regulators
- Distributed power systems
- Stepper motors

Typical Application



85V Motor Drive Configuration

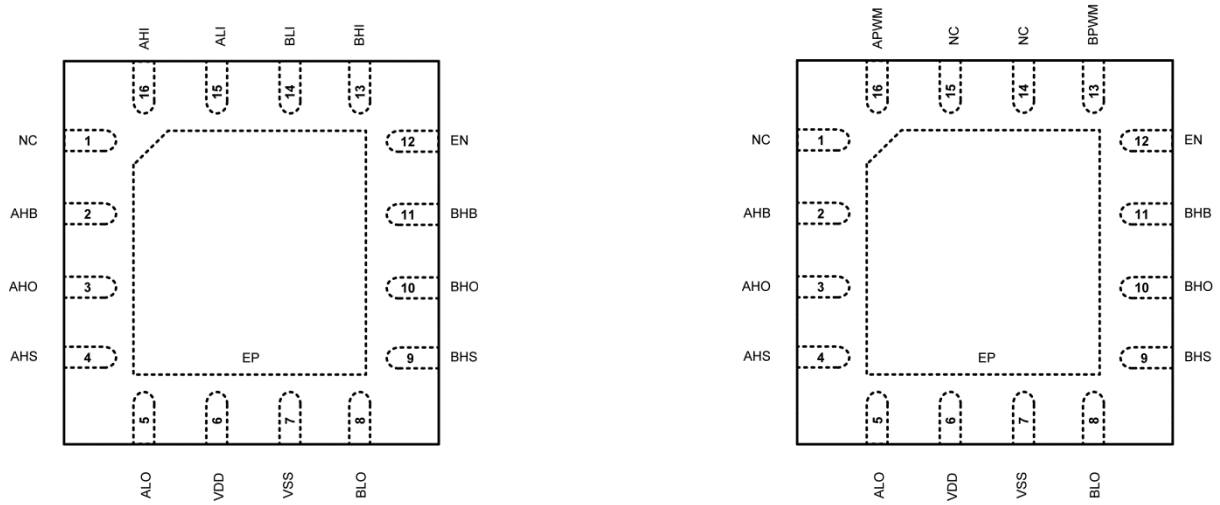
Ordering Information

Part Number	Input	Version	Junction Temperature Range	Package[1]
MIC4606-1YML	TTL	Dual Inputs	–40° to +125°C	16-Pin 4x4 QFN
MIC4606-2YML	TTL	Single PWM Inputs	–40° to +125°C	16-Pin 4x4 QFN

Note:

1. QFN is a GREEN, RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



MIC4606-1 **MIC4606-2**

16-Pin 4mm x 4mm QFN (ML)
(Top View)

Pin Description

Pin Number	MIC4606-1 Pin Name	MIC4606-2 Pin Name	Pin Name
1	NC	NC	No connect.
2	AHB	AHB	Phase A high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and AHS. An on-chip bootstrap diode is connected from VDD to AHB.
3	AHO	AHO	Phase A high-side drive output. Connect to the external high-side power MOSFET gate.
4	AHS	AHS	Phase A high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and AHB.
5	ALO	ALO	Phase A low-side drive output. Connect to the external low-side power MOSFET gate.
6	VDD	VDD	Input supply for gate drivers. Decouple this pin to VSS with a >1.0µF capacitor.
7	VSS	VSS	Driver reference supply input. Connect to the power ground of the external circuitry.
8	BLO	BLO	Phase B low-side drive output. Connect to the external low-side power MOSFET gate.
9	BHS	BHS	Phase B high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and BHB.
10	BHO	BHO	Phase B high-side drive output. Connect to the external high-side power MOSFET gate.
11	BHB	BHB	Phase B high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and BHS. An on-chip bootstrap diode is connected from VDD to BHB.
12	EN	EN	Enable input. A logic high on the enable pin results in normal operation. A logic low disables all outputs and places the driver into a low current shutdown mode. Do not leave this pin floating.
13	BHI	—	Phase B high-side drive input.
13	—	BPWM	Phase B PWM input for single input signal drive.
14	BLI	—	Phase B low-side drive input.
14	—	NC	No connect.
15	ALI	—	Phase A low-side drive input.
15	—	NC	No connect.
16	AHI	—	Phase A high-side drive input.
16	—	APWM	Phase A PWM input for single input signal drive.
EP	ePad	ePad	Exposed thermal pad. Connect to VSS. A connection to the ground plane is necessary for optimum thermal performance.

Absolute Maximum Ratings[2][6]

Supply Voltage (V_{DD}, V_{xHB} – V_{xHS}) ..... –0.3V to 18V
Input Voltages (V_{xLI}, V_{xHI}, V_{EN}) ..... –0.3V to V_{DD} + 0.3V
Voltage on xLO (V_{xLO}) ..... –0.3V to V_{DD} + 0.3V
Voltage on xHO (V_{xHO}) ..... V_{HS} – 0.3V to V_{HB} + 0.3V
Voltage on xHS (continuous) ..... –1V to 90V
Voltage on xHB 108V
Average Current in VDD to HB Diode 100mA
Storage Temperature (T_s) ..... –60°C to +150°C
ESD Rating[4]
HBM 1kV
MM 200V

Operating Ratings[3]

Supply Voltage (V_{DD}) [decreasing V_{DD}] ..... 5.25V to 16V
Supply Voltage (V_{DD}) [increasing V_{DD}] ..... 5.5V to 16V
Enable Voltage (V_{EN}) ..... 0V to V_{DD}
Voltage on xHS ..... –1V to 85V
Voltage on xHS (100ns repetitive transient) ..... –5V to 90V
HS Slew Rate 50V/ns
Voltage on xHB ..... V_{HS} + V_{DD}
and/or ..... V_{DD} - 1V to V_{DD} +85V
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
4mm x 4mm QFN-16-pin (θ_{JA}) ..... 51°C/W

Electrical Characteristics[5][6]

V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{xHS} = 0V; No load on xLO or xHO; T_A = 25°C, unless noted.
Bold values indicate –40°C≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	V_{DD} Quiescent Current	xLI = xHI = 0V		200	**350**	µA
I_{DDSH}	V_{DD} Shutdown Current	EN = 0V with xHS = floating;		2.5	**5**	µA
		EN = 0V, xLI, xHI = 12V or 0V		40	**100**	
I_{DDO}	V_{DD} Operating Current	f_S = 20kHz		0.35	**0.5**	mA
I_{HB}	Total xHB Quiescent Current	xLI = xHI = 0V or xLI = 0V and xHI =5V		35	**75**	µA
I_{HBO}	Total xHB Operating Current	f_S = 20kHz		30	**400**	µA
I_{HBS}	xHB to V_{SS} Quiescent Current	V_{xHS} = V_{xHB} = 90V		0. 5	5	µA
I_{HBSO}	xHB to V_{SS} Operating Current	f_S = 20kHz		3	**10**	µA
Input (TTL: xLI, xHI, EN) [6]						
V_{IL}	Low-Level Input Voltage				**0.8**	V
V_{IH}	High-Level Input Voltage		**2.2**			V
V_{HYS}	Input Voltage Hysteresis			0.1		V
R_I	Input Pull-Down Resistance	xHI/xLI inputs	**100**	300	**500**	kΩ
		xPWM inputs	**50**	150	**250**	kΩ
Under-Voltage Protection						
V_{DDR}	V_{DD} Falling Threshold		**4.0**	4.4	**4.9**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.25		V
V_{HBR}	xHB Falling Threshold		**4.0**	4.4	**4.9**	V
V_{HBH}	xHB Threshold Hysteresis			0.25		V

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.
4. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only
6. x in front of a pin name refers to either A or B. (e.g. xHI can be either AHI or BHI).
7. $V_{IL\ (MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH\ (MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

Electrical Characteristics[5][6] (Continued)

V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{xHS} = 0V; No load on xLO or xHO; T_A = 25°C, unless noted.

Bold values indicate –40°C≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Bootstrap Diode						
V_{DL}	Low-Current Forward Voltage	$I_{VDD-xHB}$ = 100µA		0.4	**0.70**	V
V_{DH}	High-Current Forward Voltage	$I_{VDD-xHB}$ = 50mA		0.7	**1.0**	V
R_D	Dynamic Resistance	$I_{VDD-xHB}$ = 50mA		3	**5.0**	Ω
LO Gate Driver						
V_{OLL}	Low-Level Output Voltage	I_{xLO} = 50mA		0.3	**0.6**	V
V_{OHL}	High-Level Output Voltage	I_{xLO} = –50mA, V_{OHL} = V_{DD} - V_{xLO}		0.5	**1.0**	V
I_{OHL}	Peak Sink Current	V_{xLO} = 0V		1		A
I_{OLL}	Peak Source Current	V_{xLO} = 12V		1		A
HO Gate Driver						
V_{OLH}	Low-Level Output Voltage	I_{xHO} = 50mA		0.3	**0.6**	V
V_{OHH}	High-Level Output Voltage	I_{xHO} = –50mA, V_{OHH} = V_{xHB} – V_{xHO}		0.5	**1.0**	V
I_{OHH}	Peak Sink Current	V_{xHO} = 0V		1		A
I_{OLH}	Peak Source Current	V_{xHO} = 12V		1		A
Switching Specifications[8]						
t_{LPHL}	Lower Turn-Off Propagation Delay (xLI Falling to xLO Falling)			35	**75**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (xHI Falling to xHO Falling)			35	**75**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (xLI Rising to xLO Rising)			35	**75**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (xHI Rising to xHO Rising)			35	**75**	ns
t_R/t_F	Output Rise/Fall Time	C_L = 1000pF		20		ns
t_R/t_F	Output Rise/Fall Time (3V to 9V)	C_L = 0.1µF		0.8		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns

Note:

8. xLI/xHI mode with inputs non-overlapping, assumes xHS low before xLI goes high and xLO low before xHI goes high).

Electrical Characteristics[5][6] (Continued)

V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C, unless noted.

Bold values indicate –40°C≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Switching Specifications						
t_{LOOFF}	Delay from xPWM High (or xLI Low) to xLO Low			35	**75**	ns
V_{LOOFF}	xLO Output Voltage Threshold for Low-Side FET to be Considered Off			1.9		V
t_{HOON}	Delay from xLO off to xHO High			35	**75**	ns
t_{HOOFF}	Delay from xPWM Low (or xHI Low) to xHO Low			35	**75**	ns
V_{SWTH}	Switch Node Voltage Threshold Signaling xHO is Off		**1**	2.2	**4**	V
t_{LOON}	Delay Between xHO FET neing Considered Off to xLO Turning On			35	**75**	ns
t_{LOONHI}	For xHS Low/xLI High, Delay from xPWM/xHI Low to xLO High			80	**150**	ns
t_{SWTO}	Force xLO On if V_{SWTH} is Not Detected		**100**	250	**500**	ns

Note:

9. PWM mode (MIC4606-2) or LI/HI mode (MIC4606-1) with overlapping xLI/xHI inputs.

Timing Diagrams

Non-Overlapping LI/HI Input Mode (MIC4606-1)

In LI/HI input mode, external xLI/xHI inputs are delayed to the point that xHS is low before xLI is pulled high and similarly xLO is low before xHI goes high

xHO goes high with a high signal on xHI after a typical delay of 35ns (t_{HPLH}). xHI going low drives xHO low also with typical delay of 35ns (t_{HPHL}).

Likewise, xLI going high forces xLO high after typical delay of 35ns (t_{LPLH}) and xLO follows low transition of xLI after typical delay of 35ns (t_{LPHL}).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20ns driving 1000pF capacitive loads.

All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

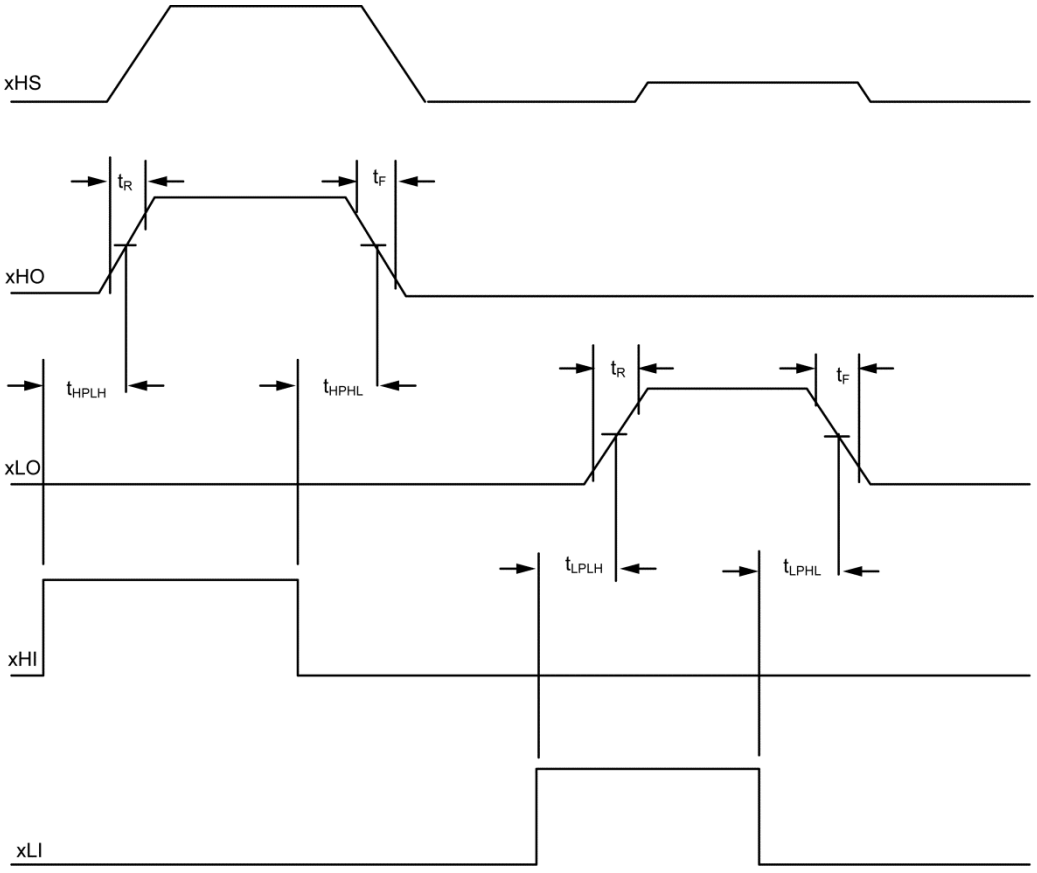


Figure 1. Separate Non-Overlapping LI/HI Input Mode (MIC4606-1)

Timing Diagrams (Continued)

Overlapping LI/HI Input Mode (MIC4606-1)

When xLI/xHI input high conditions overlap, xLO/xHO output states are dominated by the first output to be turned on. That is, if xLI goes high (on), while xHO is high, xHO stays high until xHI goes low at which point, after a delay of t_{HOOFF} and when xHS < 2.2V, xLO goes high with a delay of t_{LOON}. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xHI edge delayed by a typical 250ns will set “HS latch” allowing xLO to go high.

If xHS falls very fast, xLO will be held low by a 35ns delay gated by HI going low. Conversely, xHI going high (on) when xLO is high has no effect on outputs until xLI is pulled low (off) and xLO falls to < 1.9V. Delay from xLI going low to xLO falling is t_{LOOFF} and delay from xLO < 1.9V to xHO being on is t_{HOON}.

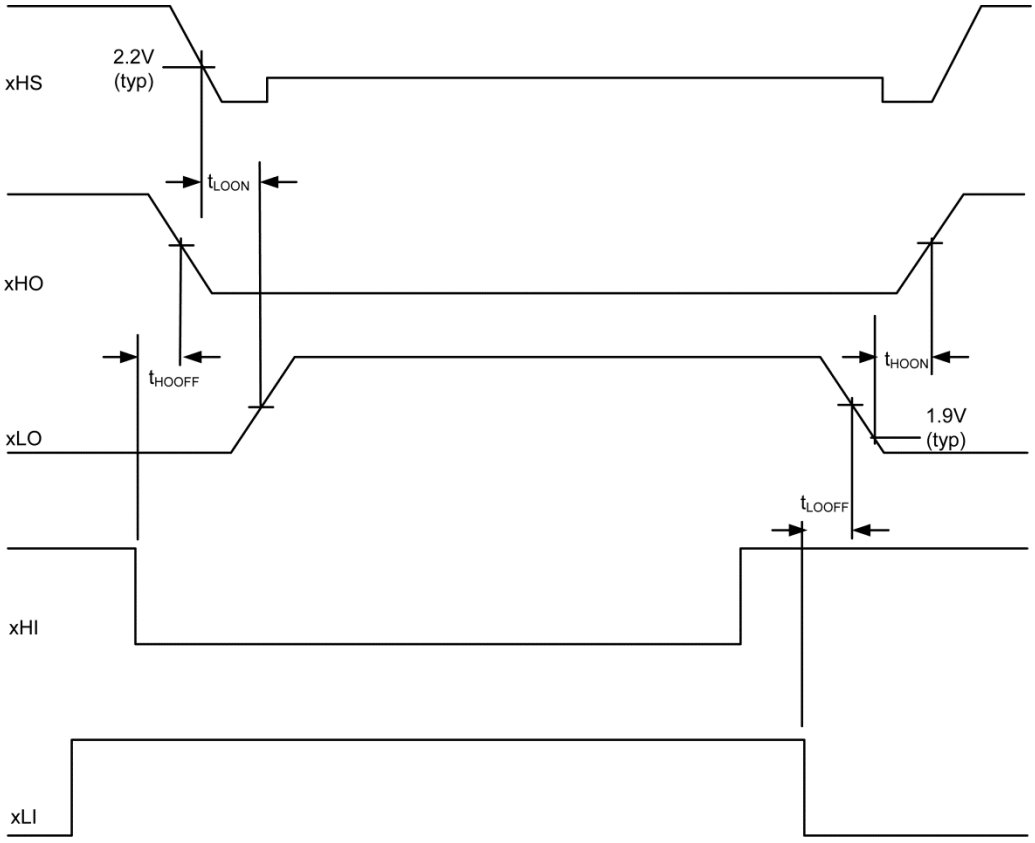


Figure 2. Separate Overlapping LI/HI Input Mode (MIC4606-1)

Timing Diagrams (Continued)

PWM Input Mode (MIC4606-2)

A low going xPWM signal applied to the MIC4606-2 causes xHO to go low, typically 35ns (t_{HOOFF}) after the xPWM input goes low, at which point the switch node, xHS, falls (1 – 2).

When xHS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and xLO goes high, typically within 35ns (t_{LOON}) (3-4). xHS falling below 2.2V sets a latch that can only be reset by xPWM going high. This design prevents ringing on xHS from causing an indeterminate xLO state. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xPWM edge delayed by 250ns will set “HS latch” allowing xLO to go high. An 80ns delay gated by xPWM going low may determine the time to xLO going high for fast falling HS designs. xPWM going high forces xLO low in typically 35ns (t_{LOOFF}) (5– 6).

When xLO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and xHO is allowed to go high. The delay between these two points is typically 35ns (t_{HOON}) (7 – 8).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20ns driving 1000pF capacitive loads.

Note: All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

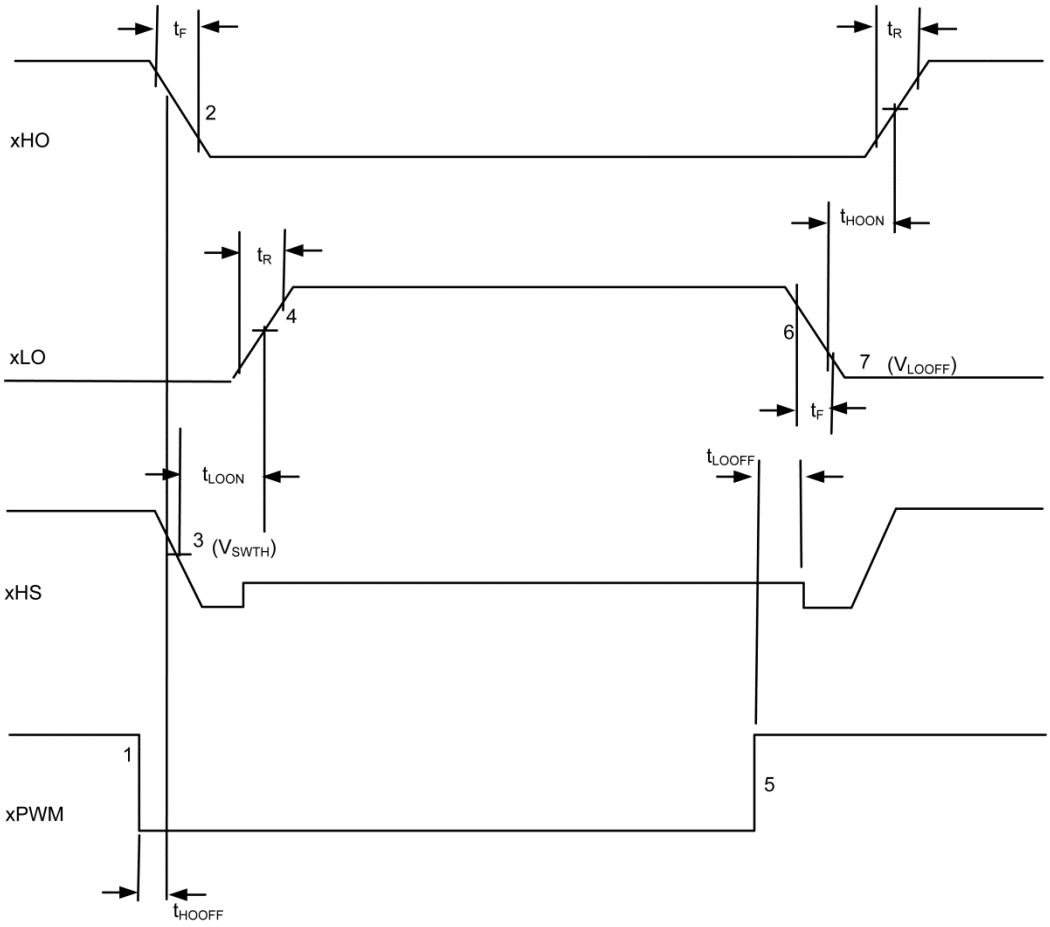
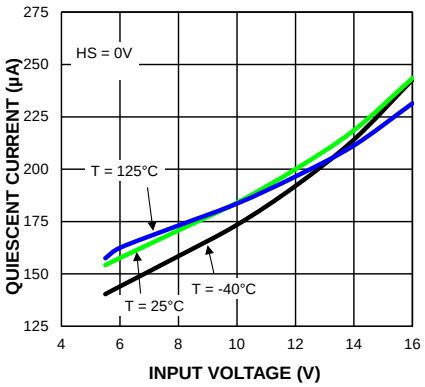


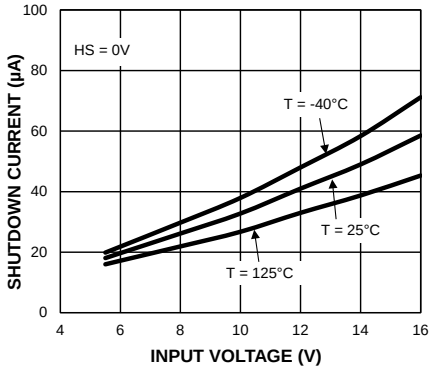
Figure 3. PWM Mode (MIC4606-2)

Typical Characteristics

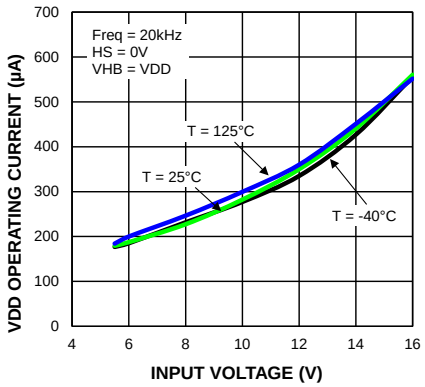
VDD Quiescent Current vs. Input Voltage



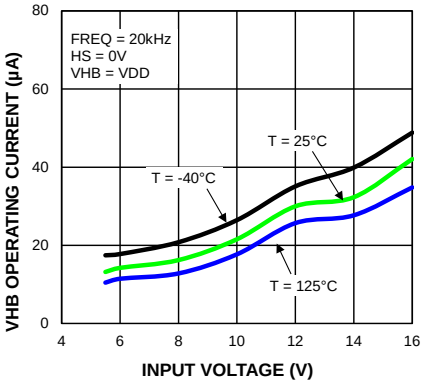
Shutdown Current vs. Input Voltage



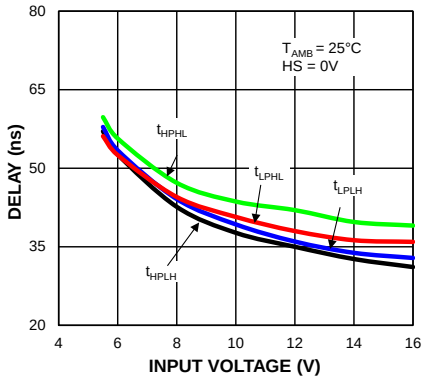
VDD Operating Current vs. Input Voltage



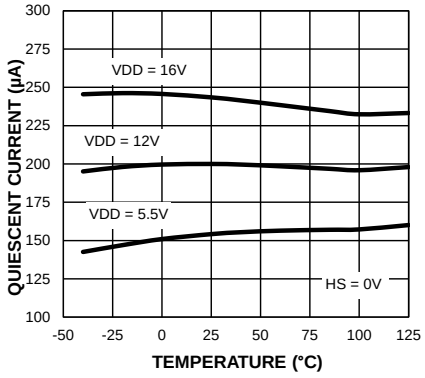
VHB Operating Current vs. Input Voltage



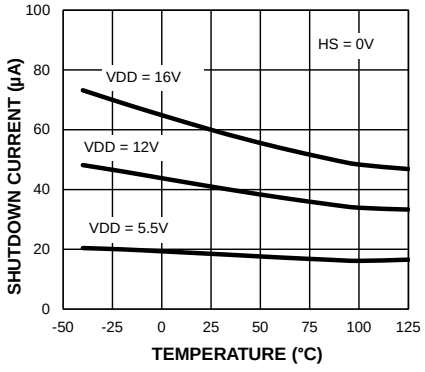
Propagation Delay vs. Input Voltage



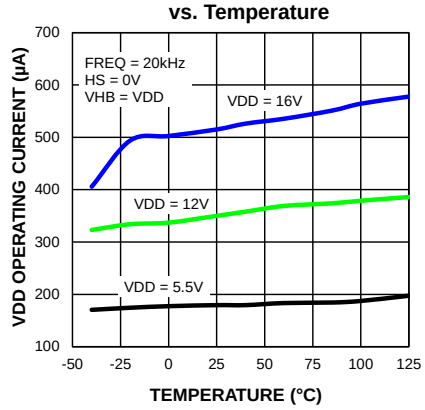
VDD Quiescent Current vs. Temperature



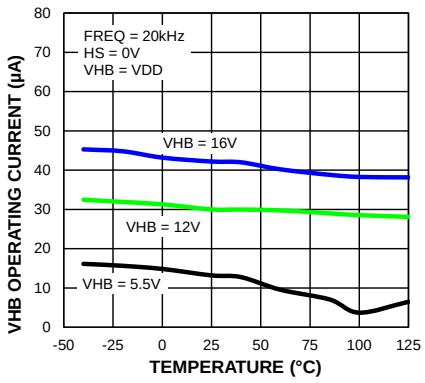
Shutdown Current vs. Temperature



VDD Operating Current vs. Temperature

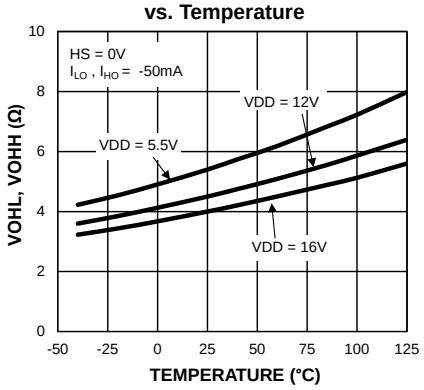


VHB Operating Current vs. Temperature

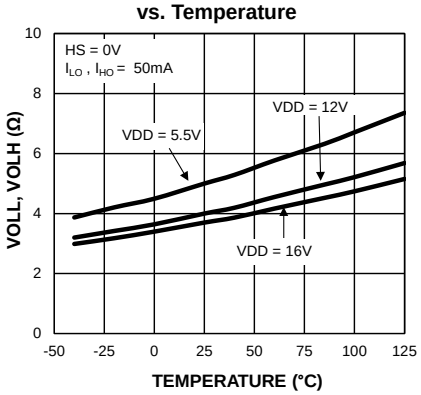


Typical Characteristics (Continued)

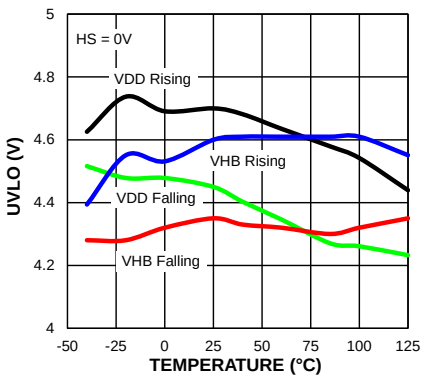
High Level Output Resistance vs. Temperature



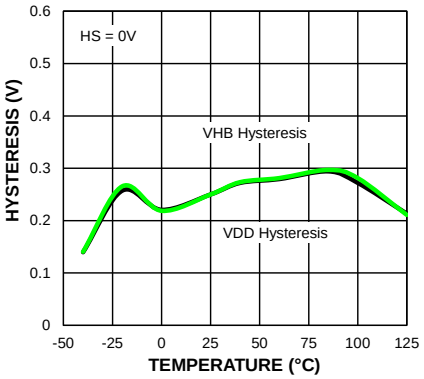
Low Level Output Resistance vs. Temperature



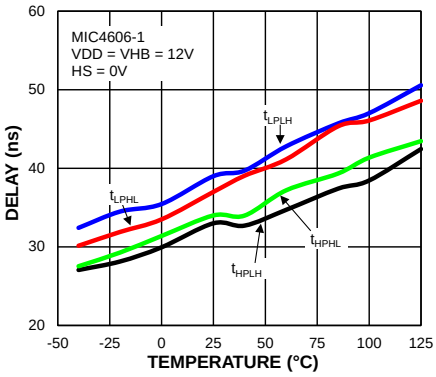
UVLO Thresholds vs. Temperature



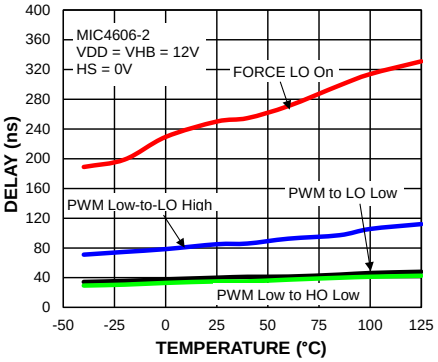
UVLO Hysteresis vs. Temperature



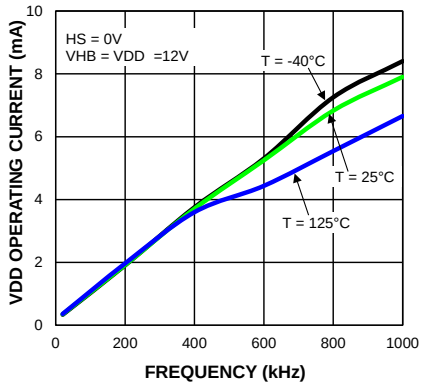
Propagation Delay vs. Temperature



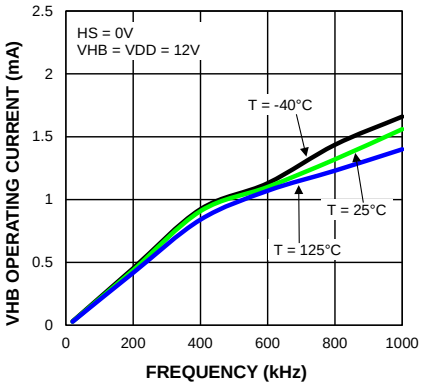
Propagation Delay (PWM) vs. Temperature



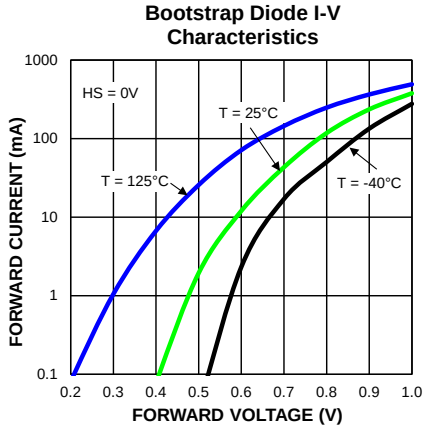
VDD Operating Current vs. Frequency

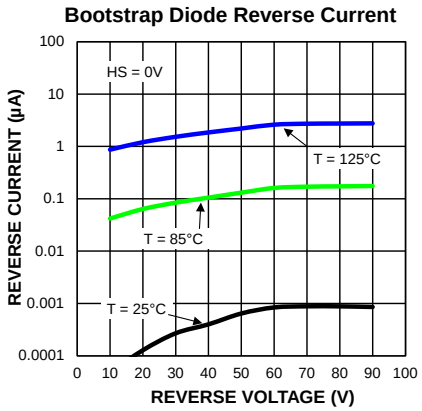


VHB Operating Current vs. Frequency



Typical Characteristics (Continued)





Functional Diagram

For xHO to be high, the xHI must be high and the xLO must be low. xHO going high is delayed by xLO falling below 1.9V. The xHI and xLI inputs must not rise at the same time to prevent a glitch from occurring on the output. A minimum 50ns delay between both inputs is recommended.

xLO is turned off very quickly on the xLI falling edge. xLO going high is delayed by the longer of 35ns delay of xHO control signal going “off” or the RS latch being set.

The latch is set by the quicker of either the falling edge of xHS or xLI gated delay of 250ns. The latch is present to lockout xLO bounce due to ringing on xHS. If xHS never adequately falls due to the absence of or the presence of a very weak external pull-down on xHS, the gated delay of 250ns at xLI will set the latch allowing xLO to transition high. This in turn allows the xLI startup pulse to charge the bootstrap capacitor if the load inductor current is very low and xHS is uncontrolled. The latch is reset by the xLI falling edge.

There is one external enable pin that controls both phases.

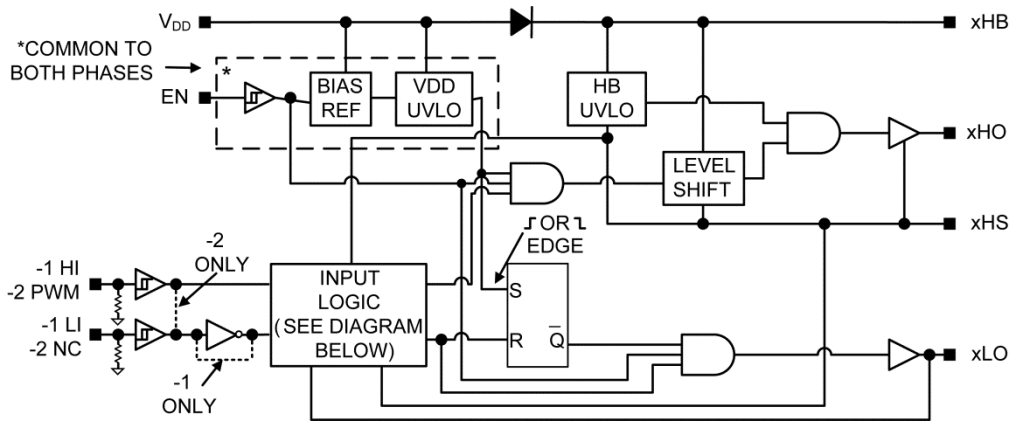


Figure 4. MIC4606 xPhase Top Level Block Diagram

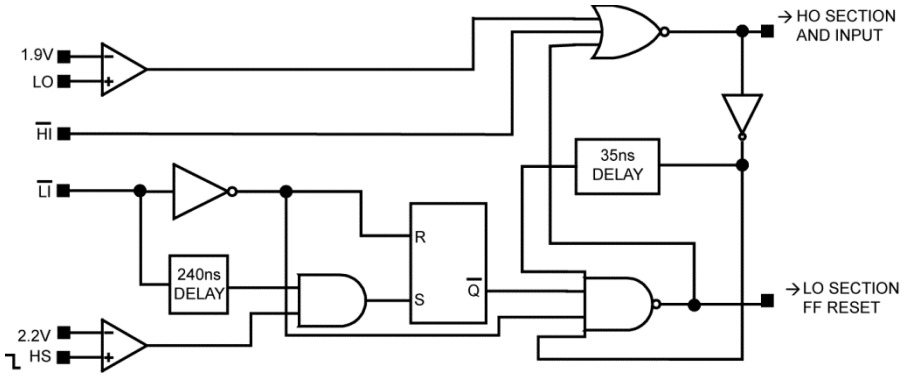


Figure 5. Input Logic Block in Figure 4.

Functional Description

The MIC4606 is a non-inverting, 85V full-bridge MOSFET driver designed to independently drive all four N-Channel MOSFETs in the bridge. The MIC4606 offers a wide 5.5V to 16V operating supply range with either four independent TTL inputs (MIC4606-1) or two PWM inputs, one for each phase (MIC4606-2). Refer to Figure 4.

The drivers contain input buffers with hysteresis, three independent UVLO circuits (two high side and one low side), and four output drivers. The high-side output drivers utilize a high-speed level-shifting circuit that is referenced to its HS pin. Each phase has an internal diode that is used by the bootstrap circuits to provide the drive voltages for each of the two high-side outputs.

Startup and UVLO

The UVLO circuits force the driver's outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuits monitor the voltage between the xHB and xHS pins. Hysteresis in the UVLO circuits prevent noise and finite circuit impedance from causing chatter during turn-on.

Enable Inputs

There is one external enable pin that controls both phases. A logic high on the enable pin (EN) allows for startup of both phases and normal operation. Conversely, when a logic low is applied on the enable pin, both phases turn-off and the device enters a low current shutdown mode. All outputs (xHO and xLO) are pulled low when EN is low. Do not leave the EN pin floating.

Input Stage

All input pins (xLI and xHI) are referenced to the VSS pin. The MIC4606 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the VDD supply voltage and there is no dependence between I_{VDD} and the input signal amplitude. This feature makes the MIC4606 an excellent level translator that will drive high level gate threshold MOSFETs from a low-voltage PWM IC.

Low-Side Driver

A block diagram of the low-side driver is shown in Figure 6. It drives a ground (VSS pin) referenced N-channel MOSFET.

Low impedances in the driver allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures high noise immunity and a low $R_{DS(ON)}$ from the external MOSFET.

A high level applied to xLI pin causes V_{DD} to be applied to the gate of the external MOSFET. A low level on the xLI pin grounds the gate of the external MOSFET.

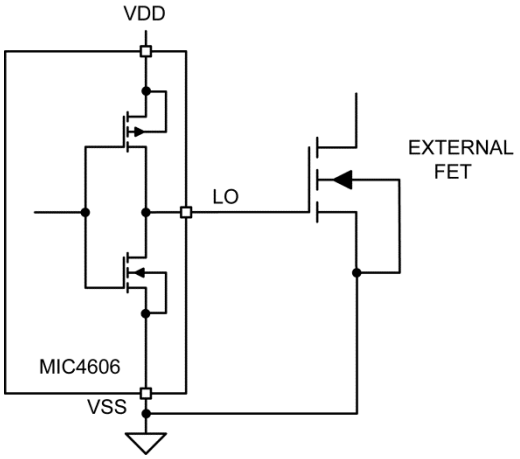


Figure 6. Low-Side Driver Block Diagram

High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 7. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

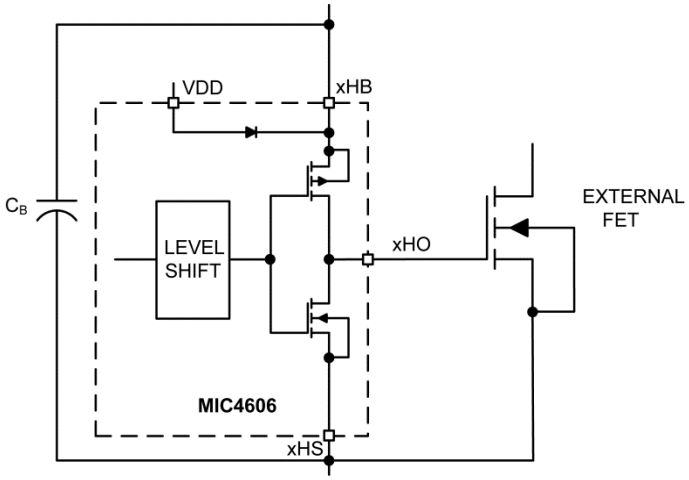


Figure 7. High-Side Driver and Bootstrap Circuit Block Diagram

A low-power, high-speed, level-shifting circuit isolates the low side (VSS pin) referenced circuitry from the high-side (xHS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap capacitor (C_B) while the voltage level of the xHS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the motor driver shown in Figure 8 (only Phase A illustrated), the AHS pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor C_B to charge up to V_{DD}-V_F during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor C_B from discharging.

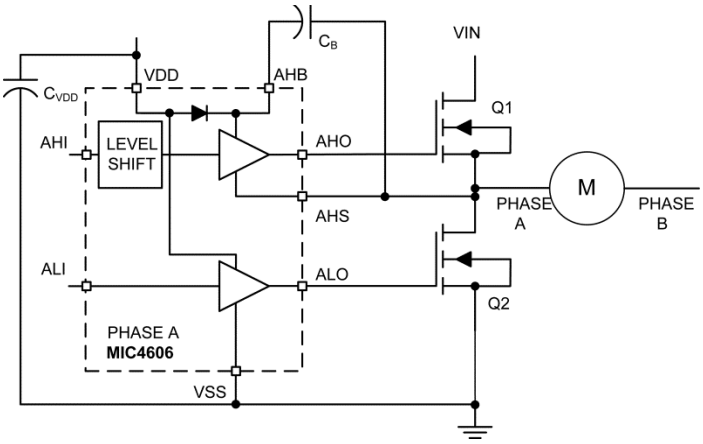


Figure 8. MIC4606 Motor Driver Example

Programmable Gate Drive

The MIC4606 offers programmable gate drive, which means the MOSFET gate drive (gate to source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in driving the MOSFETs. Different MOSFETs require different V_{GS} characteristics for optimum R_{DSON} performance. Typically, the higher the gate voltage (up to 16V), the lower the R_{DSON} achieved. For example, a NTMSF4899NF MOSFET can be driven to the ON state with a gate voltage of 5.5V but R_{DSON} is 5.2mΩ. If driven to 10V, R_{DSON} is 4.1mΩ – a decrease of 20%. In low-current applications, the losses due to R_{DSON} are minimal, but in battery-powered high-current motor drive applications such as power tools, the difference in R_{DSON} can cut into the efficiency budget, reducing run time.

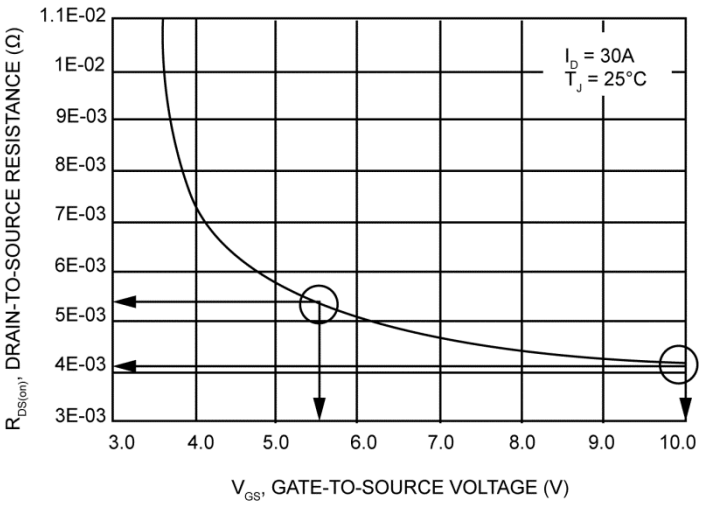


Figure 9. MOSFET RDSON vs. VGS

Application Information

Adaptive Dead Time

The door lock/unlock circuit diagram shown in Figure 11 is used to illustrate the importance of the adaptive dead time feature of the MIC4606. For each phase, it is important that both MOSFETs are not conducting at the same time or V_{IN} will be shorted to ground and current will "shoot through" the MOSFETs. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing. The high switching current and voltage ringing generate conducted and radiated EMI.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive dead time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 10 shows an equivalent circuit of the high-side gate drive, including parasitic.

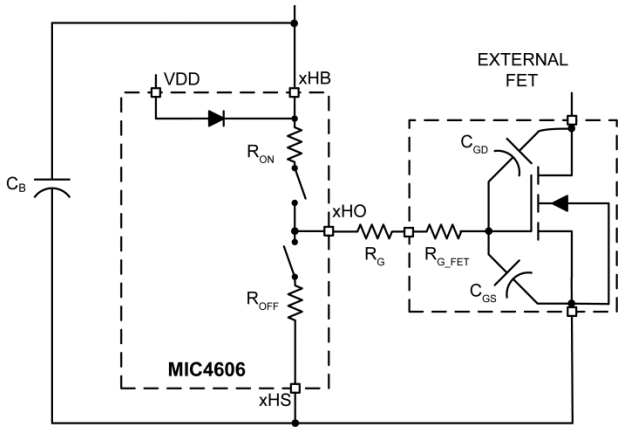


Figure 10. MIC4606 Driving an External MOSFET

The internal gate resistance (R_{G_FET}) and any external damping resistor (R_G) isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET datasheet. This delay increases when an external damping resistor is used.

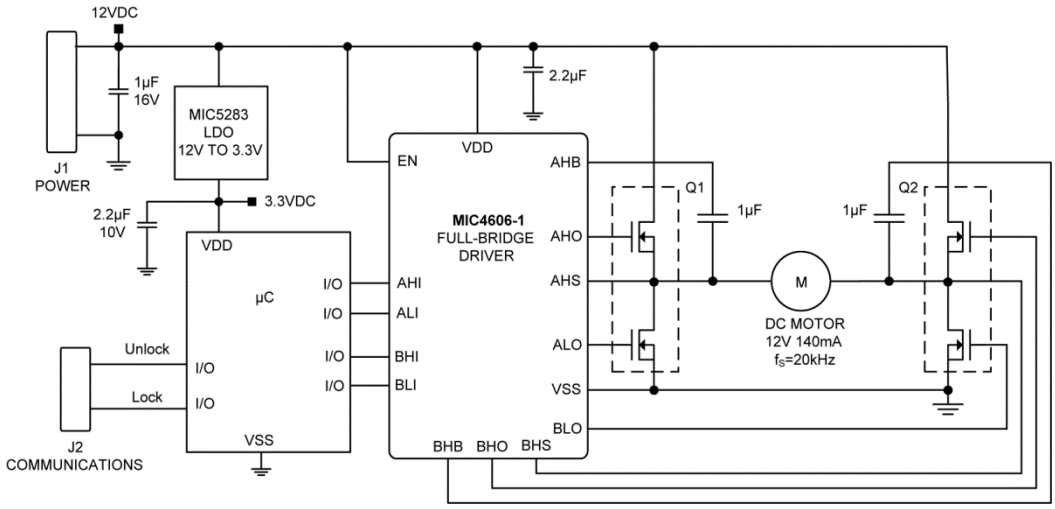


Figure 11. Door Lock/Unlock Circuit

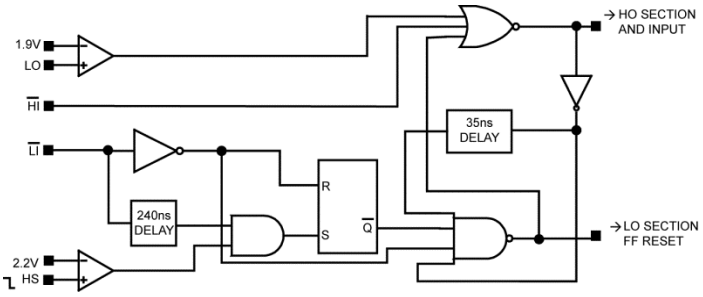


Figure 12. Adaptive Dead Time Logic Diagram

The MIC4606 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time. Figure 12 illustrates how the adaptive dead time circuitry works.

For the MIC4606-2, a high level on the xPWM pin causes /HI to go high and /LI to go low. This causes the xLO pin to go low. The MIC4606 monitors the xLO pin voltage and prevents the xHO pin from turning on until the voltage on the xLO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4606 drives the xHO pin high. Monitoring the xLO voltage eliminates any excessive delay due to the MOSFET drivers turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the xLO pin voltage settle out. An external resistor between the xLO output and the MOSFET may affect the performance of the xLO pin monitoring circuit and is not recommended.

A low on the xPWM pin causes /HI to go low and /LI to go high. This causes the xHO pin to go low after a short delay (t_{HOOFF}). Before the xLO pin can go high, the voltage on the switching node (xHS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the xHO pin voltage eliminates timing variations and excessive delays due to the high side MOSFET turn-off. The xLO driver turns on after a short delay (t_{LOON}). Once the xLO driver is turned on, it is latched on until the xPWM signal goes high. This prevents any ringing or oscillations on the switch node or xHS pin from turning off the xLO driver. If the xPWM pin goes low and the voltage on the xHS pin does not cross the V_{SWTH} threshold, the xLO pin will be forced high after a short delay (t_{SWTO}), insuring proper operation.

The internal logic circuits also insure a “first on” priority at the inputs. If the xHO output is high, the xLI pin is inhibited. A high signal or noise glitch on the xLI pin has no effect on the xHO or xLO outputs until the xHI pin goes low. Similarly, the xLO being high holds xHO low until xLI and xLO are low.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead time circuit in the MIC4606 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti shoot-through circuit’s control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

The scope photo in Figure 13 shows the dead time (<20ns) between the high and low-side MOSFET transitions as the low-side driver switches off while the high-side driver transitions from off to on.

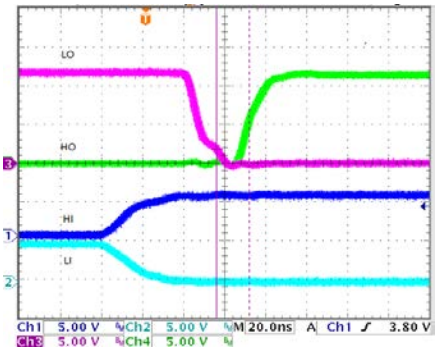


Figure 13. Adaptive Dead Time LO (low) to HO (high)

Table 1 contains truth tables for the MIC4606-1 (Independent TTL inputs) and Table 2 is for the MIC4606-2 (PWM inputs) that details the “first on” priority as well as the failsafe delay (t_{SWTO}).

Table 1. MIC4606-1 Truth Table

xLI	xHI	xLO	xHO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	xHO will not go high until xLO falls below 1.9V.
1	0	1	0	xLO will be delayed an extra 250ns if xHS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes low.

Table 2. MIC4606-2 Truth Table

xPWM	xLO	xHO	Comments
0	1	0	xLO will be delayed an extra 240ns if xHS never falls below 2.2V.
1	0	1	xHO will not go high until xLO falls below 1.9V.

Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the bootstrap capacitor (C_B) multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

$$I_{F(AVE)} = Q_{gate} \times f_S \quad \textbf{Eq. 1}$$

where;
Q_{gate} = total gate charge at V_{HB} - V_{HS}
f_s = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

$$Pdiode_{fwd} = I_{F(AVE)} \times V_F \quad \textbf{Eq. 2}$$

where; V_F = diode forward voltage drop

There are two phases in the MIC4606. The power dissipation for each of the bootstrap diodes must be calculated and summed to obtain the total bootstrap diode power dissipation for the package.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1mW and can be ignored.

An optional external bootstrap diode may be used instead of the internal diode (Figure 14). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

$$Pdiode_{REV} = I_R \times V_{REV} \times (1 - D) \quad \textbf{Eq. 3}$$

where;
I_R = reverse current flow at V_{REV} and T_J
V_{REV} = diode reverse voltage
D = duty cycle = $t_{ON} \times f_S$

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

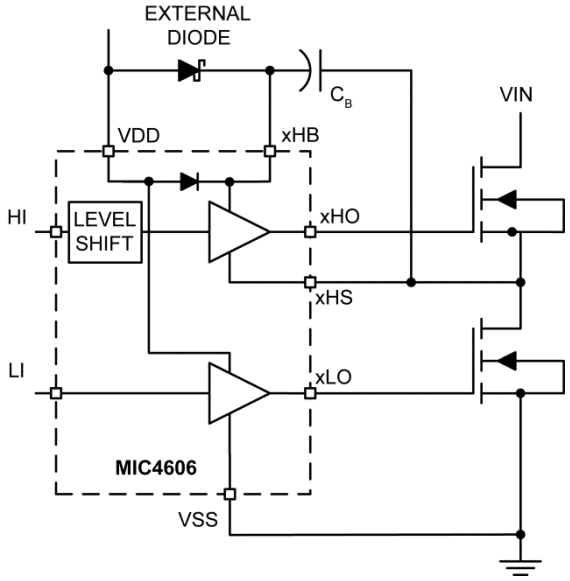


Figure 14. Optional Bootstrap Diode

Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 15 shows a simplified equivalent circuit of the MIC4606 driving an external high-side MOSFET.

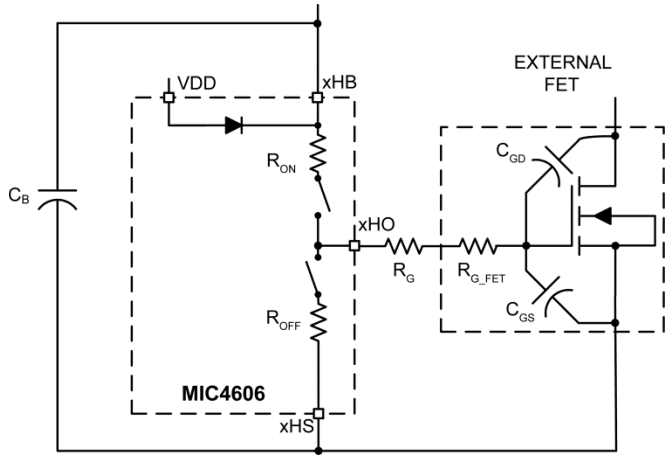


Figure 15. MIC4606 Driving an External High-Side MOSFET

Dissipation during the External MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4606. R_G is the series resistor (if any) between the driver and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus V_{GS}. Figure 16 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

$$E = \tfrac{1}{2} \times C_{ISS} \times V_{GS}^{\,2}$$
$$but$$
$$Q = C \times V \qquad \textbf{Eq. 4}$$
$$so$$
$$E = \tfrac{1}{2} \times Q_G \times V_{GS}$$

Where
C_{ISS} = total gate capacitance of the MOSFET

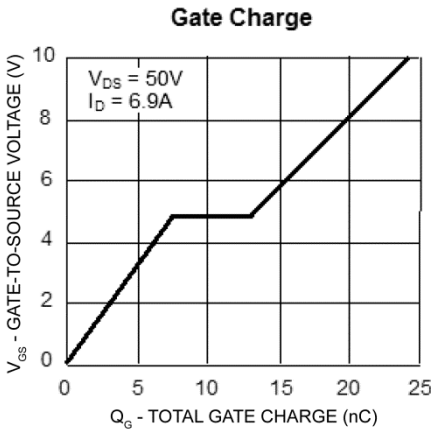


Figure 16. Typical Gate Charge vs. V_{GS}

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is:

$$E_{DRIVER} = Q_G \times V_{GS}$$
$$and \qquad \textbf{Eq. 5}$$
$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:
E_{DRIVER} = energy dissipated per switching cycle
P_{DRIVER} = power dissipated per switching cycle
Q_G = total gate charge at V_{GS}
V_{GS} = gate to source voltage on the MOSFET
f_S = switching frequency of the gate drive circuit

The power dissipated in the driver equals the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting R_{ON} = R_{OFF}, the power dissipated in the driver due to driving the external MOSFET is:

$$Pdiss_{driver} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}} \qquad \textbf{Eq. 6}$$

There are four MOSFETs driven by the MIC4606. The power dissipation for each of the drivers must be calculated and summed to obtain the total driver diode power dissipation for the package.

In some cases, the high-side FET of one phase may be pulsed at a frequency, f_S, while the low-side FET of the other phase is kept continuously on. Since the MOSFET gate is capacitive, there is no driver power if the FET is not switched. The operation of each of the four drivers must be considered to accurately calculate power dissipation.

Supply Current Power Dissipation

Power is dissipated in the input and control sections of the MIC4606, even if there is no external load. Current is still drawn from the VDD and HB pins for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The VDD and HB currents are proportional to operating frequency and the VDD and VHB voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4606 due to supply current is

$$Pdiss_{supply} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB} \quad \textbf{Eq. 7}$$

Values for I_{DD} and I_{HB} are found in the EC table and the typical characteristics graphs.

Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4606 is equal to the power dissipation caused by driving the external MOSFETs, the supply currents and the internal bootstrap diodes.

$$Pdiss_{total} = Pdiss_{supply} + Pdiss_{drive} + Pdiode \quad \textbf{Eq. 8}$$

The die temperature can be calculated after the total power dissipation is known.

$$T_J = T_A + Pdiss_{total} \times \theta_{JA} \quad \textbf{Eq. 9}$$

Where:
T_A = maximum ambient temperature
T_J = junction temperature (°C)
$Pdiss_{total}$ = total power dissipation of the MIC4606
θ_{JA} = thermal resistance from junction to ambient air

Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (VDD) and high side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from HB to HS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1µF is required for C_B (HB to HS capacitors) and 1µF for the VDD capacitor, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the VDD and VSS pins. The bypass capacitor (C_B) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section Grounding, Component Placement and Circuit Layout for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}} \quad \textbf{Eq. 10}$$

Where:
Q_{GATE} = total gate charge at V_{HB}
ΔV_{HB} = voltage drop at the HB pin

If the high-side MOSFET is not switched but held in an on state, the voltage in the bootstrap capacitor will drop due to leakage current that flows from the HB pin to ground. This current is specified in the EC table. In this case, the value of CB is calculated as:

$$C_B \geq \frac{I_{HBS} \times t_{ON}}{\Delta V_{HB}} \quad \textbf{Eq. 11}$$

Where:
I_{HBS} = maximum HB pin leakage current
t_{ON} = maximum high-side FET on-time

The larger value of C_B from Equation 10 or 11 should be used.

DC Motor Applications

MIC4606 MOSFET drivers are widely used in DC motor applications. They address both stepper and brushed motors in full-bridge topologies. As shown in Figure 17 and Figure 18, the driver switches the MOSFETs at variable duty cycles that modulate the voltage to control motor speed. The full-bridge topology allows for bi-directional control.

The MIC4606's 85V operating voltage offers ample operating voltage margin to protect against voltage spikes in the motor drive circuitry. It is good practice to have at least twice the HV voltage of the motor supply. The MIC4606's 85V operating voltage allows sufficient margin for 12V, 24V, and 40V motors.

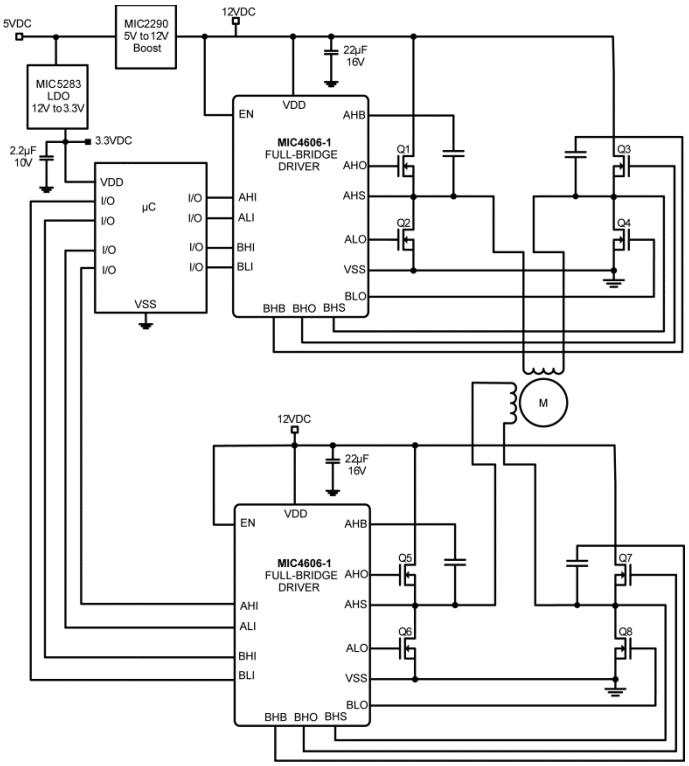


Figure 17. Stepper Motor Driver

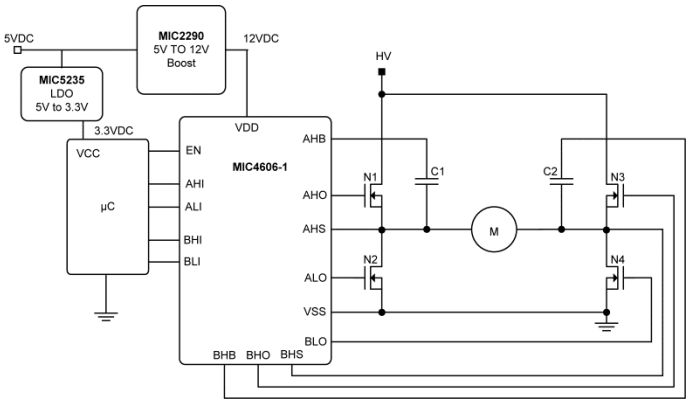


Figure 18. Full-Bridge DC Motor

The MIC4606 is offered in a small 4mm × 4mm QFN 16 lead package for applications that are space constrained. The motor trend is to put the motor control circuit inside the motor casing, which requires small packaging because of the size of the motor.

The MIC4606 offers low UVLO threshold and programmable gate drive, which allows for longer operation time in battery operated motors such as power hand tools.

Power Inverter

Power inverters are used to supply AC loads from a DC operated battery system, mainly during power failure. The battery voltage can be 12VDC, 24VDC, or up to 36VDC, depending on the power requirements. There two popular conversion methods, Type I and Type II, that convert the battery energy to AC line voltage (110VAC or 230VAC).

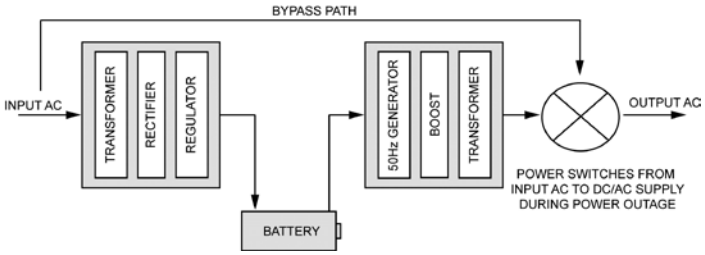


Figure 19. Type I Inverter Topology

As shown in Figure 19, Type I is a dual-stage topology where line voltage is converted to DC through a transformer to charge the storage batteries. When a power failure is detected, the stored DC energy is converted to AC through another transformer to drive the AC loads connected to the inverter output. This method is simplest to design but tends to be bulky and expensive because it uses two transformers.

Type II is a single-stage topology that uses only one transformer to charge the bank of batteries to store the energy. During a power outage, the same transformer is

used to power the line voltage. The Type II topology switches at a higher frequency compared to the Type I topology to maintain a small transformer size.

Both types use a full bridge topology to invert DC to AC. The MIC4606's operating voltage offers enough of a margin to address all of the available banks of batteries commonly used in inverter applications. The 85V operating voltage allows designers to increase the bank of batteries up to 72V, if desired. The MIC4606 can sink as much as 1A, which is sufficient to drive the MOSFET's gate capacitance while switching the MOSFET up to 50kHz. This makes the MIC4606 an ideal solution for single phase inverter applications.

Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4606 driver require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 20 shows the critical current paths of the high and low-side driver when their outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the xHB pin and out the xHO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the xHB and xHS pins. This capacitor not only provides all the energy for turn-on but it must also keep xHB pin noise and ripple low for proper operation of the high-side drive circuitry.

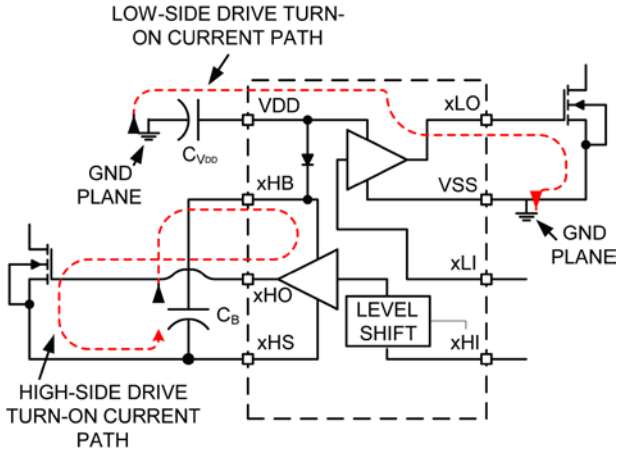


Figure 20. Turn-On Current Paths

Figure 21 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

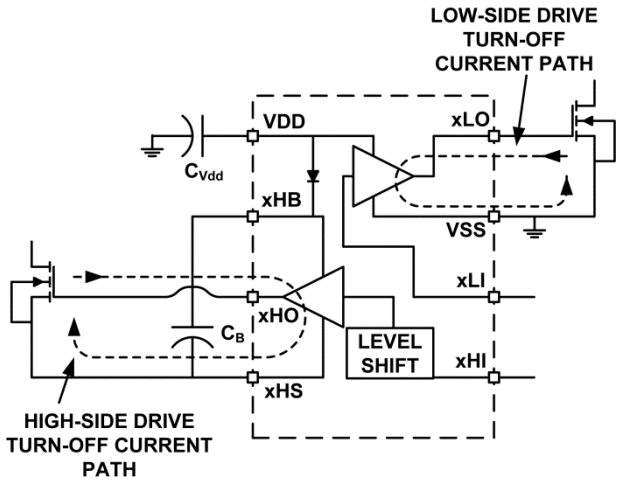
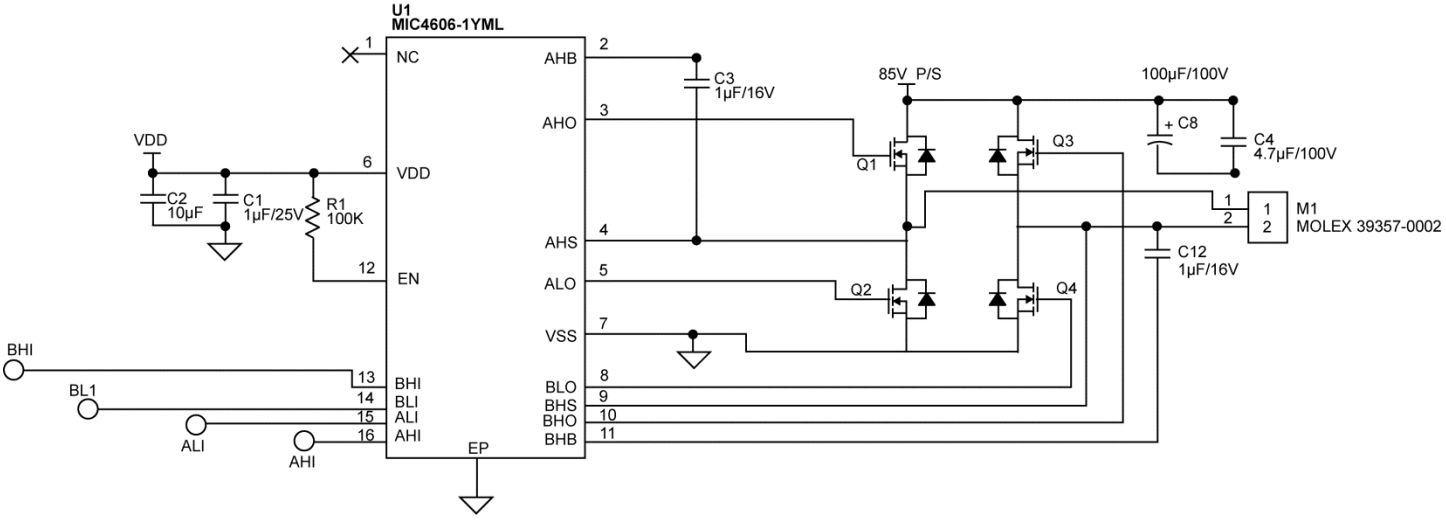


Figure 21. Turn-Off Current Paths

Typical Application Schematic



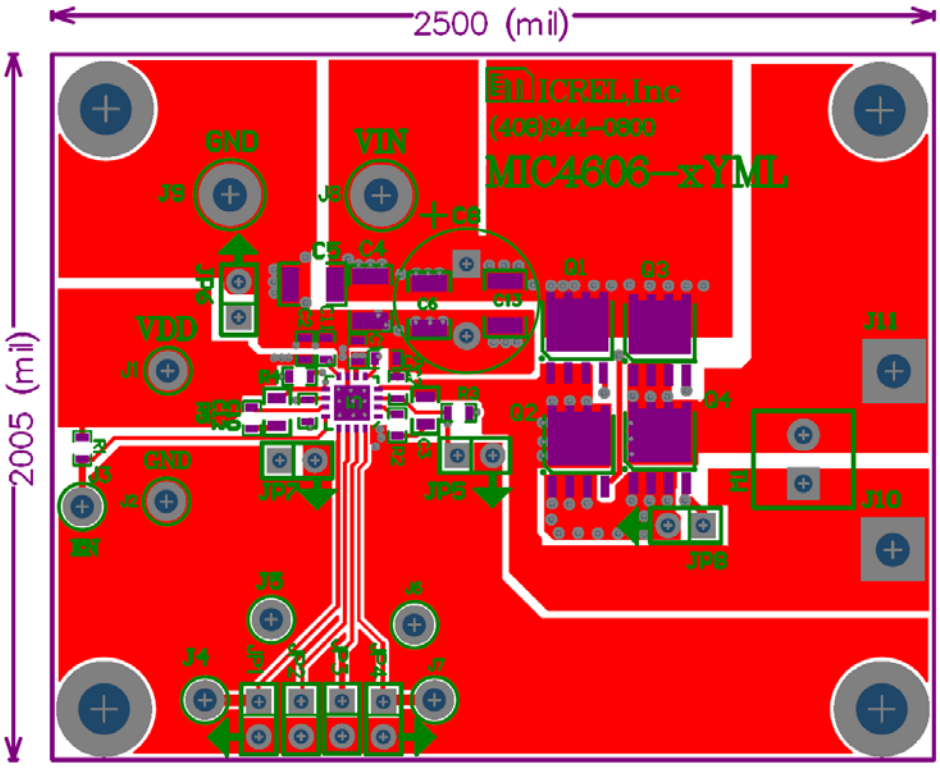
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	06033D105MAT2A	AVX[10]	1µF Ceramic Capacitor, 25V, X5R, Size 0603	1
C2	C1608X5R1C106M080AB	TDK[11]	10µF Ceramic Capacitor, 16V, X5R, Size 0603	1
C3, C12	0805YD105MAT2A	AVX	1µF Ceramic Capacitor, 16V, X5R, Size 0805	2
C4	C3225X7S2A475M200AB	TDK	4.7µF Ceramic Capacitor, 100V, X7S, Size 1210	1
C8	B41827A9107M	EPCOS[12]	100µF Aluminum Electrolytic Capacitor, 100V	1
Q1, Q2, Q3, Q4	AM7414	Analog Power[13]	100V, N-Channel MOSFET	4
R1	CRCW06030000FRT1	Vishay[14]	100kΩ, Tolerance 1%, Size 0603	1
U1	**MIC4606-1YML**	**Micrel, Inc.[15]**	**85V Full-Bridge MOSFET Drivers with Adaptive Dead Time and Shoot-Through Protection**	1

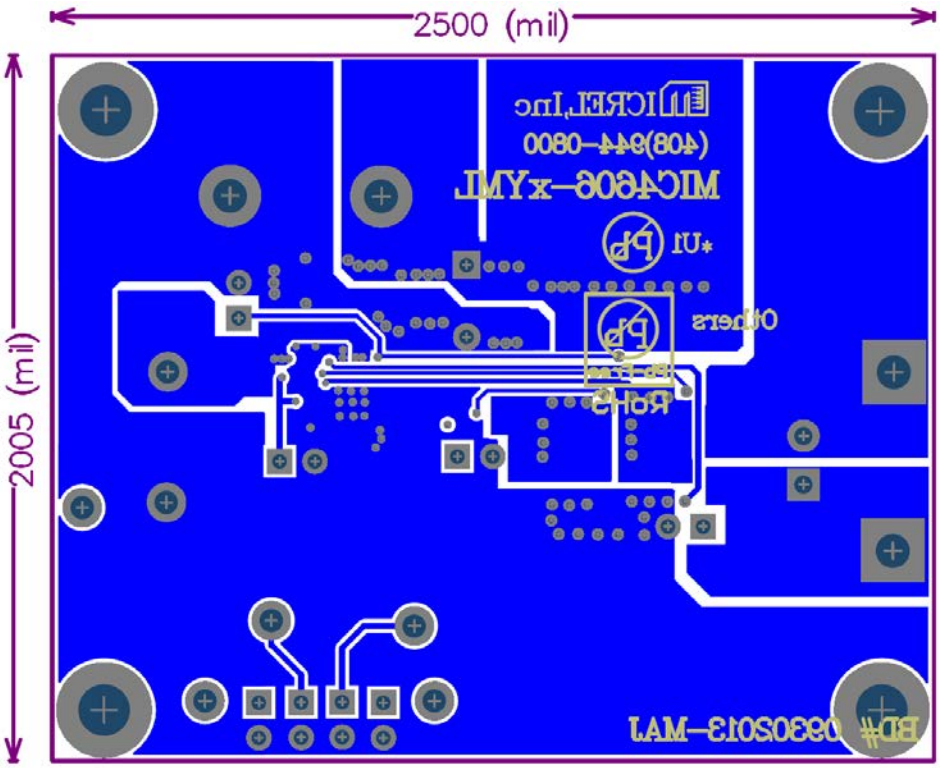
Notes:

10. AVX: www.avx.com.
11. TDK: www.tdk.com.
12. EPCOS: www.epcos.com.
13. Analog Power: www.analogpowerinc.com.
14. Vishay: www.vishay.com.
15. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations



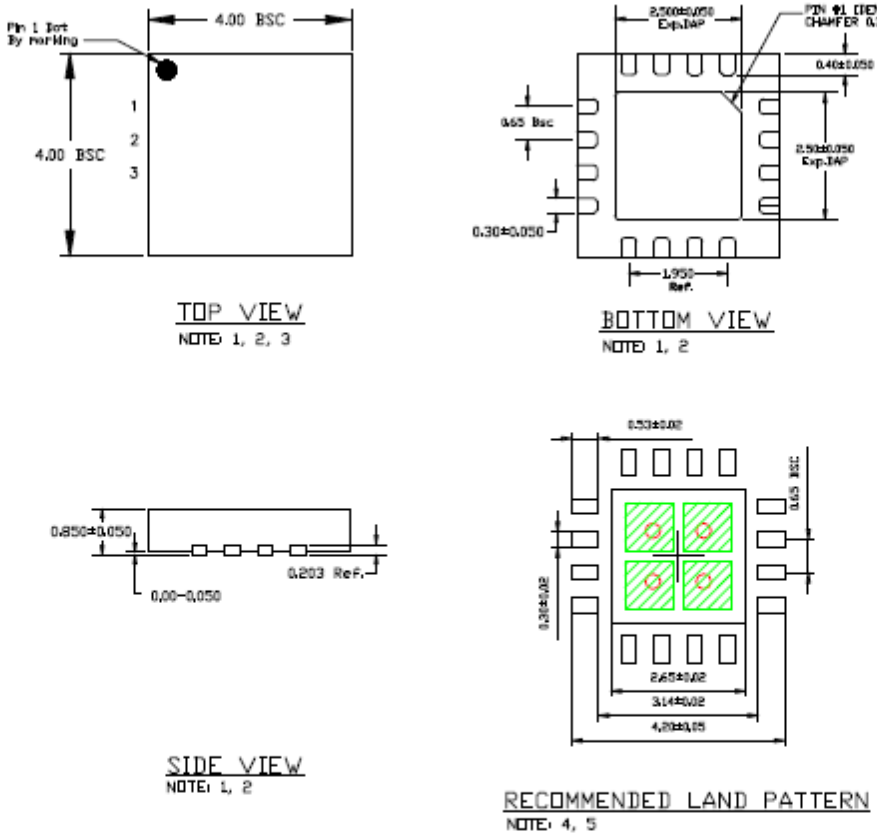
Top Layer



Bottom Layer

Package Information[7]

DRAWING #	QFN44-16LD-PL-2	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. GREEN RECTANGLES (SHADED AREA) REPRESENT STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.95X0.95mm, 1.15MM PITCH SPACING.
5. RED CIRCLES REPRESENT THERMAL VIAS & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30-0.35mm. RECOMMENDED DIAMETER, 1.0mm PITCH SPACING.

16-Pin QFN 4mm x 4mm (ML)

Note:

16. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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Micrel, Inc. is a leading global manufacturer of IC solutions for the worldwide high performance linear and power, LAN, and timing & communications markets. The Company's products include advanced mixed-signal, analog & power semiconductors; high-performance communication, clock management, MEMs-based clock oscillators & crystal-less clock generators, Ethernet switches, and physical layer transceiver ICs. Company customers include leading manufacturers of enterprise, consumer, industrial, mobile, telecommunications, automotive, and computer products. Corporation headquarters and state-of-the-art wafer fabrication facilities are located in San Jose, CA, with regional sales and support offices and advanced technology design centers situated throughout the Americas, Europe, and Asia. Additionally, the Company maintains an extensive network of distributors and reps worldwide.

Revision History

Date	Change Description/Edits by:	Rev.
6/18/08	Locked document. M.Mclean	15
5/28/09	Unlocked document, removed some styles, minor formatting. M.Galvan	16
6/3/09	Fixed EC table font from 10pt to 9pts, moved Typ. App. dwg to front page. M. Galvan	17
6/9/09	Fixed EC table font from 10pt to 9pt. fixed a few minor font. M.Galvan	18
12/1/09	Added Recommended Landing Pattern to template. M. Galvan	19
8/4/10	Added new paragraph to disclaimer in boiler plate. Per Colin Sturt. M.Galvan	20
1/7/13	Complete rework	1.0
4/30/13	Made notes run continuously, rather than restart on each page	2.1