- Single Chip Mixer/Oscillator and Synthesizer
- VHF-L, VHF-H, UHF 3-Band Local Oscillator
- I²C Bus Protocol
- Bidirectional Data Transmission
- 30-V Tuning Voltage Output
- 4-Channel NPN Type Band Switch Drivers
- Programmable Reference Divider Ratio (512, 640 or 1024)
- 5-V Power Supply
- 32-Pin TSSOP Package

description

SN761672A is a single chip synthesized tuner IC designed for TV/VCR tuning systems. The circuit consists of a PLL synthesizer, 3-band local oscillators and mixer, a 30-V output tuning amplifier, and four NPN band switch drivers. It is available in a small package outline. The 15-bit

DA PACKAGE (TOP VIEW)

VOL OSC B	1 0 32	UHF RF IN2
VOL OSC C	2 31	UHF RF IN1
OSC GND	3 30	☐ VHF RF IN2
VHS OSC B	4 29	☐ VHF RF IN1
VHS OSC C 🗆	5 28	RF GND
UHF OSC B1 □□□	6 27	☐☐ MIX OUT2
UHF OSC C1	7 26	☐☐ MIX OUT1
UHF OSC C2 \Box	8 25	□□ BS4
UHF OSC B2	9 24	□□ BS3
IF GND □□□	10 23	□□ BS2
IF OUT1	11 22	□□ BS1
IF OUT2	12 21	□□ NC
V _{CC} □□	13 20	□□ ADC
CP \Box	14 19	□□ AS
VTU 🗀	15 18	□□ SDA
XTAL 🗆	16 17	□□ SCL

NC - No internal connection

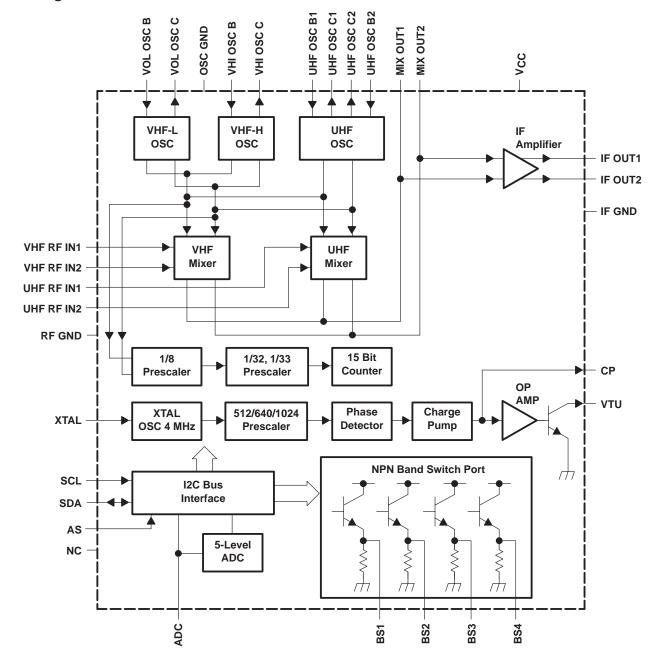
programmable counter and reference divider is controlled by I²C bus protocol. Tuning step frequency is selectable by this reference-divider ratio for a 4-MHz crystal oscillator.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



block diagram





Terminal Functions

TERMINAL						
NAME	NO.	1/0	DESCRIPTION			
ADC	20	1	ADC input (see Figure 7)			
AS	19	1	ddress selection input (see Figure 7)			
BS1	22	0	Band switch1 output (NPN emitter follower) (see Figure 8)			
BS2 BS3	23 24					
BS4	25					
СР	14	0	Charge pump output (see Figure 5)			
IF GND	10		IF ground (see Figure 4)			
IF OUT1	11	0	IF output (see Figure 4)			
IF OUT2	12	0	IF output (see Figure 4)			
MIX OUT1 MIX OUT2	26 27	0	Mixer outputs (see Figure 9)			
OSC GND	3		OSC ground			
RF GND	28		RF ground			
SCL	17	I	Serial clock input (see Figure 7)			
SDA	18	I/O	Serial data input/output (see Figure 7)			
UHF OSC B1	6	I	UHF oscillator input, base 1 (see Figure 3)			
UHF OSC B2	9	I	UHF oscillator input, base 2 (see Figure 3)			
UHF OSC C1	7	0	UHF oscillator output, collector 1 (see Figure 3)			
UHF OSC C2	8	0	UHF oscillator output, collector 2 (see Figure 3)			
UHF RF IN1 UHF RF IN2	31 32	ı	UHF RF inputs (see Figure 11)			
VCC	13		Supply voltage for mixer/oscillator/PLL: 5 V			
VHF RF IN1 VHF RF IN2	29 30	I	VHF RF inputs (see Figure 10)			
VHI OSC B	4	ı	VHF hi oscillator input base (see Figure 2)			
VHI OSC C	5	0	VHF hi oscillator output collector (see Figure 2)			
VLO OSC B	1	I	VHF low oscillator input base (see Figure 1)			
VLO OSC C	2	0	VHF low oscillator output collector (see Figure 1)			
VTU	15	0	Tuning voltage amplifier output (see Figure 5)			
XTAL	16	I	4-MHz crystal oscillator input (see Figure 6)			

schematics

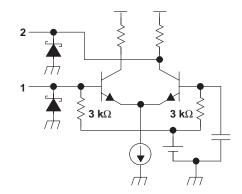


Figure 1

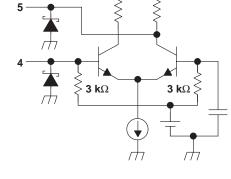


Figure 2

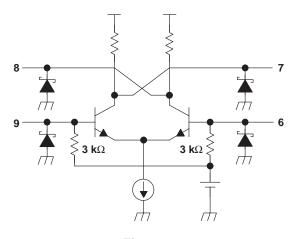


Figure 3

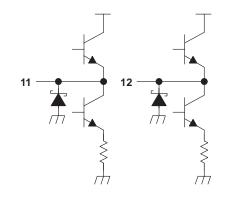


Figure 4

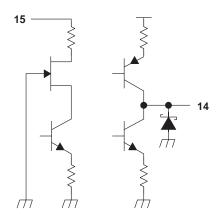


Figure 5

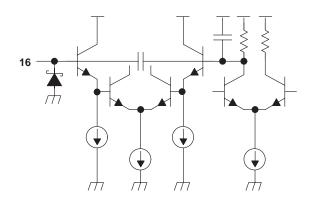


Figure 6

schematics (continued)

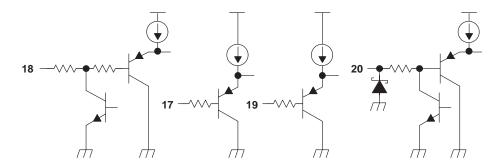


Figure 7

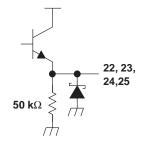


Figure 8

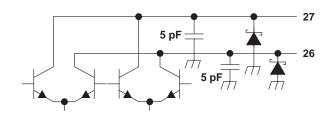


Figure 9

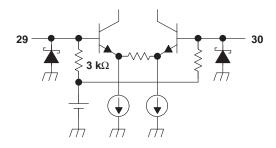


Figure 10

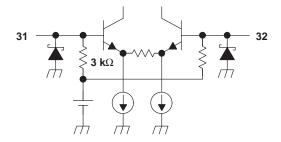


Figure 11

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	
Input voltage 1, V _{I(GND)} (see Note 1)	0.4 V ~ 0.4 V
Input voltage 2, V _{I(VTU)}	
Input voltage 3, V _(VTU) (see Note 1)	
Continuous total dissipation at (or below T _A = 25°C	See Dissipation Rating Table
Operating free-air temperature, T _A	–20°C to 85°C
Storage temperature range, T _{stq}	65°C to 150°C
Maximum junction temperature, T _J	150°C
Maximum lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Maximum short circuit time, t _(SCMAX) , All pins to V _{CC}	TBD

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the IF GND of the circuit.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \le 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	OPERATING FACTOR $T_A \le 25^{\circ}C$
DA	1040 mW	8.33 mW/°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.5	V
Tuning supply voltage, VSS(TU)		30	33	V
Output current of band switch, one port ON, IO			10	mA
Operating free-air temperature, T _A	-20		85	°C

CAUTION:

It is advised that precautions to be taken to avoid damage due to high static voltages or electrostatic fields in handling this device. Pins 4–6 and 9 withstand 150 V, and all other pins withstand 200 V, according to EIAJ (0 Ω , 200 pF).



electrical characteristics

total device and serial interface (V_{CC} 4.5 V to 5.5 V, $T_A = -20^{\circ}$ C to 85°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _{CC(1)}	Supply current 1				60	80	mA
ICC(2)	Supply current 2		One band switch ON – I(BS) = 10 mA		70	90	mA
VIH	High-level input voltage (SCL, SDA)			3			V
V _{IL}	Low-level input voltage (SCL, SDA)					1.5	V
lιΗ	High-level input current (SCL, SDA)					10	μΑ
I _{IL}	Low-level input current (SCL, SDA)			-10			μΑ
V(POR)	Power on reset supply voltage		Threshold of supply voltage between reset and operation mode	2.1	2.8	3.5	V
V(ASH)		High	0.9 V _{CC} ~ V _{CC}	4.5		5	
V(ASM)	Address select input voltage (AS)	Mid	0.4 V _{CC} ~ 0.6 V _{CC}	2		3	V
V(ASL)	7 [0 V _{CC} ~ 0.1 V _{CC}			0.5	
I(ASH)	Address solestingut surrent (AC)	High				10	^
I(ASL)	Address select input current (AS)	Low		-10			μΑ
V(ADC)	ADC input voltage		See Table 9	0		VCC	V
I _{IL(ADH)}	ADC high-level input current		$V_{(ADC)} = V_{CC}$			10	μΑ
I _{IL(ADL)}	ADC low-level input current		V(ADC) = 0 V	-10			μΑ
f(SCL)	Clock frequency (SCL)				100	400	kHz
th(HLD)	Data hold time		See timing chart, Figure 1	0			μs
VOL	Low-level output voltage (SDA)		$V_{CC} = 5 \text{ V}, \qquad I_{OL} = 3 \text{ mA}$			0.4	V
I _{lkg} (SDA)	High-level output leakage current (SD/	A)	V(SDA) = 5.5 V			10	μΑ

PLL and band switch (V_{CC} 4.5 V to 5.5 V, $T_A = -20^{\circ}$ C to 85°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIO	NS	MIN	TYP	MAX	UNIT
N	Divider ratio	14-bit frequency word		256		16383	
N	Divider fatio	15-bit frequency word		256		32767	
F _(XTAL)	Crystal oscillator	R_{XTAL} = 25 Ω to 300 Ω			4		MHz
Z(XTAL)	Crystal oscillator input impedance				1.6		k
V(VTUL)	Tuning amplifier low-level output voltage	$R_L = 27K$, $V_{(TU)}$	= 33 V	0.2	0.3	0.46	V
I _(VTUOFF)	Tuning amplifier leakage current (OFF)	OS = 1, V _(TU)	= 33 V			10	μΑ
I _(CPH)	Charge pump high-level input current	CP = 1			280		μΑ
I(CPL)	Charge pump low-level input current	CP = 0			60		μΑ
V _(CP)	Charge pump output voltage	In-lock			1.95		V
I(CPOFF)	Charge pump leakage current	$T2 = 0$, $T1 = 1$, $V_{CP} = T_A = 25^{\circ}C$	= 2 V,	-15		15	nA
I _(BS)	Band switch driver output current					10	mA
V(SBS1)		I _(BS) = 10 mA		3			
V(SBS2)	Band switch driver output voltage	$I_{(BS)} = 10 \text{ mA},$ $V_{CC} = T_A = 25^{\circ}\text{C}$	= 5 V,	3.5	3.9		V
Ilkg(BSOFF)	Band switch driver leakage current	V _(BS) = 0 V				3	μΑ

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electrical characteristics (continued)

mixer, oscillator, IF amplifier (V_{CC} 5 V, T_A = 25°C, measured in reference measurement circuit at 50 W system, IF filter characteristics: f_{peak} = 43 MHz) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
G _(c1)	Conversion gain (mixer ~ IF amplifier, VHF-low	f _{in} = 59 MHz (see Note 2)	20	23	26	dB	
G _(c3)	Conversion gain (mixer ~ ir ampililer, vmr-iow	f _{in} = 130 MHz	20	23	26	шь	
G _(C4)	Conversion gain (mixer ~ IF amplifier, VHF-high	f _{in} = 136 MHz (see Note 2)	20	23	26	dB	
G _(c6)	Conversion gain (mixer ~ ir ampililer, vmr-nigh	f _{in} = 364 MHz	20	23	26	uБ	
G _(c7)	Conversion gain (mixer ~ IF amplifier, VHF-UHF	f _{in} = 370 MHz (see Note 2)	22	25	28	dB	
G _(c9)	Conversion gain (mixer ~ ir ampliller, vhr-ohr	f _{in} = 804 MHz	20	23	26	uБ	
NF ₁	Noise figure VHE low	f _{in} = 55.25 MHz		9.5		dB	
NF ₃	Noise figure VHF-low	f _{in} = 127.25 MHz		9.5		uБ	
NF ₄	Noise figure VHF-low	f _{in} = 133.25 MHz		10		dB	
NF ₆	Noise ligure var-low	f _{in} = 361.25 MHz		10		uБ	
NF ₇	Noise figure UHF	f _{in} = 367.25 MHz	9			dB	
NF ₉	Noise ligure one	f _{in} = 801.25 MHz		10		l ub	
CM ₁	1% cross modulation distortion VHF-low	f _{in} = 55.25 MHz (see Note 3)		91		dΒμV	
CM ₃	1% cross modulation distortion var-low	f _{in} = 801.25 MHz	91			чъμν	
CM ₄	1% cross modulation distortion VHF-high	f _{in} = 133.25 MHz (see Note 3)		91		dΒμV	
CM ₆	1 % cross modulation distortion vi ii -nigh	f _{in} = 361.25 MHz	91			αυμν	
CM ₇	1% cross modulation distortion UHF	f _{in} = 367.25 MHz (see Note 3)	88			dD\/	
CM ₉	1 % Closs modulation distortion of in	f _{in} = 801.25 MHz	88			d BμV	
V(IFO1)	IF output voltage VHF-low	f _{in} = 55.25 MHz (see Note 4)	117			dB:://	
V _(IFO3)	Tr output voltage vinr-low	f _{in} = 127.25 MHz	117			dBμV	
V(IFO4)	IF output voltage VHF-high	f _{in} = 133.25 MHz (see Note 4)		117		4Bii//	
V(IFO6)	in output voitage vin -ingn	f _{in} = 361.25 MHz	117		dBμV		
V _(IFO7)	IF output voltage UHF	f _{in} = 367.25 MHz (see Note 4)		117		dBu\/	
V _(IFO9)	in output voitage of in	f _{in} = 801.25 MHz	117			dBμV	
	Prescaler beat (see Note 5)				25	dΒμV	

NOTES: 2. IF = 43 MHz, RF input level = 80 dB μ V

3. f(undes) = f(des) ± 6 MHz, pin = 80 dBµV, AM 1 kHz, 30%, DES/CM=S/I=46 dB 4. IF = 45.75 MHz

5. Design parameter, not tested



function description

The device can be controlled according to the I^2C bus format.

Table 1. Serial Interface Function

PIN	PIN NAME	FUNCTION
17	SCL Clock input	
18	SDA	Data input/output
19	AS	Address selection input
20	ADC	ADC input/test output

I²C bus mode

 I^2C write mode (R/W = 0)

Table 2. Write Data Format

	MSB							LSB	ACKNOWLEDGE
Address byte (ADV)	1	1	0	0	0	MA1	MA0	R/W 0	А
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	А
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	А
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	os	А
Band switch byte (BB)	Х	Х	Х	Х	BS4	BS3	BS2	BS1	А

Table 3. Description of Data Symbol

SYMBOL		DESCRIPTION				
MA1, MA0	Address set bits (see Ta	Address set bits (see Table 4)				
N14N0	Programmable counter	set bits	N=N14*2	^14+N13*2^13++N1*2+N0	Nn = 0	
СР	Charge pump current se	et bit	60 μA (Cl	P=0) 280 μA (CP=1)	CP = 1	
T2, T1, T0	Test bits (see table 5)		Normal M	lode: T2=0, T1=0, To=1/0	T2=0, T1=0, T0=1	
RSA, RSB	Reference divider ratio	Reference divider ratio selection bits (see Table 6)				
os	Tuning amplifier control	bit	Tuning voltage on (OS=0) Tuning voltage off, high impedance (OS=1)		OS=0	
BS4BS1	Band switch ports control Band selection by BS1,2		BSn=0:O 't care)	FF BSn=1:ON	BSn=0	
		BS1	BS2	BS4		
	VHF-LO	1	0	0		
	VHF-HI	Χ	1	0		
	UHF	Χ	Χ	1		
Х	Don't care					

Table 4. Address Selection

VOLTAGE APPLIED ON CE INPUT	MA1	MA0
0 V to 0.1 V _{CC}	0	0
Always valid	0	1
0.4 V _{CC} to 0.6 V _{CC}	1	0
0.9 V _{CC} to V _{CC}	1	1



I²C bus mode (continued)

Table 5. Test Bits (see Note 7)

T2	T1	T0	FUNCTION	
0	0	0	Normal operation	
0	0	1	Normal operation	Default
0	1	Х	Charge pump off	
1	1	0	Charge pump sink	
1	1	1	Charge pump source	
1	0	0	Reference counter output is available on ADC pin.	Not available ADC
1	0	1	Main counter output is available on ADC pin (see Note 7).	Not available ADC

NOTES: 6. Not used for other bit-patterns.

7. Main counter input is bypassed 1.8 and 1.32, 1/33 prescaler from oscillator, at this mode. (F_{OSC} ≤ 4 MHz)

Table 6. Ratio Select Bits

RSA	RSB	REFERENCE DIVIDER RATIO					
Х	0	640					
0	1	1024					
1	1	512					

I^2C read mode (R/W = 1)

Table 7. Read Data Format

	MSB							LSB	ACKNOWLEDGE
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W=1	Α
Status byte (SB)	POR	FL	1	1	1	A2	A1	A0	A

Table 8. Description of Data Symbol

SYMBOL		DEFAULT					
MA1, MA0	Address set bits (see Tab	Address set bits (see Table 4)					
POR	Power-on reset flag	POR set: power on POR reset: end-of-data transmission procedure	POR = 1				
FL	In-lock flag	PLL lock (FL = 1) Unlock (FL = 0)					
A2A0	Digital data of ADC (see	Digital data of ADC (see Table 9)					

Table 9. ADC Level

VOLTAGE APPLIED ON ADC INPUT	A2	A1	A0
0.6 V to V _{CC}	1	0	0
0.45 V _{CC} to 0.6 V _{CC}	0	1	1
0.3 V _{CC} to 0.45 V _{CC}	0	1	0
0.15 V _{CC} to 0.3 V _{CC}	0	0	1
0 V _{CC} to 0.15 V _{CC}	0	0	0



I²C read mode (R/W = 1) (continued)

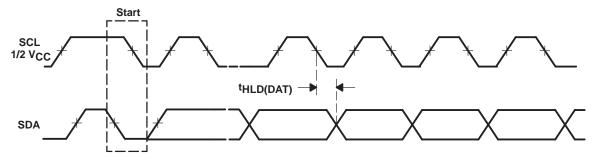
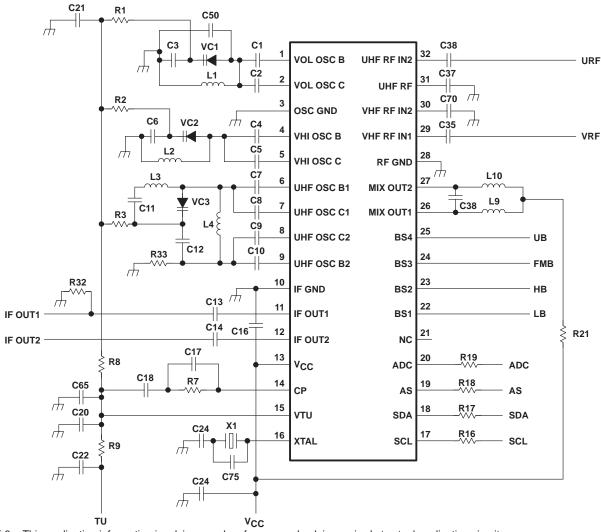


Figure 12. I²C Timing Chart

APPLICATION INFORMATION



NOTE 8: This application information is advisory and performance-check is required at actual application circuits.

Figure 13. Reference Measurement Circuit



APPLICATION INFORMATION

component values for measurement circuit

PARTS NAME	VALUE	PARTS NAME	VALUE
U1	SN761672A	C1	1 pF
VC1	1T363A	C2	1 pF
VC2	1T363A	C3	47 pF
VC3	1T363A	C4	2 pF
L1	Diameter 3.0 mm 8T	C5	3 pF
L2	Diameter 2.4 mm 4T	C6	86 pF
L3	Diameter 3.0 mm 2T	C7	1.5 pF
L4	Diameter 2.0 mm 3T	C8	1.5 pF
L9	Diameter 2.4 mm 15T	C9	1.5 pF
L10	Diameter 2.4 mm 15T	C10	1.5 pF
X1	X'tal 4 MHz	C11	100 pF
R1	33 kΩ	C12	12 pF
R2	33 kΩ	C13	2.2 nF
R5	33 kΩ	C14	2.2 nF
R7	22 kΩ	C16	2.2 nF
R8	33 kΩ	C17	2.2 nF
R9	22 kΩ	C18	0.1 μF
R16	330 Ω	C20	2.2 nF
R17	330 Ω	C21	2.2 nF
R18	330 Ω	C22	2.2 nF
R21	0 Ω	C24	5 pF
R19	330 Ω	C33	27 pF
R32	56 Ω	C35	2.2 nF
R33	22 kΩ	C37	2.2 nF
		C38	2.2 nF
		C39	2.2 nF
		C50	3 pF
		C65	2.2 nF
		C70	2.2 nF
		C75	10 pF

APPLICATION INFORMATION

test circuit

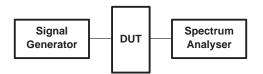


Figure 14. Measurement Circuit of Conversion Gain

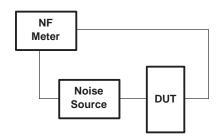


Figure 15. Noise Figure Measurement Circuit

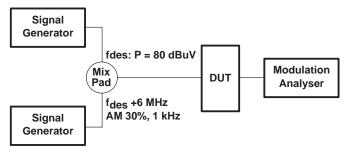
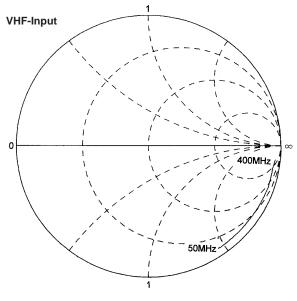


Figure 16. 1% Cross Modulation Distortion Measurement Circuit



TYPICAL CHARACTERISTICS

S-parameter



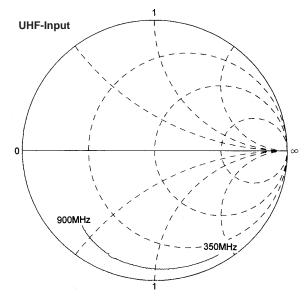


Figure 17

Figure 18

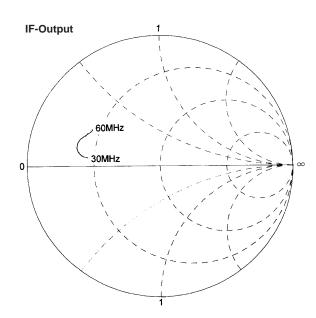


Figure 19

TYPICAL CHARACTERISTICS

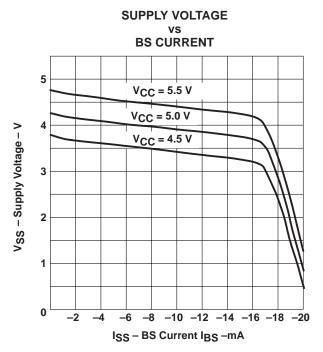


Figure 20. Band Switch Driver Output Voltage





PACKAGE OPTION ADDENDUM

24-Apr-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins P	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN761672ADA	OBSOLETE	TSSOP	DA	32		TBD	Call TI	Call TI	0 to 70	SN761672A	
SN761672ADAR	OBSOLETE	TSSOP	DA	32		TBD	Call TI	Call TI	0 to 70	SN761672A	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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24-Apr-2014

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