ACPL-061L, ACPL-C61L and ACNW261L

Ultra Low Power 10 MBd Digital CMOS Optocoupler

Data Sheet

Description

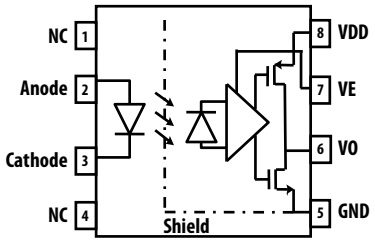
The ACPL-061L/ACPL-C61L/ACNW261L is an optically coupled optocoupler that combines an AlGaAs light emitting diode and an integrated high gain photo detector addresses the low power need. The optocoupler consumes extremely low power, at maximum 1.5 mA I_{DD} per channel across temperature. The forward current is as low as 1.6 mA to 4 mA and allows direct current drive by most microprocessors.

These optocouplers support both 3.3 V and 5 V supply voltage with guaranteed AC and DC operational parameters from temperature range -40° C to +105° C. The output of the detector IC is a CMOS output. An enable input allows the detector output to be strobed. The internal Faraday shield provides a guaranteed common mode transient immunity specification of 20 kV/μs.

The CMOS output is slew-rate controlled and is designed to allow the rise time and fall time to be controlled over a wide range of the load capacitance.

This unique design provides maximum AC and DC circuit isolation while achieving TTL/CMOS compatibility. These optocouplers are suitable for high speed logic interfacing, while consuming extremely low power.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	Z
OFF	L	Z
ON	NC	L
OFF	NC	H

A 0.1 μF bypass capacitor must be connected between pins VDD and GND

Features

- Ultra low current I_{DD} consumption: 1.5 mA max
- Low input current capability: 1.6 mA min (ACPL-061L), 3 mA min (ACPL-C61L), 4 mA min (ACNW261L)
- Available packages: SO-8, Stretched SO-8 and 400 mil widebody
- Built-in slew-rate controlled output
- Tri-state output with enable pin V_E
- Glitch free power-up and power-down
- 20 kV/μs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V
- High Speed: 10 MBd min
- Guaranteed AC and DC performance over wide temperature: -40° C to +105° C
- Safety and Regulatory Approval
  - UL 1577 recognized – 3750 Vrms for 1 minute for ACPL-061L and 5000 Vrms for 1 minute for ACPL-C61L/ACNW261L
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-5 Approval for Reinforced Insulation

Applications

- Communication Interface: RS485, CANBus, I^2C
- Microprocessor System Interfaces
- Digital isolation for A/D, D/A conversion

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-061L is UL Recognized with 3750 V_{rms} for 1 minute per UL1577. ACPL-C61L and ACNW261L are UL Recognized with 5000 V_{rms} for 1 minute per UL1577.

Part number	Option (RoHS Compliant)	Package	Surface Mount	Gull Wing	Tape & Reel	UL 1577 5000 V_{rms} / 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-061L	-000E	SO-8	X					100 per tube
	-060E		X				X	100 per tube
	-500E		X		X			1500 per reel
	-560E		X		X		X	1500 per reel
ACPL-C61L	-000E	Stretched SO-8	X			X		80 per tube
	-060E		X			X	X	80 per tube
	-500E		X		X	X		1000 per reel
	-560E		X		X	X	X	1000 per reel
ACNW261L	-000E	400 mil DIP-8				X	X	42 per tube
	-300E		X	X		X	X	42 per tube
	-500E		X	X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

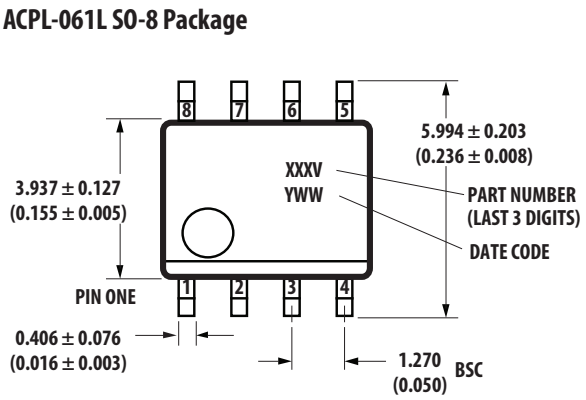
Example 1:

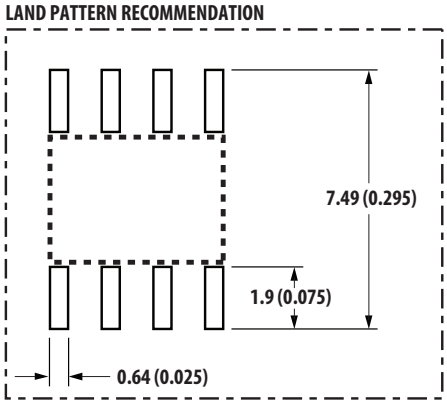
ACPL-061L-560E to order product of Small Outline SO-8 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

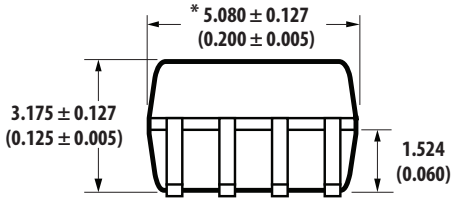
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

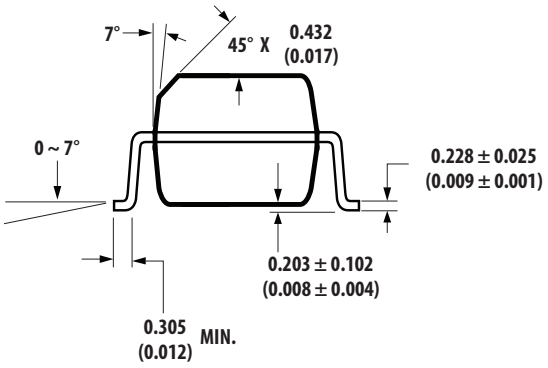
Package Outline Drawing

ACPL-061L SO-8 Package







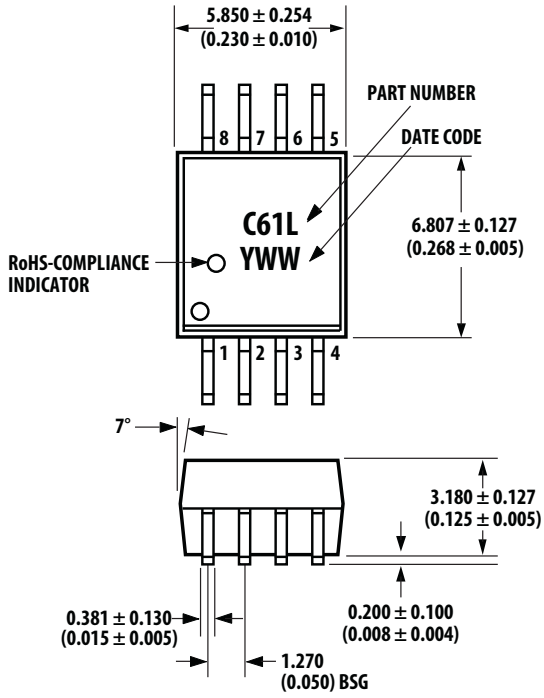


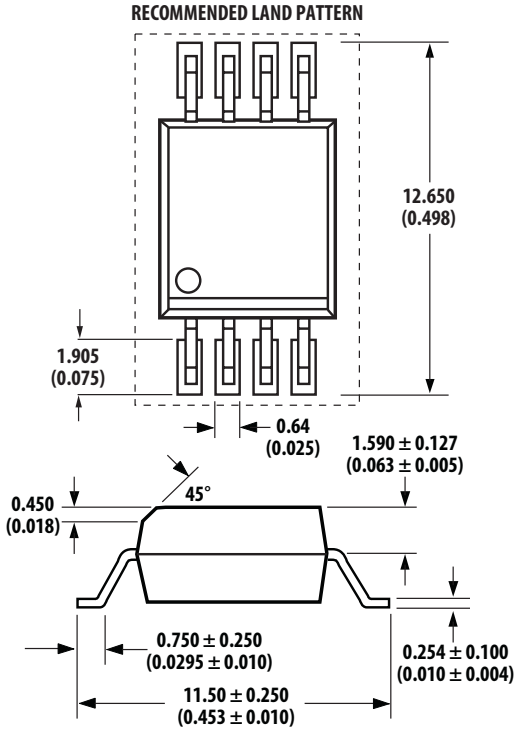
* Total package length (inclusive of mold flash)
5.207 ± 0.254 (0.205 ± 0.010)

Notes:
Lead coplanarity = 0.10 mm (0.004 inches) max.
Floating lead protrusion is 0.15 mm (6 mils) max.
Option number 500 not marked

Dimensions in Millimeters (Inches)

ACPL-C61L Stretched SO-8 Package

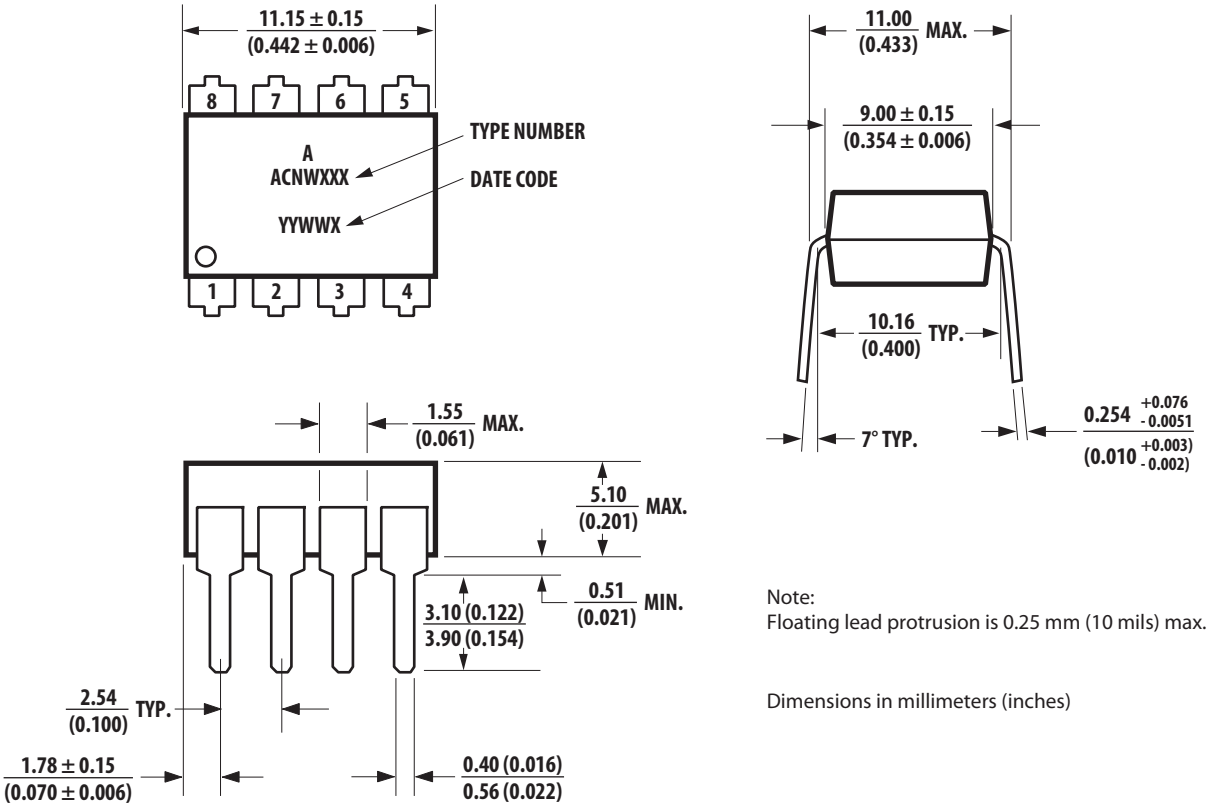




Dimensions in millimeters (inches)

Notes:
Lead coplanarity = 0.1 mm (0.004 inches)
Floating lead protrusion is 0.25mm (10mils) max

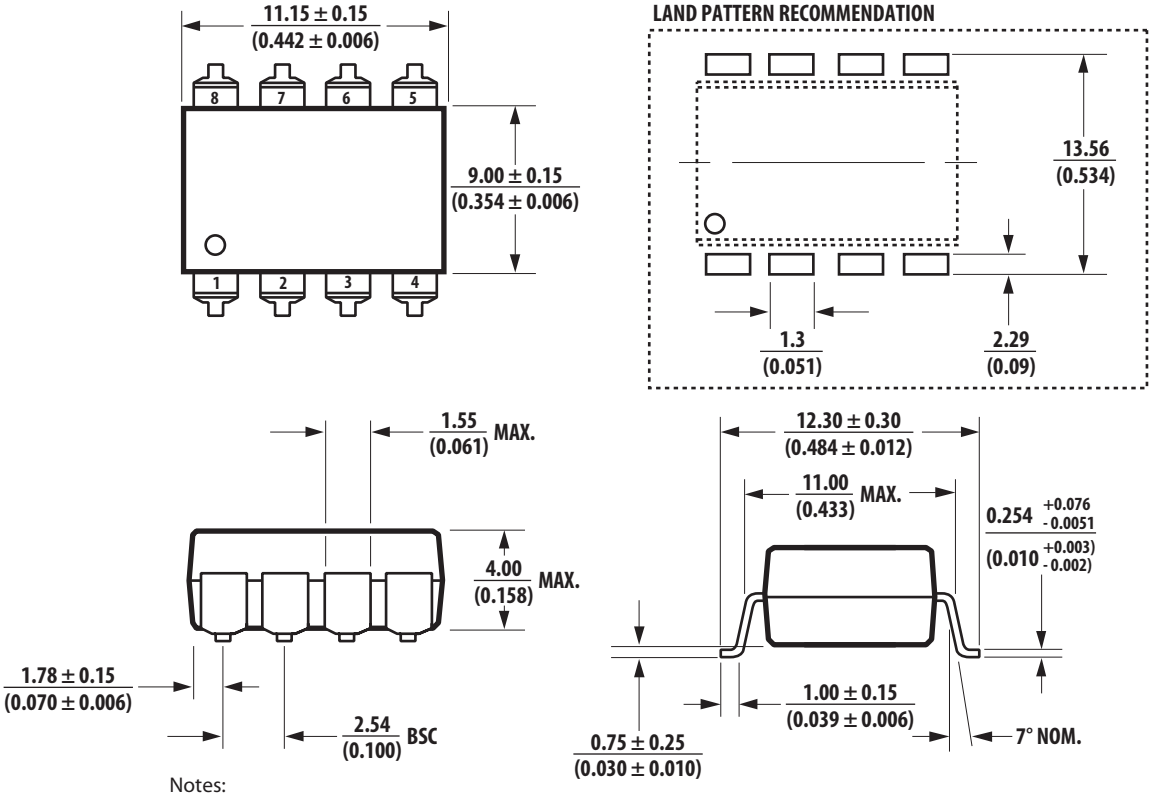
ACNW261L 8-Pin Widebody DIP Package



Note:
Floating lead protrusion is 0.25 mm (10 mils) max.

Dimensions in millimeters (inches)

ACNW261L 8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300E



Notes:
Lead coplanarity = 0.10 mm (0.004 inches)
Floating lead protrusion is 0.25 mm (10 mils) max.

Dimensions in millimeters (inches)

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-061L, ACPL-C61L, ACNW261L and are pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-5 (Option 060E only)

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} for ACPL-061L and V_{ISO} = 5000 V_{RMS} for ACPL-C61L/ACNW261L File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

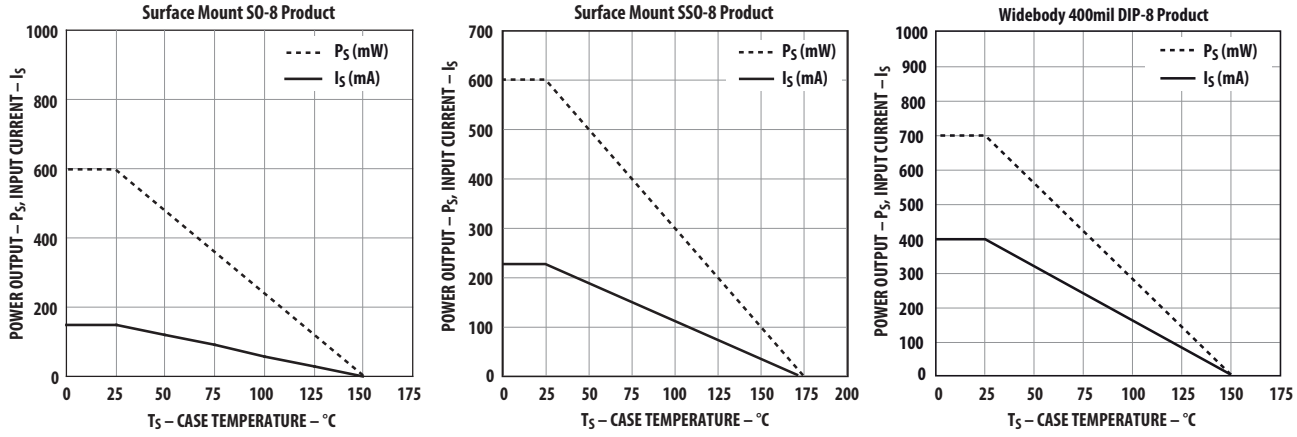
Parameter	Symbol	ACPL-061L	ACPL-C61L	ACNW261L	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	4.9	8	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	4.8	8	10	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.5	1.0	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060)

Description	Symbol	Characteristic			Unit
		ACPL-061L	ACPL-C61L	ACNW261L	
Installation classification per DIN VDE 0110/39, Table 1					
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – III	I – IV	I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – II	I – IV	I – IV	
for rated mains voltage ≤ 1000 V_{rms}			I – III	I – III	
Climatic Classification		55/105/21	55/105/21	55/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	2	
Maximum Working Insulation Voltage	V_{IORM}	567	1414	1414	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1063	2651	2651	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	907	2262	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.					
Case Temperature	T_S	150	175	150	°C
Input Current**	$I_{S, INPUT}$	150	230	400	mA
Output Power**	$P_{S, OUTPUT}$	600	600	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Ambient Temperature	T_A	-40	105	°C	
Reversed Input Voltage	V_R		5	V	
Supply Voltage	V_{DD}		6.5	V	
Average Forward Input Current	I_F	–	8	mA	
Peak Transient Input Current	$I_{F(TRAN)}$	–	1	A	< 1 μs Pulse Width, < 300 pulses per second
			80	mA	< 1 μs Pulse Width, <10% Duty Cycle
Output Current	I_O		10	mA	
Output Voltage	V_O	-0.5	V_{DD} + 0.5	V	
Input Power Dissipation	P_I		14	mW	per channel
Output Power Dissipation	P_O		20	mW	per channel
Lead Solder Temperature	T_{LS}		260°C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile		Refer to Solder Reflow Profile section			

Recommended Operating Conditions

Parameter	Symbol	Part Number	Min	Max	Units
Operating Temperature	T_A		-40	105	°C
Input Current, Low Level	I_{FL}		0	250	μA
Input Current, High Level	I_{FH}	ACPL-061L	1.6	6	mA
		ACPL-C61L	3	8	mA
		ACNW261L	4	8	mA
Power Supply Voltage	V_{DD}		2.7	5.5	V
Forward Input Voltage	$V_{F\ (OFF)}$			0.8	V

Electrical Specifications (DC)

Over recommended temperature (T_A = -40° C to 105° C) and supply voltage (2.7 V ≤ V_{DD} ≤ 5.5 V). All typical specifications are at V_{DD} = 5 V, T_A = 25° C.

Parameter	Symbol	Part Number	Min	Typ	Max	Units	Test Conditions
Input Forward Voltage	V_F	ACPL-061L	0.95	1.3	1.7	V	I_F = 2 mA, Figure 1a, 2a
		ACPL-C61L	1.2	1.5	1.9	V	I_F = 5 mA, Figure 1b, 2b
		ACNW261L	1.2	1.5	1.9	V	I_F = 5 mA, Figure 1b, 2b
Input Reverse Breakdown Voltage	BV_R	ACPL-061L	3	5		V	I_R = 10 μA
		ACPL-C61L	7	10		V	I_R = 10 μA
		ACNW261L	7	10		V	I_R = 10 μA
Logic High Output Voltage	V_{OH}		V_{DD} - 0.1	V_{DD}		V	I_F = 0 mA, VI = 0 V, I_O = -20 μA
			V_{DD} - 1.0	V_{DD}		V	I_F = 0 mA, VI = 0 V, I_O = -3.2mA
Logic Low Output Voltage	V_{OL}			0.03	0.1	V	I_F = 2 mA, VI = 5 V/3.3 V, I_O = 20 μA
				0.18	0.4	V	I_F = 2 mA, VI = 5 V/3.3 V, I_O = 3.2 mA
Input Threshold Current	I_{TH}	ACPL-061L		0.7	1.3	mA	Figure 3a
		ACPL-C61L		1.5	2.2	mA	Figure 3b
		ACNW261L		1.5	3	mA	Figure 3b
Logic Low Output Supply Current	I_{DDL}			0.8	1.5	mA	Figure 4
Logic High Output Supply Current	I_{DDH}			0.8	1.5	mA	Figure 5
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V
High Level Enable Current	I_{EH}			-0.7	-1.6	mA	V_{DD} = 5.5 V, V_E = 3.0 V
Low Level Enable Current [4]	I_{EL}			-0.9	-1.6	mA	V_{DD} = 5.5 V, V_E = 0.5 V
High Level Enable Voltage [10]	V_{EH}		0.7 x V_{DD}			V	3.0 V ≤ V_{DD} ≤ 5.5 V
Low Level Enable Voltage [10]	V_{EL}				0.3 x V_{DD}	V	3.0 V ≤ V_{DD} ≤ 5.5 V
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	ACPL-061L		-1.6		mV/°C	I_F = 2 mA
		ACPL-C61L		-1.9		mV/°C	I_F = 3 mA
		ACNW261L		-1.9		mV/°C	I_F = 5 mA

Switching Specifications (AC)

Over recommended temperature (T_A = -40° C to +105° C), supply voltage (2.7 V ≤ V_{DD} ≤ 5.5 V). All typical specifications are at V_{DD} = 5 V, T_A = 25° C

Parameter	Symbol	Part Number	Min	Typ	Max	Units	Test Conditions
Propagation Delay Time to Logic Low Output [1]	t_{PHL}	ACPL-061L		46	80	ns	I_F = 2 mA, V_I = 5 V, R_T = 1.68 kΩ, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic High Output [1]	t_{PLH}			40	80	ns	I_F = 2 mA, V_I = 3.3 V, R_T = 870 Ω, C_L= 15 pF, CMOS Signal Levels. Figure 6a, 7a
Pulse Width	t_{PW}		100			ns	
Pulse Width Distortion [2]	PWD			6	30	ns	
Propagation Delay Skew [3]	t_{PSK}				30	ns	
Output Rise Time (10% – 90%)	t_R			12		ns	I_F = 2 mA, V_I = 5 V, R_T = 1.68 kΩ, C_L= 15 pF, CMOS Signal Levels.
				10		ns	I_F = 2 mA, V_I = 3.3 V, R_T = 870 Ω, C_L= 15 pF, CMOS Signal Levels.
Output Fall Time (90% – 10%)	t_F			12		ns	I_F = 2 mA, V_I = 5 V, R_T = 1.68 kΩ, C_L= 15 pF, CMOS Signal Levels.
				10		ns	I_F = 2 mA, V_I = 3.3 V, R_T = 870 Ω, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic Low Output [1]	t_{PHL}	ACPL-C61L		47	90	ns	I_F = 5 mA, V_I = 5 V, R_T = 680 Ω, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic High Output [1]	t_{PLH}			38	90	ns	I_F = 5 mA, V_I = 3.3 V, R_T = 340 Ω, C_L= 15 pF, CMOS Signal Levels. Figure 6b, 7b
Pulse Width	t_{PW}		100			ns	
Pulse Width Distortion [2]	PWD			9	40	ns	
Propagation Delay Skew [3]	t_{PSK}				30	ns	
Output Rise Time (10% – 90%)	t_R			12		ns	I_F = 5 mA, V_I = 5 V, R_T = 680 Ω, C_L= 15 pF, CMOS Signal Levels.
				10		ns	I_F = 5 mA, V_I = 3.3 V, R_T = 340 Ω, C_L= 15 pF, CMOS Signal Levels.
Output Fall Time (90% - 10%)	t_F			12		ns	I_F = 5 mA, V_I = 5 V, R_T = 680 Ω, C_L= 15 pF, CMOS Signal Levels.
				10		ns	I_F = 5 mA, V_I = 3.3 V, R_T = 340 Ω, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic Low Output [1]	t_{PHL}	ACNW261L		66	95	ns	I_F = 5 mA, V_I = 5 V, R_T = 680 Ω, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic High Output [1]	t_{PLH}			47	95	ns	I_F = 5 mA, V_I = 3.3 V, R_T = 340 Ω, C_L= 15 pF, CMOS Signal Levels. Figure 6c, 7c
Pulse Width	t_{PW}		100			ns	
Pulse Width Distortion [2]	PWD			19	40	ns	
Propagation Delay Skew [3]	t_{PSK}				30	ns	
Output Rise Time (10% – 90%)	t_R			12		ns	I_F = 5 mA, V_I = 5 V, R_T = 680 Ω, C_L= 15 pF, CMOS Signal Levels.
				10		ns	I_F = 5 mA, V_I = 3.3 V, R_T = 340 Ω, C_L= 15 pF, CMOS Signal Levels.
Output Fall Time (90% - 10%)	t_F			12		ns	I_F = 5 mA, V_I = 5 V, R_T = 680 Ω, C_L= 15 pF, CMOS Signal Levels.
				10		ns	I_F = 5 mA, V_I = 3.3 V, R_T = 340 Ω, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time of Enable from V_{EH} to V_{EL} [5]	t_{ELH}			9		ns	V_{EL} = 0 V, V_{EH} = 3 V, C_L= 15 pF Figure 8
Propagation Delay Time of Enable from V_{EL} to V_{EH} [6]	t_{EHL}			12		ns	

Switching Specifications (AC) (Continued)

Parameter	Symbol	Part Number	Min	Typ	Max	Units	Test Conditions
Static Common Mode Transient Immunity at Logic High Output [7]	$\|CM_H\|$	ACPL-061L	20	35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 0 mA, V_I = 0V, C_L= 15 pF, CMOS Signal Levels. Figure 9
Static Common Mode Transient Immunity at Logic Low Output [8]	$\|CM_L\|$		20	35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 2 mA, V_I = 5 V/3.3 V, C_L= 15 pF, CMOS Signal Levels. Figure 9
Dynamic Common Mode Transient Immunity [9]	CMR_D			35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 2 mA, V_I = 5 V/3.3 V, 10 MBd data rate, the absolute increase of PWD <10 ns. Figure 9
Static Common Mode Transient Immunity at Logic High Output [7]	$\|CM_H\|$	ACPL-C61L	20	35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 0 mA, V_I = 0 V, C_L= 15 pF, CMOS Signal Levels. Figure 9
Static Common Mode Transient Immunity at Logic Low Output [8]	$\|CM_L\|$		20	35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 5 mA, V_I = 5 V/3.3 V, C_L= 15 pF, CMOS Signal Levels.
Dynamic Common Mode Transient Immunity [9]	CMR_D			35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 5 mA, V_I = 5 V/3.3 V, 10 MBd datarate, the absolute increase of PWD <10 ns. Figure 9
Static Common Mode Transient Immunity at Logic High Output [7]	$\|CM_H\|$	ACNW261L	20	35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 0 mA, V_I = 0 V, C_L= 15 pF, CMOS Signal Levels. Figure 9
Static Common Mode Transient Immunity at Logic Low Output [8]	$\|CM_L\|$		20	35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 5 mA, V_I = 5 V/3.3 V, C_L= 15pF, CMOS Signal Levels. Figure 9
Dynamic Common Mode Transient Immunity [9]	CMR_D			35		kV/µs	V_{CM} = 1000 V, T_A = 25° C, I_F = 5 mA, V_I = 5 V/3.3 V, 10 MBd datarate, the absolute increase of PWD <10 ns. Figure 9

Package Characteristics

All typical at T_A = 25° C.

Parameter	Symbol	Part Number	Min	Typ	Max	Units	Test Conditions
Input-Output Insulation	V_{ISO}	ACPL-061L	3750			V_{rms}	RH < 50% for 1 min. T_A = 25° C
		ACPL-C61L ACNW261L	5000				
Input-Output Resistance	R_{I-O}			10^{12}		W	V_{I-O} = 500 V
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz, T_A = 25° C

Notes:

1. t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
4. The JEDEC registration for the ACPL-061L/ACPL-C61L/ACNW261L specifies a maximum I_{EL} of -2.0 mA. Avago guarantees a maximum I_{EL} of -1.6 mA.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.
9. CM_D is the maximum tolerable rate of the common mode voltage during data transmission to assure that the absolute increase of the PWD is less than 10 ns.
10. When V_E pin is not used, connects V_E to V_{DD} will result in improved CMR performance.

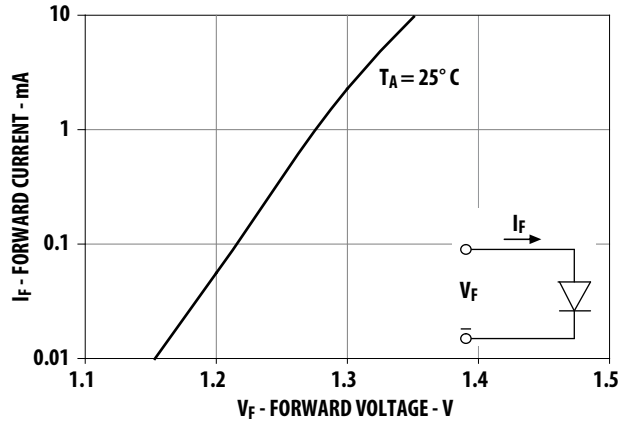


Figure 1a. Typical input diode forward characteristic (ACPL-061L)

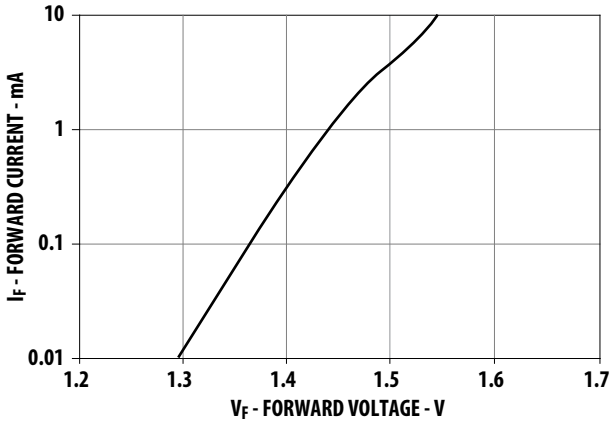


Figure 1b. Typical input diode forward characteristic (ACPL-C61L/ACNW261L)

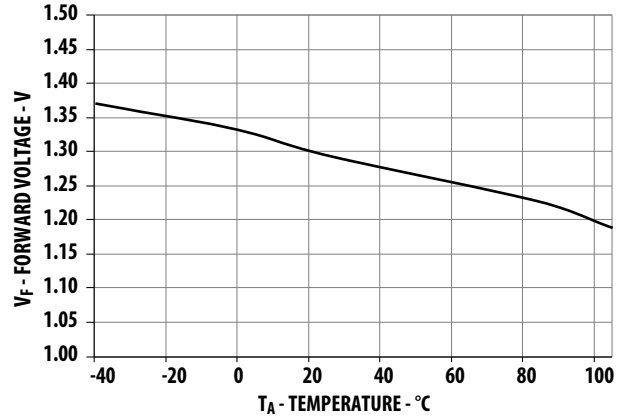


Figure 2a. Typical V_F versus temperature (ACPL-061L)

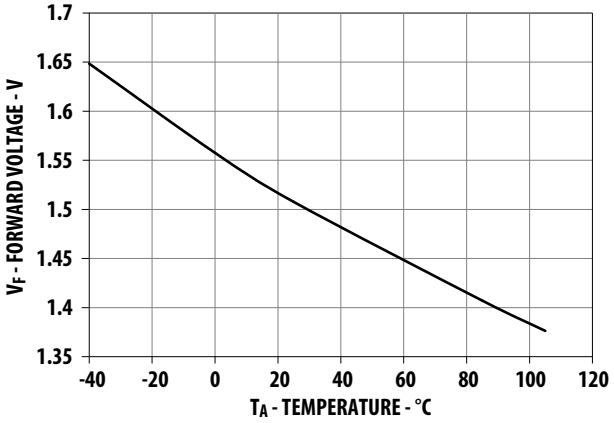


Figure 2b. Typical V_F versus temperature (ACPL-C61L/ACNW261L)

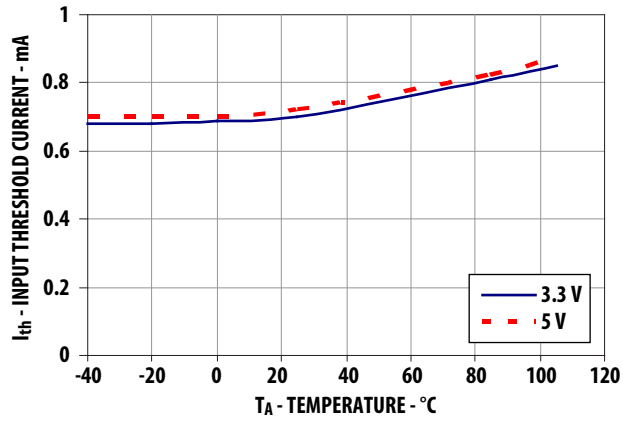


Figure 3a. Typical input threshold current I_{TH} versus temperature (ACPL-061L)

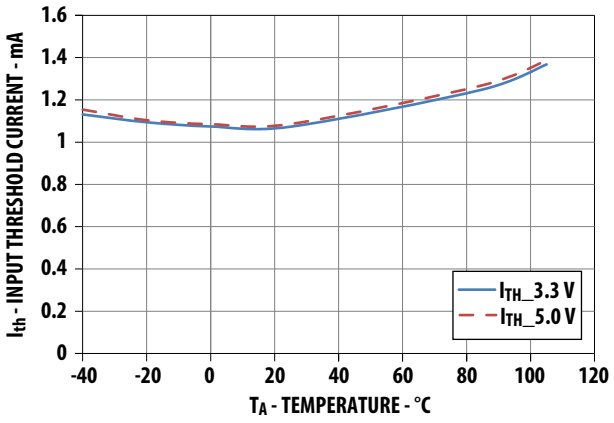


Figure 3b. Typical input threshold current I_{TH} versus temperature (ACPL-C61L/ACNW261L)

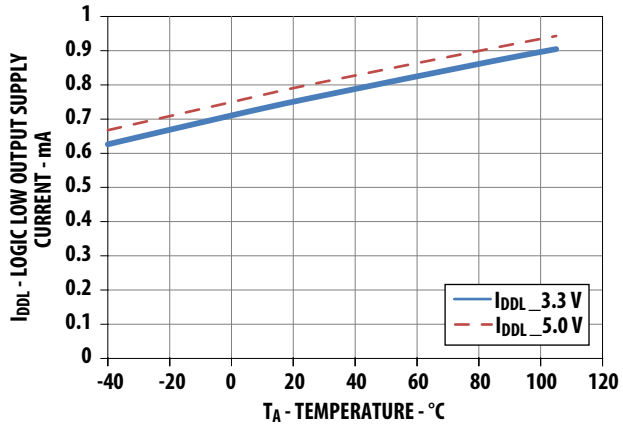


Figure 4. Typical logic low output supply current I_{DDL} versus temperature

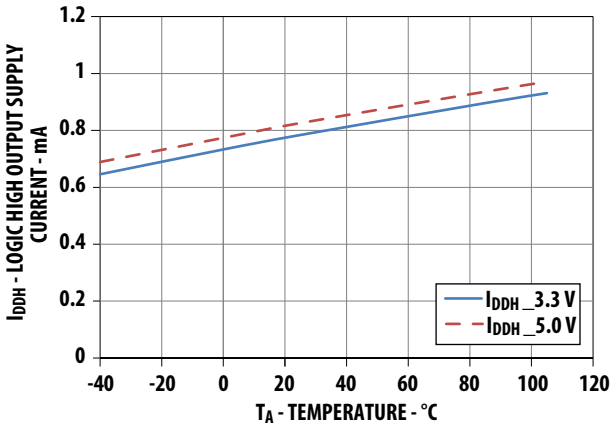


Figure 5. Typical logic high output supply current I_{DDH} versus temperature

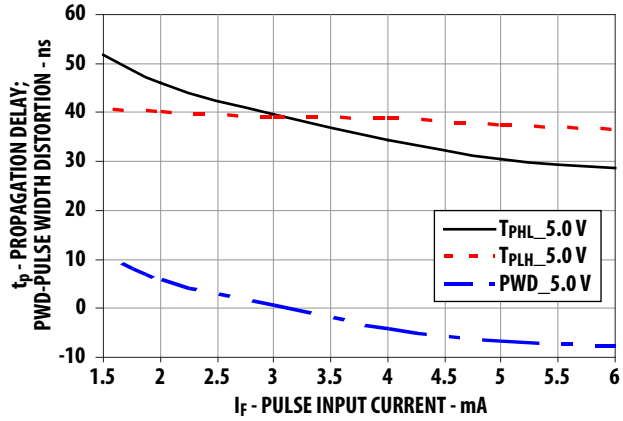


Figure 6a. Typical switching speed versus pulse input current at 5 V supply voltage (ACPL-061L)

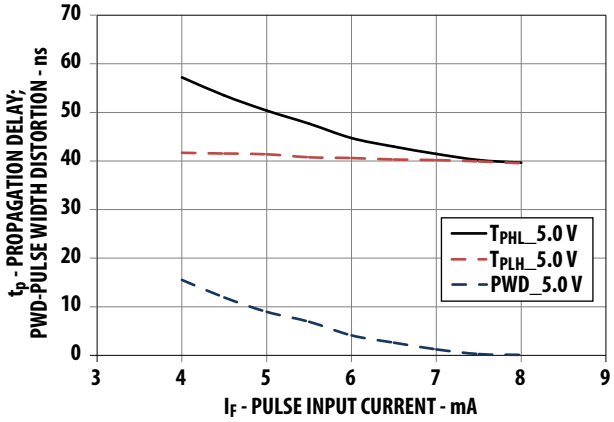


Figure 6b. Typical switching speed versus pulse input current at 5 V supply voltage (ACPL-C61L)

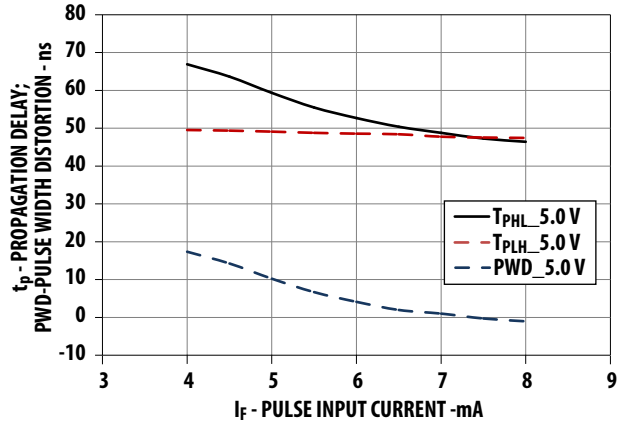


Figure 6c. Typical switching speed versus pulse input current at 5 V supply voltage (ACNW261L)

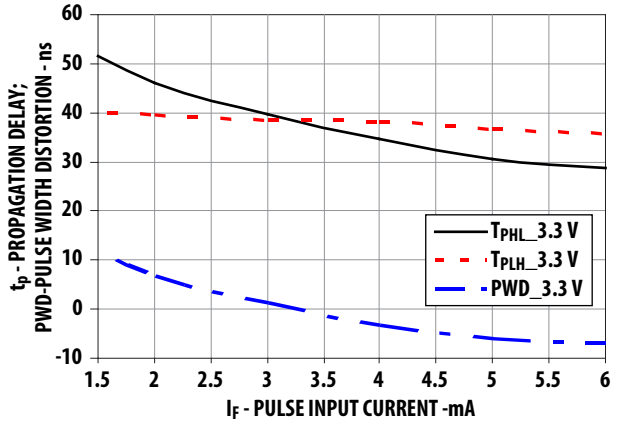


Figure 7a. Typical switching speed versus pulse input current at 3.3 V supply voltage (ACPL-061L)

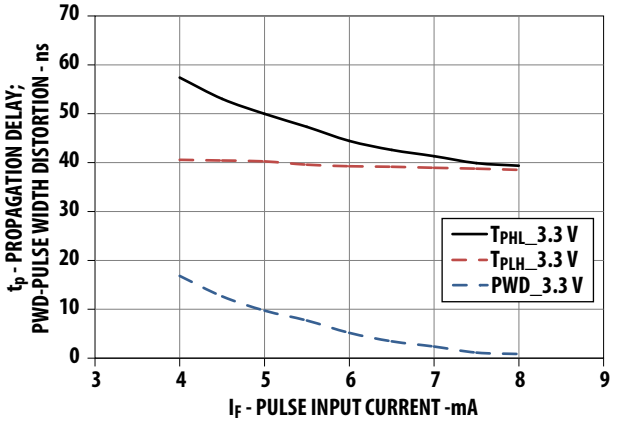


Figure 7b. Typical switching speed versus pulse input current at 3.3 V supply voltage (ACPL-C61L)

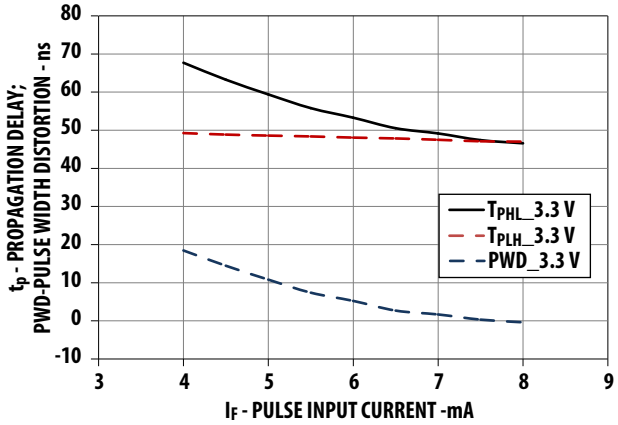


Figure 7c. Typical switching speed versus pulse input current at 3.3 V supply voltage (ACNW261L)

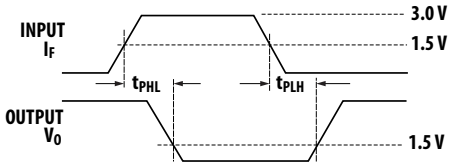


Figure 8. Timing diagrams for t_{EHL} and t_{ELH}

Bypassing and PC Board Layout

The ACPL-061L/ACPL-C61L/ACNW261L optocouplers are extremely easy to use. ACPL-061L/ACPL-C61L/ACNW261L provide CMOS logic output due to the high-speed CMOS IC technology used.

The external components required for proper operation are the input limiting resistors and the output bypass capacitor. Capacitor values should be 0.1 μF.

For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 9).

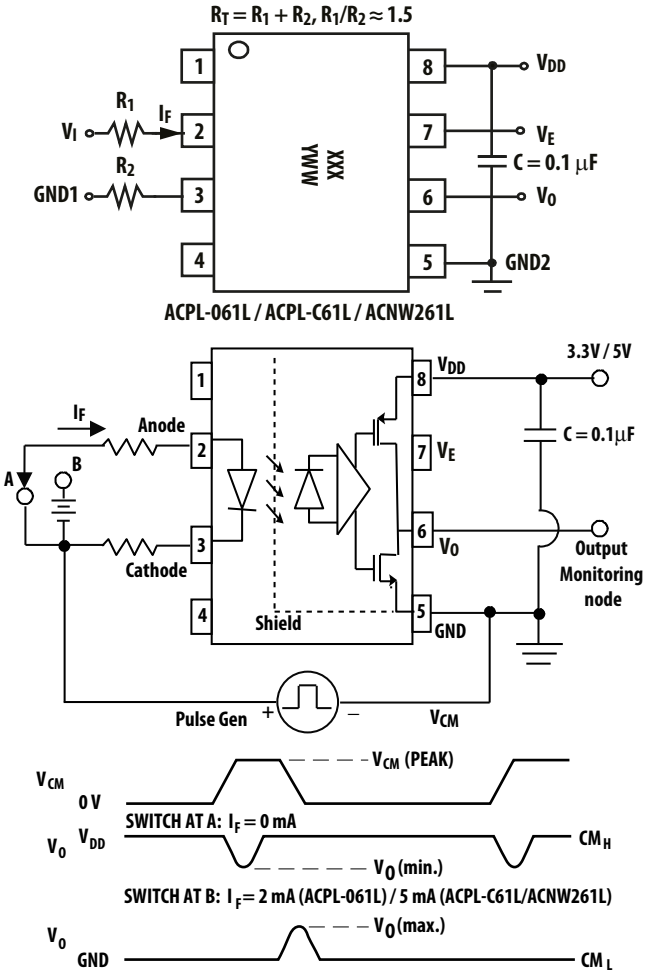


Figure 9. Recommended printed circuit board layout

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often PWD is defined as the difference between t_{PLH} and t_{PHL}. This parameter determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD in the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation

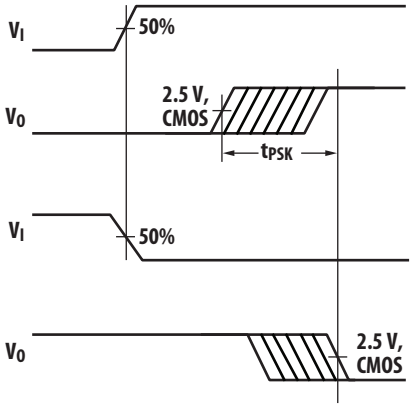


Figure 10. Propagation delay skew waveform

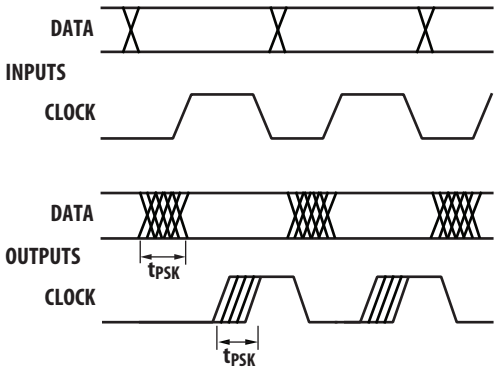


Figure 11. Parallel data transmission example

delay, either t_{PLH} or t_{PHL}. As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate.

Figure 10 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 10 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

Optocoupler CMR performance

The principal protection against common mode noise comes down to the fundamental isolation properties of the optocoupler, this in turn is directly related to the input-output leakage capacitance of the optocoupler.

To provide maximum protection to circuitry connected to the input or output of the optocoupler the leakage capacitance is minimized by having large separation distances at all points in the optocoupler construction, including the LED/photodiode interface.

In addition to the constructional design, additional circuit design steps are taking to further mitigate the effects of common mode noise. The most important of these is the use of a Faraday shield on the photodetector stage. This faraday shield is effective in optocouplers because the internal modulation frequency (light) is many orders of magnitude higher than the common mode noise frequency.

Application level CMR Performance

In application, it desirable that the optocoupler's common mode isolation perform as close as possible to that indicated in the data sheets specifications.

The first step in meeting this goal is to ensure maintaining maximum separation between PCB interconnects on either side of the optocoupler and avoid routing tracks beneath the optocoupler. Nonetheless, it is inevitable that a certain amount of CMR noise will be coupled into the inputs which can potentially result in false-triggering of the input.

This problem is frequently observed in devices with input high input impedence such as CMOS buffered inputs in either optocoupler or alternate isolator technologies. In some cases, this not only causes momentary missing pulses but in some technologies may even cause input circuitry to latch-up.

ACPL-061L/ACPL-C61L/ACNW261L optocoupler family does not face input latch up issue even at very high CMR levels, such as those experienced in end equipment level tests (for example IEC61004-4-4) due to the simple diode structure of the LED.

In some cases achieving the rated data sheet CMR performance levels is not possible in the intended application, often because of the practical need to actually connect the isolator input to the output of a dynamically changing signal rather than tying the input statically to VDD1 or GND1.

This specsmanship issue is often observable with alternative isolators utilizing AC encoding techniques.

To address this requirement for clear transparency on the achievable end application performance, the ACPL-061L/ACPL-C61L/ACNW261L series of optocouplers includes an additional typical performance indication of the dynamic CMR in the electrical parameter table. What this information indicates is the achievable CMR performance whilst the input is being toggled on or off during the occurrence of a CMR transient. The logic output of the optocoupler is mainly controlled by the level of the LED current due to the short transition rise/fall time of the LED current (approximately 10ns), the dynamic noise immunity is essentially the same as the static noise immunity.

To achieve this goal of meeting the maximum inherent CMR capabilities of the ACPL-061L/ACPL-C61L/ACNW261L family, some simple consideration needs to be given to the operation of the LED at the application level.

In particular ensuring that the LED stays either on or off during a CMR transient.

Some common design techniques which are sometimes used to meet this goal:

Keeping LED On:

i) Overdrive the LED with a higher than required forward current.

Keeping LED Off:

i) Reverse bias the LED during the off state.
ii) Minimize the off state impedance across the anode and cathode of the LED during the off state.

All these methods are fully capability of enabling the full CMR capabilities off the ACPL-061L/ACPL-C61L/ACNW261L family to be achieved. But they do come at the cost of practical implementation issues or a compromise on power consumption.

An effective method to meet the goal of maintaining the LED status during a CMR event with no other design compromises other the addition of a single low cost component (resistor).

This CMR optimization method fundamentally makes use of the differential input capability of the LED input. By ensuring the common mode impedance on both the cathode and anode of the LED are balanced, it effectively nullifies the effect of a CMR transient on the LED. This is most easily achieved by splitting the input bias resistor into two (as shown in Figure 9).

Split resistor configuration for ACPL-061L/ACPL-C61L/ ACNW261L

Figure 12 shows the recommended drive circuit for the ACPL-061L/ACPL-C61L/ACNW261L for optimal common-mode rejection performance. Two LED-current setting resistors are used to balance the common mode impedance at LED anode and cathode. Common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure12 shows the parasitic capacitances which exists between LED anode/ cathode and output ground (C_{LA} and C_{LC}).

Table 1 indicates the directions of I_{LP} and I_{LN} flow depending on the direction of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CML, since the output is in the "low" state) depends upon the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CML also depends on the extent which I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in IF (i.e. when $dV_{CM}/dt>0$ and $|I_{FP}| > |I_FN|$, referring to Table 1) will cause common-mode failure for transients which are fast enough.

Likewise for common-mode transients which occur when the LED is off (i.e. CM_H, since the output is "high"), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike below 2 V (which constitutes a CM_H failure).

The balanced I_{LED}-setting resistors help equalize the common mode voltage change at anode and cathode to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}.

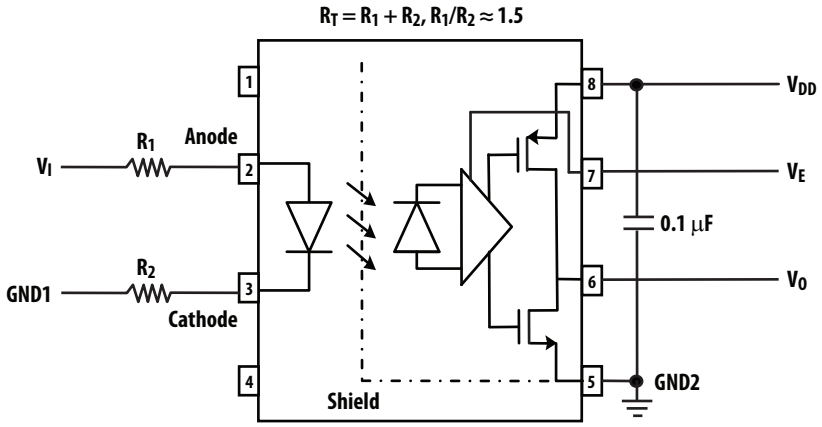


Figure 12. Recommended drive circuit for ACPL-061L/ACPL-C61L/ACNW261L for high-CMR

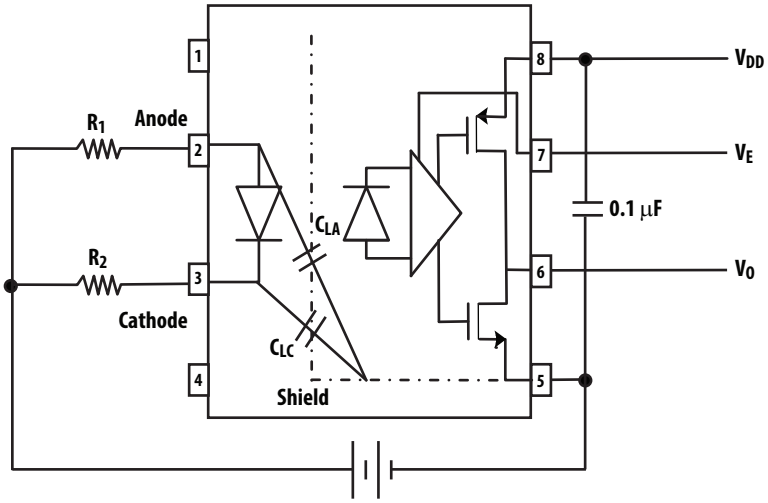


Figure 13. AC equivalent of ACPL-061L/ACPL-C61L/ACNW261L

Table 1. Effects of Common Mode Pulse Direction on Transient I_{LED}

If dV_{CM}/dt Is:	then I_{LP} Flows:	and I_{LN} Flows:	If $\|I_{LP}\| < \|I_{LN}\|$, LED I_F Current Is Momentarily:	If $\|I_{LP}\| > \|I_{LN}\|$, LED I_F Current Is Momentarily:
positive (>0)	away from LED anode through C_{LA}	away from LED cathode through C_{LC}	increased	decreased
negative (<0)	toward LED anode through C_{LA}	toward LED cathode through C_{LC}	decreased	increased

Glitch free power-up and power-down

Upon power-up or power-down of the optocoupler, glitches produced in the output are undesirable. Glitches can lead to false data in the optocoupler application. ACPL-061L/ACPL-C61L/ACNW261L has a feature that holds the output in a known state until VDD is at a safe level. Figure 14 and 15 show typical output waveforms during power-up and power-down.

Slew-rate controlled output

Typically, the output slew rate (rise and fall time) will vary with the output load, as more time is needed to charge up the higher load. The propagation delay and the PWD will increase with the load capacitance. This will be an issue especially in parallel communication because different communication line will have different load capacitances. However, ACPL-061L/ACPL-C61L/ACNW261L has built in slew-rate controlled feature, to ensure that the output rise and fall time remain stable across wide load capacitance.

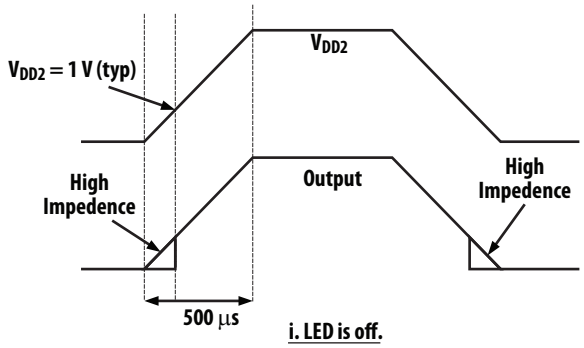


Figure 14. V_{DD} Ramp when LED is off.

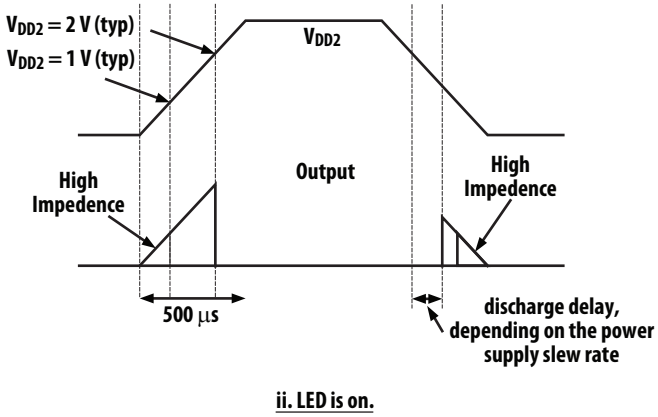


Figure 15. V_{DD} Ramp when LED is on.

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