S6AP413A

ASSP
4CH DCDC converter with I^2C interface and internal SW FETs

Data Sheet (Preliminary)

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications.

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S6AP413A

ASSP
4CH DCDC converter internal switching FETs

Data Sheet (Preliminary)

1. Description

S6AP413A contains 4ch buck DC/DC converter and 1ch buck-boost DC/DC converter. S6AP413A can supply the main power line in several systems by using only its chip. The current mode control is adopted for the DC/DC converter, and it is possible to use the small chip inductor with the high switching frequency operation which contains internal switching FETs. S6AP413A contains the output setting resistor and the phase compensation circuit, and contributes to reduce the number of external components and its mount area. Also it contains the CTL input pin which can control the ON/OFF for each DC/DC converter, the Power Good signal output pin and I^2C communication interface, therefore it is easy to design the power supply sequence. It is possible to tune in the output voltage exactly using the I^2C communication.

2. Features

- Operating input voltage range: 2.5V to 5.5V (Maximum rating: 6.5V)
- Output voltage setting range: DD1*:0.7V to 1.32V (20mV/step)
  DD2*:1.2V to 1.95V (50mV/step)
  DD3*:2.8V to 3.5V (100mV/step)
  DD4*:0.7V to 1.32V (20mV/step)
- Maximum output current: DD1:2A, DD2:1.2A, DD3:0.6A, DD4:2A
- Internal switching FETS, output voltage setting resistor, phase compensation circuit and output discharge resistor (all DC/DC converters)
- Buck-boost DC/DC converter is seamless to change operation mode
- Soft start time setting range: 1 ms to 16 ms (approximately 1ms/step)
- Switching frequency for the DC/DC converter: 3 MHz
- Communication interface: I^2C (ON/OFF, Output voltage, Soft start time)
- Internal PFM/PWM auto switching mode
- Each DC/DC converter Power Good function (open drain)
- Several protection functions: Under voltage lockout (UVLO), Over current protection (OCP), Thermal shut down (TSD)
- Small package: QFN32 (5mm × 5mm × 0.71mm, 0.5mm pitch)

*: DD1,DD2,DD3,DD4 : DC/DC converter block 1,2,3,4

3. Application

Network equipment, Factory automation, Security system, Surveillance camera, Electrical music instrument, Multi-function printer, Scanner, Printer, Copy machine, Home appliances ,Data storage (HDD, SSD), Mobile equipment for Li+ battery (1 cell)

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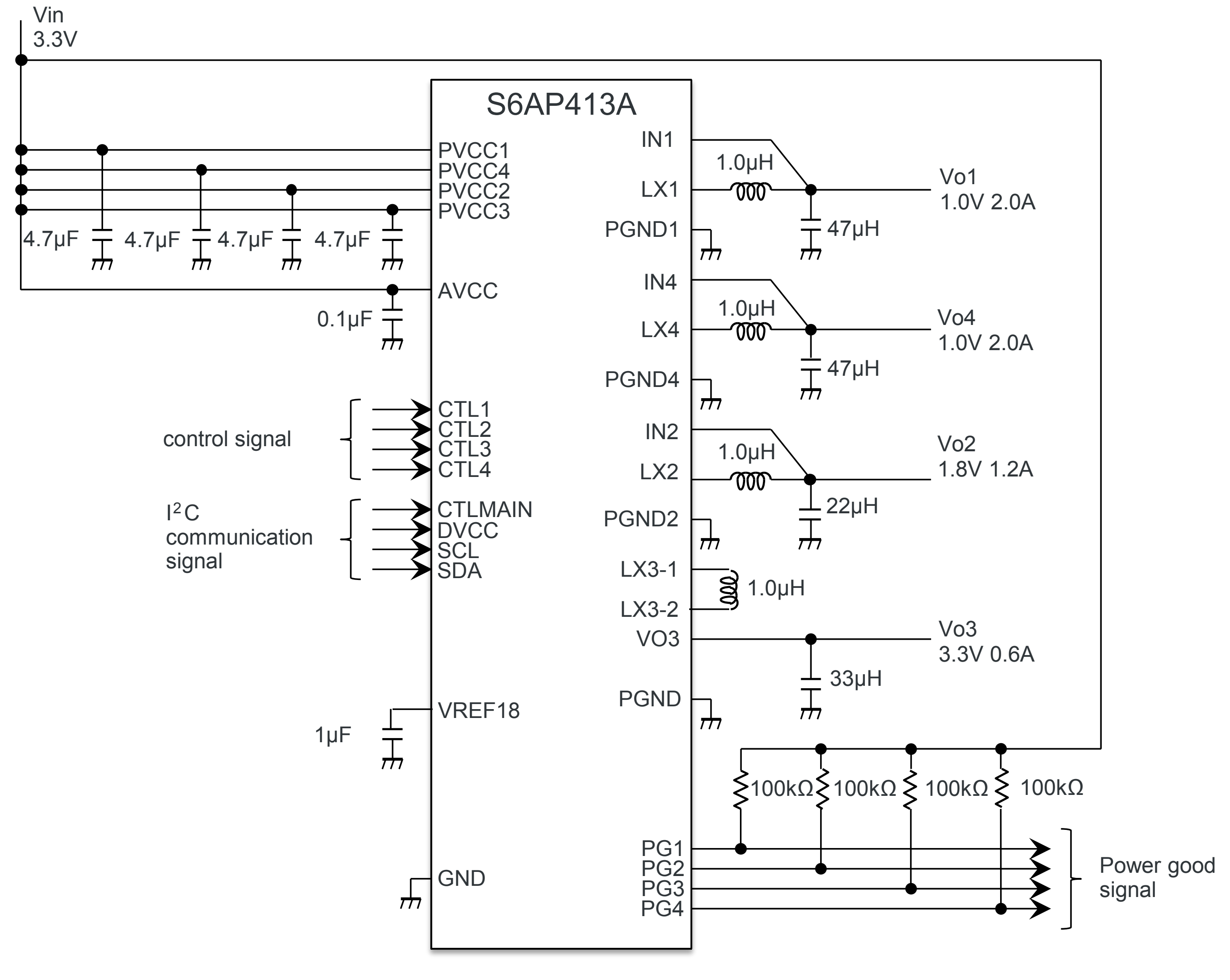
4. Application Circuit Example

Figure 4-1 Application Circuit



5. Recommended Application Specification

[Input Voltage Range]

Input voltage Vin(V)		
Min	**Typ**	**Max**
2.5	3.3	5.5

[Output specification]

(Ta=+25°C)

Channel	Symbol	Accuracy	Output Voltage (V)			Output Current (mA)	Limit Current (mA)	Mode	Switching frequency (MHz)	Inductor (μH)	Output capacitance	Soft-start time (ms)	Discharge resistance (kΩ)	Remarks
			Min	**Typ**	**Max**	**Max**	**Min**							
DD1	VO1	±1.2%	0.692	0.700	0.708	2000	(2400)	Buck (synchronous rectification) C-mode	3.0	1.0	22	1 to 16ms At the time of 1.0V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			0.711	0.720	0.729									
			0.731	0.740	0.749									
			0.751	0.760	0.769									
			0.771	0.780	0.789									
			0.790	0.800	0.810									
			0.810	0.820	0.830									
			0.830	0.840	0.850									
			0.850	0.860	0.870									
			0.869	0.880	0.891									
			0.889 (*1)	0.900 (*1)	0.911 (*1)									
			0.909	0.920	0.931									
			0.929	0.940	0.951									
			0.948	0.960	0.972									
			0.968	0.980	0.992									
			0.988 (*1)	1.000 (*1)	1.012 (*1)									
			1.008	1.020	1.032									
			1.028	1.040	1.052									
			1.047	1.060	1.073									
			1.067	1.080	1.093									
			1.087 (*1)	1.100 (*1)	1.113 (*1)									
			1.107	1.120	1.133									
			1.126	1.140	1.154									
			1.146	1.160	1.174									
			1.166	1.180	1.194									
			1.186 (*1)	1.200 (*1)	1.214 (*1)									
			1.205	1.220	1.235									
			1.225	1.240	1.255									
			1.245	1.260	1.275									
			1.265	1.280	1.295									
			1.284	1.300	1.316									
			1.304	1.320	1.336									

*1: default

(It is selectable with the default output voltage)

Channel	Symbol	Accuracy	Output Voltage (V)			Output Current (mA)	Limit Current (mA)	Mode	Switching frequency (MHz)	Inductor (µH)	Output capacitance	Soft-start time (ms)	Discharge resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD2	VO2	±1.2%	1.186 (*1)	1.200 (*1)	1.214 (*1)	1200	(1500)	Buck (synchronous rectification) C-mode	3.0	1.0	10	1 to 16ms At the time of 1.8V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			1.235	1.250	1.265									
			1.284	1.300	1.316									
			1.334 (*1)	1.350 (*1)	1.366 (*1)									
			1.383	1.400	1.417									
			1.433	1.450	1.467									
			1.482 (*1)	1.500 (*1)	1.518 (*1)									
			1.531	1.550	1.569									
			1.581	1.600	1.619									
			1.630	1.650	1.670									
			1.680	1.700	1.720									
			1.729	1.750	1.771									
			1.778 (*1)	1.800 (*1)	1.822 (*1)									
			1.828	1.850	1.872									
			1.877	1.900	1.923									
			1.927	1.950	1.973									
DD3	VO3	±1.8%	2.74 (*1)	2.80 (*1)	2.86 (*1)	600	(750)	Buck-Boost (synchronous rectification) C-mode	3.0	1.0	22	1 to 16ms At the time of 3.3V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			2.84	2.90	2.96									
			2.94 (*1)	3.00 (*1)	3.06 (*1)									
			3.04	3.10	3.16									
			3.14	3.20	3.26									
			3.23 (*1)	3.30 (*1)	3.37 (*1)									
			3.33	3.40	3.47									
			3.43 (*1)	3.50 (*1)	3.57 (*1)									

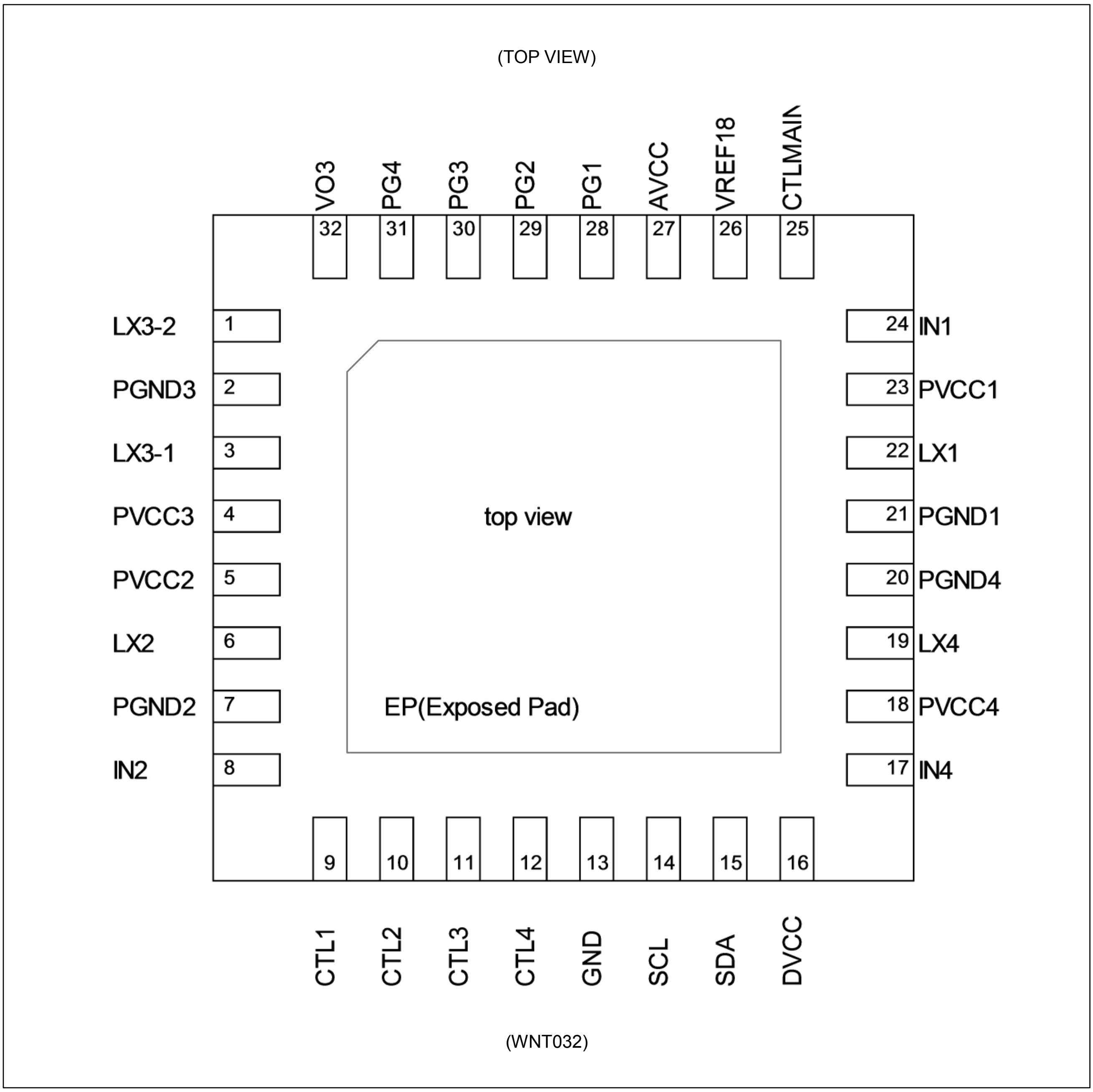
*1: default
(It is selectable with the default output voltage)

Channel	Symbol	Accuracy	Output Voltage (V)			Output Current (mA)	Limit Current (mA)	Mode	Switching frequency (MHz)	Inductor (µH)	Output capacitance	Soft-start time (ms)	Discharge resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD4	VO4	±1.2%	0.692	0.700	0.708	2000	(2400)	Buck (synchronous rectification) C-mode	3.0	1.0	22	1 to 16ms At the time of 1.8V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compen sation circuit
			0.711	0.720	0.729									
			0.731	0.740	0.749									
			0.751	0.760	0.769									
			0.771	0.780	0.789									
			0.790	0.800	0.810									
			0.810	0.820	0.830									
			0.830	0.840	0.850									
			0.850	0.860	0.870									
			0.869	0.880	0.891									
			0.889 (*1)	0.900 (*1)	0.911 (*1)									
			0.909	0.920	0.931									
			0.929	0.940	0.951									
			0.948	0.960	0.972									
			0.968	0.980	0.992									
			0.988 (*1)	1.000 (*1)	1.012 (*1)									
			1.008	1.020	1.032									
			1.028	1.040	1.052									
			1.047	1.060	1.073									
			1.067	1.080	1.093									
			1.087 (*1)	1.100 (*1)	1.113 (*1)									
			1.107	1.120	1.133									
			1.126	1.140	1.154									
			1.146	1.160	1.174									
			1.166	1.180	1.194									
			1.186 (*1)	1.200 (*1)	1.214 (*1)									
			1.205	1.220	1.235									
			1.225	1.240	1.255									
			1.245	1.260	1.275									
			1.265	1.280	1.295									
			1.284	1.300	1.316									
			1.304	1.320	1.336									

*1: default
(It is selectable with the default output voltage)

6. Pin Configuration

Figure 6-1 Pin Configuration



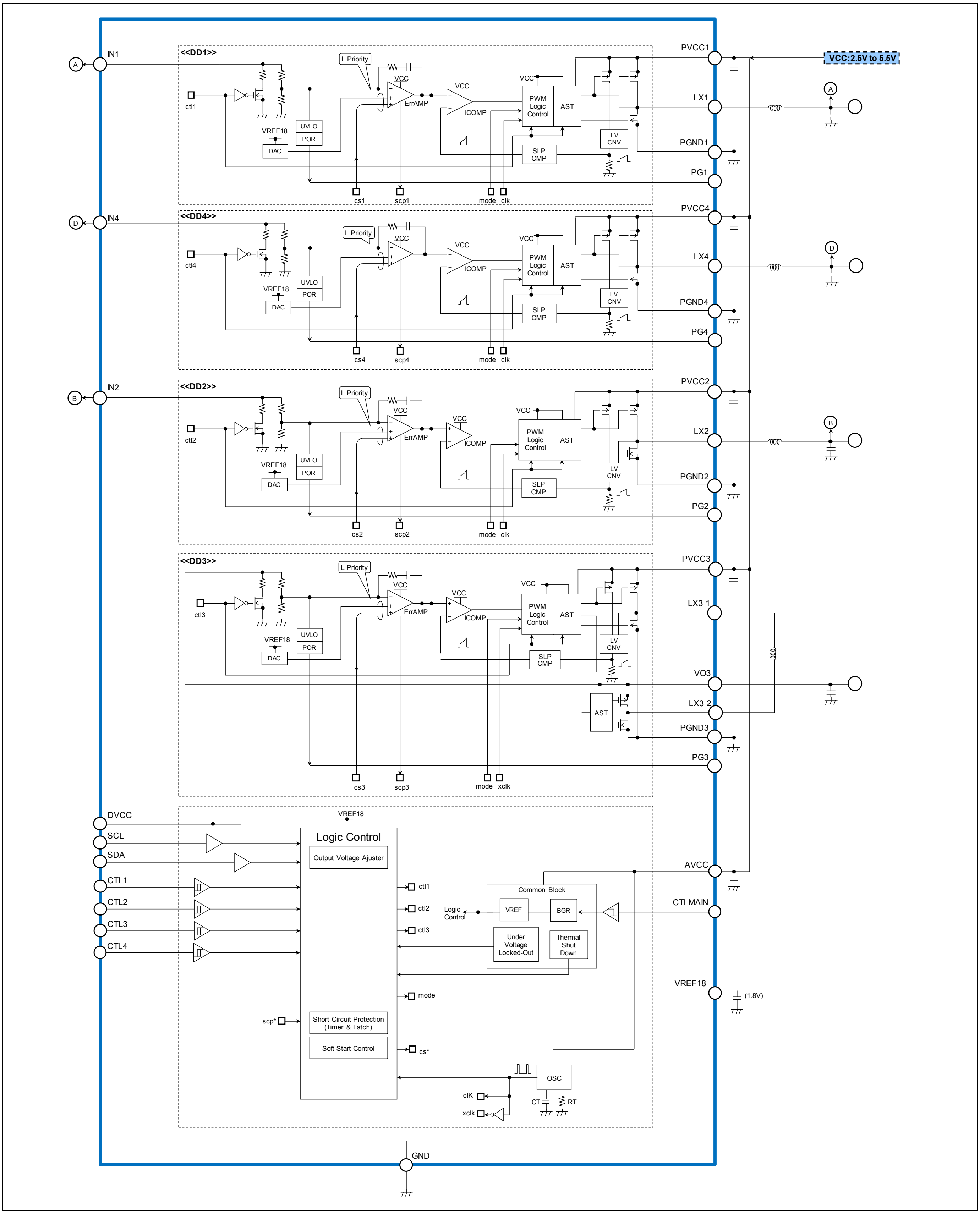
7. Pin Descriptions

Figure 7-1 Pin Descriptions

Block	Pin name	Pin number	I/O	Description	Pull-down resistor	Unused DD1	Unused DD2	Unused DD3	Unused DD4	Unused I^{2}C
DD1 Buck	IN1	24	I	DD1 output voltage feedback	-	GND	-	-	-	-
	PVCC1	23	-	DD1 output block power supply	-	AVCC	-	-	-	-
	LX1	22	O	DD1 inductor connection	-	Open	-	-	-	-
	PG1	28	O	DD1 Power Good output	-	GND	-	-	-	-
	PGND1	21	O	DD1 output block ground	-	GND	-	-	-	-
DD2 Buck	IN2	8	I	DD2 output voltage feedback	-	-	GND	-	-	-
	PVCC2	5	-	DD2 output block power supply	-	-	AVCC	-	-	-
	LX2	6	O	DD2 inductor connection	-	-	Open	-	-	-
	PG2	29	O	DD2 Power Good output	-	-	GND	-	-	-
	PGND2	7	-	DD2 output block ground	-	-	GND	-	-	-
DD3 Buck-boost	PVCC3	4	-	Power supply for DD3 output block	-	-	-	AVCC	-	-
	VO3	32	O	Output voltage for DD3	-	-	-	GND	-	-
	LX3-1	3	O	DD3 inductor connection1	-	-	-	Open	-	-
	LX3-2	1	O	DD3 inductor connection2	-	-	-	Open	-	-
	PG3	30	O	Output for DD3 Power Good	-	-	-	GND	-	-
	PGND3	2	-	Ground for DD3 output block	-	-	-	GND	-	-
DD4 Buck	IN4	17	-	DD4 output voltage feedback	-	-	-	-	GND	-
	PVCC4	18	-	DD4 output block power supply	-	-	-	-	AVCC	-
	LX4	19	O	DD4 inductor connection	-	-	-	-	Open	-
	PG4	31	O	DD4 Power Good output	-	-	-	-	GND	-
	PGND4	20	-	DD4 output block ground	-	-	-	-	GND	-
CTL	CTLMAIN	25	I	Control for reference voltage output	Exist	-	-	-	-	-
	CTL1	9	I	DD1 control	Exist	Open	-	-	-	-
	CTL2	10	I	DD2 control	Exist	-	Open	-	-	-
	CTL3	11	I	DD3 control	Exist	-	-	Open	-	-
	CTL4	12	I	DD4 control	Exist	-	-	-	Open	-
I^{2}C	DVCC	16	I	Power supply for I^{2}C communication	-	-	-	-	-	GND
	SCL	14	I	Clock for I^{2}C communication	-	-	-	-	-	Open
	SDA	15	I/O	Data for I^{2}C communication	Exist	-	-	-	-	Open
Reference control	AVCC	27	-	Power supply for reference voltage	-	-	-	-	-	-
	VREF18	26	O	Output reference voltage	-	-	-	-	-	-
	GND	13	-	Ground for reference voltage	-	-	-	-	-	-
	GND	EP	-	Ground for reference voltage	-	-	-	-	-	-

8. Block Diagram

Figure 8-1 Block Diagram



9. Absolute Maximum Ratings

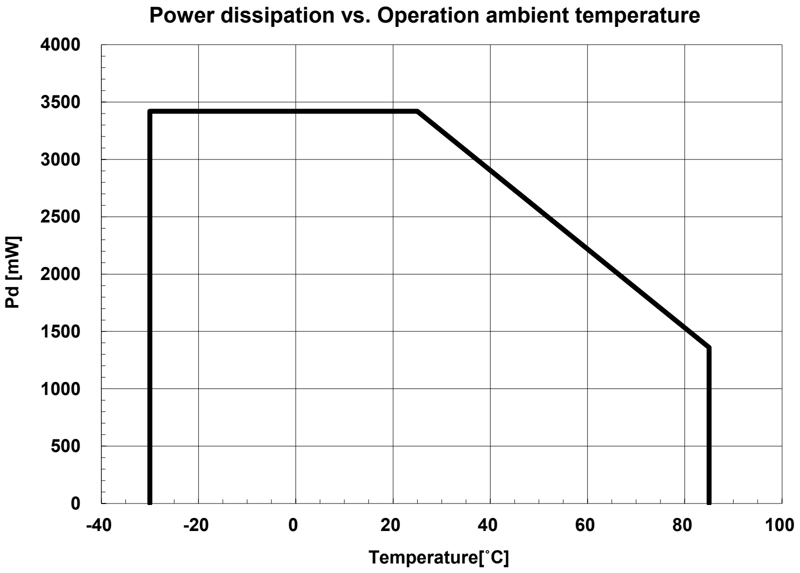
Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{VCC1}	AVCC,PVCC input voltage	-0.3	6.5	V
	V_{VCC2}	DVCC input voltage	-0.3	6.5	V
Terminal voltage	V_{CTL1}	CTL1, CTL2, CTL3 input voltage	-0.3	6.5	V
	V_{CTL2}	CTLMAIN input voltage	-0.3	6.5	V
	V_{LOGIC}	SDA,SCL input voltage	-0.3	6.5	V
	V_{PG}	PG1, PG2, PG3, PG4 drain voltage	-0.3	6.5	V
	V_{OUT}	IN1, IN2, IN3, IN4 input voltage	-0.3	6.5	V
LX voltage	V_{LX}	LX1, LX2, LX3, LX4 voltage	-1.0	6.5	V
Permission loss	P_D	Ta≤+25°C Thermal resistance(θja):(29.2°C /W(*1))	0	3420	mW
Maximum junction temperature	T_{jmax}	-	-	+125	°C
Storage temperature	T_{STG}	-	-55	+125	°C

*1: When the IC is mounted on 74mm × 74mm four-layer square epoxy board. IC is mounted on a four-layer epoxy board, which terminal bias, and the IC's thermal pad is connected to the epoxy board.

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Figure 9-1 Power Dissipation vs. Operation Ambient Temperature



10. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. Reference control block						
Power supply voltage	V_{VCC}	AVCC	2.5	3.3	5.5	V
Output current for reference voltage	I_{REF}	VREF18	-1	-	0	mA
Operating temperature	T_a	-	-30	+25	+85	°C
2. DC/DC channel						
Power supply voltage	V_{VCC}	PVCC1, PVCC2, PVCC3, PVCC4	2.5	3.3	5.5	V
Input voltage	V_{OUT}	IN1,IN2	0	-	AVCC	V
PG input voltage	V_{PG}	PG1, PG2, PG3, PG4	0	-	5.5	V
3. Input block						
Input voltage	V_{CTL} V_{MODE}	CTL1, CTL 2, CTL3, MODE CTLMAIN	0	-	AVCC	V
4. I²C communication block						
Power supply voltage	V_{VCC}	DVCC	1.70	-	3.50	V
Input voltage	V_{LOGIC}	SDA,SCL	0	-	DVCC	V

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

11. Electrical Characteristics

11.1 Reference Control block

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0VT_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. Reference voltage		[VREF18]				
Output voltage	V_{VREF1}	VREF18 pin = 0mA	1.773	1.800	1.827	V
	V_{VREF2}	AVCC pin = 2.5V to 5.5V VREF18 pin = 0mA	1.768	1.800	1.832	V
	V_{VREF3}	VREF18 pin =0mA to -1mA	1.768	1.800	1.832	V
2. Under voltage lockout		[VCC UVLO]				
Threshold voltage	V_{TH}	AVCC rising	2.156	2.20	2.244	V
Hysteresis width	V_H	-	-	0.20(*1)	-	V
3. Over current protection		[OCP]				
Timer	t_{OCP1}	DD1, DD2, DD3, DD4	0.9	1	1.1	ms
4. Thermal shut down		[TSD]				
Stop temperature	T_{TSDH}	-	125(*2)	150	-	°C
5. Input block (CTL,MODE,CTLMAIN)		[CTL, CTLMAIN]				
Input voltage	V_{IH}	CTL1, CTL2, CTL3, CTL4 pin CTLMAIN pin	AVCC × 0.7	-	AVCC	V
Input voltage	V_{IL}	CTL1, CTL2, CTL3, CTL4 pin CTLMAIN pin	0	-	0.4	V
Input current	I_{CTLH} I_{MODEH}	CTL1, CTL2, CTL3, CTL4 pin = 3.3V CTLMAIN pin = 3.3V	2.5	3.3	4.7	μA
	I_{CTLL} I_{MODEL}	CTL1, CTL2, CTL3, CTL4 pin = 0V CTLMAIN pin = 0V	-	-	1	μA
Input pull-down resistor	R_P	CTL1, CTL2, CTL3, CTL4 pin CTLMAIN pin	-	1(*1)	-	MΩ
6. Consumption current (DC/DC converter block)						
Power supply current	I_{VCCS1}	CTL1, CTL2, CTL3, CTL4 pin = 0V CTLMAIN pin = 0V	-	0	1.0	μA
	I_{VCCS2}	CTL1, CTL2, CTL3, CTL4 pin = 0V CTLMAIN pin =3.3V	-	30	45	μA
	I_{VCC}	DD1,DD2,DD3,DD4=ON, ALL DD are 0mA (operation mode: PFM/PWM mode)	-	450	670	μA
	I_{VCC}	DD1,DD2,DD3,DD4=ON, ALL DD are 0mA (operation mode: Fixed PWM mode)	-	18	27	mA

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

11.2 DD1

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. DC/DC converter block		[DD1]				
Output voltage	V_{OUT}	IOUT = -10mA, Output voltage setting: 1.0V	0.988	1.000	1.012	V
Input stability	V_{LINE}	IOUT = -10mA, PVCC1 = 2.5V to 5.5V	-5	-	+5	mV
Load stability	V_{LOAD}	IOUT = -1mA to -4000mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V_{LOAD}	IOUT = -1mA to -4000mA (PFM/PWM mode)	-10	-	+15	mV
IN1 input impedance	R_{IN}	IN1 = 2.0V	-	190(*1)	-	kΩ
SW PMOS-Tr on resistance	R_{PMOS}	LX1 = -30mA	-	120(*1)	-	mΩ
SW NMOS-Tr on resistance	R_{NMOS}	LX1 = 30mA	-	80(*1)	-	mΩ
SW PMOS-Tr leakage current	I_{LEAK}	LX1 = 0V	-3	-	-	μA
SW NMOS-Tr Leakage current	I_{LEAK}	LX1 = 3.3V	-	-	3	μA
Over current protection value	I_{LIMIT}	L=1.0μH	2400(*2)	-	-	mA
PFM/PWM mode changeover current	I_{PFM}	L=1.0μH	-	100(*1)	-	mA
Discharge resistor	R_{DIS}	-	-	5(*1)	-	kΩ
Soft start time	t_{SS}	Soft start time setting: 1ms	0.9	1	1.1	ms
Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

11.3 DD2

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
2. DC/DC converter block		[DD2]				
Output voltage	V_{OUT}	IOUT = -10mA, Output voltage setting:1.8V	1.778	1.800	1.822	V
Input stability	V_{LINE}	IOUT = -10mA PVCC2 = 2.5V to 5.5V	-5	-	+5	mV
Load stability	V_{LOAD}	IOUT = -1mA to -1200mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V_{LOAD}	IOUT = -1mA to -1200mA (PFM/PWM mode)	-10	-	+20	mV
IN2 input impedance	R_{IN}	IN2 = 2.0V	-	150(*1)	-	kΩ
SW PMOS-Tr on resistance	R_{PMOS}	LX2 = -30mA	-	190(*1)	-	mΩ
SW NMOS-Tr on resistance	R_{NMOS}	LX2 = 30mA	-	135(*1)	-	mΩ
SW PMOS-Tr leakage current	I_{LEAK}	LX2 = 0V	-3	-	-	µA
SW NMOS-Tr leakage current	I_{LEAK}	LX2 = 3.3V	-	-	3	µA
Over current protection value	I_{LIMIT}	L=1.0µH	1500(*2)	-	-	mA
PFM/PWM mode changeover current	I_{PFM}	L=1.0µH	-	65(*1)	-	mA
Discharge resistor	R_{DIS}	-	-	5(*1)	-	kΩ
Soft start time	t_{SS}	Soft start time setting: 1ms	0.9	1	1.1	ms
Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

11.4 DD3

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
3. DC/DC converter block		[DD3]				
Output voltage	V_{OUT}	IOUT = -10mA, Output voltage setting: 3.3V	3.241	3.300	3.359	V
Input stability	V_{LINE}	IOUT = -10mA, PVCC3 = 2.5V to 5.5V	-5	-	+5	mV
Load stability	V_{LOAD}	IOUT = -1mA to -600mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V_{LOAD}	IOUT = -1mA to -600mA (PFM/PWM mode)	-10	-	+15	mV
VO3 impedance	R_{Vo3}	VO3= 2.0V	-	550(*1)	-	kΩ
SW PMOS-Tr on resistance	R_{PMOS}	LX3-1 = -30mA	-	115(*1)	-	mΩ
SW NMOS-Tr on resistance	R_{NMOS}	LX3-1 = 30mA	-	140(*1)	-	mΩ
SW PMOS-Tr on resistance	R_{PMOS}	LX3-2 = -30mA	-	155(*1)	-	mΩ
SW NMOS-Tr on resistance	R_{NMOS}	LX3-2 = 30mA	-	220(*1)	-	mΩ
SW PMOS-Tr leakage current	I_{LEAK}	LX3-1 = 0V	-3	-	-	μA
SW NMOS-Tr leakage current	I_{LEAK}	LX3-1 = 3.3V	-	-	1	μA
SW PMOS-Tr leakage current	I_{LEAK}	LX3-2 = 0V	-3	-	-	μA
SW NMOS-Tr leakage current	I_{LEAK}	LX3-2 = 3.3V	-	-	1	μA
Over current protection value	I_{LIMIT}	L=1.0μH	1000(*2)	-	-	mA
PFM/PWM mode changeover current	I_{PFM}	L=1.0μH	-	200(*1)	-	mA
Discharge resistor	R_{DIS}	-	-	5(*1)	-	kΩ
Soft start time	t_{SS}	Soft start time setting:1ms	0.9	1	1.1	ms
Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

11.5 DD4

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
4. DC/DC converter block		[DD4]				
Output voltage	V_{OUT}	IOUT = -10mA, Output voltage setting: 1.0V	0.988	1.000	1.012	V
Input stability	V_{LINE}	IOUT = -10mA, PVCC4 = 2.5V to 5.5V	-5	-	+5	mV
Load stability	V_{LOAD}	IOUT = -1mA to -4000mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V_{LOAD}	IOUT = -1mA to -4000mA (PFM/PWM mode)	-10	-	+15	mV
IN4 input impedance	R_{IN}	IN4 = 2.0V	-	190(*1)	-	kΩ
SW PMOS-Tr on resistance	R_{PMOS}	LX4 = -30mA	-	120(*1)	-	mΩ
SW NMOS-Tr on resistance	R_{NMOS}	LX4 = 30mA	-	80(*1)	-	mΩ
SW PMOS-Tr leakage current	I_{LEAK}	LX4 = 0V	-3	-	-	μA
SW NMOS-Tr Leakage current	I_{LEAK}	LX4 = 3.3V	-	-	3	μA
Over current protection value	I_{LIMIT}	L=1.0μH	2300(*2)	-	-	mA
PFM/PWM mode changeover current	I_{PFM}	L=1.0μH	-	75(*1)	-	mA
Discharge resistor	R_{DIS}	-	-	5(*1)	-	kΩ
Soft start time	t_{SS}	Soft start time setting: 1ms	0.9	1	1.1	ms
Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

11.6 Digital block

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. Power good block		[Power Good]				
Output voltage	V_{OL}	PG1, PG2, PG3, PG4 I_{OL} = 1mA	-	-	0.4	V
Output current	I_{OL}	PG1, PG2, PG3, PG4	1	-	-	mA
Low voltage detection	V_{th}	IN1, IN2, IN4 = falling VO3 = falling	-	V_O × 0.90 (*1)	-	V
Power on detection	V_{th}	IN1, IN2, IN4 = rising VO3 = rising	-	V_O × 0.93 (*1)	-	V
2. I^2C block		[I^2C]				
Input voltage	V_{IH}	SCL,SDA	DVCC ×0.7	-	DVCC	V
	V_{IL}	SCL,SDA	0	-	DVCC ×0.3	V
Input current	I_{IH}	SCL,SDA DVCC = 3.3V	-	-	10	μA
	I_{IL}	SCL,SDA DVCC = 3.3V	-10	-	-	μA
Output voltage	V_{OL}	SDA I_{OL} = 3mA	-	-	0.4	V
Output current	I_{OL}	SDA	3	-	-	mA

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

12. Operation Mode List

Table 12-1 Operation Mode List

	Mode	Stand-by	Stand-by2	Normal	ERR detection
CTL signal	CTLMAIN (external)	L	H	H	H
	CTL1 (external/I^2C)	L	L	H/L(*1)	X
	CTL2 (external/I^2C)	L	L	H/L(*1)	X
	CTL3 (external/I^2C)	L	L	H/L(*1)	X
	CTL4 (external/I^2C)	L	L	H/L(*1)	X
Operation Block	Reference	OFF	ON	ON	ON
	Digital	OFF	ON	ON	ON
	DD1	OFF	OFF	ON/OFF	OFF
	DD2	OFF	OFF	ON/OFF	OFF
	DD3	OFF	OFF	ON/OFF	OFF
	DD4	OFF	OFF	ON/OFF	OFF
I^2C communication	I^2C communication	disable	enable	enable	enable
Protection operating	Thermal shut down (TSD)	Not available	Not available	available	(*2)
	Over current protection (OCP)	Not available	Not available	available	(*2)

*1: normal mode means that CTLMAIN pin is "H" level and each DD CTL pin is "H" level

*2: This state is after each err detection. ERR state will release, when the power supply voltage or CTLMAIN pin will turn off and on.

Priority of the External CTL pin and I^2C Communication

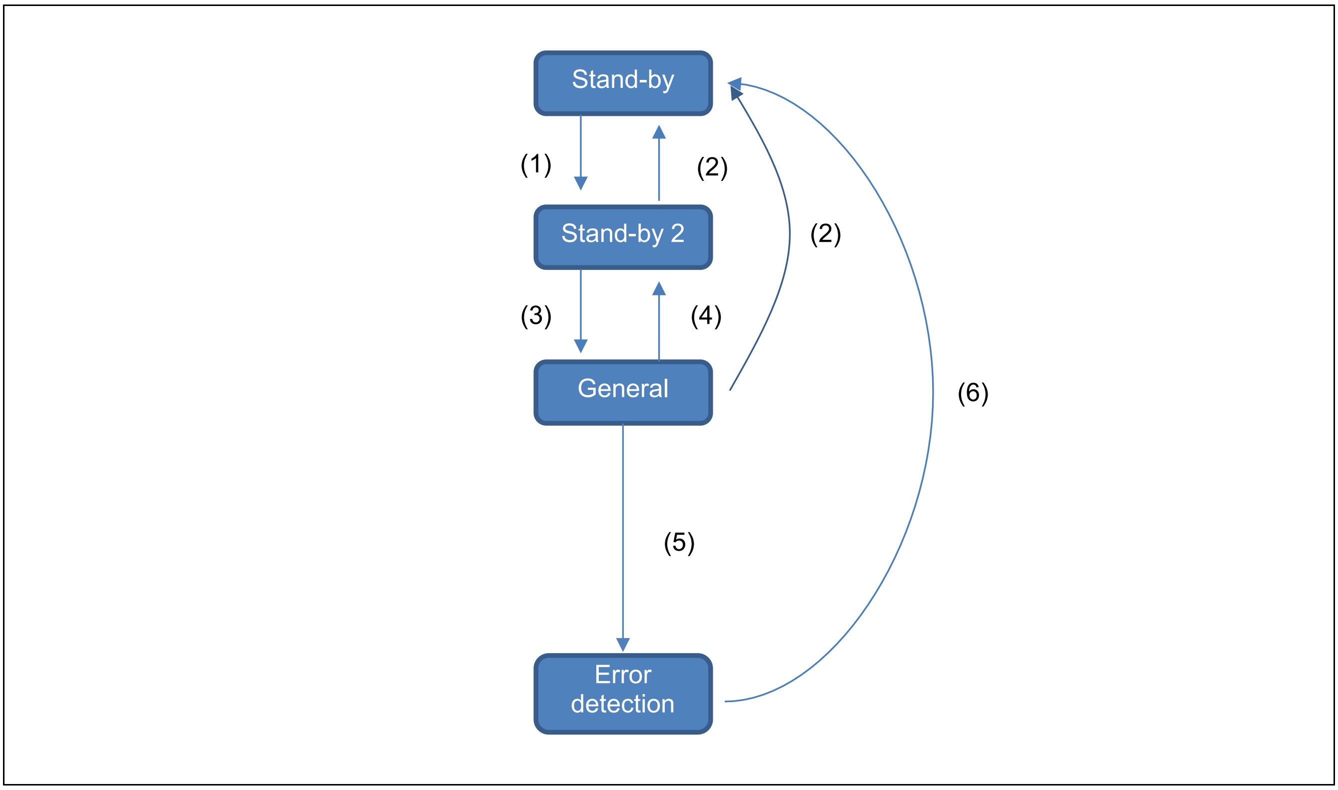
CTLMAIN (external)	CTL1, CTL2, CTL3, CTL4 (external)	30h resistor (I^2C)	Relevant CH
H	H	1	ON
H	H	0	ON
H	L	1	ON
H	L	0	OFF
L	X	disable	OFF

Notes:

- *The I^2C communication is valid after the reference control block and digital block activation setting the external CTLMAIN pin to "H" level.*
- *Please attention below note about ON/OFF control of DD1, DD2, DD3, DD4 by I^2C communication. When each DD control is turned off by I^2C communication and external CTL pin remains "H" level, DCDC converter keep operating.*

13. State Transition Diagram

Figure 13-1 State Transition Diagram



(1) External CTLMAIN pin is "H" level.

(2) External CTLMAIN pin is "L" level.

(3) External CTL pin or I^2C communication "relevant CH_ON"

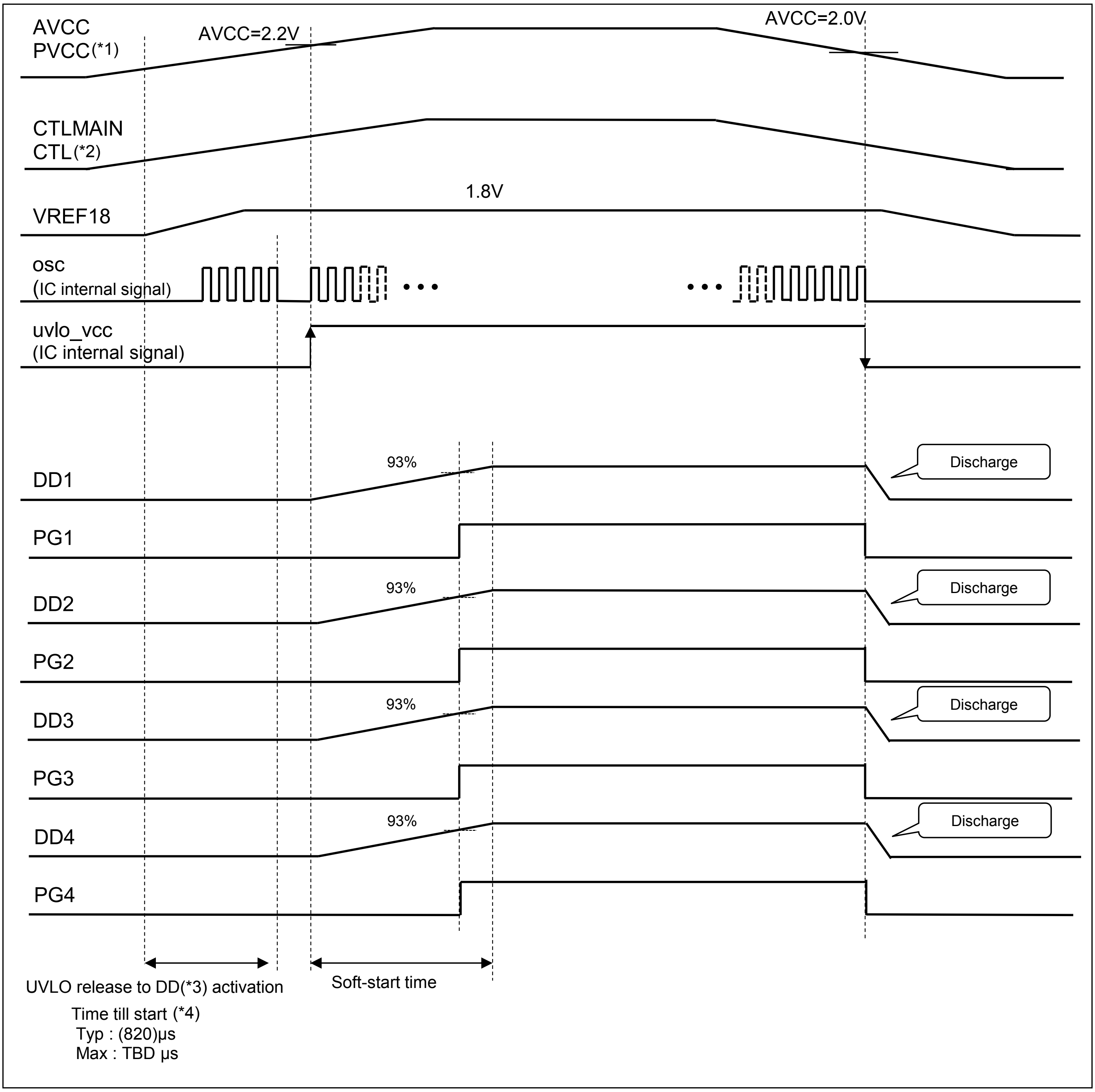
(4) External CTL pin or I^2C communication "relevant CH_OFF"

(5) ERR detection (TSD, OCP 1ms continuation)

(6) Turning on the power supply again (equal to or less than uvlo_vcc rest voltage) or setting CTLMAIN to "L" level

14. Turning on and off Sequence (AVCC=CTLMAIN, CTL1, CTL2, CTL3, CTL4)

Figure 14-1 Turning on and off Sequence (AVCC=CTLMAIN, CTL1, CTL2, CTL3, CTL4)



*1: PVCC1, PVCC2, PVCC3, PVCC4

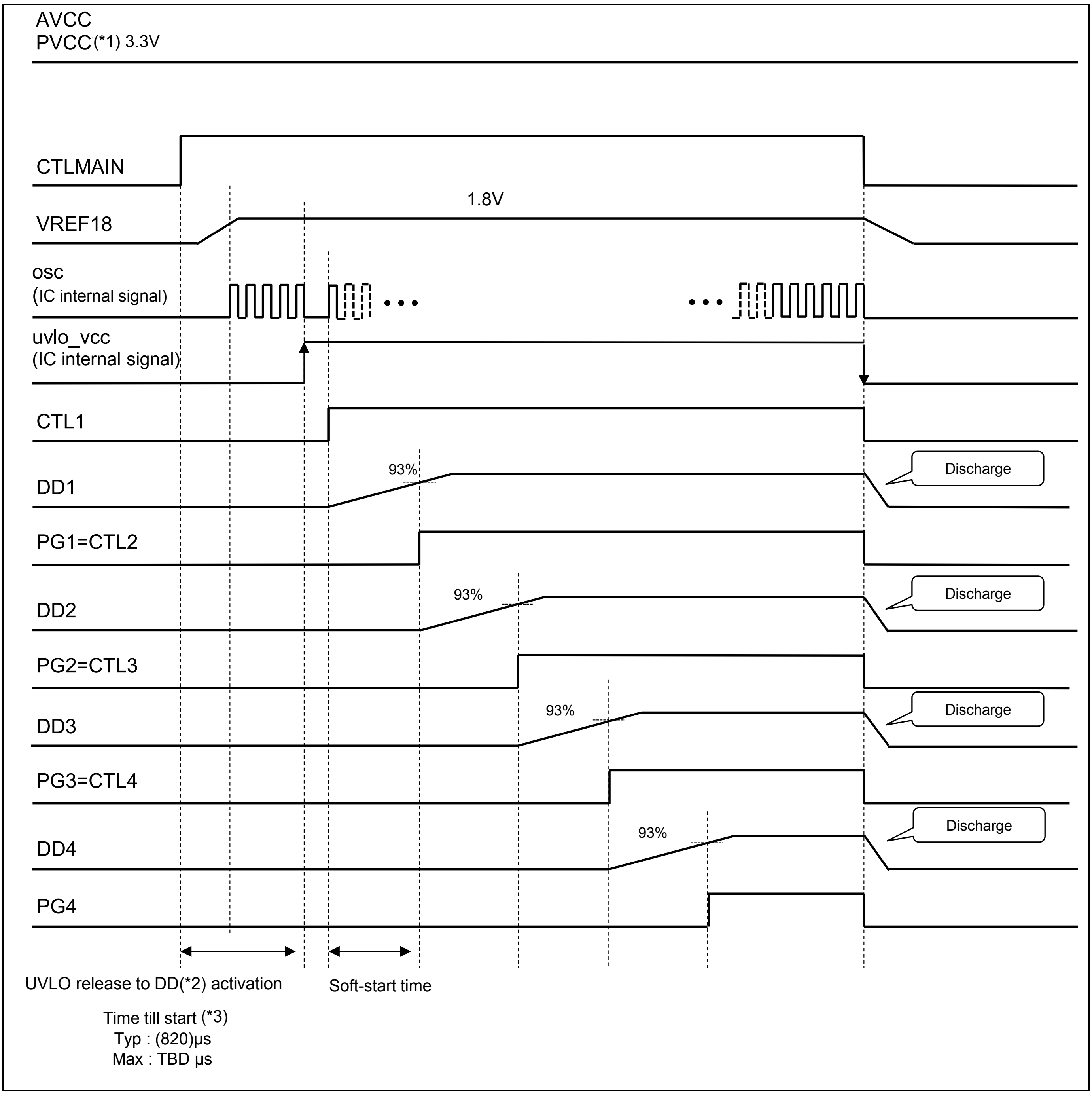
*2: CTL1, CTL2, CTL3, CTL4

*3: DD1, DD2, DD3, DD4

*4: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0μF

15. Turning on and off Sequence (AVCC → CTLMAIN → CTL1 → CTL2 → CTL3 → CTL4)

Figure 15-1 Turning on and off Sequence (AVCC → CTLMAIN → CTL1 → CTL2 → CTL3 → CTL4)



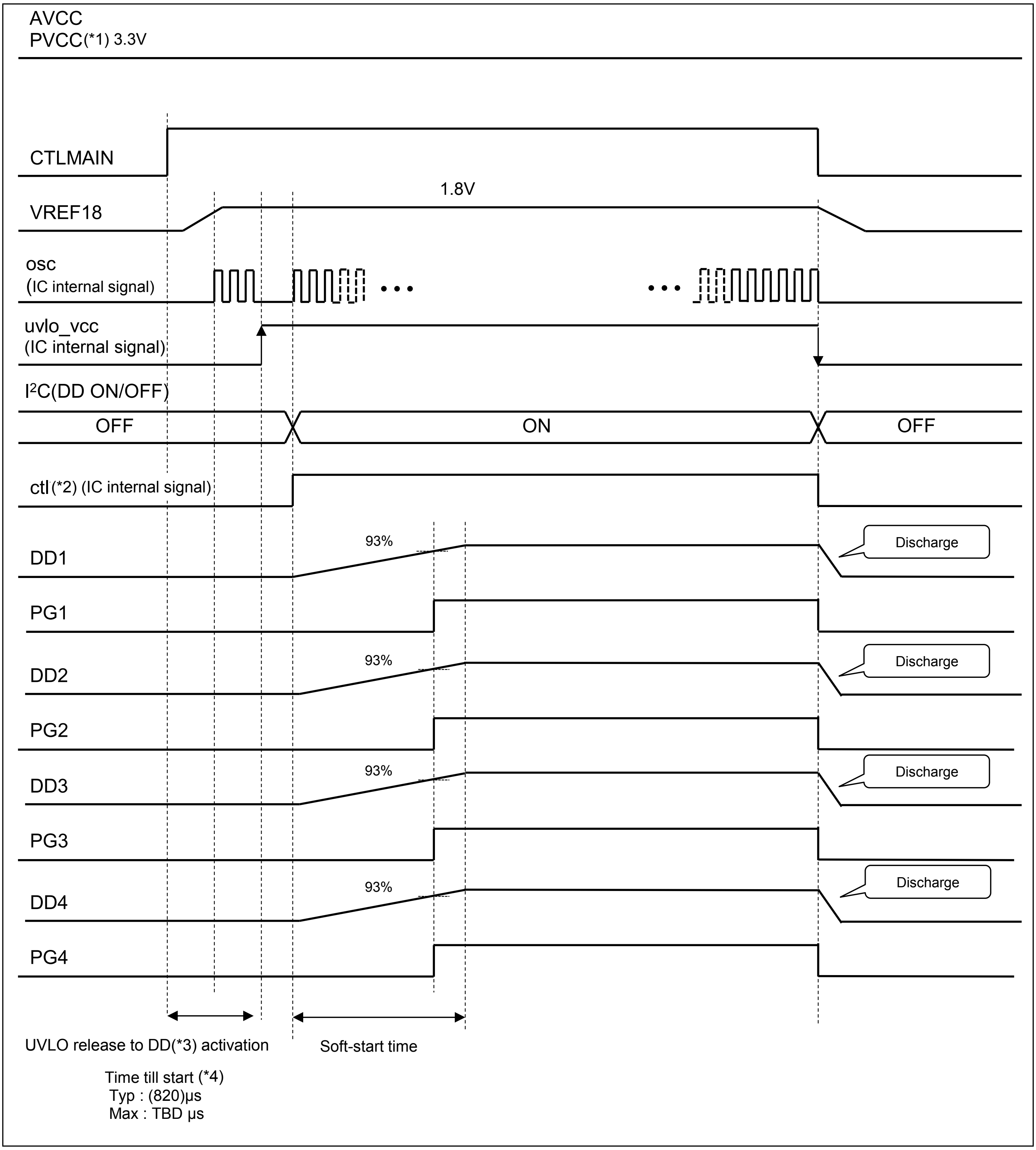
*1: PVCC1, PVCC2, PVCC3, PVCC4

*2: DD1, DD2, DD3, DD4

*3: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0µF

16. Turning on and off Sequence (AVCC → CTLMAIN → I^2C)

Figure 16-1 Turning on and off Sequence (AVCC → CTLMAIN → I^2C)



*1: PVCC1, PVCC2, PVCC3, PVCC4

*2: CTL1, CTL2, CTL3

*3: DD1, DD2, DD3

*4: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0µF

17. CTL Pin Threshold Voltage

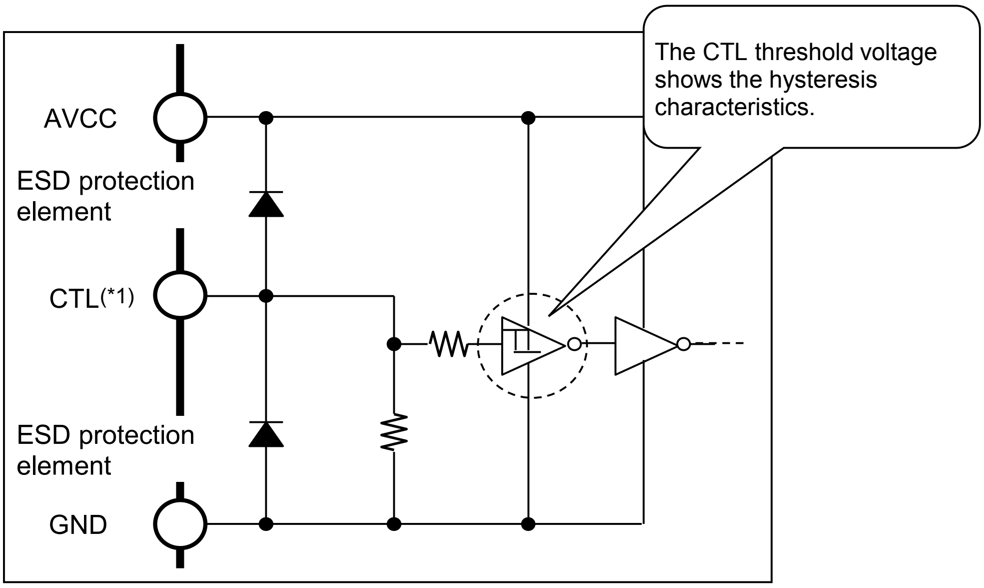
The input circuit structure for the CTL(*1) pin is the schmitt trigger style, and the threshold voltage shows the hysteresis characteristics when CTL(*1) OFF to ON and ON to OFF.

(See "CTL(*1) pin equivalent circuit diagram" below.)

Also, the threshold voltage level depends on the VCC pin voltage.

Moreover, make sure to input either the "H" level (>"VCC×0.7"V) or "L" level (<0.4V) to the CTL(*1) pin when in use.

Table 17-1 CTL(*1) Pin Equivalent Circuit Diagram



*1: CTLMAIN, CTL1, CTL2, CTL3, CTL4

18. Protection Operation Sequence

Over Current Protection (DD channel)

The DD channel monitors the peak current of FET at any time during the operation. When the DD output becomes the over current state, the output voltage is decreased. Afterward, the timer operation is performed and the output stops after about 1ms progress.

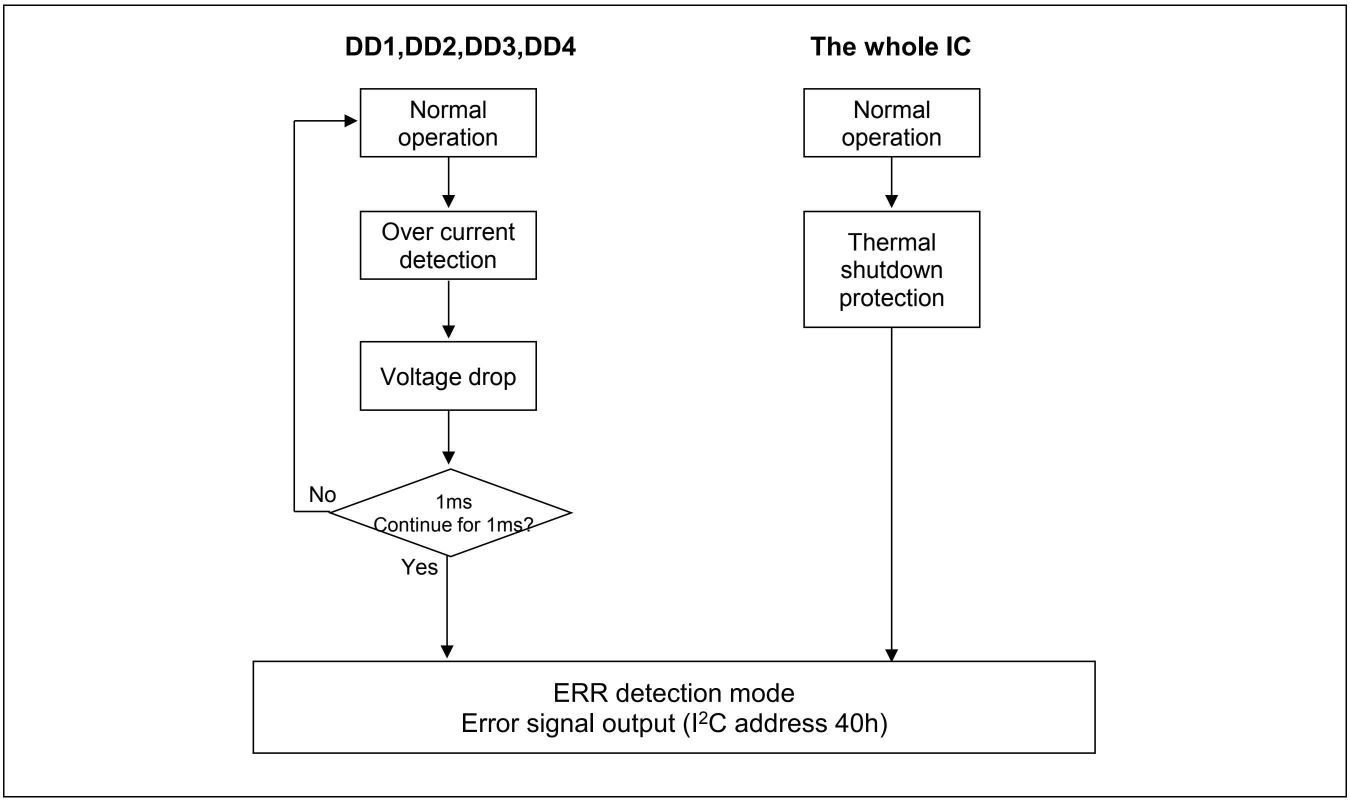
When one of each DD channel stops operation by over current protection, all DD channels stop operation.

Thermal Shut Down

If the temperature at the junction part reaches +150°C, the thermal shutdown protection circuit turns all channels off.

Error detection sequence

Table 18-1 Error Detection Sequence



ERR Detection Mode Release

It is necessary to turn the power supply turning on again, or to turn CTLMAIN turning on again to release the ERR detection mode.

19. Operation Condition, Stop Circuit and Release Condition for Protection Circuit

Table 19-1 Operation Condition, Stop Circuit and Release Condition for Protection Circuit

Channel	Operation whilst under protection	Over Current protection (OCP)	Under voltage lockout protection (UVLO)	Thermal shutdown protection (TSD)
DD1,DD2,DD3,DD4	Discharge	Operating condition: After about 1ms progress in the over current condition Process during protection operation: DD1, DD2, DD3, DD4 stop Recovery condition: (1) Power supply reasserted (2) CTLMAIN reasserted	Operating condition: Input voltage drop Process during protection operation: DD1, DD2, DD3, DD4 stop Recovery condition: Input voltage rise UVLO operates only when CTLMAIN is "H" (at VREF18 output).	Operating condition: Chip temperature increment Process during protection operation: DD1, DD2, DD3, DD4 stop Recovery condition: (1) Power supply reasserted (2) CTLMAIN reasserted Only when CTLMAIN is in the "H" state and CTL(*1) is in the "H" state, or when DD(*2) in operating condition by I^2C, will operate.
ERR output (address 40h)	-	Write "1" when detecting OCP	No change	Write "1" when detecting TSD

Thermal shutdown protection (TSD) operation during over current protection timer operation

When the thermal shutdown protection (TSD) operated during the over current protection (OCP) timer operation, the thermal shutdown protection has priority.

Operation when releasing under voltage lockout protection (UVLO)

- DD1,DD2,DD3,DD4: Activation following the condition for CTL(*1) pin or I^2C

Note:

- *When VREF18 decreases at the time of UVLO operation, I^2C register is reset, and all DD does OFF. It is necessary to let you do ON by CTL(*1) pin and communication again to let DD have ON."*

*1: CTL1, CTL2, CTL3, CTL4

*2: DD1, DD2, DD3, DD4

20. DD Soft Start Operation

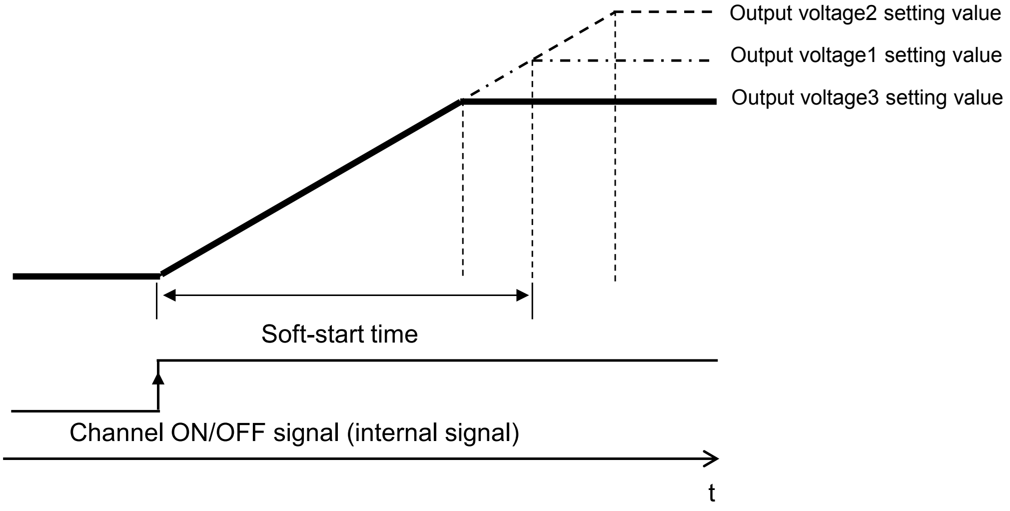
The soft-start operation for DD1, DD2, DD3 and DD4 is enabled in order to prevent the rush current during the DD activation. The soft-start time can be controlled by I^2C.

About output voltage changing option, soft start time is showed by follow equation.

Tss=Tslp × Vset/Vdef (ms)

Tss : soft start time
Tslp : slope coefficient of soft start
Vset : output voltage setting
Vdef : DD1=1.0, DD2=1.8, DD3=3.3, DD4=1.0

Figure 20-1 DD Soft Start



21. Discharge Operation

DD Channel

When executing the DD OFF operation at the CH ON/OFF signal, the DC/DC smooth capacitance charged for each output voltage is discharged using resistor for discharge which is set in the IC and the output voltage is decreased gradually. However, the discharge time changes depending on the DC/DC converter load current.

The discharge time is calculated by the following equation.

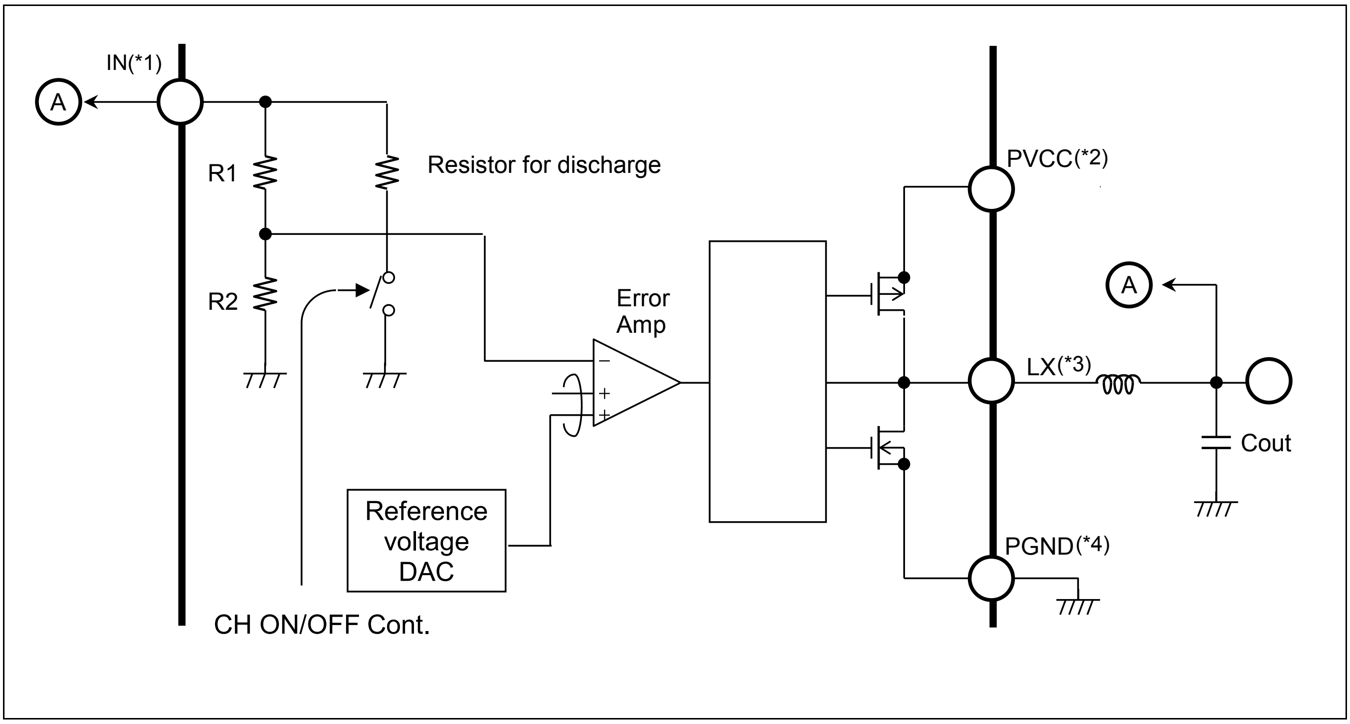
Discharge time (time till the output becomes 10% without load)

$$toff(s) \approx 2.3 \times R\_DIS \times C_{OUT} (F)$$

Note:

- *See the table in ELECTRICAL CHARACTERISTICS for the discharge resistor value.*

Figure 21-1 Discharge function



*1: IN1, IN2, IN3, IN4

*2: PVCC1, PVCC2, PVCC3, PVCC4

*3: LX1, LX2, LX3, LX4

*4: PGND1, PGND2, PGND3, PGND4

22. PG Function

The following pins for each CH POWER GOOD output are prepared.

PG1

It is the pin for DD1 POWER GOOD output.

When the output voltage exceeds 93% of the setting value at the DD1 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD1 OFF mode.

PG2

It is the pin for DD2 POWER GOOD output.

When the output voltage exceeds 93% of the setting value at the DD2 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD2 OFF mode.

PG3

It is the pin for DD3 POWER GOOD output.

When the output voltage exceeds 93% of the setting value at the DD3 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD3 OFF mode.

PG4

It is the pin for DD4 POWER GOOD output.

When the output voltage exceeds 93% of the setting value at the DD4 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD4 OFF mode.

23. I²C Interface

23.1 Structure of I²C Interface

The I²C interface executes the data communication in 1 byte (8-bit) units using two signal lines (bus), a SCL (serial clock line) and a SDA (serial data line).

This bus is connected to multiple devices;

master: device to generate the clock signal and to control the data transfer (CPU and so on)

slave: device that an address is specified by a master.

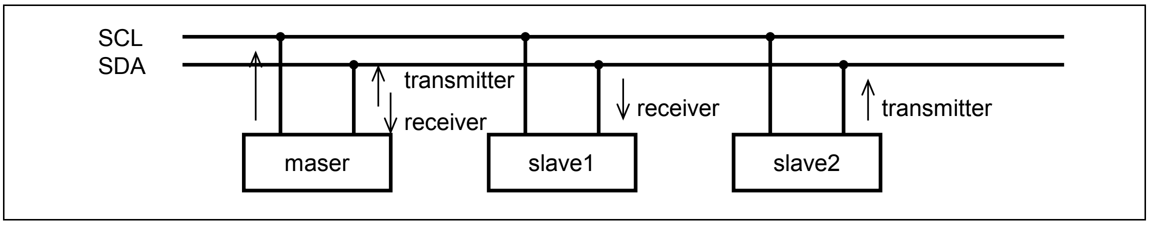
This IC is set as the slave and has no function to be the master.

Each device is defined due to the communication direction as described below.

transmitter: device to send data to bus

receiver: device to receive data from bus

The IC has the function both transmitter and receiver.



The IC defines the followings;

Write: data is transmitted from master and the IC receives data

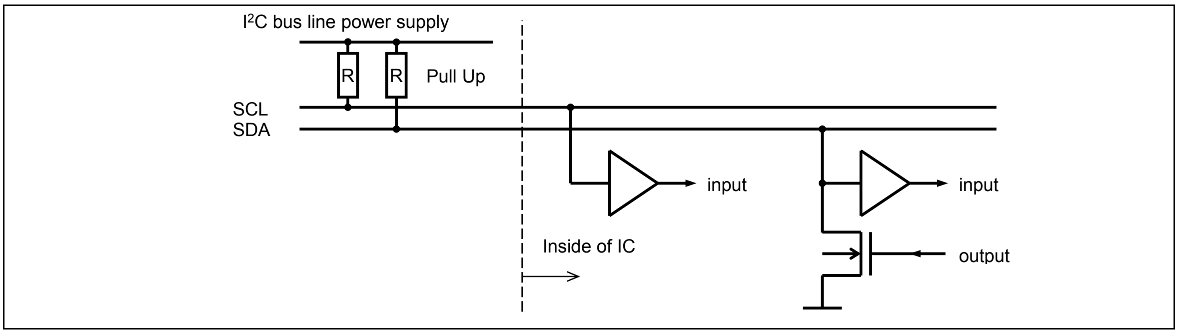
Read: The IC transmits data and master receives data.

23.2 Definition of Signal Lines

SCL and SDA are connected to the power supply by the pull-up resistor.
The output circuit is the open Drain output.
When a bus is not used (waiting state), the open "H" is set changing the open Drain to the OFF state.

Note:

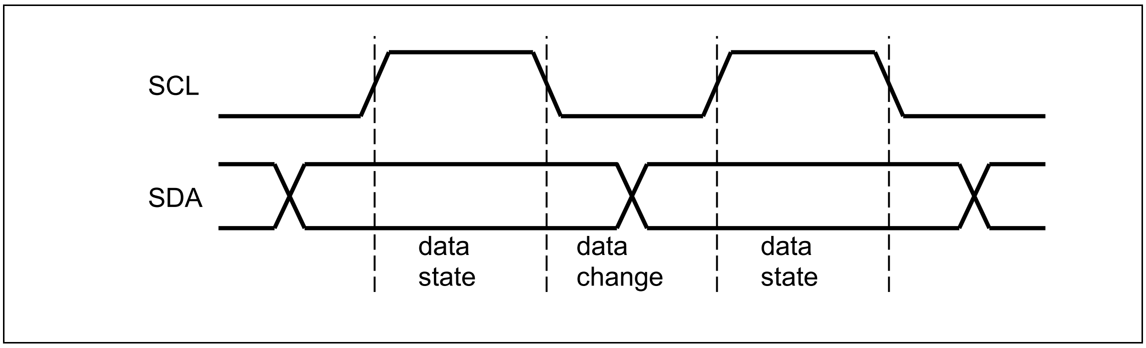
- *SCL and SDA pins adopt a different ESD protection system from standard I²C specification because of ESD enhancement (see 25. I/O Pin Equivalent Circuit Diagram). When the power supply is in the bus line, do not shut off the power supply for an IC (DVCC).*



23.3 Validity of Data

Data has the following characteristics;

- change when SCL is the "L" level
- valid if the state is kept while SCL is the "H" level.

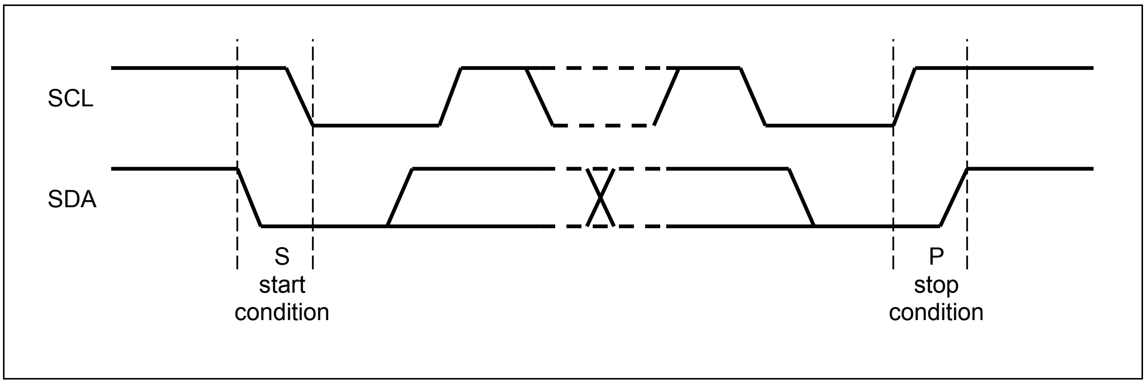


The SDA signal change means the start or stop condition when SCL is the "H" level.

23.4 Definition of Start and Stop Condition

The start and stop conditions are output from the master and shows start and stop of communications to the slave.

- Start: SDA changes from "H" to "L" when SCL is "H".
- Stop: SDA changes from "L" to "H" when SCL is "H".



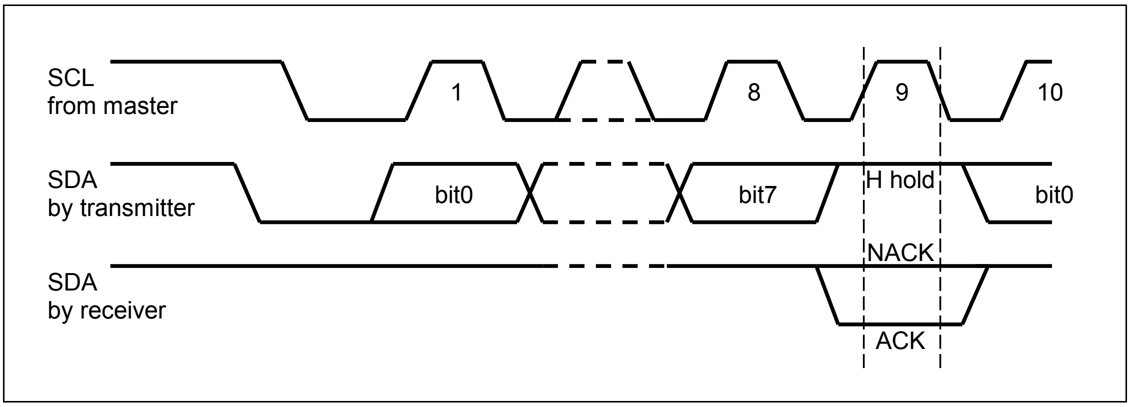
23.5 ACK Signal

This is a signal to confirm the data reception during communication.
The receiver replies the ACK signal to show the data reception to a transmitter every time
1 byte (8-bit) of data is received. The ACK signal is sent in 9clk after sending data 8-bit matching to the SCL signal that the master generates.

- A transmitter keeps SDA output "open H" in SCL9clk.
- A receiver informs the data reception situation to a transmitter outputting the followings in SCL 9 calk ;

  when data was received: SDA output "L" (ACK)
  when no data was received: SDA output "open H" (NACK)

However, if the master is changed to the receiver, ACK is not replied after the last data reception because the bus keeps open stopping the data transmission to the slave transmitter. In this case, the slave transmitter opens the bus (open H) and is set to the stop condition reception waiting state from the master.



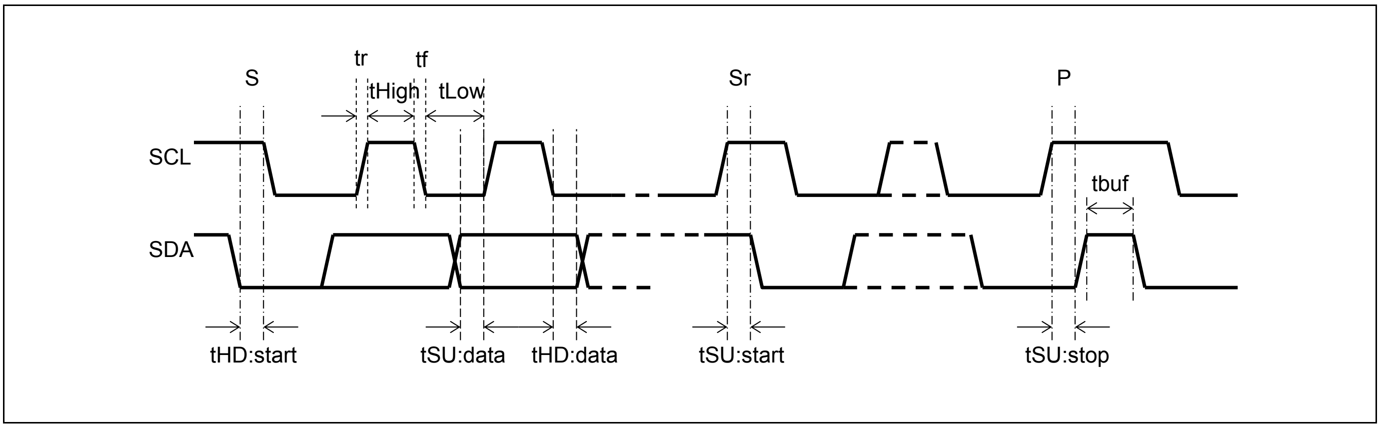
23.6 I²C Interface Input Timing

(within recommended operating conditions)

Parameter	Symbol	Value				Unit
		SCL=100kHz		SCL=400kHz		
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	-	100	-	400	kHz
Start condition hold time	$t_{HD:start}$	4.0	-	0.6	-	μs
Restart condition setup time	$t_{SU:start}$	4.7	-	0.6	-	μs
Stop condition setup time	$t_{SU:stop}$	4.0	-	0.6	-	μs
Stop to Start bus open time	t_{buf}	4.7	-	1.3	-	μs
SCL "L" time	t_{Low}	4.7	-	1.3	-	μs
SCL "H" time	t_{High}	4.0	-	0.6	-	μs
SCL/SDA rising time	t_r	-	1.0	-	0.3	μs
SCL/SDA falling time	t_f	-	0.3	-	0.3	μs
Data hold time	$t_{HD:data}$	0.0	-	0.0	-	μs
Data setup time	$t_{SU:data}$	0.25	-	0.10	-	μs
SCL/SDA capacitor load	C_b	-	400	-	400	pF

VIH/VIL level reference

Conform to I²C bus specifications



23.7 Slave Address

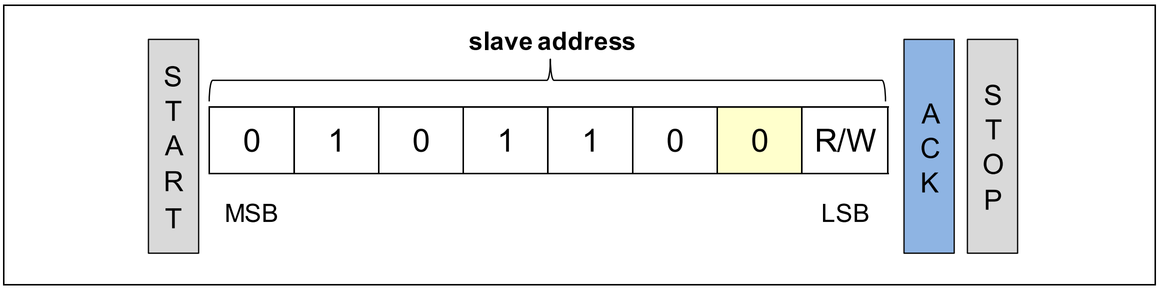
This is a slave address when communicating with the I^{2}C interface.

The slave address of this IC is set by the first seven bits as shown below.

The eighth bit is called the least significant bit (LSB) and determines the message direction. The bit "0" shows that information will be written from the master to the slave.

The bit "1" shows that the master reads information from the slave.

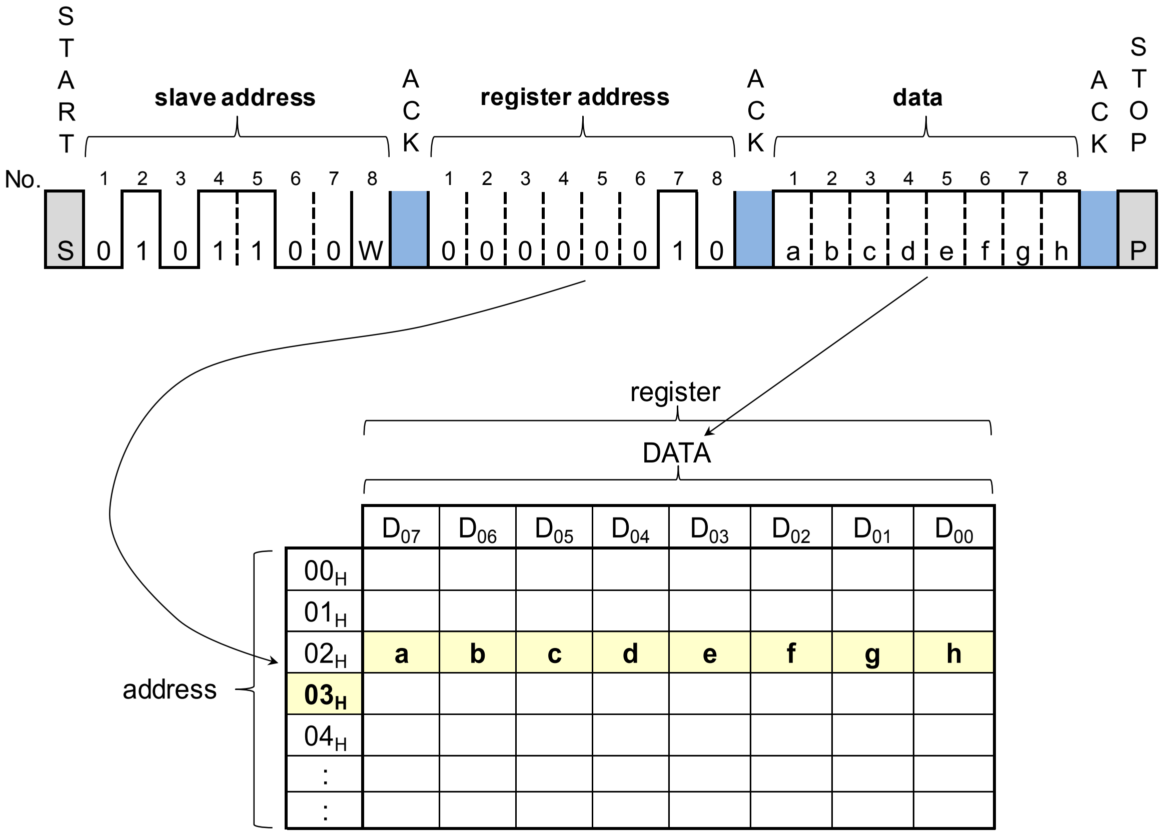
This does not support the general call address.



23.8 Bit Structure of Data on I^2C Interface

(1) Writing Data to Register and Reading Data

The data line is sent/received in the order from the most significant bit (MSB) to the least significant bit (LSB).



	D_{07}	D_{06}	D_{05}	D_{04}	D_{03}	D_{02}	D_{01}	D_{00}
00_H								
01_H								
02_H	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**
03_H								
04_H								
:								
:								

Output the "stop" condition after sending the Write data.

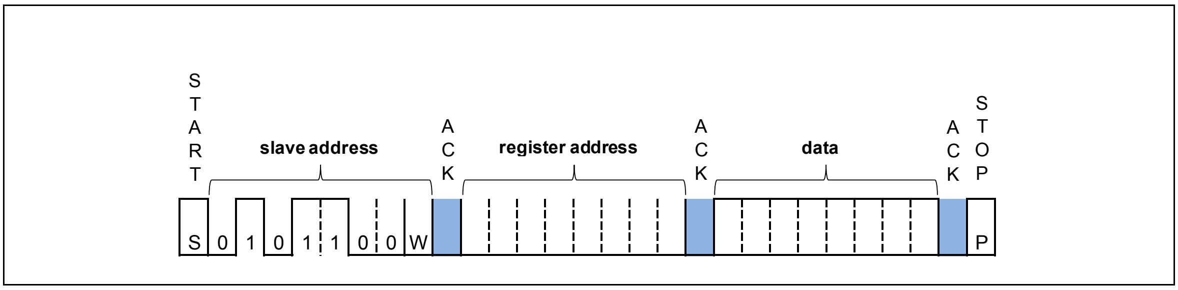
⬚ : Signal which a master sends, ▨ : Signal which this IC sends

(2) I^{2}C Interface Data Format

About I^{2}C Communication

1. When a different slave address comes, non-matching ID is informed by not replying ACK after receiving the slave address.
2. All registers write to internal registers in the ACK signal after receiving the 8-bit data of each setting.
3. If a non-existing register address is specified, data is not written to a register.
4. Output the "stop" condition after sending the write data.

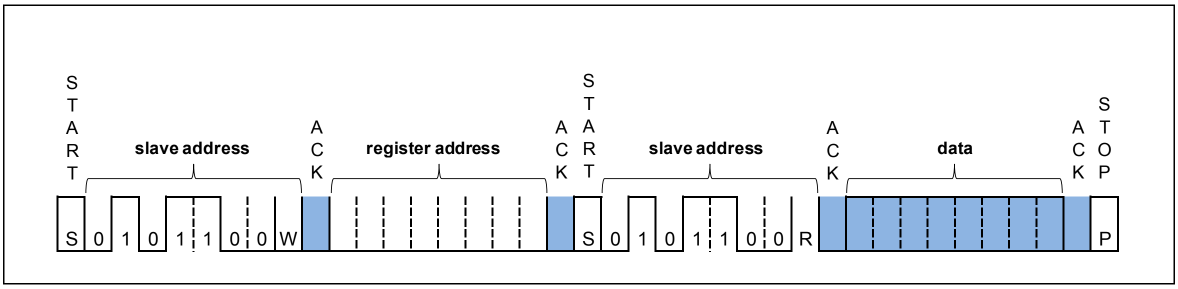
<Write (W)>



Write is allowed per one address. (Sequential writing is not allowed.)
Send register address and data as one unit.

⬚: Signal which a master sends, ▨: Signal which this IC sends

<Read (R)>



Read is allowed per one address. Be sure to perform read by specifying the register addresses. (Sequential reading is not allowed.)

⬚: Signal which a master sends, ▨: Signal which this IC sends

24. Structure of I^2C Interface and Data

Table 24-1 Register map

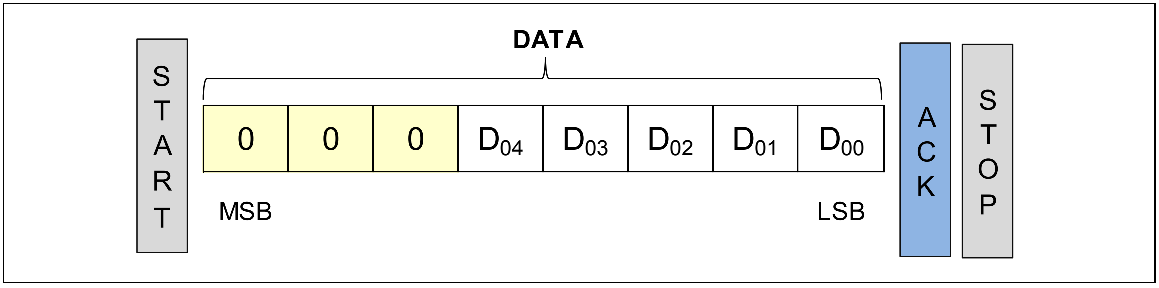
	Address	DATA									Writing timing	Remarks
		d07	**d06**	**d05**	**d04**	**d03**	**d02**	**d01**	**d00**	**Default**		
Output voltage	00_H	0	0	0	D04	D03	D02	D01	D00	$0F_H$	ACK	DD1 output voltage setting
	01_H	0	0	0	0	D03	D02	D01	D00	$0C_H$	ACK	DD2 output voltage setting
	02_H	0	0	0	0	0	D02	D01	D00	05_H	ACK	DD3 output voltage setting
	03_H	0	0	0	D04	D03	D02	D01	D00	$0F_H$	ACK	DD4 output voltage setting
Soft start	10_H	0	0	0	0	D03	D02	D01	D00	00_H	ACK	DD1 soft-start time setting
	11_H	0	0	0	0	D03	D02	D01	D00	00_H	ACK	DD2 soft-start time setting
	12_H	0	0	0	0	D03	D02	D01	D00	00_H	ACK	DD3 soft-start time setting
	13_H	0	0	0	0	D03	D02	D01	D00	00_H	ACK	DD4 soft-start time setting
DD operation mode	20_H	0	0	0	0	D03	D02	D01	D00	00_H	ACK	DD operation mode setting "0": Fixed PWM mode, "1": PFM/PWM mode
ON/OFF	30_H	0	0	0	0	D03	D02	D01	D00	00_H	ACK	DD output ON/OFF setting "0":Output OFF / "1":Output ON
ERR	40_H	0	0	0	D04	D03	D02	D01	D00	00_H	-	DD ERR state monitoring register (read only) "0": Normal / "1": Error detection
PG	50_H	0	0	0	0	D03	D02	D01	D00	00_H	-	DD PG state monitoring register (read only) "0": Non-output / "1":output
For test	EX_H	-	-	-	-	-	-	-	-	-	-	Disabled
For test	FX_H	-	-	-	-	-	-	-	-	-	-	Disabled

Note:

- *Address FX_H and address EX_H are for test.*
  Do not write/read FX_H and EX_H.

24.1 About DD1, DD4 Output Voltage Setting

- Address 00_H DD1 is allocated as resisters for the DC/DC output voltage setting.
  Address 03_H DD4 is allocated as resisters for the DC/DC output voltage setting.
- The DC/DC output voltage setting of DD1 is controlled by writing data to address 00_H.
  The DC/DC output voltage setting of DD4 is controlled by writing data to address 03_H.



address00_H: For DD1 output voltage setting
address03_H: For DD4 output voltage setting
D_{04} to D_{00}: Set the output voltage

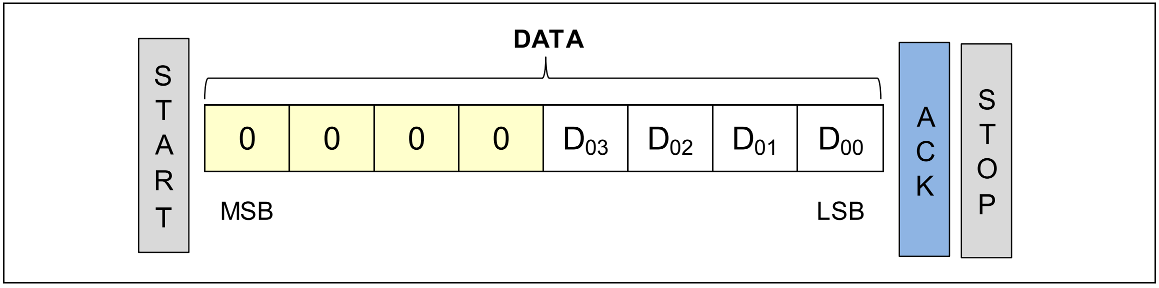
DD1, DD4 Output Voltage Setting Table

DATA	Output voltage (V)	DATA	Output voltage (V)
00_H	0.700	10_H	1.020
01_H	0.720	11_H	1.040
02_H	0.740	12_H	1.060
03_H	0.760	13_H	1.080
04_H	0.780	14_H	1.100 (*1)
05_H	0.800	15_H	1.120
06_H	0.820	16_H	1.140
07_H	0.840	17_H	1.160
08_H	0.860	18_H	1.180
09_H	0.880	19_H	1.200 (*1)
$0A_H$	0.900 (*1)	$1A_H$	1.220
$0B_H$	0.920	$1B_H$	1.240
$0C_H$	0.940	$1C_H$	1.260
$0D_H$	0.960	$1D_H$	1.280
$0E_H$	0.980	$1E_H$	1.300
$0F_H$	1.000 (*1)	$1F_H$	1.320

*1: Preset value

24.2 About DD2 Output Voltage Setting

- Address 01H DD2 is allocated as resisters for the DC/DC output voltage setting.
- The DC/DC output voltage setting of DD2 is controlled by writing data to address 01H.



address01_H: For DD2 output voltage setting

D_{03} to D_{00}: Set the output voltage

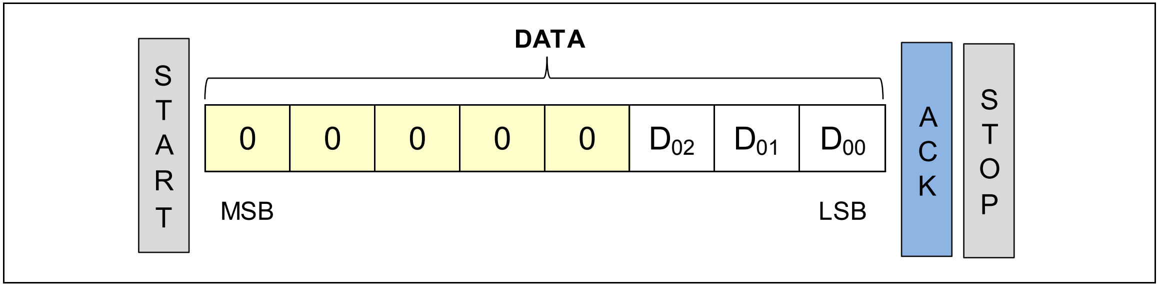
DD2 Output Voltage Setting Table

DATA	Output voltage (V)
00_H	1.200 (*1)
01_H	1.250
02_H	1.300
03_H	1.350 (*1)
04_H	1.400
05_H	1.450
06_H	1.500 (*1)
07_H	1.550
08_H	1.600
09_H	1.650
$0A_H$	1.700
$0B_H$	1.750
$0C_H$	1.800 (*1)
$0D_H$	1.850
$0E_H$	1.900
$0F_H$	1.950

*1: Preset value

24.3 About DD3 Output Voltage Setting

- Address 02_H DD3 is allocated as resisters for the DC/DC output voltage setting.
- The DC/DC output voltage setting of DD3 is controlled by writing data to address 02_H.



address02_H: For DD3 output voltage setting

D02 to D00: Set the output voltage

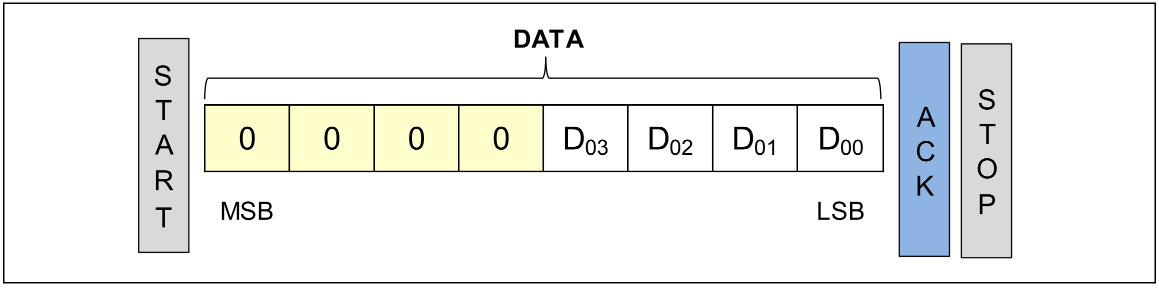
DD3 Output Voltage Setting Table

DATA	Output voltage (V)
00_H	2.80 (*1)
01_H	2.90
02_H	3.00 (*1)
03_H	3.10
04_H	3.20
05_H	3.30 (*1)
06_H	3.40
07_H	3.50 (*1)

*1: Preset value

24.4 About Soft Start Time

- Address 10_H to 12_H are allocated as registers for the soft start time control.
- The soft start time control is controlled by writing data to addresses 10_H to 12_H.



address10_H: For DD1 soft start time setting
address11_H: For DD2 soft start time setting
address12_H: For DD3 soft start time setting
address13_H: For DD4 soft start time setting

D_{03} to D_{00}: Set the soft start time

Tss=Tslp × Vset/Vdef (ms)

Tss : soft start time
Tslp : slope coefficient of soft start : refer to follow table
Vset : output voltage setting
Vdef : DD1=1.0, DD2=1.8, DD3= 3.3, DD4=1.0

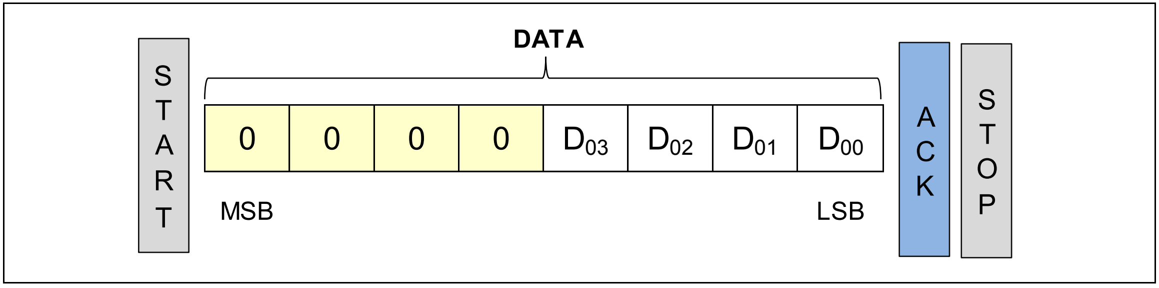
Soft Start Time Setting

DATA1	Tslp	Remarks
00_H	1.0	DD1,DD2,DD3,DD4 (*1)
01_H	2.0	
02_H	3.0	
03_H	4.0	
04_H	5.0	
05_H	6.0	
06_H	7.0	
07_H	8.0	
08_H	9.0	
09_H	10.0	
$0A_H$	11.0	
$0B_H$	12.0	
$0C_H$	13.0	
$0D_H$	14.0	
$0E_H$	15.0	
$0F_H$	16.0	

*1: Preset value

24.5 DC/DC Operation Mode

- Address 20_H is allocated as a register for the DC/DC operation mode control.
- The DC/DC operation mode is controlled by writing data to address 20_H.



address20_H: For DC/DC operation mode setting

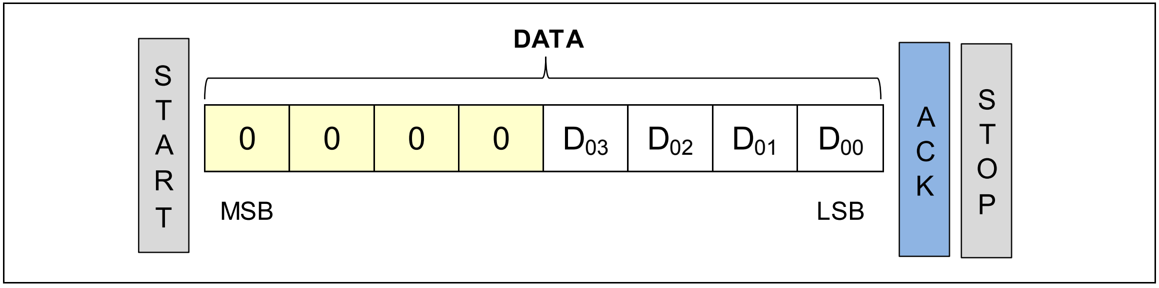
D_{01} to D_{00}: Set the DC/DC operation mode

Address	Bit	Description
20_H	D00	0: DD1 Fixed PWM (*1) 1: DD1 PFM/PWM
20_H	D01	0: DD2 Fixed PWM (*1) 1: DD2 PFM/PWM
20_H	D02	0: DD3 Fixed PWM (*1) 1: DD3 PFM/PWM
20_H	D03	0: DD4 Fixed PWM (*1) 1: DD4 PFM/PWM

*1: Preset value

24.6 ON/OFF for DC/DC

- Address 30_H is allocated as a register for the DC/DC ON/OFF.
- The DC/DC ON/OFF is controlled by writing data to address 30_H.



address30_H: For DC/DC ON/OFF

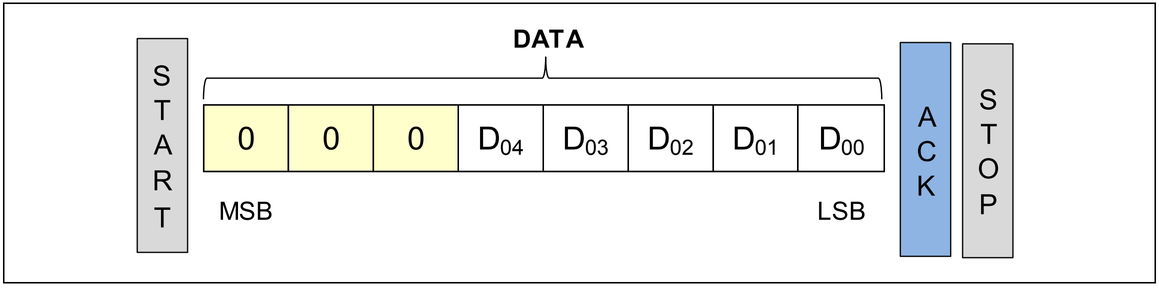
D_{02} to D_{00}: Set ON/OFF for DC/DC

Address	Bit	Description
30_H	D00	0: DD1 output OFF (*1) 1: DD1 output ON
30_H	D01	0: DD2 output OFF (*1) 1: DD2 output ON
30_H	D02	0: DD3 output OFF (*1) 1: DD3 output ON
30_H	D03	0: DD4 output OFF (*1) 1: DD4 output ON

*1: Preset value

24.7 About Error Monitor

- Address 40_H is allocated as error status monitor of each DC/DC output and thermal shut down.
- Address 40_H is read only resistor.



address40_H: For error monitor of each DC/DC output and thermal shut down

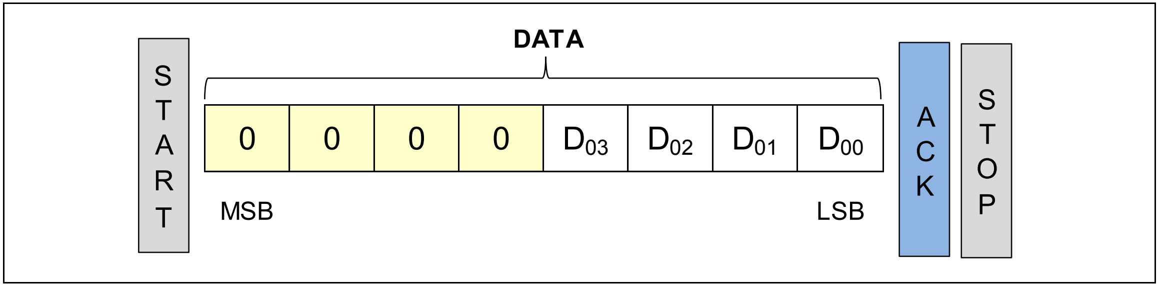
D_{04} to D_{00}: read only resistor. (Not allowed write resistor)

Address	Bit	Description
40_H	D00	0: DD1 OCP non detection (*1) 1: DD1 OCP detection
40_H	D01	0: DD2 OCP non detection (*1) 1: DD2 OCP detection
40_H	D02	0: DD3 OCP non detection (*1) 1: DD3 OCP detection
40_H	D03	0: DD4 OCP non detection (*1) 1: DD4 OCP detection
40_H	D04	0: TSD non detection (*1) 1: TSD detection

*1: Preset value

24.8 About Power Good Monitor

- Address 50_H is allocated as output monitor of each DC/DC output.
- Address 50_H is read only resistor.

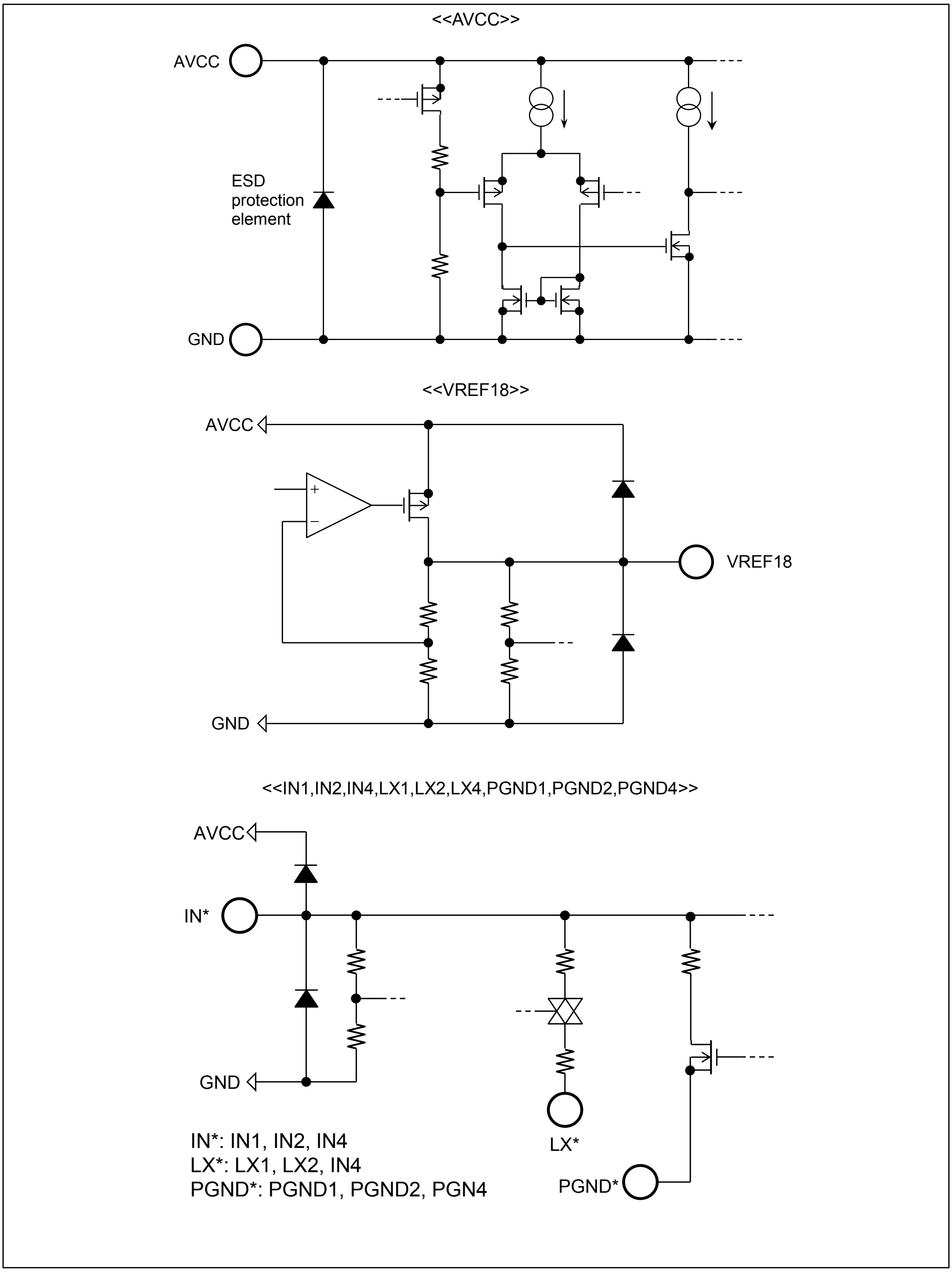


address50_H: For output monitor of each DC/DC output.
Detection level is over 93% of DCDC output voltage setting.
D_{04} to D_{00}: read only resistor. (Not allowed write resistor)

Address	Bit	Description
50_H	D00	0: DD1 non output (*1) 1: DD1 output
50_H	D01	0: DD2 non output (*1) 1: DD2 output
50_H	D02	0: DD3 non output (*1) 1: DD3 output
50_H	D03	0: DD4 non output (*1) 1: DD4 output

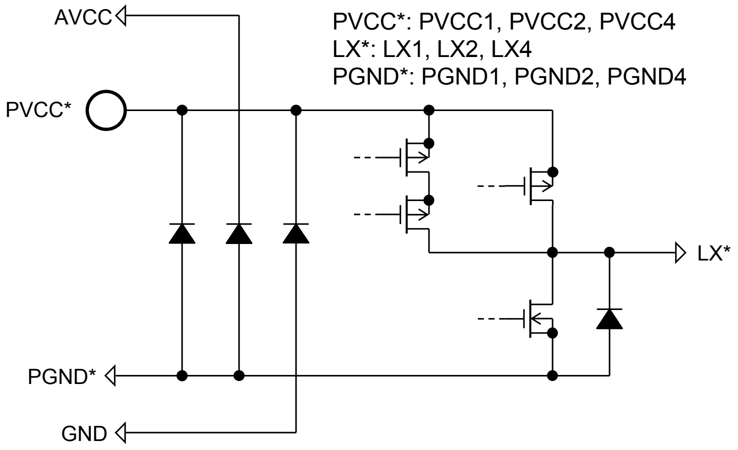
*1: Preset value

25. I/O Pin Equivalent Circuit Diagram



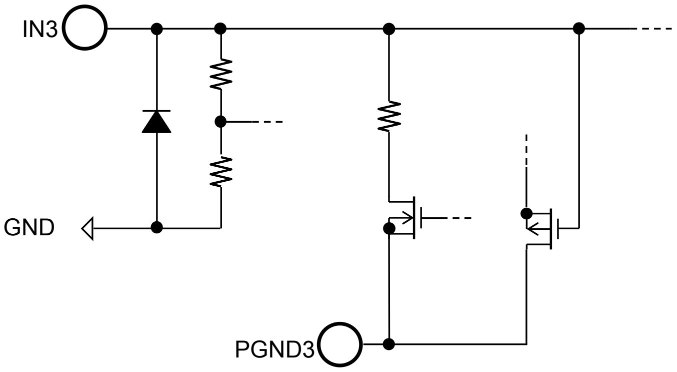
IN*: IN1, IN2, IN4
LX*: LX1, LX2, IN4
PGND*: PGND1, PGND2, PGN4

<<PVCC1,PVCC2,PVCC4>

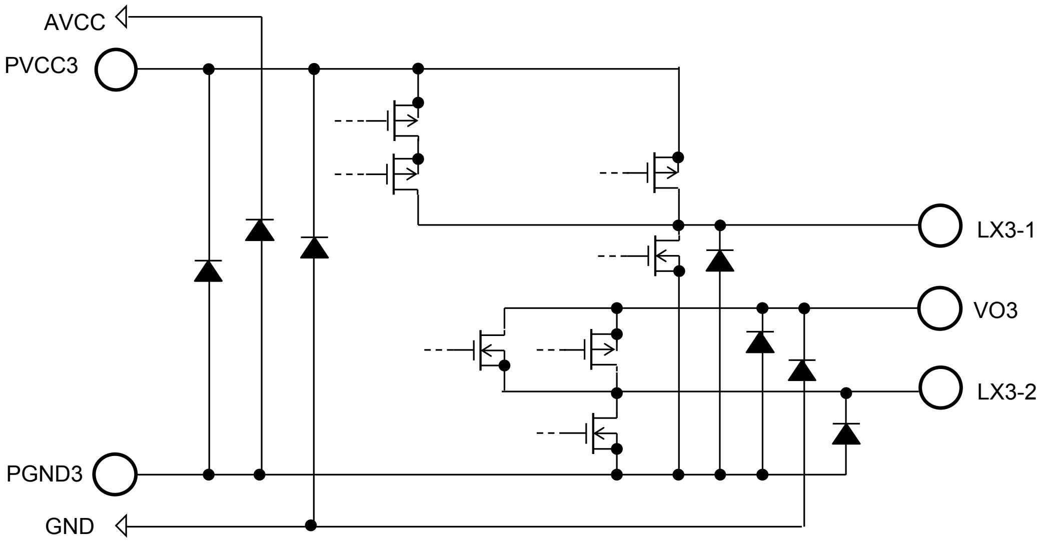


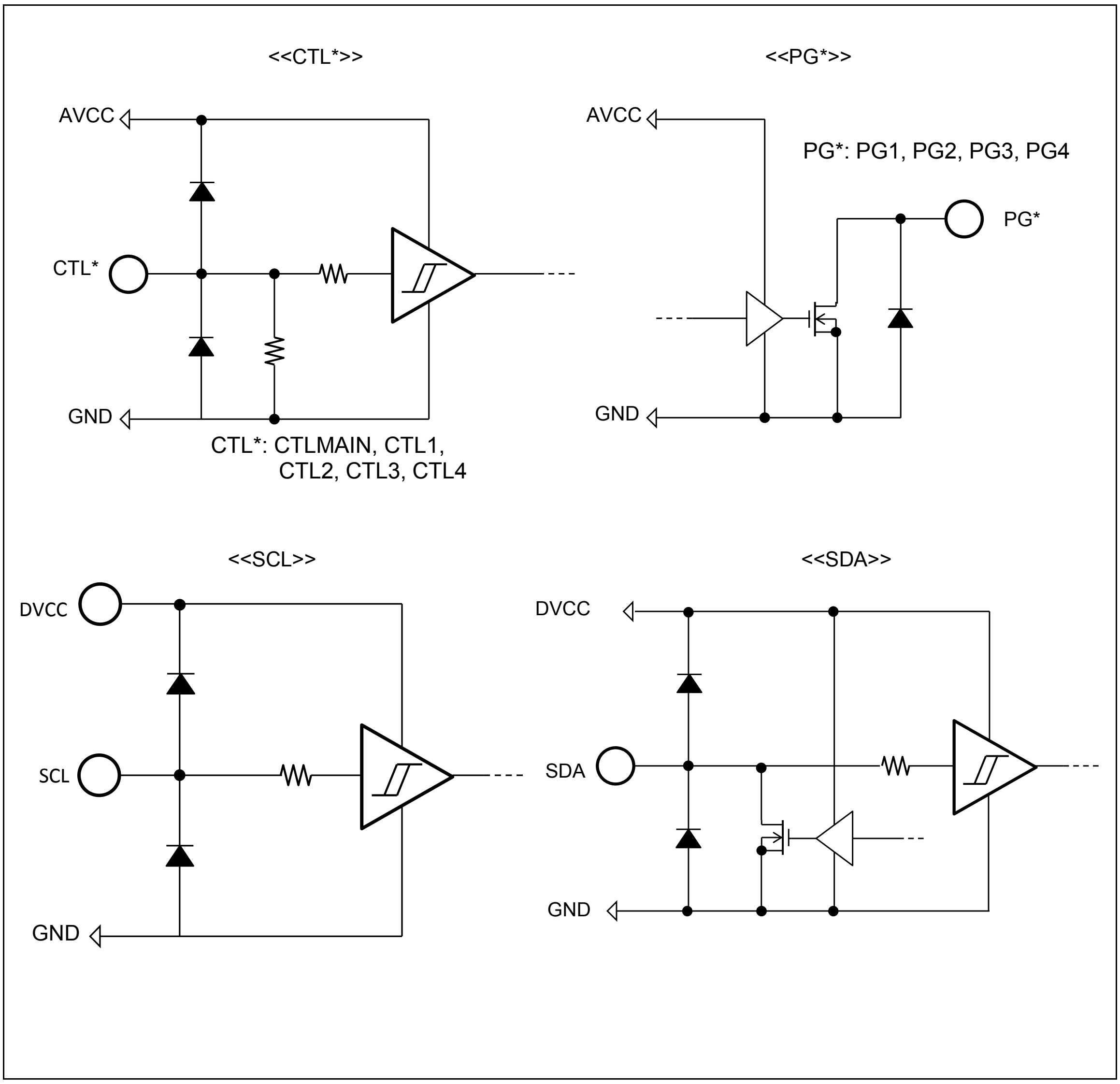
PVCC*: PVCC1, PVCC2, PVCC4
LX*: LX1, LX2, LX4
PGND*: PGND1, PGND2, PGND4

<<IN3,PGND3 >



<<PVCC3,LX3-1,LX3-2,VO3>>




<<CTL*>>
AVCC
CTL*
GND
CTL*: CTLMAIN, CTL1,
CTL2, CTL3, CTL4
<<PG*>>
AVCC
PG*: PG1, PG2, PG3, PG4
PG*
GND
<<SCL>>
DVCC
SCL
GND
<<SDA>>
DVCC
SDA
GND

26. Measurement Circuit for Characteristics of General Operation

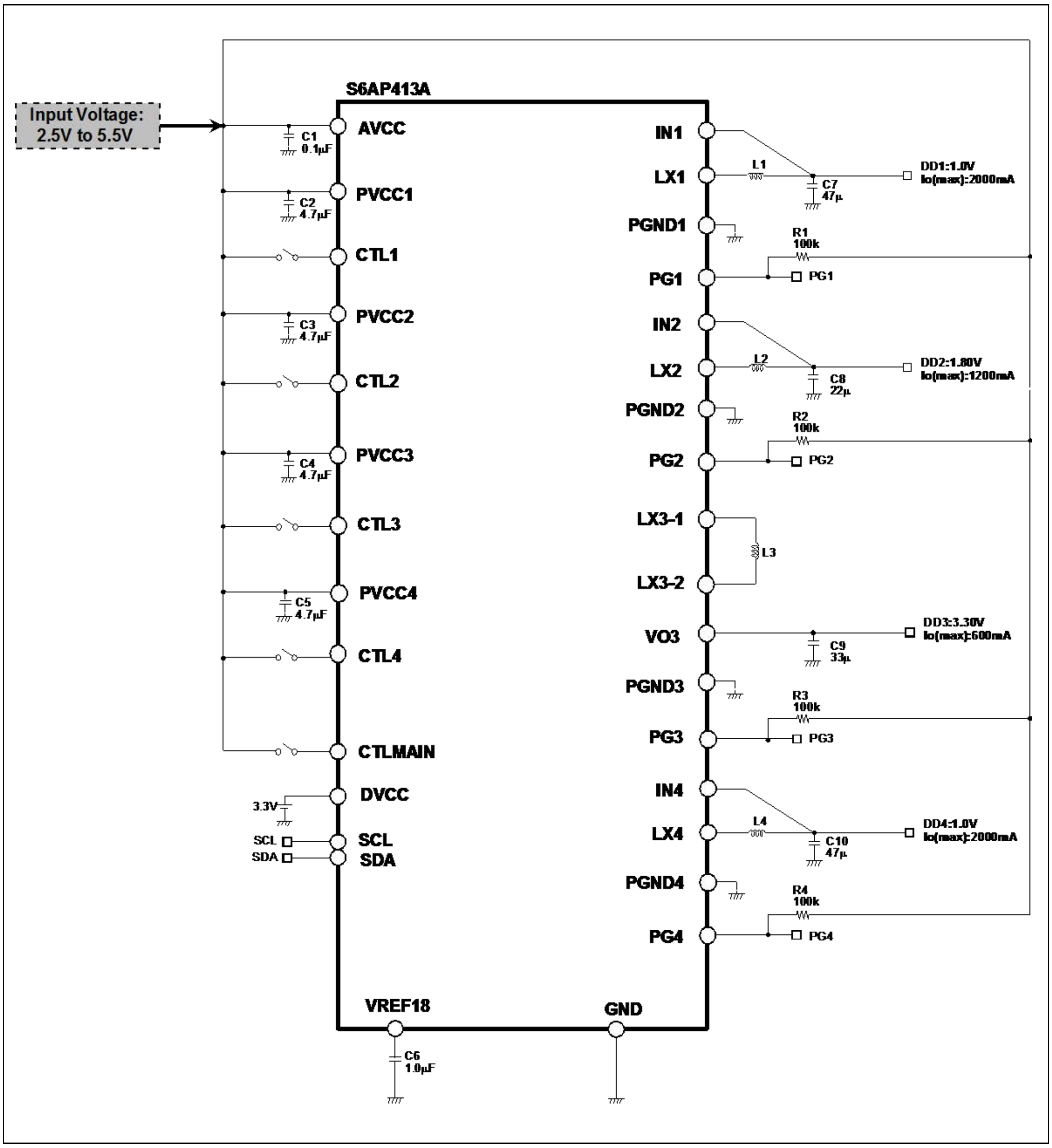


Table 26-1 Parts list

Symbol	Parts	Part number	specifications	vendor
L1	Inductor	1278AS-H-1R0M	1.0μH	TOKO
L2	Inductor	1278AS-H-1R0M	1.0μH	TOKO
L3	Inductor	1278AS-H-1R0M	1.0μH	TOKO
L4	Inductor	1278AS-H-1R0M	1.0μH	TOKO
C1	Ceramic Capacitor	C1608X5R1H104K	0.1μF	TDK
C2	Ceramic Capacitor	C1608X5R1V475K	4.7μF	TDK
C3	Ceramic Capacitor	C1608X5R1V475K	4.7μF	TDK
C4	Ceramic Capacitor	C1608X5R1V475K	4.7μF	TDK
C5	Ceramic Capacitor	C1608X5R1V475K	4.7μF	TDK
C6	Ceramic Capacitor	C2012X5R1A336M	1.0μF	TDK
C7	Ceramic Capacitor	C2012X5R1A476M	47μF	TDK
C8	Ceramic Capacitor	C1608X5R1A226M	22μF	TDK
C9	Ceramic Capacitor	C2012X5R1A336M	33μF	TDK
C10	Ceramic Capacitor	C2012X5R1A476M	47μF	TDK
R1	Resistor	RR0816P-104-D	100kΩ	SSM
R2	Resistor	RR0816P-104-D	100kΩ	SSM
R3	Resistor	RR0816P-104-D	100kΩ	SSM
R4	Resistor	RR0816P-104-D	100kΩ	SSM

TOKO : TOKO, INC.
TDK : TDK Corporation
SSM : SUSUMU CO., LTD.

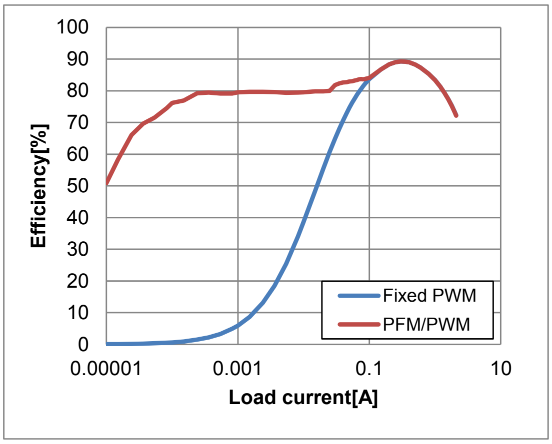
27. Reference Data

DCDC convertor efficiency data

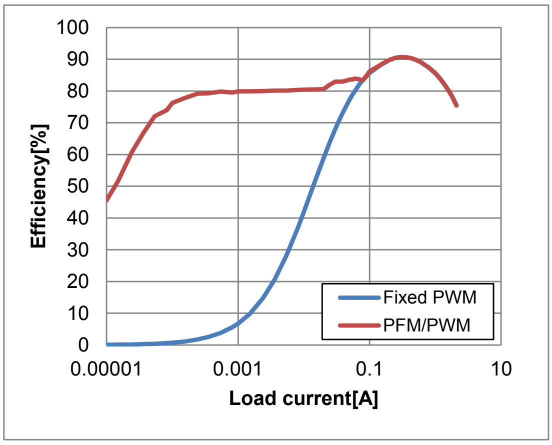
Inductor and capacitor value refer to section 26.

■ **DD1,DD4**

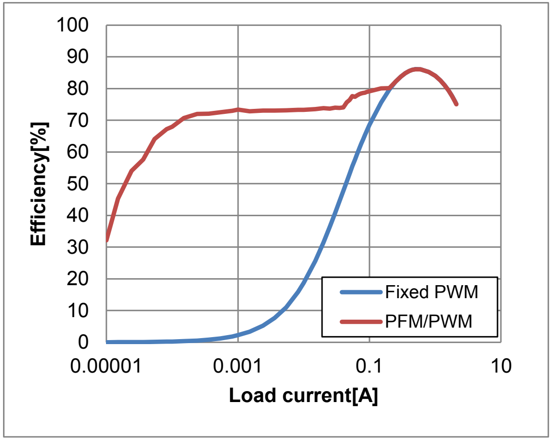
Input voltage = 3.3V, Vo = 1.0V setting



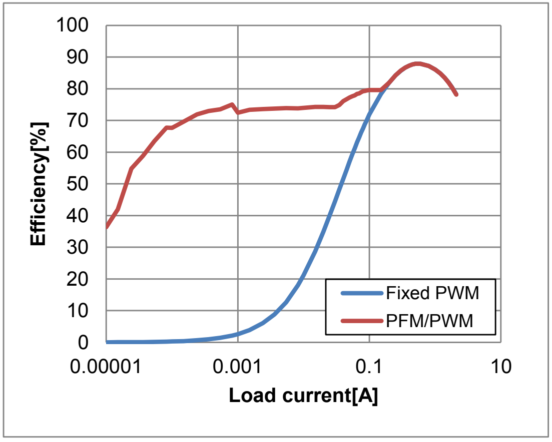
Input voltage = 3.3V, Vo=1.2V setting



Input voltage = 5.5V, Vo = 1.0V setting

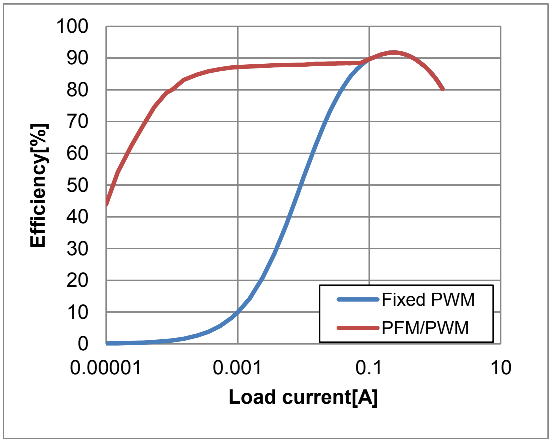


Input voltage = 5.5V, Vo = 1.2V setting

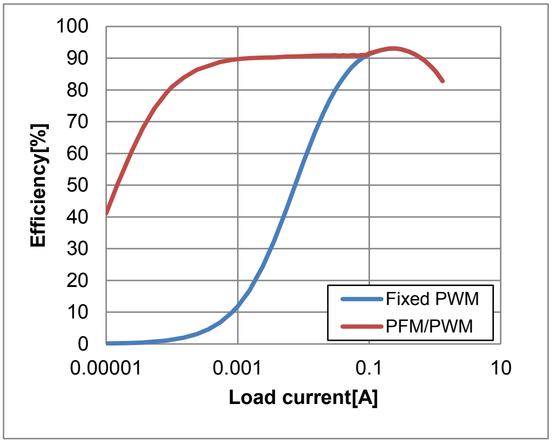


■ **DD2**

Input Voltage = 3.3V, Vo = 1.5V setting

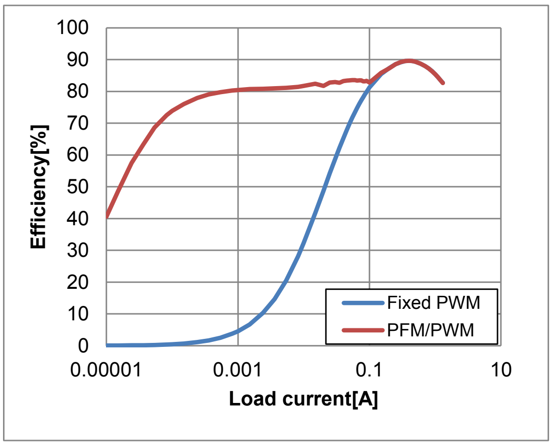


Input voltage = 3.3V, Vo = 1.8V setting

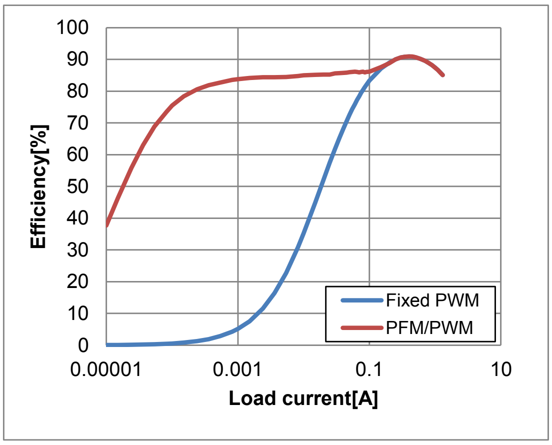


■ DD2

Input voltage = 5.5V, Vo = 1.5V setting

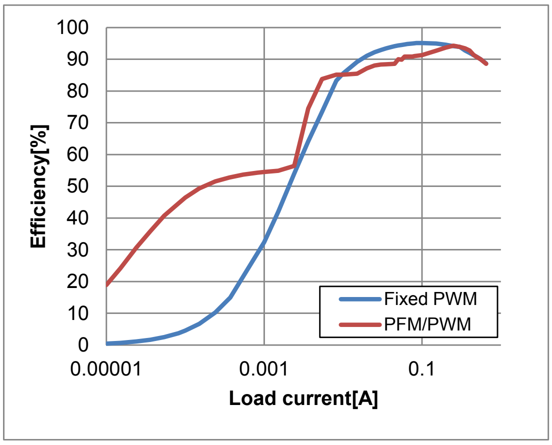


Input Voltage = 5.5V, Vo = 1.8V setting

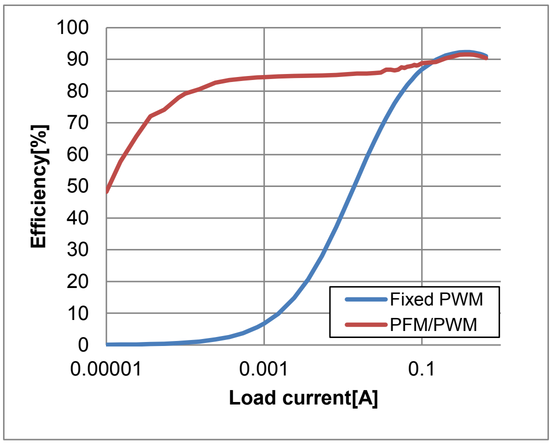


■ DD3

Input voltage = 3.3V, Vo = 3.3V setting



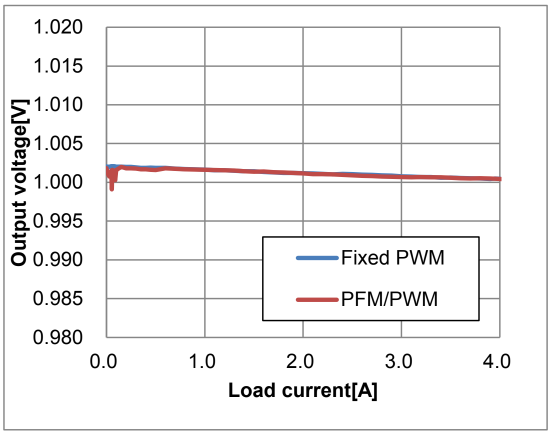
Input Voltage = 5.5V, Vo = 3.3V setting



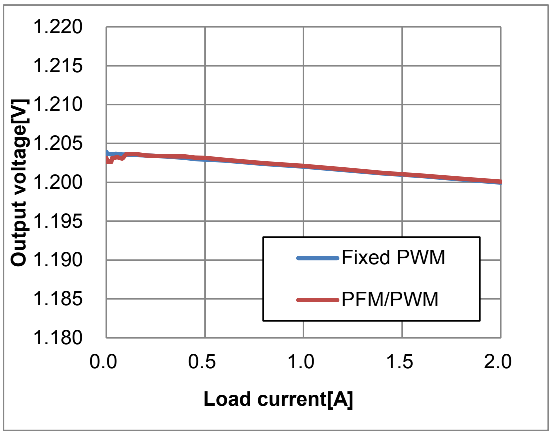
DCDC convertor regulation data

■ DD1,DD4

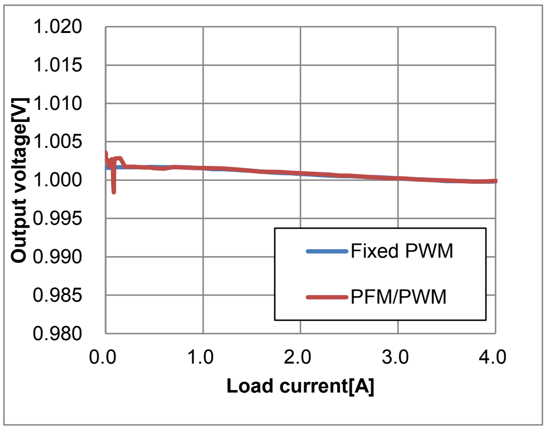
Input voltage = 3.3V, Vo = 1.0V setting



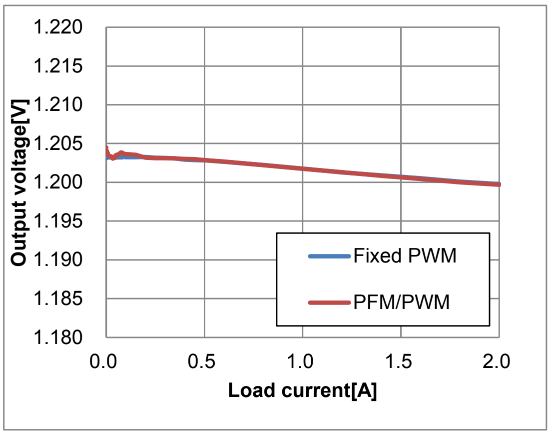
Input voltage = 3.3V, Vo=1.2V setting



Input voltage = 5.5V, Vo = 1.0V setting

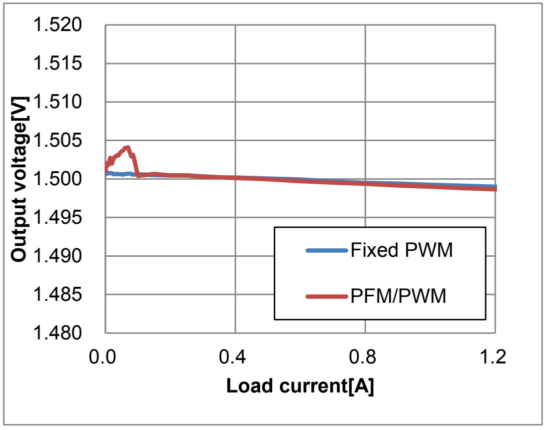


Input voltage = 5.5V, Vo = 1.2V setting

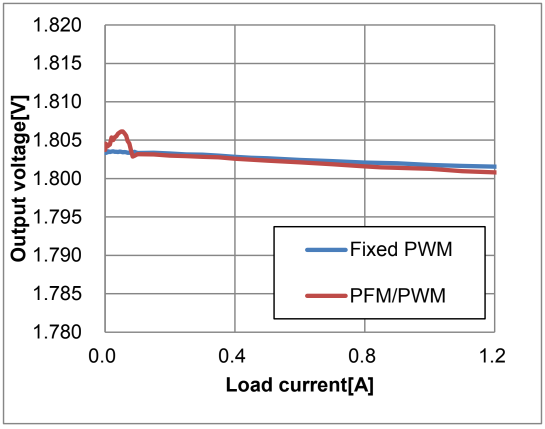


■ DD2

Input Voltage = 3.3V, Vo = 1.5V setting

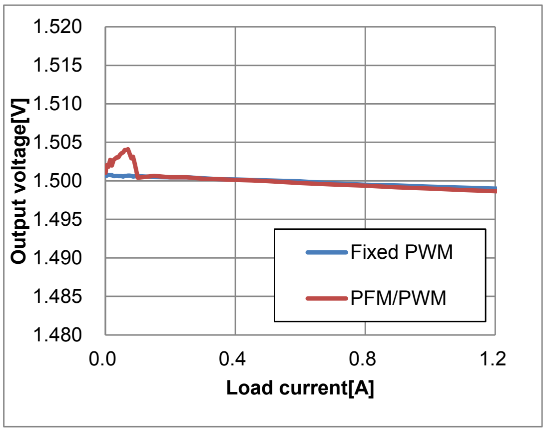


Input voltage = 3.3V, Vo = 1.8V setting

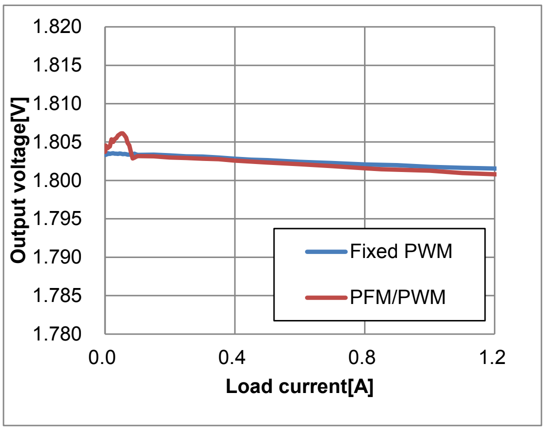


■ DD2

Input voltage = 5.5V, Vo = 1.5V setting

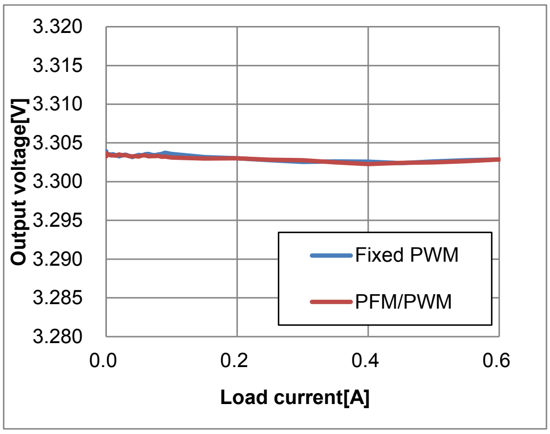


Input Voltage = 5.5V, Vo = 1.8V setting

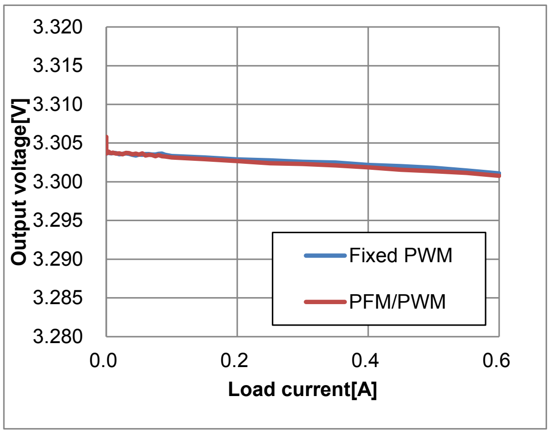


■ DD3

Input voltage = 3.3V, Vo = 3.3V setting



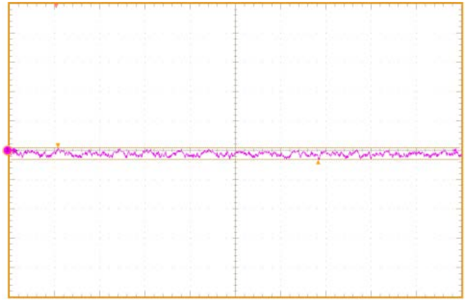
Input Voltage = 5.5V, Vo = 3.3V setting



DCDC convertor output ripple voltage

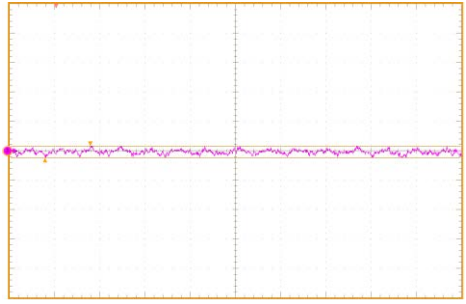
■ DD1, DD4

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 0mA , Fixed PWM



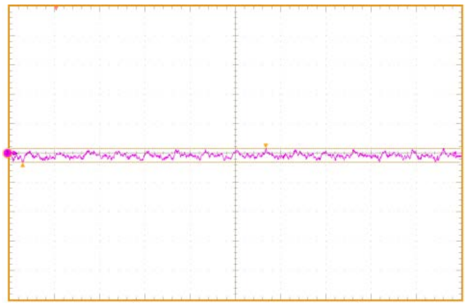
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo=1.0V setting
Load current = 2000mA, Fixed PWM



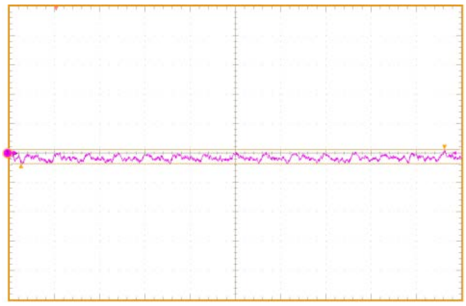
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 0mA , Fixed PWM



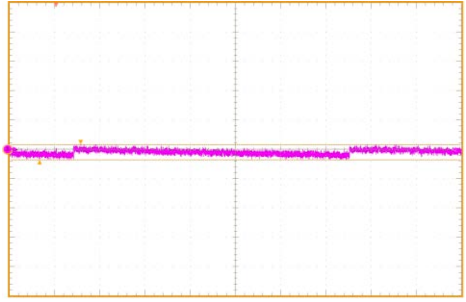
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 2000mA, Fixed PWM



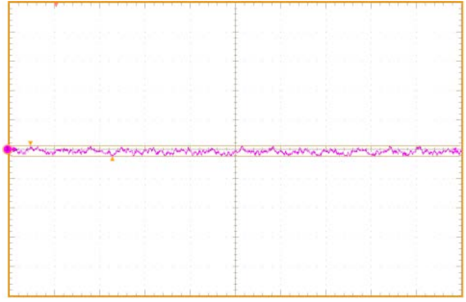
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 0mA , PFM/PWM



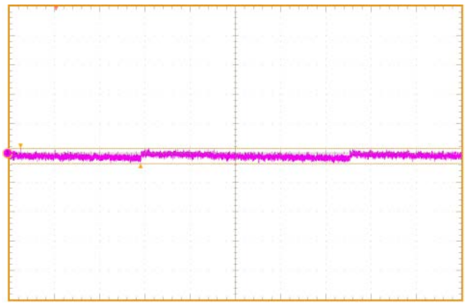
10mV/div, 2ms/div

Input voltage = 3.3V, Vo=1.0V setting
Load current = 2000mA,PFM/PWM



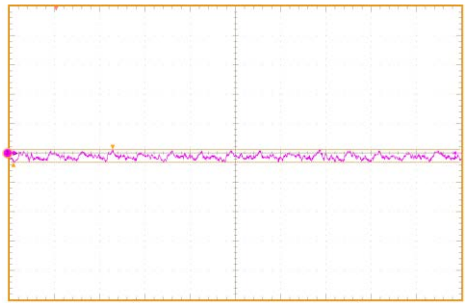
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 2000mA,PFM/PWM

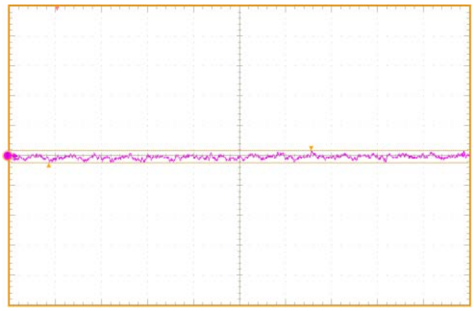


10mV/div, 0.5µs/div

DD2

Input voltage = 3.3V, Vo = 1.8V setting

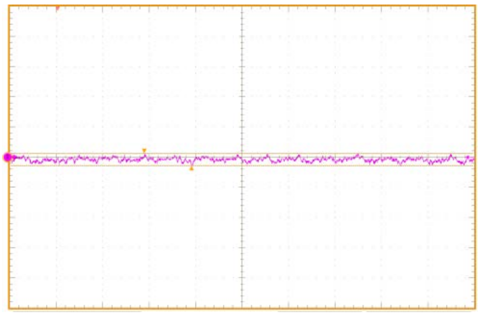
Load current = 0mA , Fixed PWM



10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo=1.8V setting

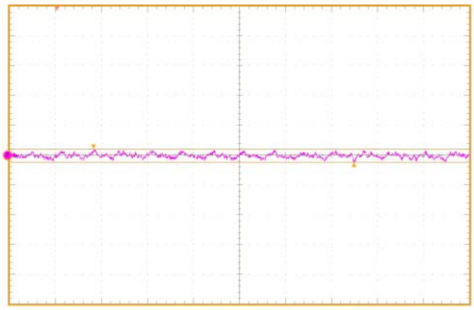
Load current = 1200mA, Fixed PWM



10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.8V setting

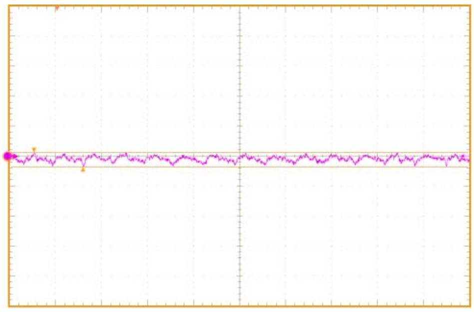
Load current = 0mA , Fixed PWM



10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.8V setting

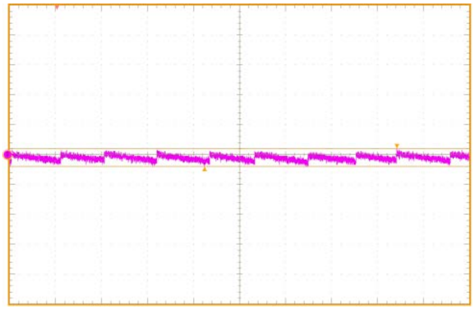
Load current =1200mA, Fixed PWM



10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo = 1.8V setting

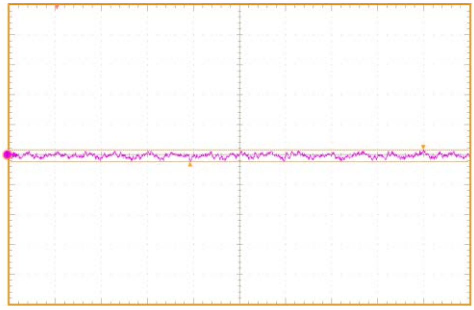
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

Input voltage = 3.3V, Vo=1.8V setting

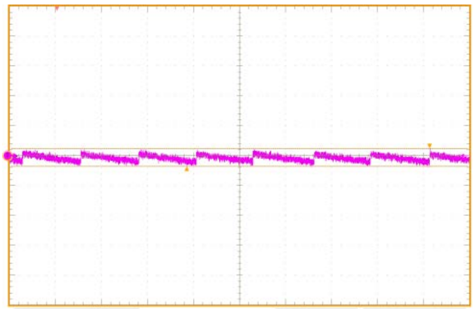
Load current =1200mA,PFM/PWM



10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.8V setting

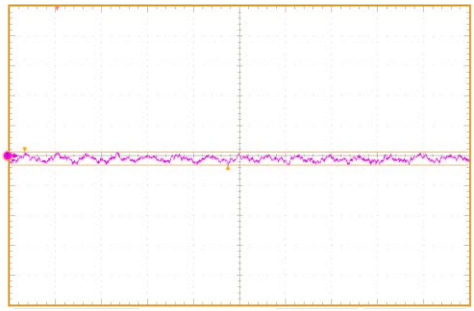
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

Input voltage = 5.5V, Vo = 1.8V setting

Load current = 1200mA,PFM/PWM

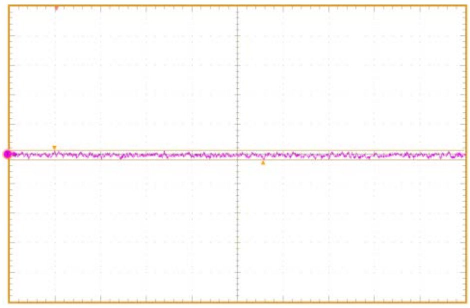


10mV/div, 0.5µs/div

DD3

Input voltage = 3.3V, Vo = 3.3V setting

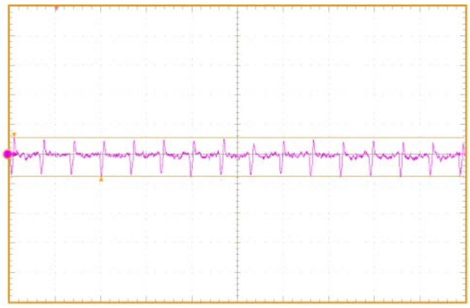
Load current = 0mA , Fixed PWM



10mV/div, 0.5μs/div

Input voltage = 3.3V, Vo=3.3V setting

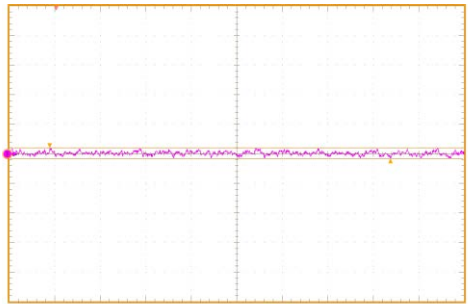
Load current = 600mA, Fixed PWM



10mV/div, 0.5μs/div

Input voltage = 5.5V, Vo = 3.3V setting

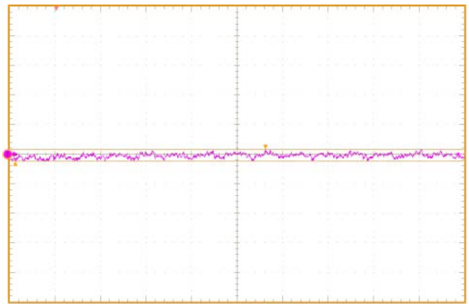
Load current = 0mA , Fixed PWM



10mV/div, 0.5μs/div

Input voltage = 5.5V, Vo = 3.3V setting

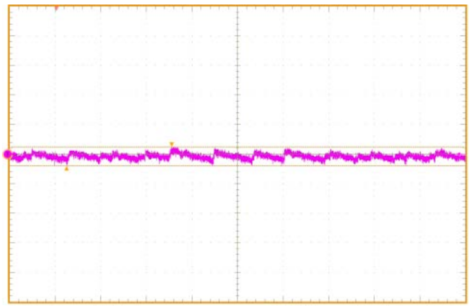
Load current =600mA, Fixed PWM



10mV/div, 0.5μs/div

Input voltage = 3.3V, Vo = 3.3V setting

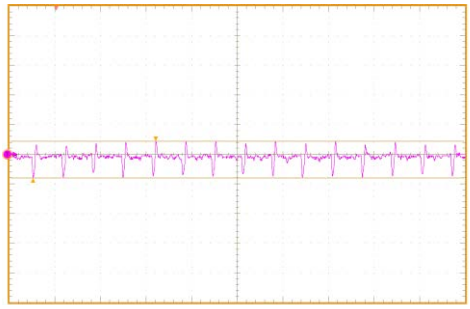
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

Input voltage = 3.3V, Vo=3.3V setting

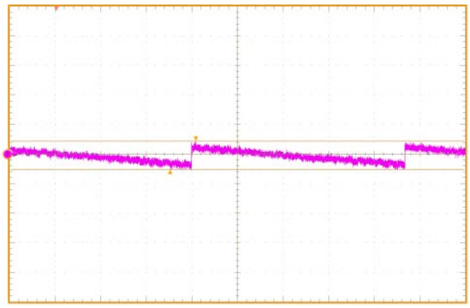
Load current = 600mA,PFM/PWM



10mV/div, 0.5μs/div

Input voltage = 5.5V, Vo = 1.0V setting

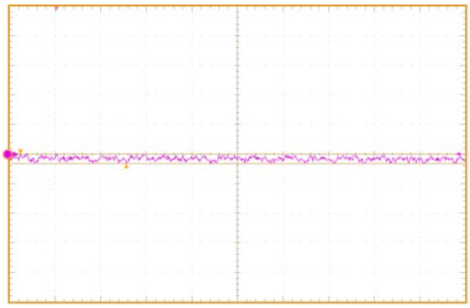
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

Input voltage = 3.3V, Vo =3.3V setting

Load current = 600mA,PFM/PWM

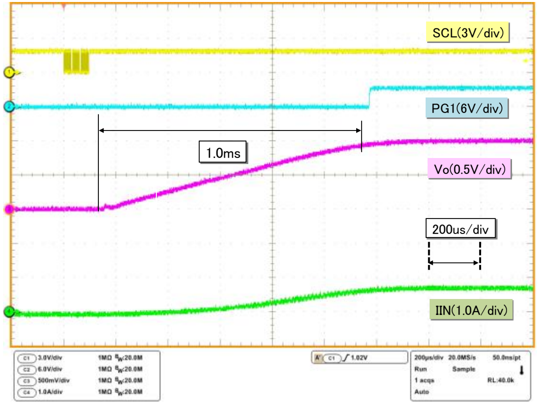


10mV/div, 0.5μs/div

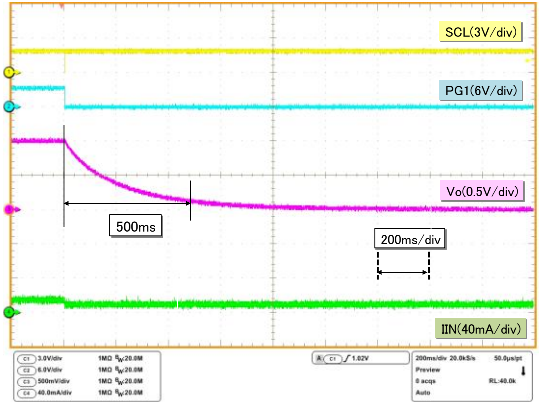
DCDC convertor enable/disable

■ DD1,DD4(Fixed PWM)

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 2000mA, Tss = 1msec setting

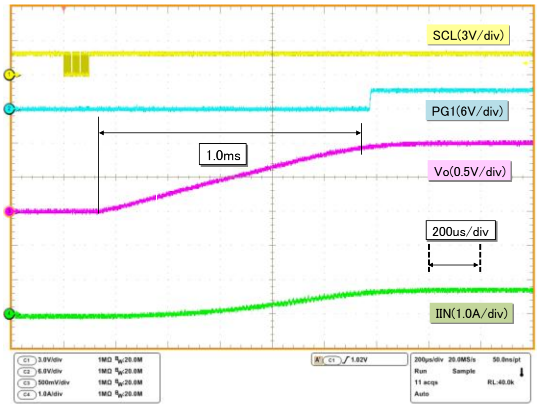


Input voltage = 3.3V, Vo=1.0V setting
Load current = 0mA, Tss = 1msec setting

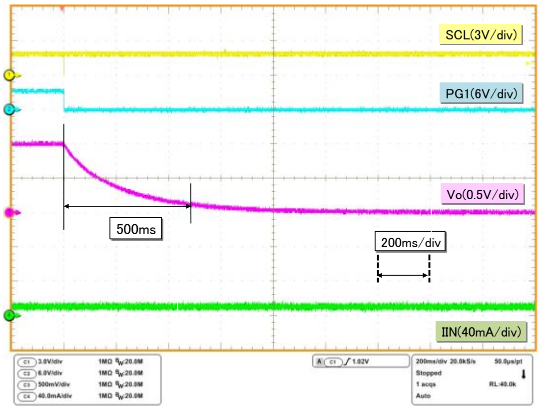


■ DD1,DD4(PFM/PWM)

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 2000mA, Tss = 1msec setting

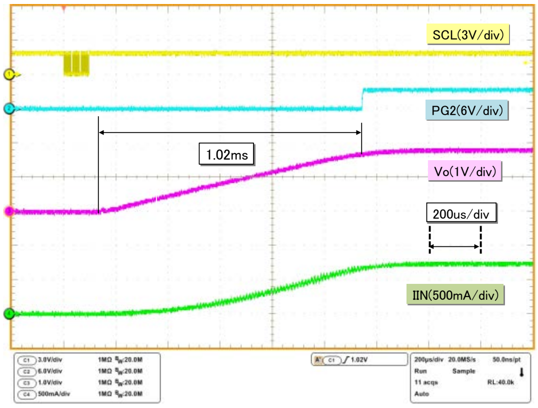


Input voltage = 3.3V, Vo=1.0V setting
Load current = 0mA, Tss = 1msec setting

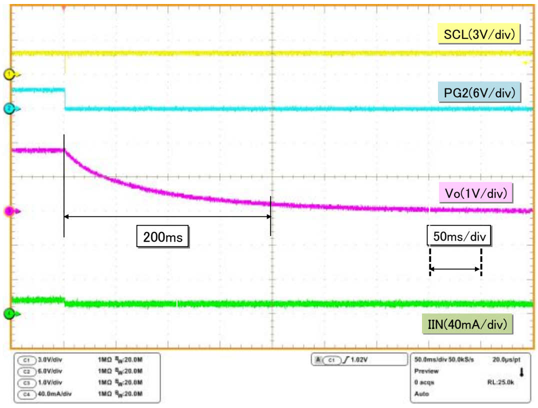


■ DD2(Fixed PWM)

Input voltage = 3.3V, Vo = 1.8V setting
Load current = 1200mA, Tss = 1msec setting



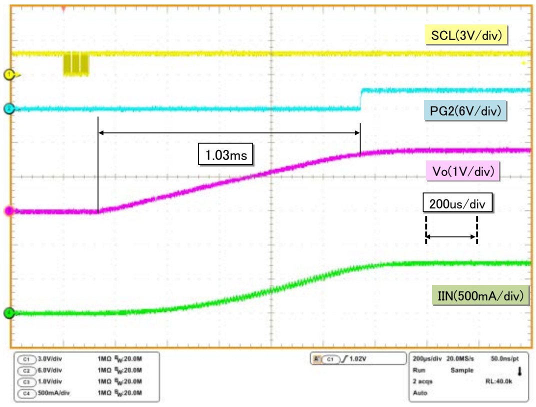
Input voltage = 3.3V, Vo=1.8V setting
Load current = 0mA, Tss = 1msec setting



■ DD2(PFM/ PWM)

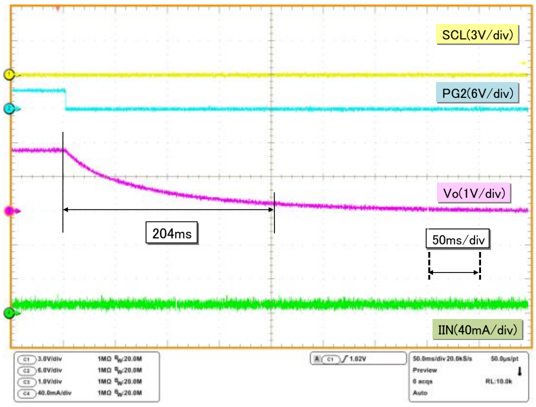
Input voltage = 3.3V, Vo = 1.8V setting

Load current = 1200mA, Tss = 1msec setting



Input voltage = 3.3V, Vo=1.8V setting

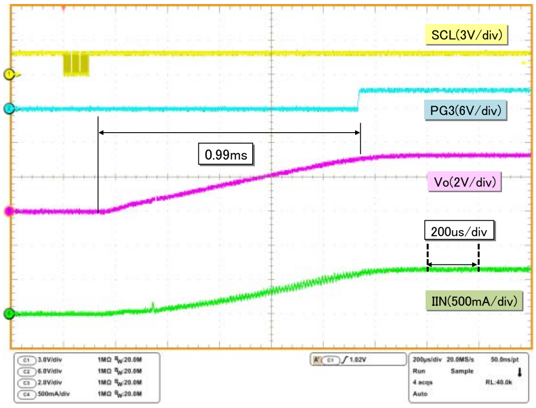
Load current = 0mA, Tss = 1msec setting



■ DD3 (Fixed PWM)

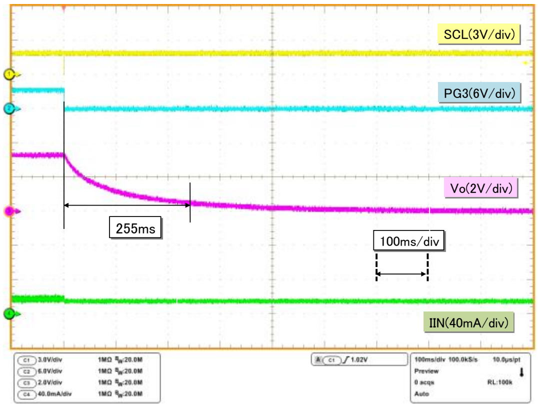
Input voltage = 3.3V, Vo = 3.3V setting

Load current = 600mA, Tss = 1msec setting



Input voltage = 3.3V, Vo=3.3 V setting

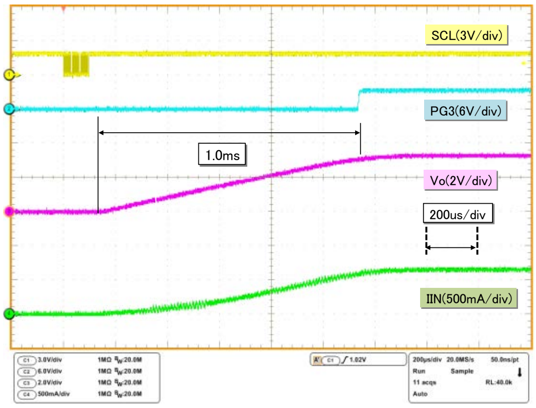
Load current = 0mA, Tss = 1msec setting



■ DD3 (PFM/PWM)

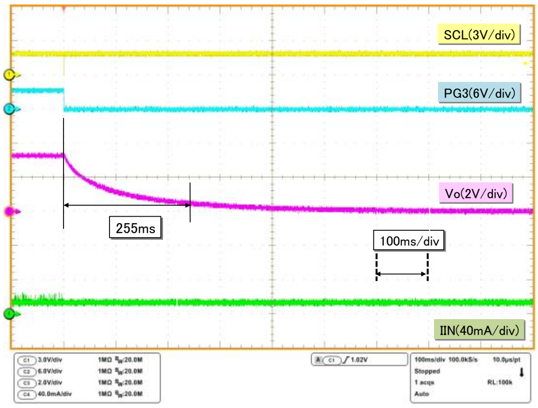
Input voltage = 3.3V, Vo = 3.3V setting

Load current = 600mA, Tss = 1msec setting



Input voltage = 3.3V, Vo=3.3 V setting

Load current = 0mA, Tss = 1msec setting

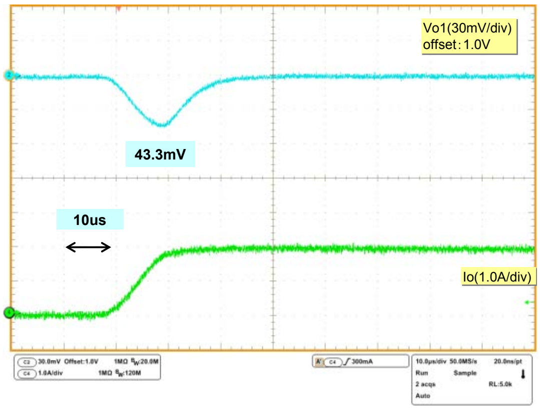


DCDC convertor load transient

■ DD1(Fixed PWM)

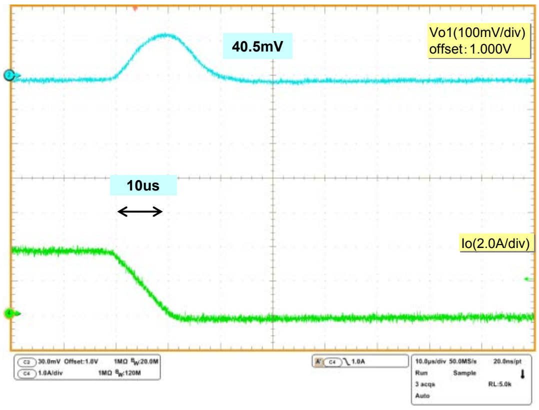
Input voltage = 3.3V, Vo = 1.0V setting

Load current = from 0mA to 2000mA per 10usec



Input voltage = 3.3V, Vo=1.0V setting

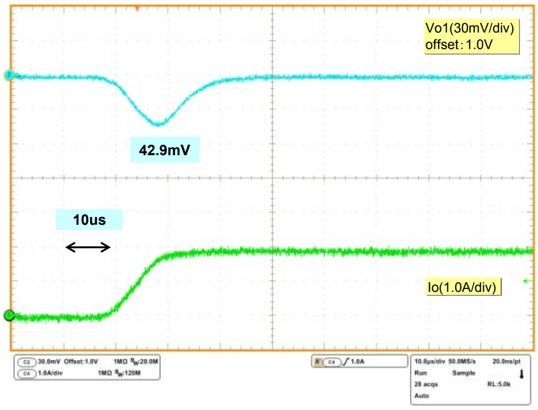
Load current = from 2000mA to 0mA per 10usec



■ DD1(PFM/PWM)

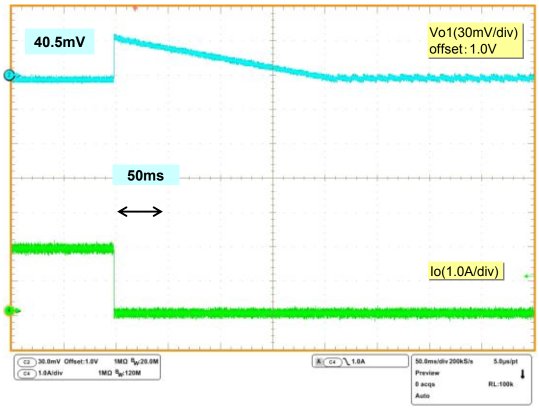
Input voltage = 3.3V, Vo = 1.0V setting

Load current = from 0mA to 2000mA per 10usec



Input voltage = 3.3V, Vo=1.0V setting

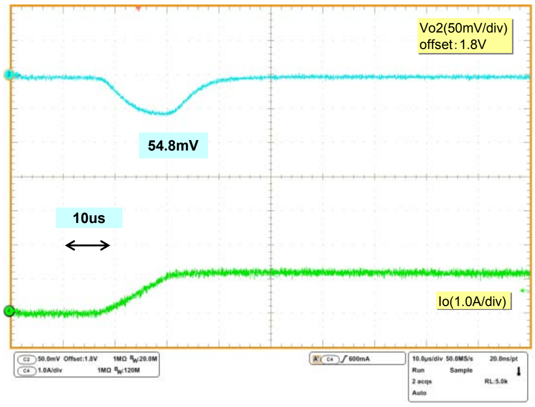
Load current = from 2000mA to 0mA per 10usec



■ DD2(Fixed PWM)

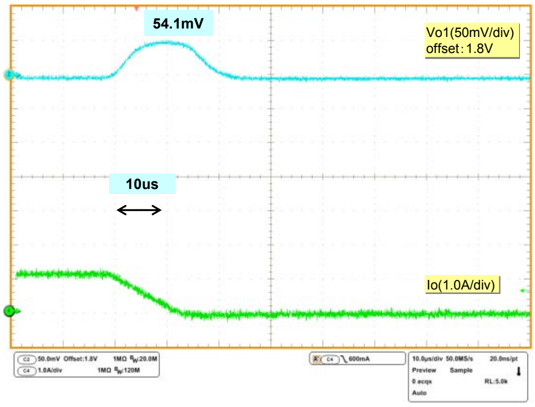
Input voltage = 3.3V, Vo = 1.8V setting

Load current = from 0mA to 1200mA per 10usec



Input voltage = 3.3V, Vo=1.8V setting

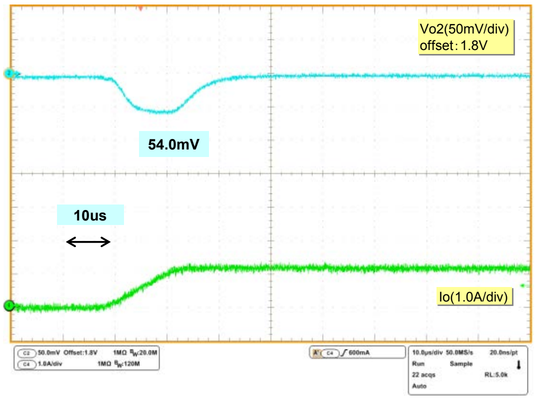
Load current = from 1200mA to 0mA per 10usec



■ DD2(PFM/ PWM)

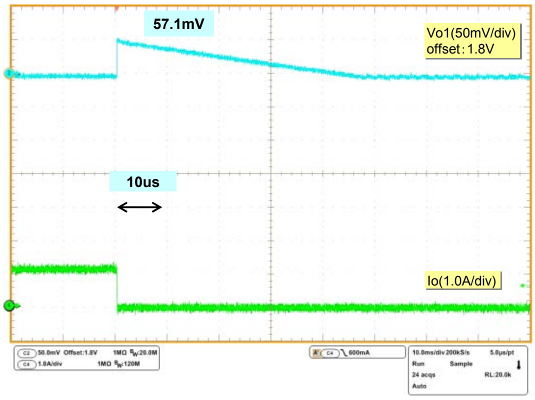
Input voltage = 3.3V, Vo = 1.8V setting

Load current = from 0mA to 1200mA per 10usec



Input voltage = 3.3V, Vo=1.8V setting

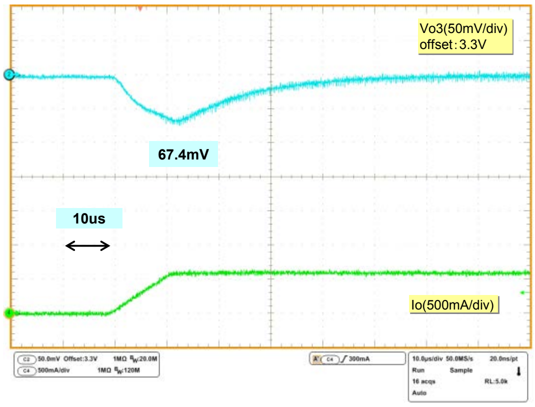
Load current = from 1200mA to 0mA per 10usec



■ DD3 (Fixed PWM)

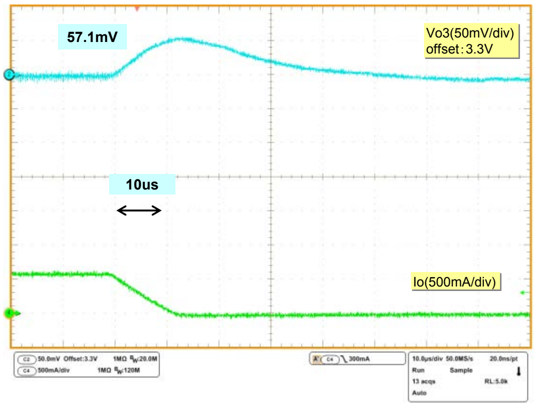
Input voltage = 3.3V, Vo = 3.3V setting

Load current = 600mA, Tss = 1msec setting



Input voltage = 3.3V, Vo=3.3 V setting

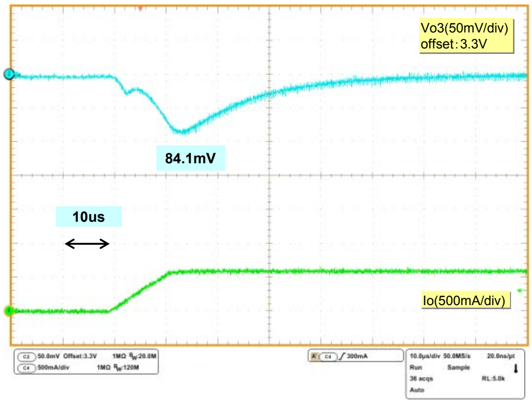
Load current = 0mA, Tss = 1msec setting



■ DD3 (Fixed PWM)

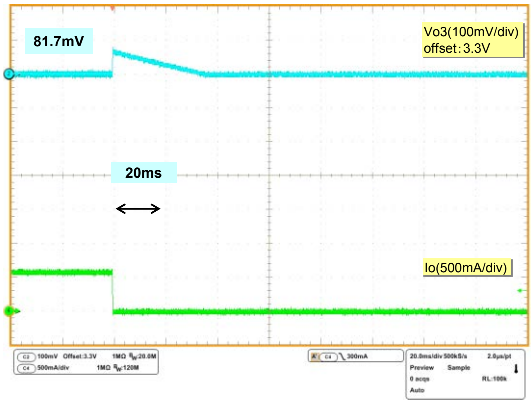
Input voltage = 3.3V, Vo = 3.3V setting

Load current = 600mA, Tss = 1msec setting



Input voltage = 3.3V, Vo=3.3 V setting

Load current = 0mA, Tss = 1msec setting

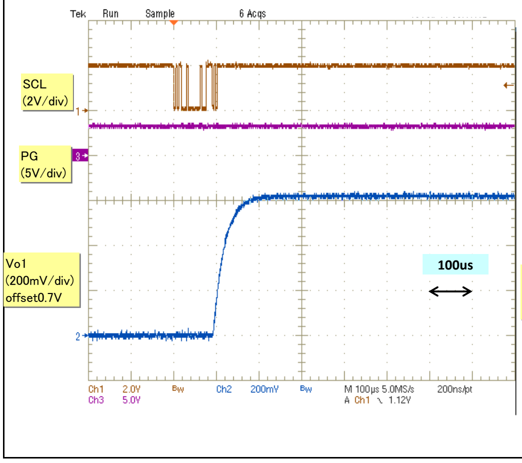


DCDC convertor DVFS function

■ DD1 (Fixed PWM)

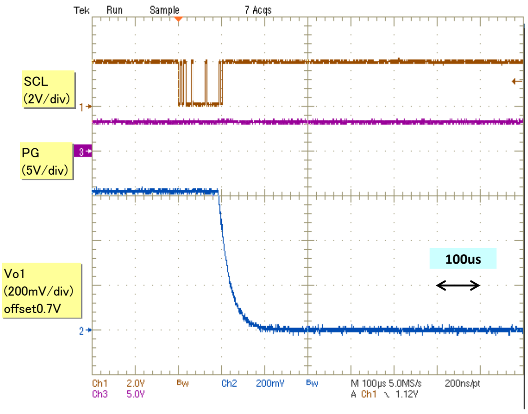
Input voltage = 3.3V,

Vo =from 0.7V to 1.32V setting by I2C



Input voltage = 3.3V

Vo =from 1.32V to 0.7V setting by I2C



28. Ordering Information

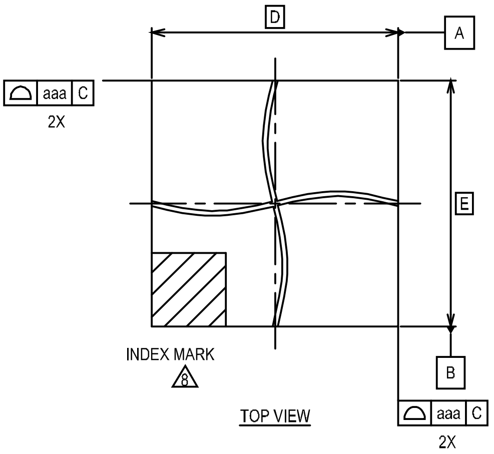
Table 28-1 Ordering Information

Part number	Package	Remarks
S6SAP413A18	32-pin plastic QFN (WNT032)	
S6SAP413A19		
S6SAP413A1A		
S6SAP413A1B		
S6SAP413A28		
S6SAP413A29		
S6SAP413A2A		
S6SAP413A2B		
S6SAP413A38		
S6SAP413A39		
S6SAP413A3A		
S6SAP413A3B		
S6SAP413A5A		
S6SAP413A5B		
S6SAP413A69		
S6SAP413A6A		
S6SAP413A6B		
S6SAP413A79		
S6SAP413A7A		
S6SAP413A7B		
S6SAP413A9A		
S6SAP413A9B		
S6SAP413AAA		
S6SAP413AAB		
S6SAP413ABA		
S6SAP413ABB		
S6SAP413ADB		
S6SAP413AEB		
S6SAP413AFB		

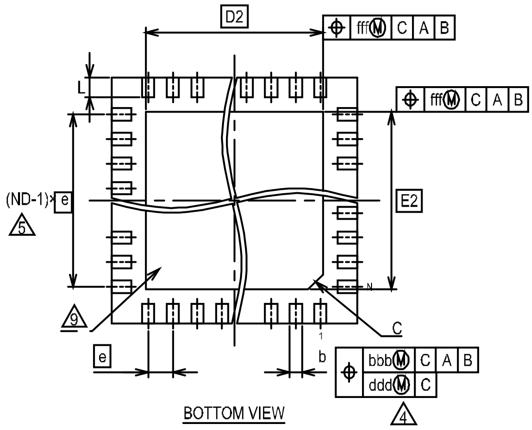
29. Preset Code List

Preset code	DD1 Output Voltage Preset code value	DD2 Output Voltage Preset code value	DD3 Output Voltage Preset code value	DD3 Output Voltage Preset code value
18	0.90V	1.35V	3.30V	0.90V
19	0.90V	1.35V	3.30V	1.00V
1A	0.90V	1.35V	3.30V	1.10V
1B	0.90V	1.35V	3.30V	1.20V
28	0.90V	1.50V	3.30V	0.90V
29	0.90V	1.50V	3.30V	1.00V
2A	0.90V	1.50V	3.30V	1.10V
2B	0.90V	1.50V	3.30V	1.20V
38	0.90V	1.80V	3.30V	0.90V
39	0.90V	1.80V	3.30V	1.00V
3A	0.90V	1.80V	3.30V	1.10V
3B	0.90V	1.80V	3.30V	1.20V
59	1.00V	1.35V	3.30V	1.00V
5A	1.00V	1.35V	3.30V	1.10V
5B	1.00V	1.35V	3.30V	1.20V
69	1.00V	1.50V	3.30V	1.00V
6A	1.00V	1.50V	3.30V	1.10V
6B	1.00V	1.50V	3.30V	1.20V
79	1.00V	1.80V	3.30V	1.00V
7A	1.00V	1.80V	3.30V	1.10V
7B	1.00V	1.80V	3.30V	1.20V
9A	1.10V	1.35V	3.30V	1.10V
9B	1.10V	1.35V	3.30V	1.20V
AA	1.10V	1.50V	3.30V	1.10V
AB	1.10V	1.50V	3.30V	1.20V
BA	1.10V	1.80V	3.30V	1.10V
BB	1.10V	1.80V	3.30V	1.20V
DB	1.20V	1.35V	3.30V	1.20V
EB	1.20V	1.50V	3.30V	1.20V
FB	1.20V	1.80V	3.30V	1.20V

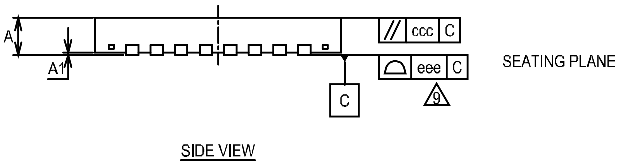
30. Package Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.75	PROFILE
A_1	0.00	—	0.05	TERMINAL HEIGHT
D		5.00 BSC.		BODY SIZE
E		5.00 BSC.		BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D_2		3.60 BSC.		EXPOSED PAD SIZE
E_2		3.60 BSC.		EXPOSED PAD SIZE
e		0.50 BSC.		TERMINAL PITCH
n		32		TERMINAL COUNT
L	0.33	0.40	0.47	TERMINAL LENGTH
C		C0.30		EXPOSED PAD CHAMFER
aaa		0.07		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.05		
fff		0.10		

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

31. Layout

Consider the points listed below and do the layout design.

- Provide the ground plane as much as possible on the IC mounted face. GND and PGNDx provide the through hole proximal to GND and PGNDx pins of IC, and connect it with GND of internal layer.
- Provide the power plane as much as possible to lower impedance of VCC.
- Play the most attention to the loop composed of input capacitor (CPVCCx) and SWFET. Input capacitor (CPVCCx) connected with PVCCx should be placed close to the pin as much as possible to make the current loop as small as possible. Also connect the GND pin of the input capacitor with PGNDx.
- Output capacitor (CVO3) connected with VO3 should be placed close to the pin as much as possible. Also connect the GND pin of the output capacitor with PGND3.
- GND pins of the switching system parts provide the through hole at the proximal place, and connect it with GND of internal layer.
- By-pass capacitor (CVREF, CAVCC) connected with VREF and AVCC should be placed close to the pin as much as possible. Also connect the GND pin of the by-pass capacitor with GND of internal layer in the proximal through-hole.
- Pull the feedback line to be connected to the INx pin of the IC separately from near the output capacitor pin, whenever possible. Consider the line connected with INx pins to keep away from a switching system parts as much as possible because it is sensitive to the noise.
- There is leaked magnetic flux around the inductor or backside of place equipped with inductor.

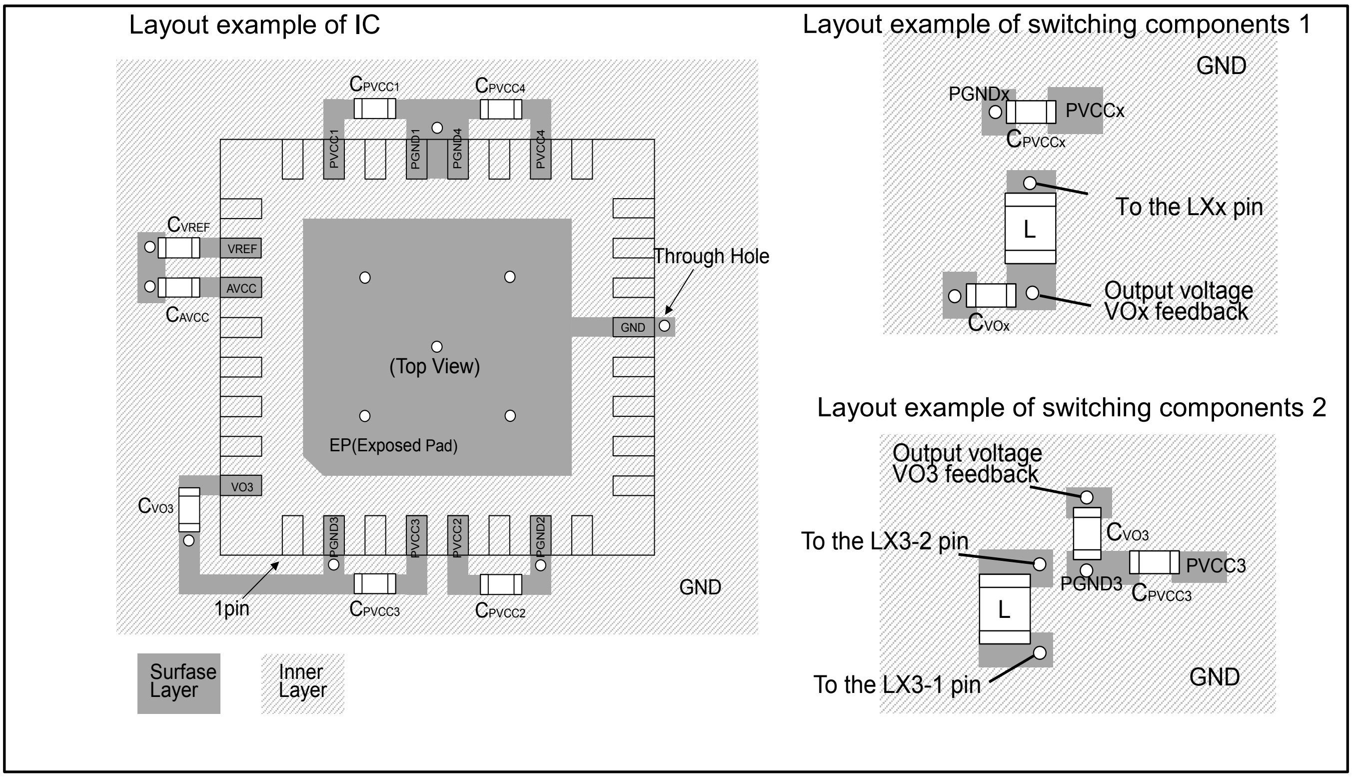
Line and parts sensitive to noise should be considered to be placed away from the inductor (or backside of place equipped with inductor).

Switching system parts: Input capacitor(CPVCCx), Inductor(L), Output capacitor(CVOx)

Note:

- *x: Each channel number*

Figure 31-1 Layout example



32. Major Changes

Page	Section	Change Results
Revision 0.1		
-	-	Initial release

Colophon

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