



FAN7190_F085

High-Current, High & Low-Side, Gate-Drive IC

Features

- Floating Channels for Bootstrap Operation to +600V
- Typically 4.5A/4.5A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input
- Qualified to AEC Q100

Applications

- Diesel and gasoline Injectors/Valves
- MOSFET-and IGBT high side driver applications

Description

The FAN7190_F085 is a monolithic high- and low-side gate-drive IC, which can drive high speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit offers high-side gate driver operation up to $V_S = -9.8V$ (typical) for $V_{BS} = 15V$.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop feature make this device suitable for magnetic- and piezo type injectors and general MOSFET/IGBT based high side driver applications.

8-SOP



Ordering Information

Part Number	Package	Operating Temperature Range	 Eco Status	Packing Method
FAN7190M_F085	8-SOP	-40°C ~ 125°C	RoHS	Tube
FAN7190MX_F085				Tape & Reel



For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Circuit

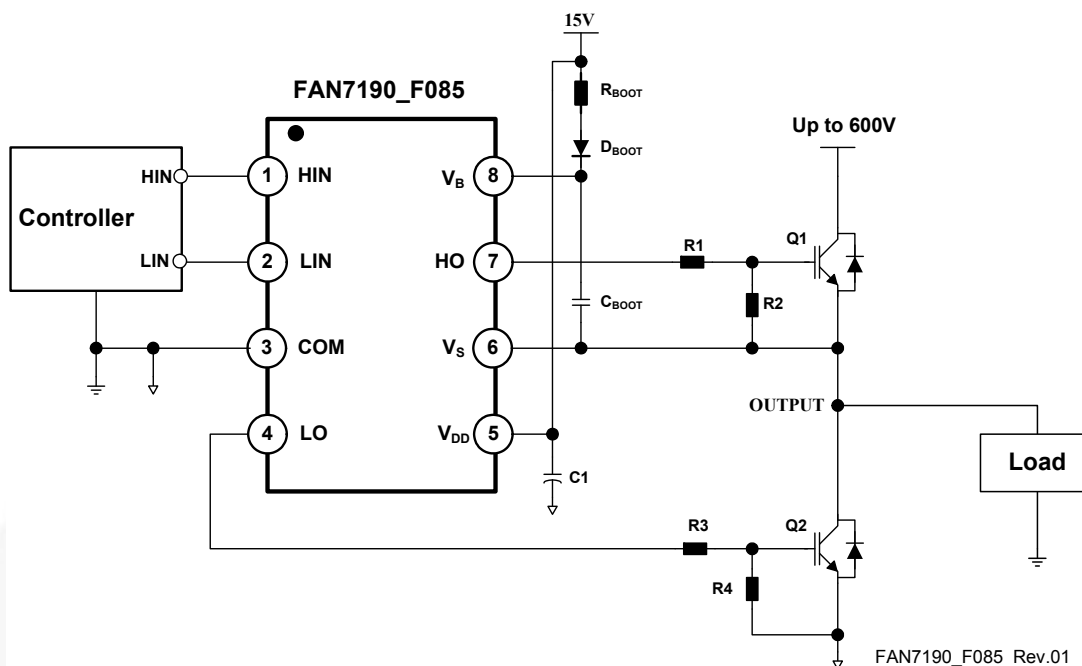


Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

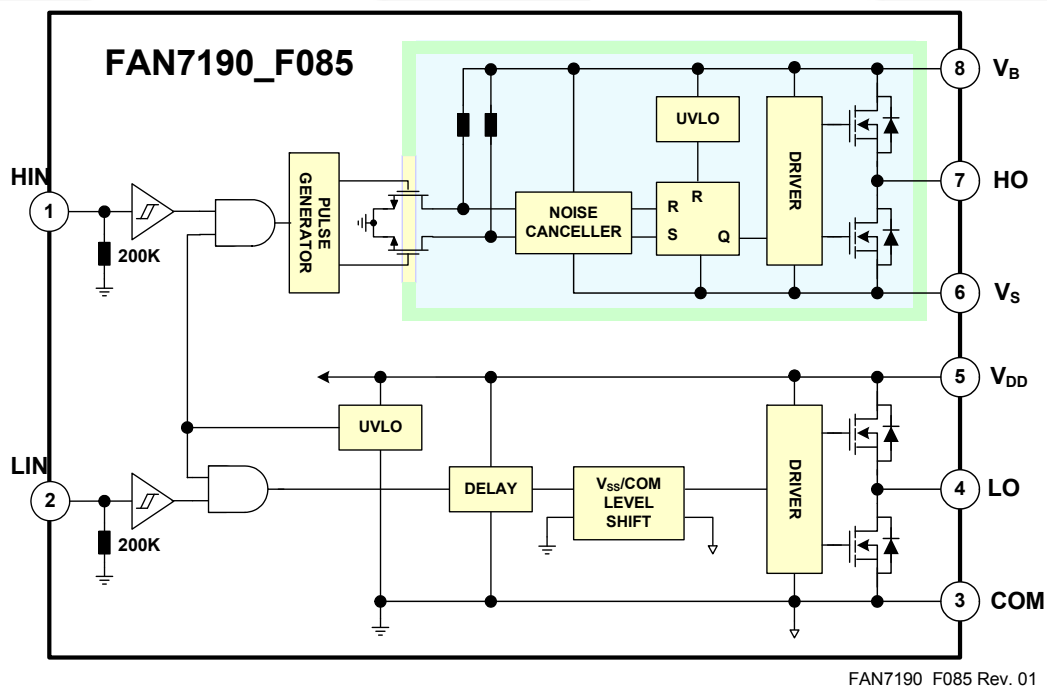


Figure 2. Functional Block Diagram

Pin Configurations

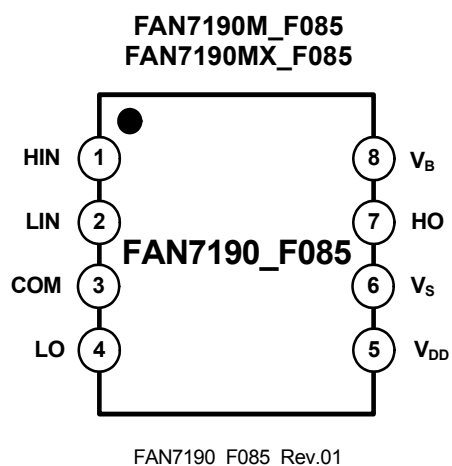


Figure 3. Pin Assignments (Top View)

Pin Definitions

8-Pin	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	COM	Low-Side Driver Return
4	LO	Low-Side Driver Output
5	V _{DD}	Low-Side and Logic Part Supply Voltage
6	V _S	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V _B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-Side Floating Supply Offset Voltage	V_B-25	$V_B+0.3$	V
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_{HO}	High-Side Floating Output Voltage HO	$V_S-0.3$	$V_B+0.3$	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
V_{LO}	Low-Side Output Voltage LO	-0.3	$V_{DD}+0.3$	V
V_{IN}	Logic Input Voltage (HIN and LIN)	-0.3	$V_{DD}+0.3$	V
dV_S/dt	Allowable Offset Voltage Slew Rate		50	V/ns
$P_D^{(1)(2)(3)}$	Power Dissipation	8-SOP	0.625	W
θ_{JA}	Thermal Resistance, Junction-to-Ambient	8-SOP	200	$^{\circ}\text{C/W}$
T_J	Junction Temperature		+150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature		+150	$^{\circ}\text{C}$

Notes:

1. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
 JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
 JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	V_S+10	V_S+22	V
V_S	High-Side Floating Supply Offset Voltage	$6-V_{DD}$	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{DD}	Low-Side and Logic Supply Voltage	10	22	V
V_{LO}	Low-Side Output Voltage	COM	V_{DD}	V
V_{IN}	Logic Input Voltage (HIN and LIN)	COM	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	$^{\circ}\text{C}$
T_{pulse}	Minimum Pulse Width ⁽⁴⁾	80	-	ns

Notes:

4. Guaranteed by design. Refer to Figure 28,29 and 30 on page 11

Electrical Characteristics

V_{BIAS} (V_{DD} , V_{BS})=15.0V, V_S =COM, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, unless otherwise specified. The V_{IL} , V_{IH} , and I_{IN} parameters are referenced to COM and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM and V_S is applicable to the respective output signals HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION (V _{DD} AND V _{BS})						
V _{DDUV+} V _{BSUV+}	V _{DD} and V _{BS} Supply Under-Voltage Positive-going Threshold		7.8	8.8	9.8	V
V _{DDUV-} V _{BSUV-}	V _{DD} and V _{BS} Supply Under-Voltage Negative-going Threshold		7.2	8.3	9.1	
V _{DDUVH} V _{BSUVH}	V _{DD} and V _{BS} Supply Under-Voltage Lockout Hysteresis Voltage			0.5		
I _{LK}	Offset Supply Leakage Current	V _B =V _S =600V			50	μA
I _{QBS}	Quiescent V _{BS} Supply Current	V _{IN} =0V or 5V		45	110	
I _{QDD}	Quiescent V _{DD} Supply Current	V _{IN} =0V or 5V		75	150	
I _{PBS}	Operating V _{BS} Supply Current	f _{IN} =20kHz, rms value		530	700	μA
I _{PDD}	Operating V _{DD} Supply Current	f _{IN} =20kHz, rms value		530	750	
LOGIC INPUT SECTION (H _{IN} , L _{IN})						
V _{IH}	Logic "1" Input Voltage		2.5			V
V _{IL}	Logic "0" Input Voltage				1.2	
I _{IN+}	Logic "1" Input Bias Current	V _{IN} =5V		25	50	μA
I _{IN-}	Logic "0" Input Bias Current	V _{IN} =0V		1.0	2.0	
R _{IN}	Input Pull-down Resistance		100	200		KΩ
GATE DRIVER OUTPUT SECTION (H _O , L _O)						
V _{OH}	High-level Output Voltage, V _{BIAS} -V _O	No Load			1.5	V
V _{OL}	Low-level Output Voltage, V _O	No Load			35	mV
I _{O+}	Output High, Short-circuit Pulsed Current ⁽⁴⁾	V _O =0V, V _{IN} =5V with PW<10μs	3.5	4.5		A
I _{O-}	Output Low, Short-circuit Pulsed Current ⁽⁴⁾	V _O =15V, V _{IN} =0V with PW<10μs	3.5	4.5		
V _S	Allowable Negative V _S Pin Voltage for H _{IN} Signal Propagation to H _O			-9.8	-7.0	V

Note:

4. This parameter guaranteed by design.

Dynamic Electrical Characteristics

V_{BIAS} (V_{DD} , V_{BS})=15.0V, V_S =COM=0V, C_L =1000pF and $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Propagation Delay	$V_S = 0\text{V}$		140	200	ns
t_{off}	Turn-off Propagation Delay	$V_S = 0\text{V}$		140	200	
MT	Delay Matching, HS & LS Turn-on/off			0	50	
t_r	Turn-on Rise Time			25	50	
t_f	Turn-off Fall Time			20	45	

Typical Characteristics

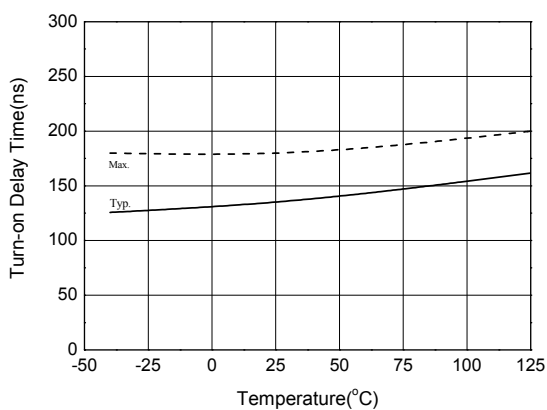


Figure 4. Turn-on Propagation Delay vs. Temperature

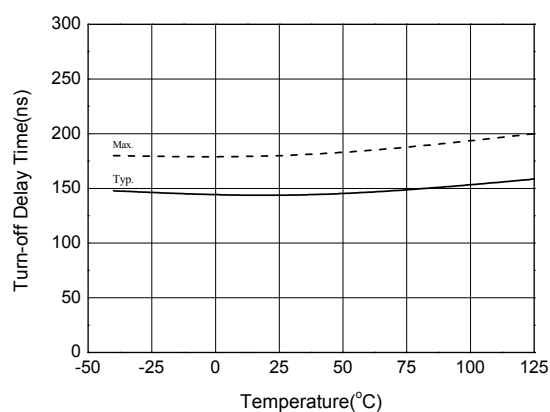


Figure 5. Turn-off Propagation Delay vs. Temperature

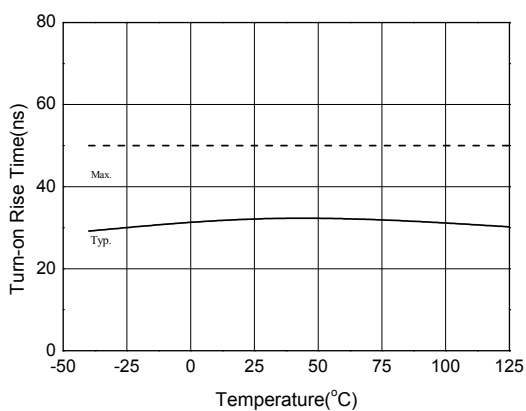


Figure 6. Turn-on Rise Time vs. Temperature

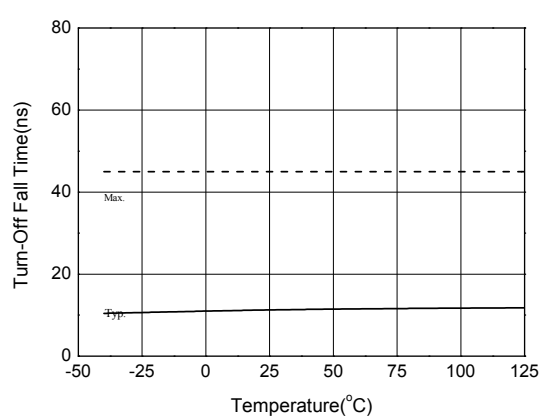


Figure 7. Turn-off Fall Time vs. Temperature

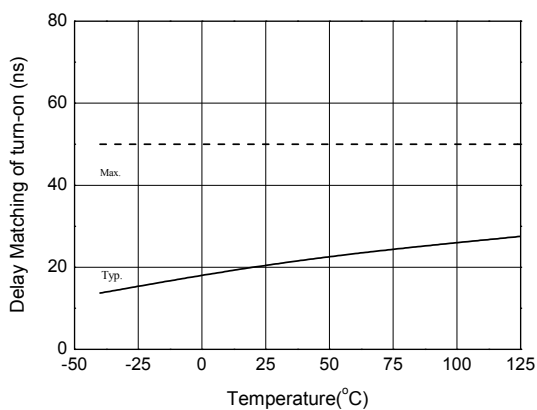


Figure 8. Turn-on Delay Matching vs. Temperature

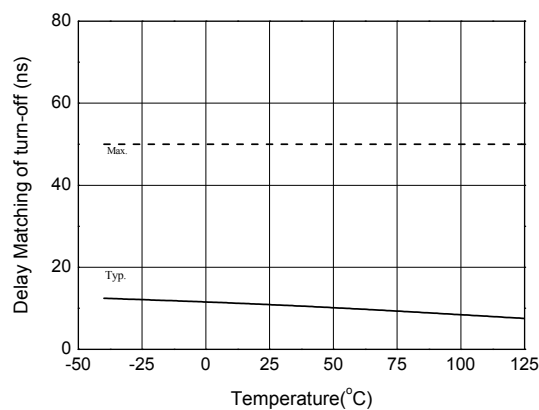


Figure 9. Turn-off Delay Matching vs. Temperature

Typical Characteristics (Continued)

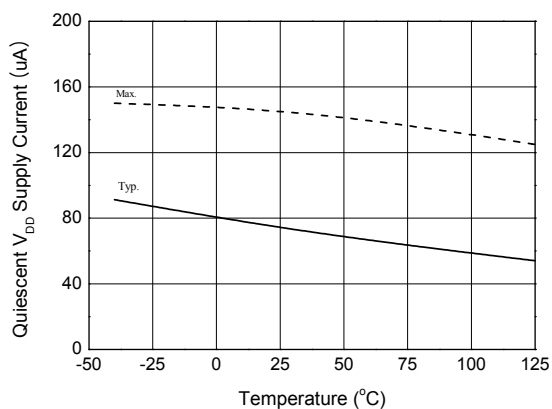


Figure 10. Quiescent V_{DD} Supply Current vs. Temperature

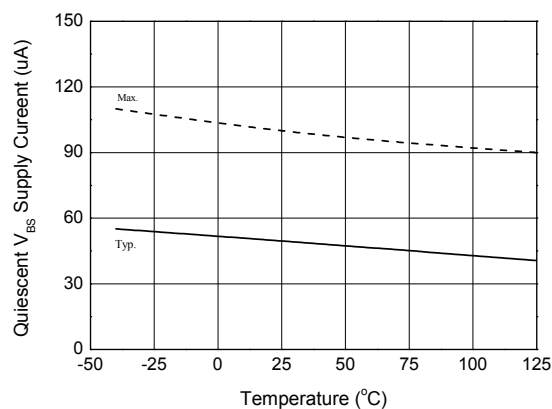


Figure 11. Quiescent V_{BS} Supply Current vs. Temperature

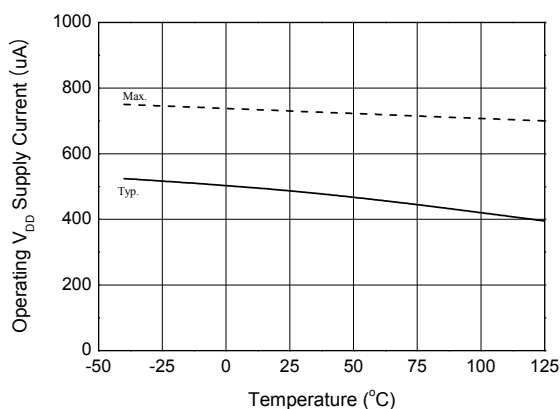


Figure 12. Operating V_{DD} Supply Current vs. Temperature

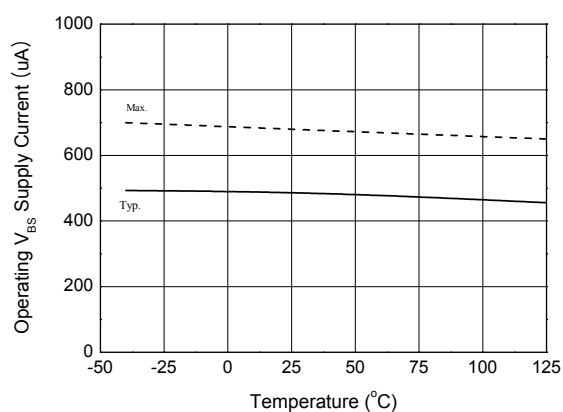


Figure 13. Operating V_{BS} Supply Current vs. Temperature.

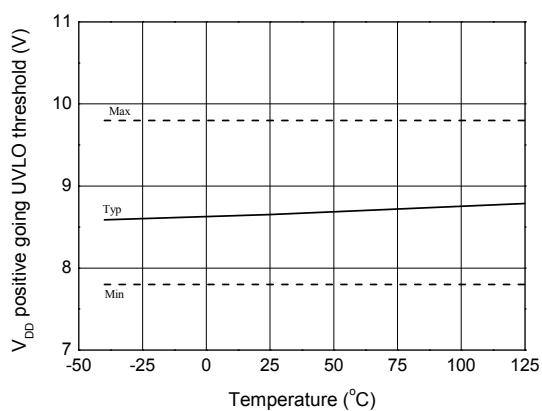


Figure 14. V_{DD} UVLO+ vs. Temperature

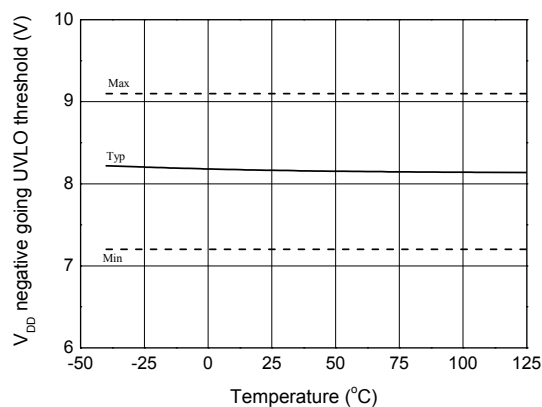


Figure 15. V_{DD} UVLO- vs. Temperature

Typical Characteristics (Continued)

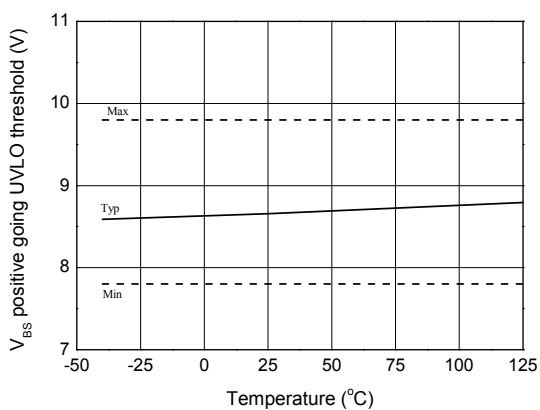


Figure 16. V_{BS} UVLO+ vs. Temperature

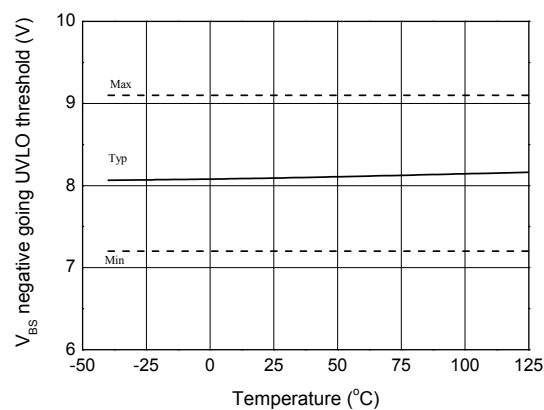


Figure 17. V_{BS} UVLO- vs. Temperature

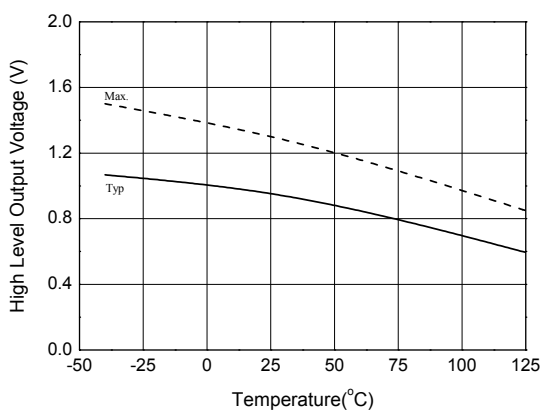


Figure 18. High-Level Output Voltage vs. Temperature

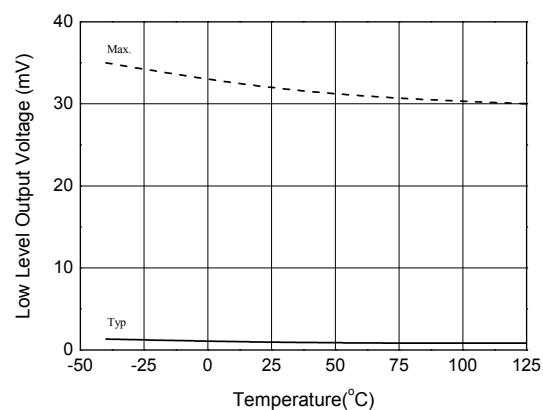


Figure 19. Low-Level Output Voltage vs. Temperature

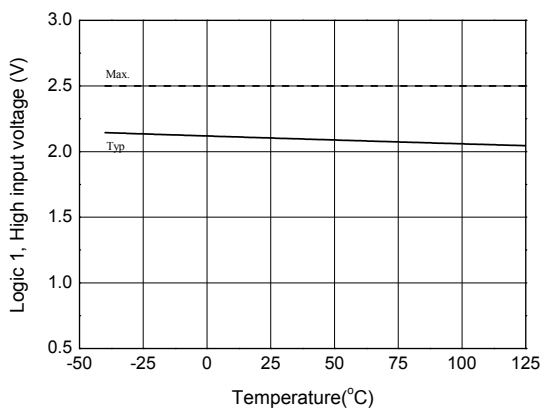


Figure 20. Logic High Input Voltage vs. Temperature

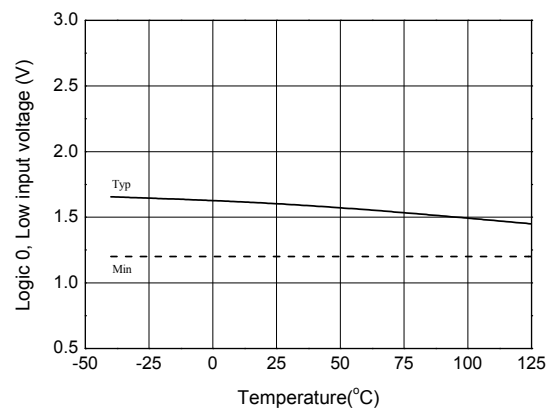


Figure 21. Low Input Voltage vs. Temperature

Typical Characteristics (Continued)

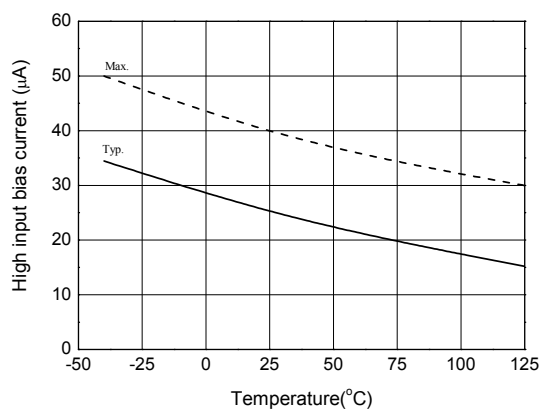


Figure 22. Logic Input High Bias Current vs. Temperature

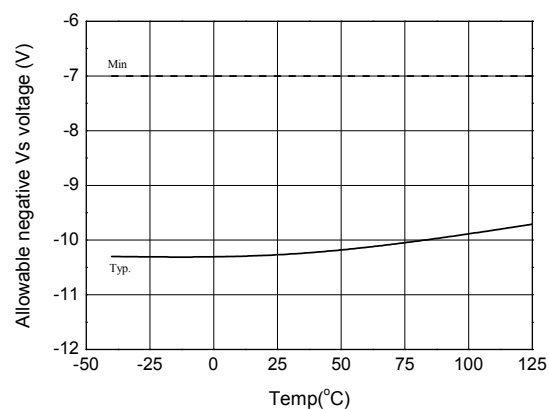


Figure 23. Allowable Negative V_S Voltage vs. Temperature

Switching Time Definitions

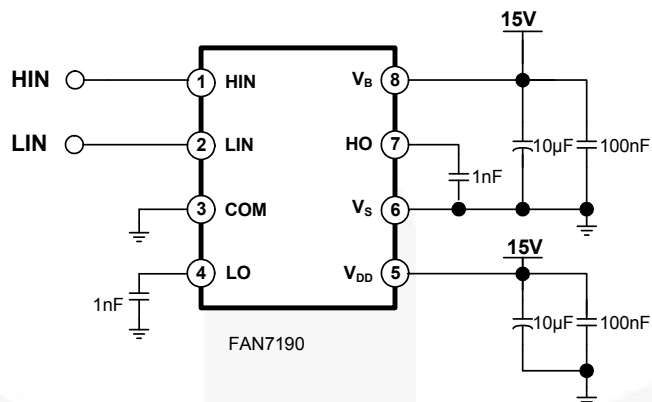


Figure 24. Switching Time Test Circuit (Referenced 8-SOP)

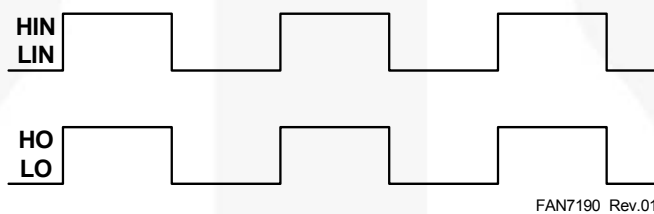


Figure 25. Input/Output Timing Diagram

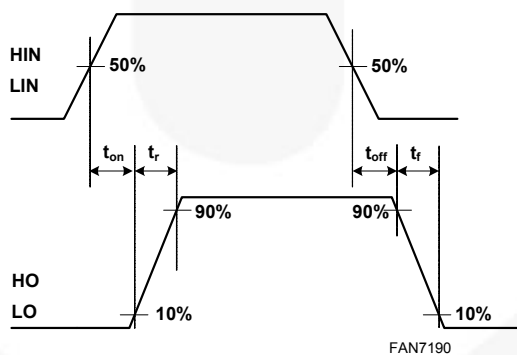


Figure 26. Switching Time Waveform Definitions

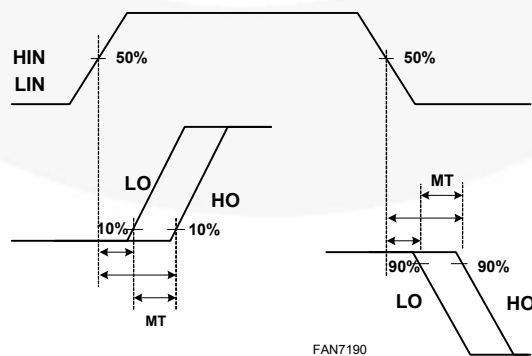


Figure 27. Delay Matching Waveform Definitions

Switching Time Definitions

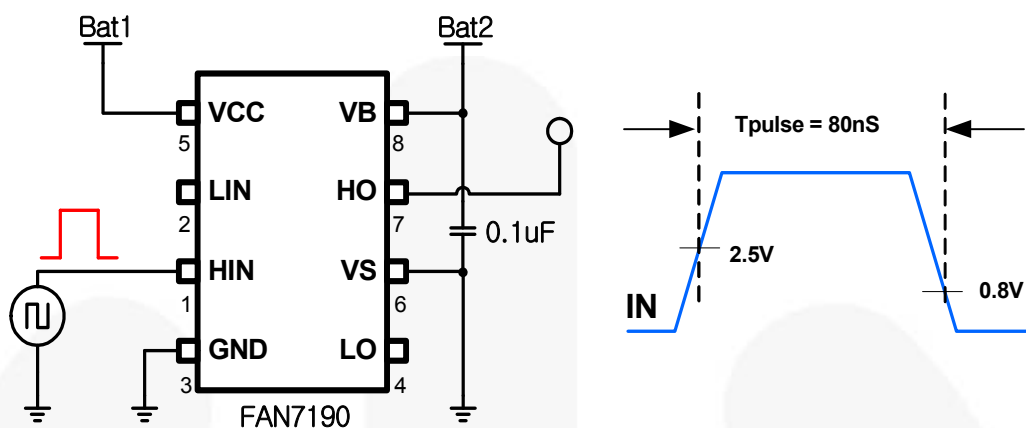


Figure 28. Short Pulse Width Test Circuit and Pulse Width Waveform

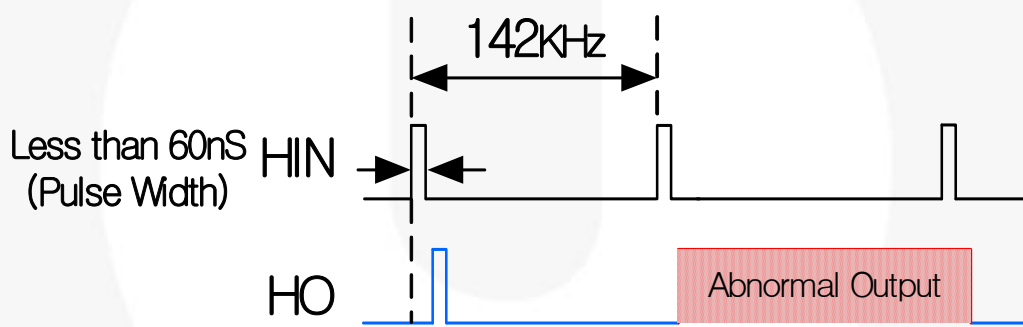


Figure 29. Abnormal Output Waveform with short pulse width

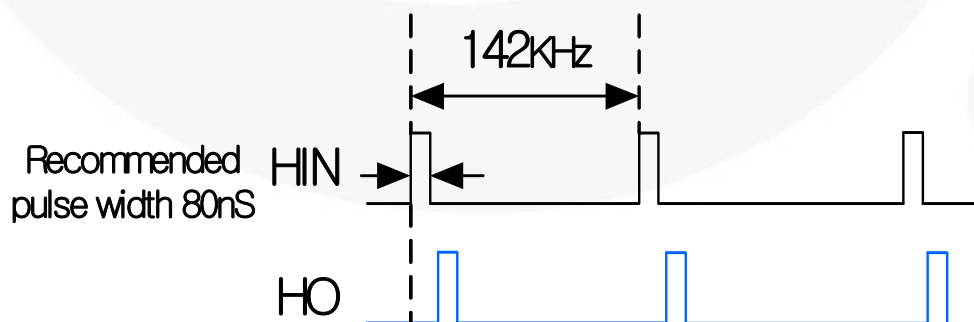
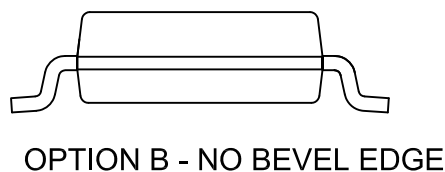
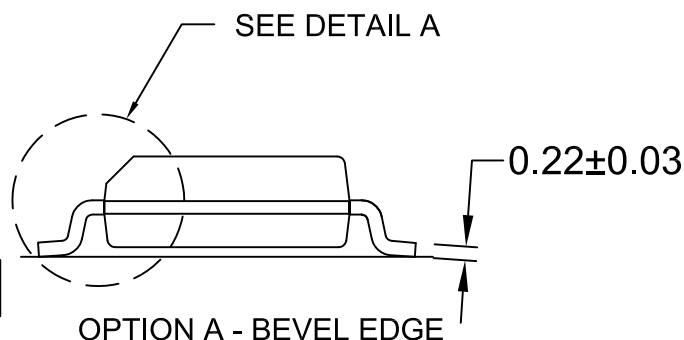
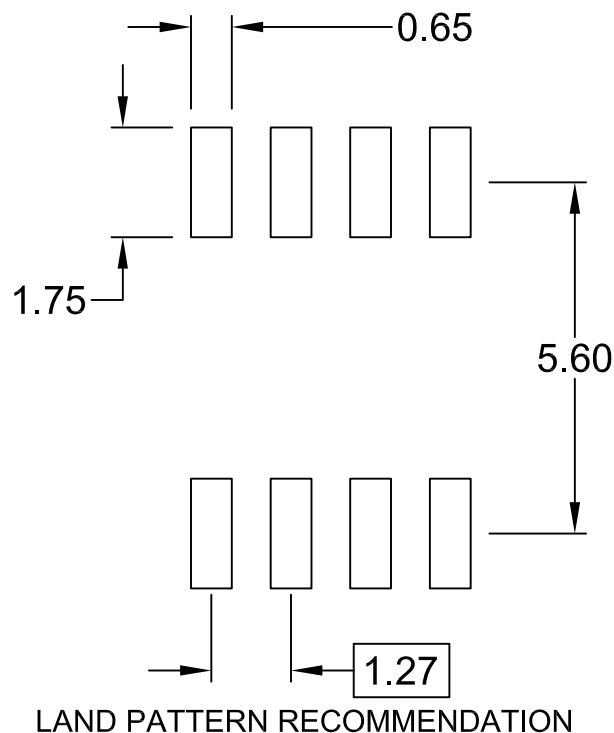


Figure 30. Recommendation of pulse width Output Waveform



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	F-PFS™	OPTOPLANAR®	SYSTEM GENERAL®*
Awinda®	FRFET®	 ®	TinyBoost®
AX-CAP®*	Global Power Resource™	PowerTrench®	TinyBuck®
BitSiC™	GreenBridge™	PowerXS™	TinyCalc™
Build it Now™	Green FPS™	Programmable Active Droop™	TinyLogic®
CorePLUS™	Green FPS™ e-Series™	QFET®	TINYOPTO™
CorePOWER™	Gmax™	QS™	TinyPower™
CROSSVOLT™	GTO™	Quiet Series™	TinyPWM™
CTL™	IntelliMAX™	RapidConfigure™	TinyWire™
Current Transfer Logic™	ISOPLANAR™	 ™	TranSiC™
DEUXPEED®	Making Small Speakers Sound Louder and Better™	Saving our world, 1mW/W/kW at a time™	TriFault Detect™
Dual Cool™	MegaBuck™	SignalWise™	TRUECURRENT®*
EcoSPARK®	MICROCOUPLER™	SmartMax™	μSerDes™
EfficientMax™	MicroFET™	SMART START™	 SerDes®
ESBC™	MicroPak™	Solutions for Your Success™	UHC®
 ®	MicroPak2™	SPM®	Ultra FRFET™
Fairchild®	MillerDrive™	STEALTH™	UniFET™
Fairchild Semiconductor®	MotionMax™	SuperFET®	VCX™
FACT Quiet Series™	MotionGrid®	SuperSOT™-3	VisualMax™
FACT®	MTi®	SuperSOT™-6	VoltagePlus™
FAST®	MTx®	SuperSOT™-8	XS™
FastvCore™	MVN®	SupreMOS®	Xsens™
FETBench™	mWSaver®	SyncFET™	仙童™
FPS™	OptoHit™	Sync-Lock™	
	OPTOLOGIC®		

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I72