

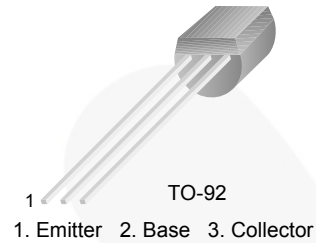


October 2014

KSP44 / KSP45 NPN Epitaxial Silicon Transistor

Features

- High-Voltage Transistor
- Collector-Emitter Voltage: V_{CEO} = KSP44: 400 V
KSP45: 350 V



Ordering Information

Part Number	Top Mark	Package	Packing Method
KSP44BU	KSP44	TO-92 3L	Bulk
KSP44TA	KSP44	TO-92 3L	Ammo
KSP44TF	KSP44	TO-92 3L	Tape and Reel
KSP45TA	KSP45	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit	
V_{CBO}	Collector-Base Voltage	KSP44	500	V
		KSP45	400	
V_{CEO}	Collector-Emitter Voltage	KSP44	400	V
		KSP45	350	
V_{EBO}	Emitter-Base Voltage	6	V	
I_C	Collector Current	300	mA	
T_J	Junction Temperature	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature	-55 to 150	$^\circ\text{C}$	

KSP44 / KSP45 — NPN Epitaxial Silicon Transistor

Thermal Characteristics⁽¹⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit	
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	625	mW
		$T_C = 25^\circ\text{C}$	1.5	W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	83.3	$^\circ\text{C/W}$	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	$^\circ\text{C/W}$	

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
BV_{CBO}	Collector-Base Breakdown Voltage	KSP44	$I_C = 100 \mu\text{A}, I_E = 0$	500		V
		KSP45		400		
BV_{CEO}	Collector-Emitter Breakdown Voltage ⁽²⁾	KSP44	$I_C = 1 \text{ mA}, I_B = 0$	400		V
		KSP45		350		
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 100 \mu\text{A}, I_C = 0$	6		V	
I_{CBO}	Collector Cut-Off Current	KSP44	$V_{CB} = 400 \text{ V}, I_E = 0$		0.1	μA
		KSP45		$V_{CB} = 320 \text{ V}, I_E = 0$		
I_{CES}	Collector Cut-Off Current	KSP44	$V_{CE} = 400 \text{ V}, I_B = 0$		0.5	μA
		KSP45		$V_{CE} = 320 \text{ V}, I_B = 0$		
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = 4 \text{ V}, I_C = 0$		0.1	μA	
h_{FE}	DC Current Gain ⁽²⁾		$V_{CE} = 10 \text{ V}, I_C = 1 \text{ mA}$	40		
			$V_{CE} = 10 \text{ V}, I_C = 10 \text{ mA}$	50	200	
			$V_{CE} = 10 \text{ V}, I_C = 50 \text{ mA}$	45		
			$V_{CE} = 10 \text{ V}, I_C = 100 \text{ mA}$	40		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage ⁽²⁾		$I_C = 1 \text{ mA}, I_B = 0.1 \text{ mA}$		0.40	V
			$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$		0.50	
			$I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$		0.75	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage ⁽²⁾	$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$		0.75	V	
C_{ob}	Output Capacitance	$V_{CB} = 20 \text{ V}, I_E = 0,$ $f = 1 \text{ MHz}$		7	pF	

Note:

2. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Performance Characteristics

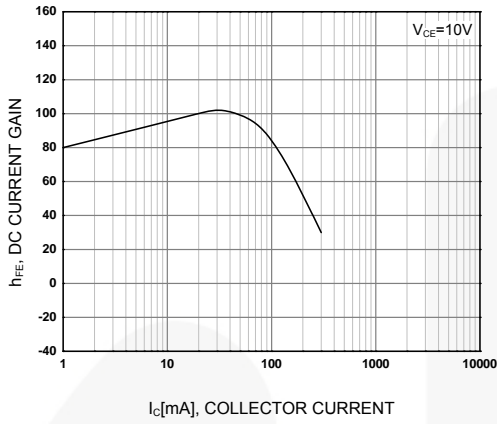


Figure 1. DC Current Gain

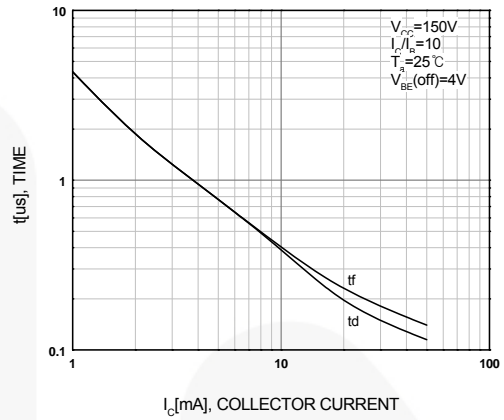


Figure 2. Turn-On Switching Times

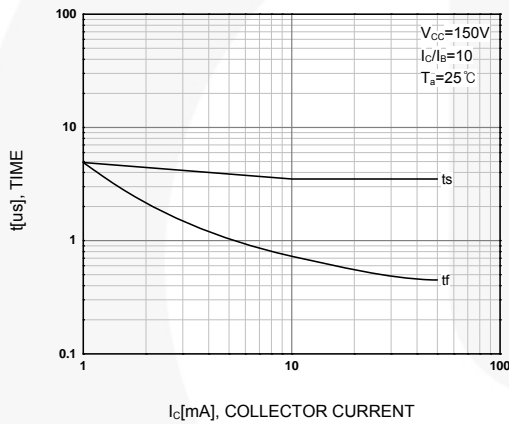


Figure 3. Turn-Off Switching Times

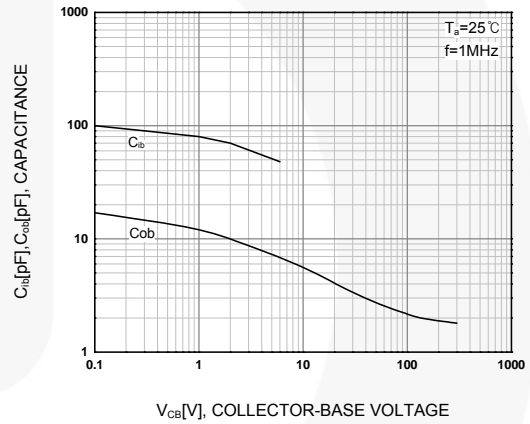


Figure 4. Capacitance

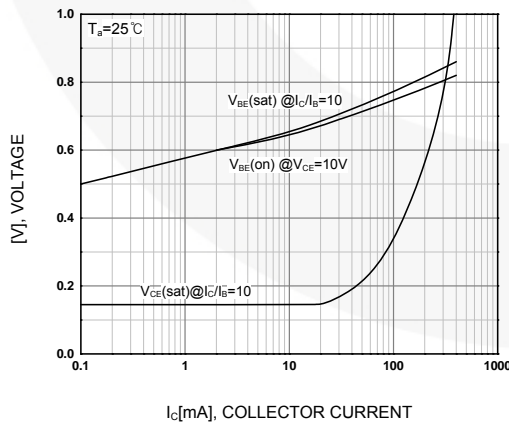


Figure 5. On Voltage

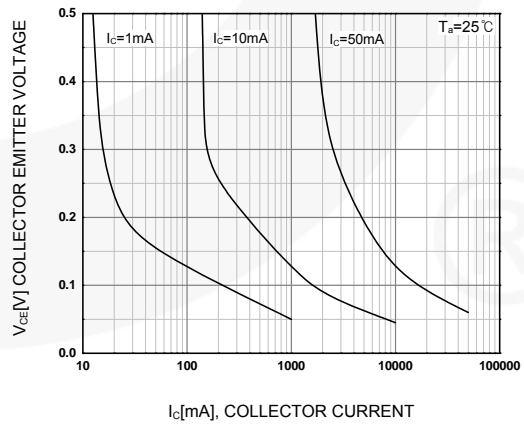


Figure 6. Collector Saturation Region

Typical Performance Characteristics (Continued)

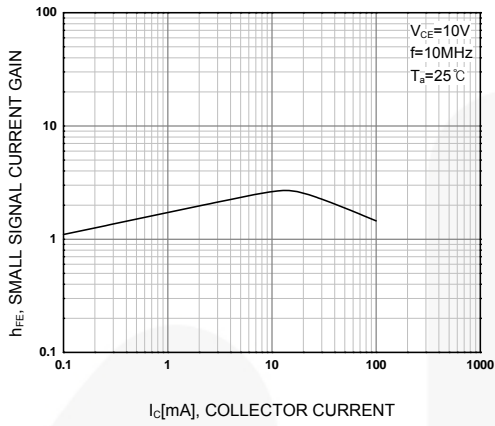


Figure 7. High-Frequency Current Gain

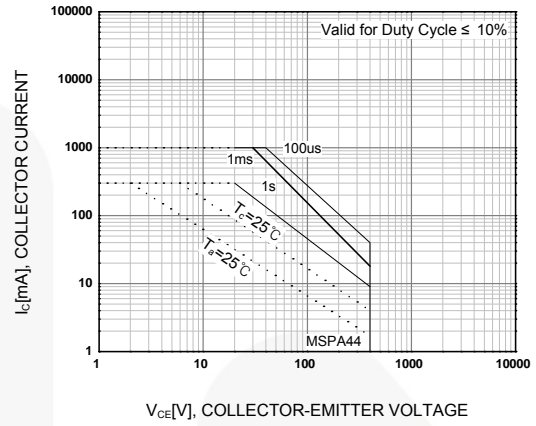


Figure 8. Safe Operating Area



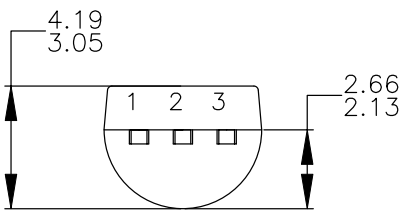
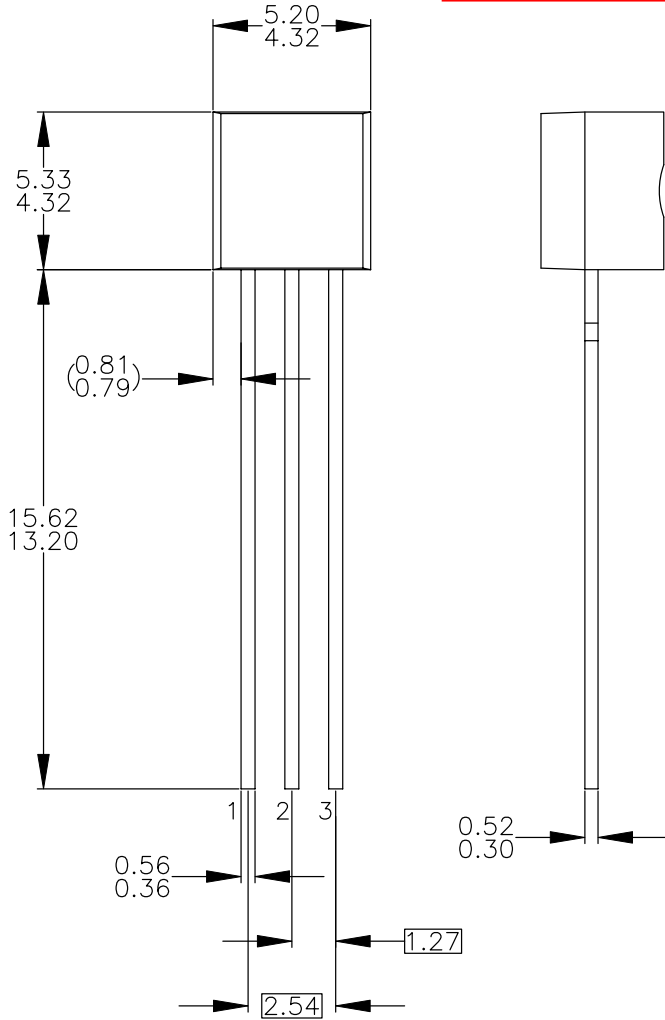
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APPROVED
 July-14-2008

REVISIONS			
NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH(MM) TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14-1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32- 4.70 TO 4.32-4.83; CHG PKG HEIGHT DIM FR 4.32-4.70 TO 4.32-4.78; CHG LD THICK DIM FR 0.30- 0.48 TO 0.30-0.52; DAMBAR-PKG DIM FR 1.27-1.65 TO 0.90-1.65; LD LGH DIM FR 14.47-15.64 TO 14.47-15.62; PKG DIM: 1.02-1.52 TO 0.92-1.52, 3.81-4.45 TO 3.40-4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C. MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	4OCT1999	RCM/MRG
3	CHG LD LEN FR 1.81 TO 1.88 ; CHG MOLD BODY HT FR 1.33 TO 1.33 ; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO (0.81); CHG MOLD BODY WIDTH FR 1.33 TO 1.33 ; ADD PKG THICKNESS DIM "E"; CHG "S" DIM FR 2.13 TO 2.13 ; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M-1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR	E - EMITTER	D - DRAIN
F - JFET	B - BASE	S - SOURCE
M - DMOS	C - COLLECTOR	G - GATE






- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

APPROVALS	DATE	 FAIRCHILD SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	03APR2008	
CHECKED: L. GALERA		
APPROVED: M.R. GESTOLE		
G.S. BAJE		3LD, TO-92, MOLDED STD STRAIGHT LD (NO EOL CODE)
		SCALE: 1:1 SIZE: N/A DRAWING NUMBER: MKT-ZA03D FORMERLY: N/A
		REV: 3 SHEET: 1 OF 1



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