

# P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
	0.150 at V <sub>GS</sub> = - 4.5 V	1.06			
- 20	0.166 at V <sub>GS</sub> = - 2.5V	1.0	6.0		
	0.214 at V <sub>GS</sub> = - 1.8V	0.49			

### **FEATURES**

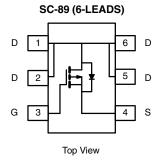
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

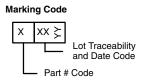


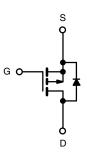
ROHS COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

· Load Switch for Portable Devices







Ordering Information: Si1067X-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	<b>5</b> (T <sub>A</sub> = 25 °C, unle	ess otherwise no	ted)		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 20	V		
Gate-Source Voltage		V <sub>GS</sub>		± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	,	- 1.06 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	l D	- 0.85 <sup>b, c</sup>		
Pulsed Drain Current		I <sub>DM</sub>	- 8	Α	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	- 0.2 <sup>b, c</sup>		
	T <sub>A</sub> = 25 °C	В	0.236 <sup>b, c</sup>	10/	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	P <sub>D</sub>	0.151 <sup>b, c</sup>	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Manipulation to Applicate h	t ≤ 5 s	- R <sub>thJA</sub>	440	530	°C/W	
Maximum Junction-to-Ambient <sup>a, b</sup>	Steady State		540	650	C/VV	

#### Notes:

- a. Maximum under steady state conditions is 650 °C/W.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Γ <sub>J</sub>		- 32.07		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	l <sub>D</sub> = - 250 μA		3.02		mv/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \mu A$	- 0.45		- 0.95	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zana Oata Vallana Busin Oamant	I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			- 1	μΑ	
Zero Gate Voltage Drain Current					- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = \ge 5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 8			Α	
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 1.06 A		0.125	0.150		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1.0 A		0.138	0.166	Ω	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 0.49 A		0.165	0.214		
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 1.06 A		4.0		S	
Dynamic <sup>b</sup>						,	
Input Capacitance	C <sub>iss</sub>			375		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		82			
Reverse Transfer Capacitance	C <sub>rss</sub>			62			
Tatal Cata Observe	Qg	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 5 V, I <sub>D</sub> = - 1.06 A		6.5	9.3		
Total Gate Charge				6.0	9.1	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -1.06 \text{ A}$		0.76			
Gate-Drain Charge	Q <sub>gd</sub>			2.23		1	
Gate Resistance	R <sub>q</sub> f = 1 MHz			8.8	13.2	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			14	21		
Rise Time	t <sub>r</sub>	$V_{DD} = -10 \text{ V}, R_L = 19.74 \Omega$		22	33	1	
urn-Off Delay Time t <sub>d(off)</sub>		$I_D \cong -0.76 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		48	72	ns	
Fall Time	t <sub>f</sub>			17	25.5		
Drain-Source Body Diode Characteris	stics					ı	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				8	А	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 0.63 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			12.8	19.2	nC	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			4.5	6.8		
Reverse Recovery Fall Time	t <sub>a</sub>	I <sub>F</sub> = - 0.7 A, dl/dt = 100 A/μs		7.3		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			5.5			

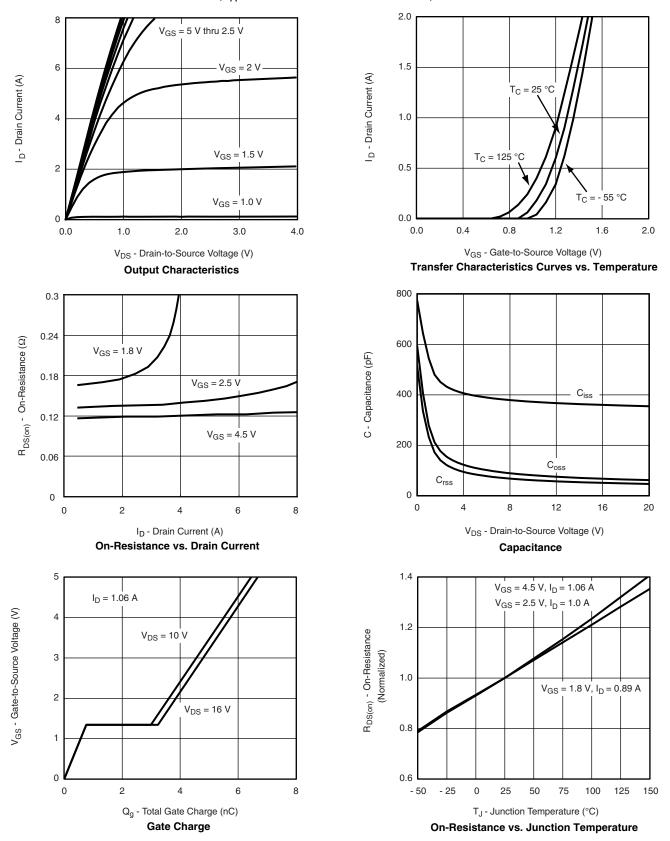
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



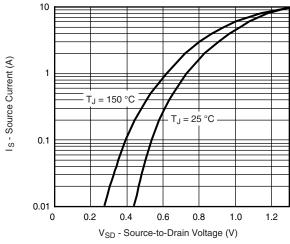
## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



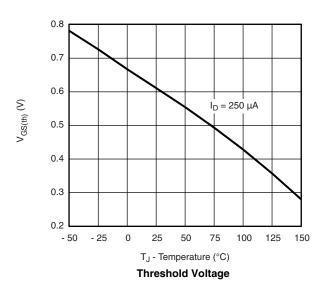
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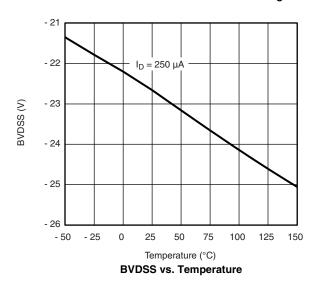
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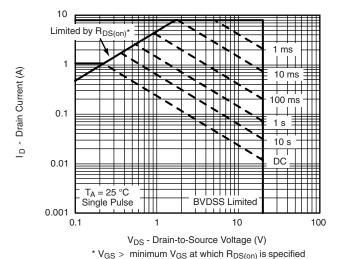


#### Source-Drain Diode Forward Voltage



0.28  $I_D = 1.06 \text{ A}$   $T_A = 125 \,^{\circ}\text{C}$  0.14  $T_A = 25 \,^{\circ}\text{C}$  0.00 0 1 2 3 4 5



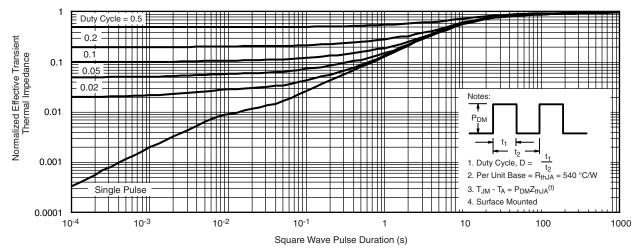


Safe Operating Area, Junction-to-Ambient





# **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



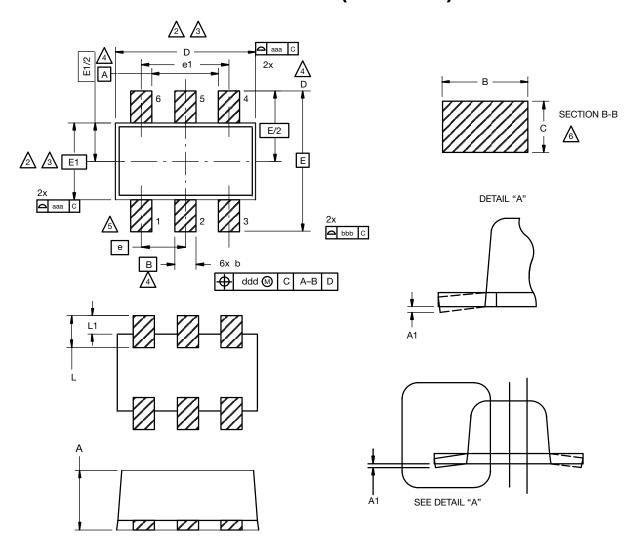
Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?74322">www.vishay.com/ppg?74322</a>.

Document Number: 74322 S10-2542-Rev. D, 08-Nov-10



# **SC-89 6-Leads (SOT-563F)**



#### Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

ADatums A, B and D to be determined 0.10 mm from the lead tip.

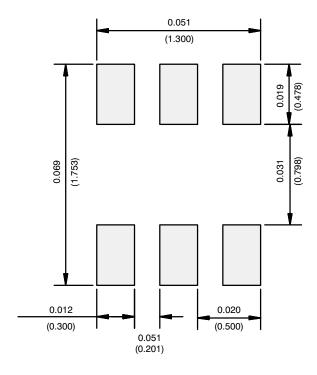
A Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS				
	MIN.	NOM.	MAX.		
Α	0.56	0.58	0.60		
A1	0	0.02	0.10		
b	0.15	0.22	0.30		
С	0.10	0.14	0.18		
D	1.50	1.60	1.70		
E	1.50	1.60	1.70		
E1	1.15	1.20	1.25		
е	0.45	0.50	0.55		
e1	0.95	1.00	1.05		
L	0.25	0.35	0.50		
L1	0.10	0.20	0.30		
C14-0439-Rev. C, 11-Aug-14 DWG: 5880					



### **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

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