

N- and P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
N-Channel	12	0.017 at V _{GS} = 4.5 V	11.8
		0.025 at V _{GS} = 2.5 V	9.8
P-Channel	- 12	0.032 at V _{GS} = - 4.5 V	- 8.9
		0.053 at V _{GS} = - 2.5 V	- 6.9

FEATURES

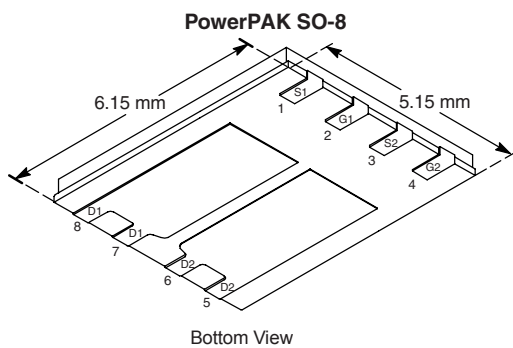
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- PWM Optimized for High Efficiency
- 100 % R_g Tested



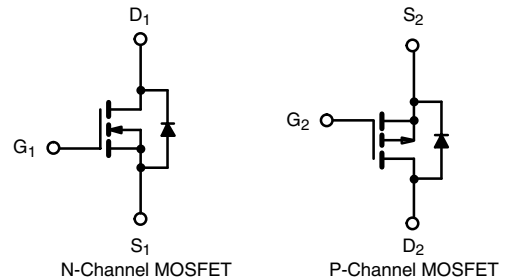
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Point-of-Load Synchronous Rectifier
- 5 V or 3.3 V BUS Step Down
- Q_g Optimized for 500 kHz Operation
- Synchronous Buck, Shoot-Thru Resistant



Ordering Information: Si7540DP-T1-E3 (Lead (Pb)-free)
Si7540DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 s	Steady	10 s	Steady		
Drain-Source Voltage	V _{DS}	12		- 12		V	
Gate-Source Voltage	V _{GS}	± 8					
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	11.8	7.6	- 8.9	- 5.7	A
		T _A = 70 °C	9.5	6.1	- 7.1	- 4.6	
Pulsed Drain Current	I _{DM}	20				A	
Continuous Source Current (Diode Conduction) ^a	I _S	2.9	1.1	- 2.9	- 1.1		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.5	1.4	3.5	1.4	W
		T _A = 70 °C	2.2	0.9	2.2	0.9	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	
Soldering Recommendations (Peak Temperature) ^{b,c}		260					

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typical	Maximum	Typical	Maximum		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	26	35	26	35	°C/W
		Steady State	60	85	60	85	
Maximum Junction-to-Case (Drain)	R _{thJC}	3.9	5.5	3.9	5.5		

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

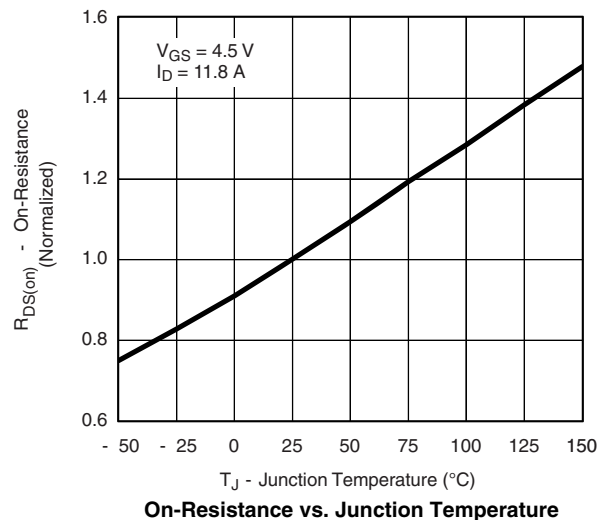
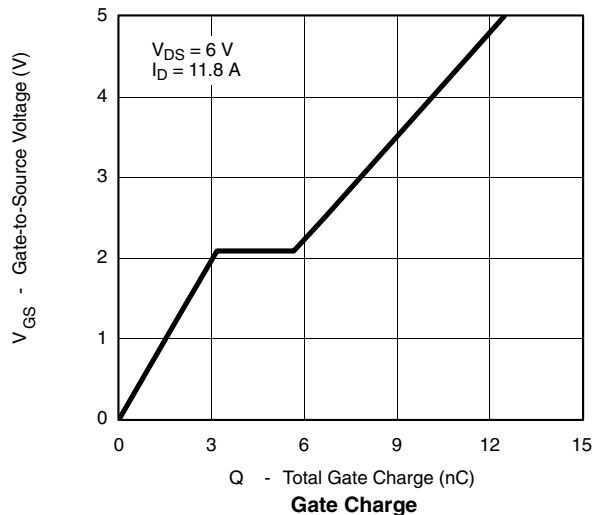
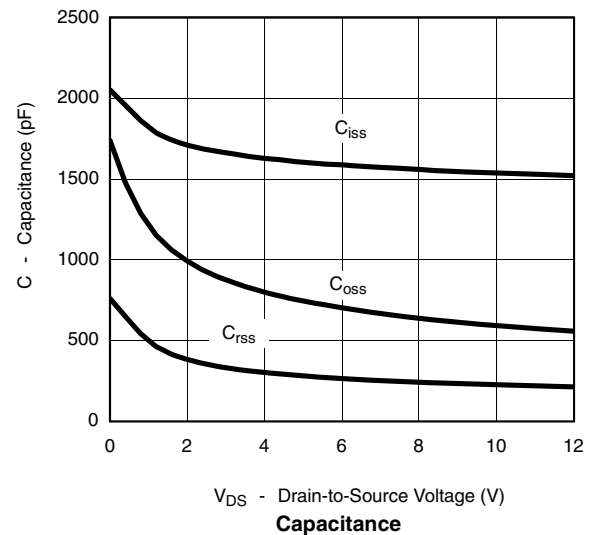
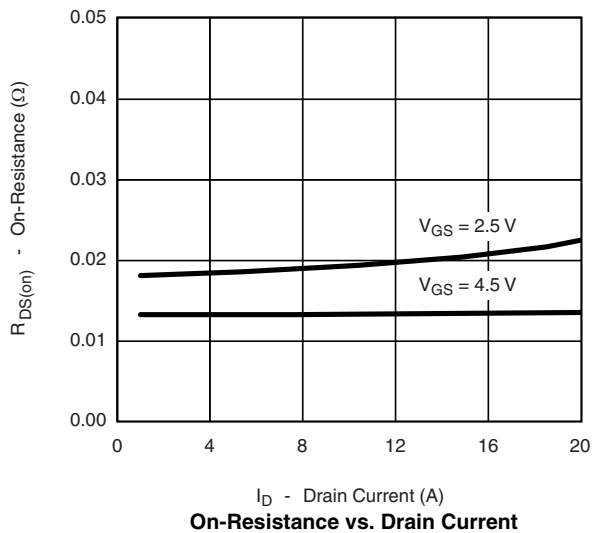
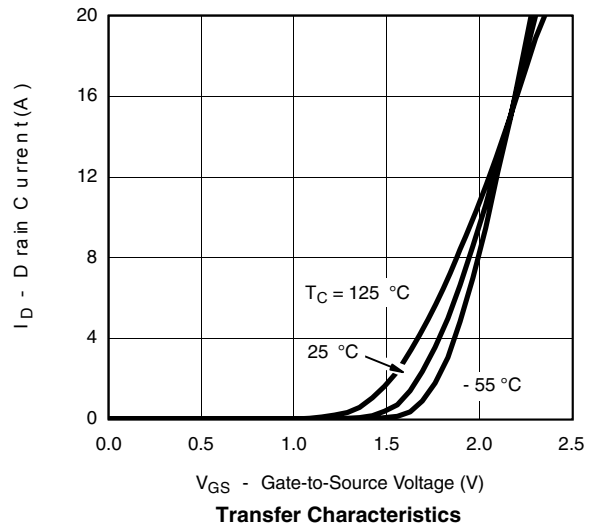
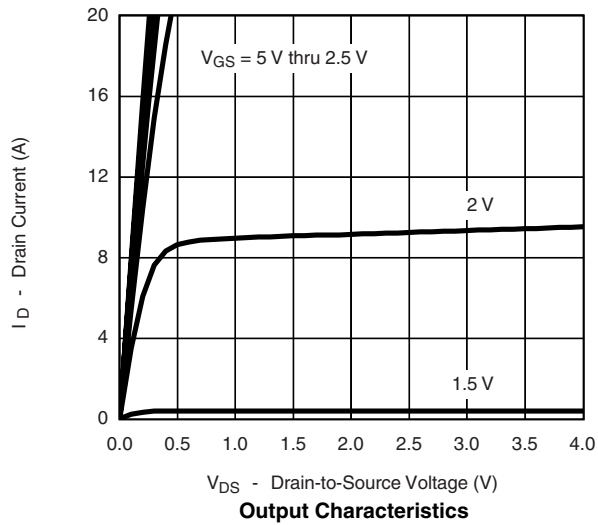
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6	1.5	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6	-1.5		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	N-Ch P-Ch		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		1	μA	
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$	P-Ch		-1		
		$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch		5		
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch		-5		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	20		A	
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-20			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 11.8\text{ A}$	N-Ch		0.014	0.017	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -8.9\text{ A}$	P-Ch		0.026	0.032	
		$V_{GS} = 2.5\text{ V}, I_D = 9.8\text{ A}$	N-Ch		0.020	0.025	
		$V_{GS} = -2.5\text{ V}, I_D = -6.9\text{ A}$	P-Ch		0.043	0.053	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 11.8\text{ A}$	N-Ch		32	S	
		$V_{DS} = -5\text{ V}, I_D = -8.9\text{ A}$	P-Ch		23		
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.77	1.2	V
		$I_S = -2.9\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 11.8\text{ A}$	N-Ch		11.5	17	nC
Gate-Source Charge	Q_{gs}		P-Ch		13	20	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -8.9\text{ A}$	N-Ch		3.2		
			P-Ch		4.1		
Gate Resistance	R_g		N-Ch	0.5	1.7	2.5	Ω
			P-Ch	1.5	3.5	5.6	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 6\text{ }\Omega$	N-Ch		30	45	ns
Rise Time	t_r		P-Ch		35	55	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$	N-Ch		50	75	
			P-Ch		42	65	
Fall Time	t_f		N-Ch		60	90	
			P-Ch		54	85	
Source-Drain Reverse Recovery Time	t_{rr}		N-Ch		25	40	
			P-Ch		17	30	
			N-Ch		40	80	
			P-Ch		40	80	

Notes:

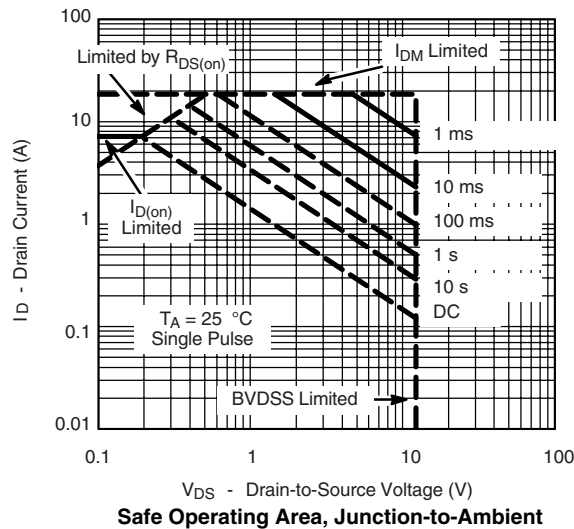
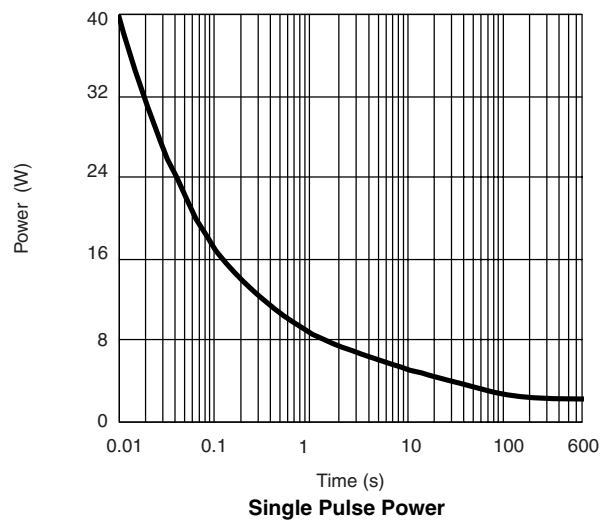
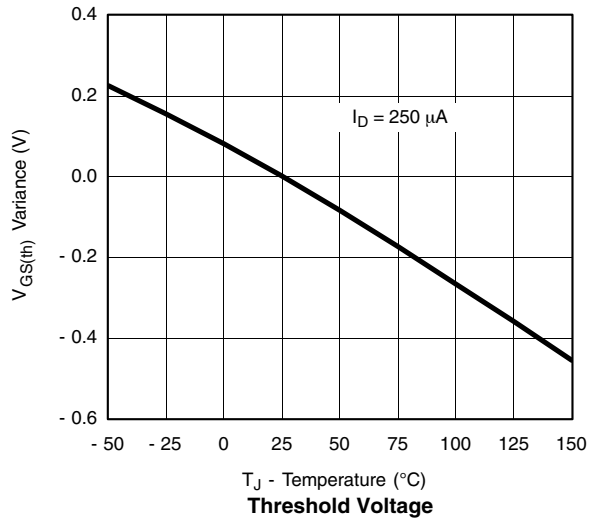
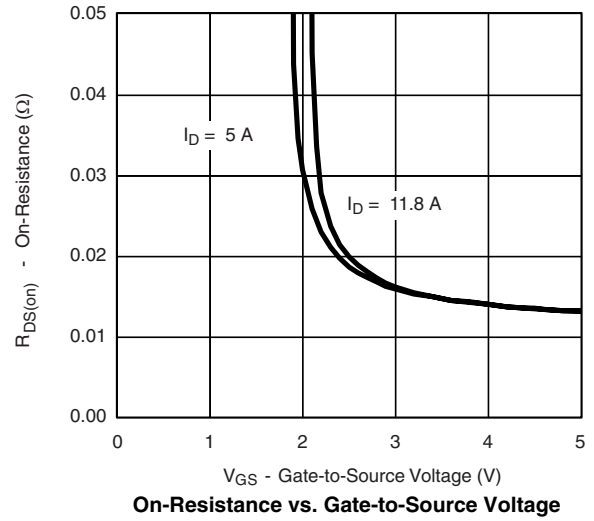
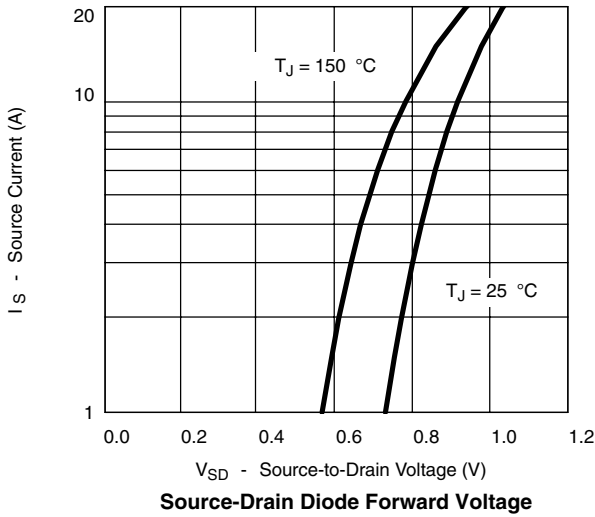
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

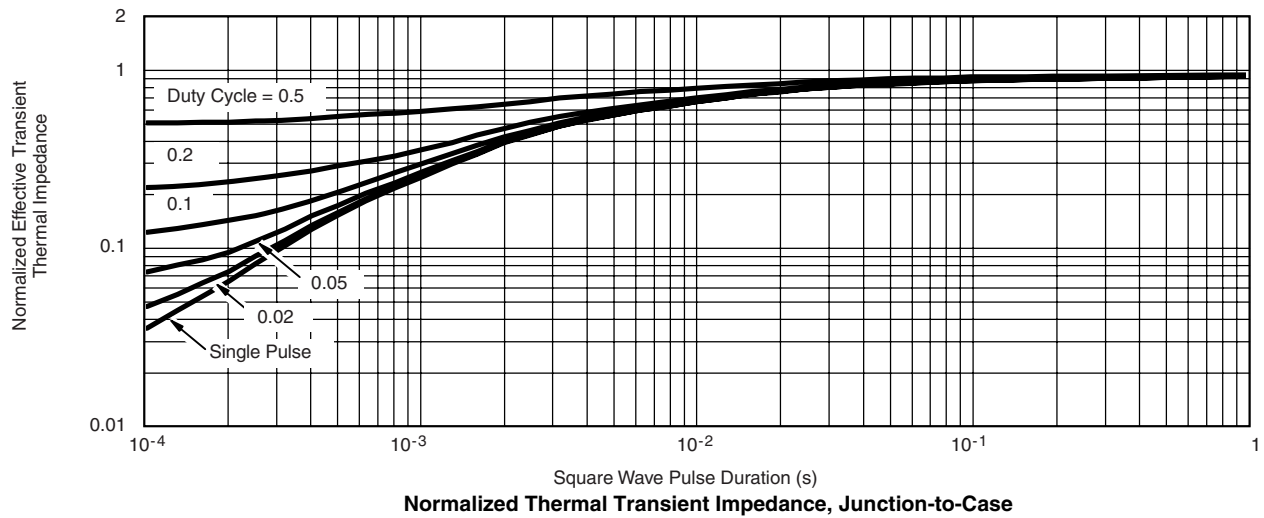
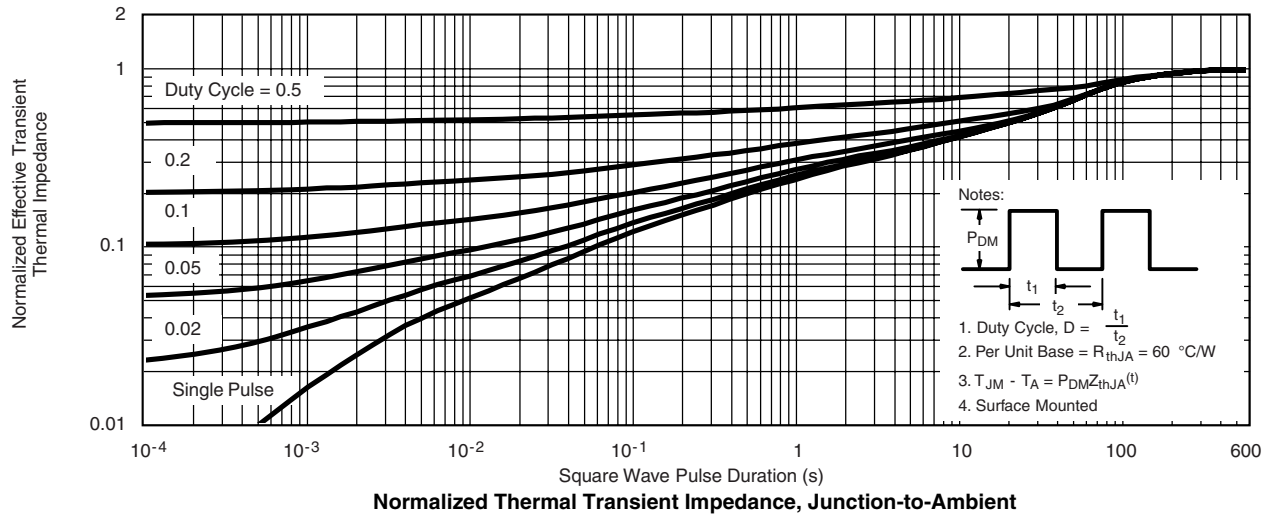
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



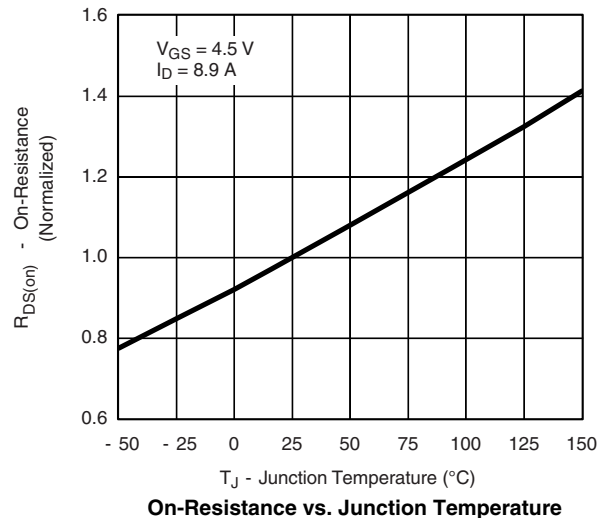
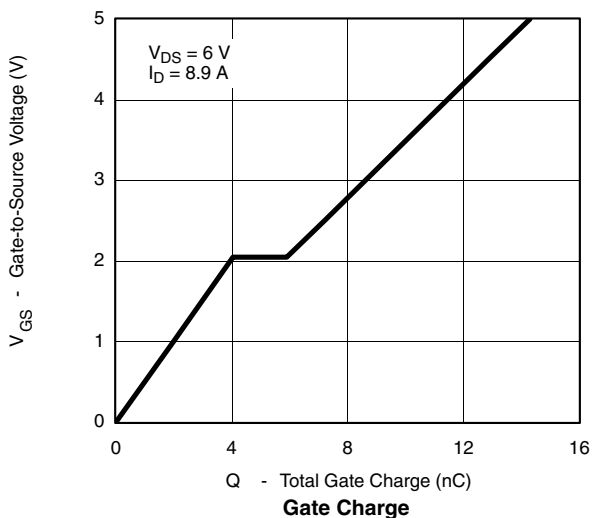
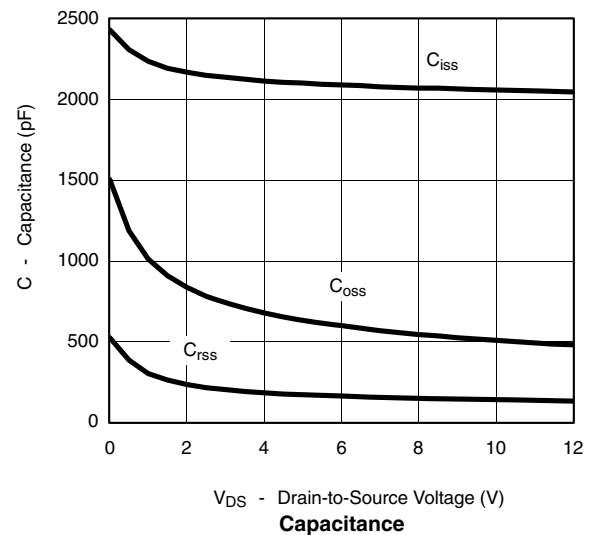
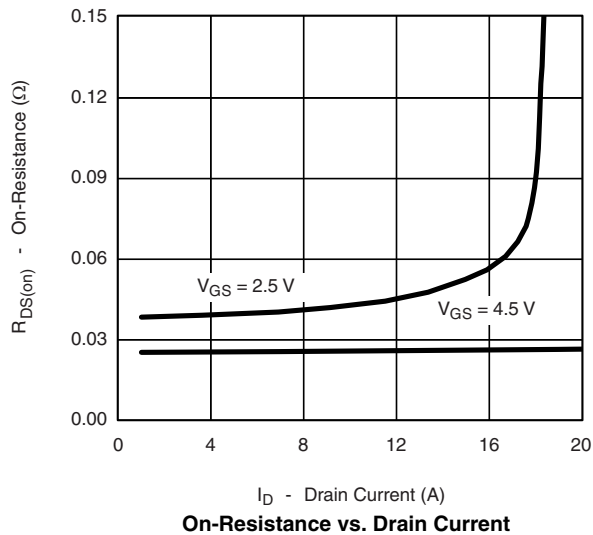
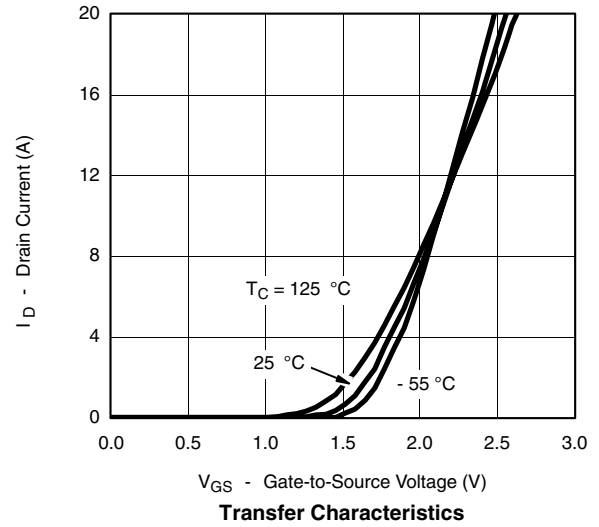
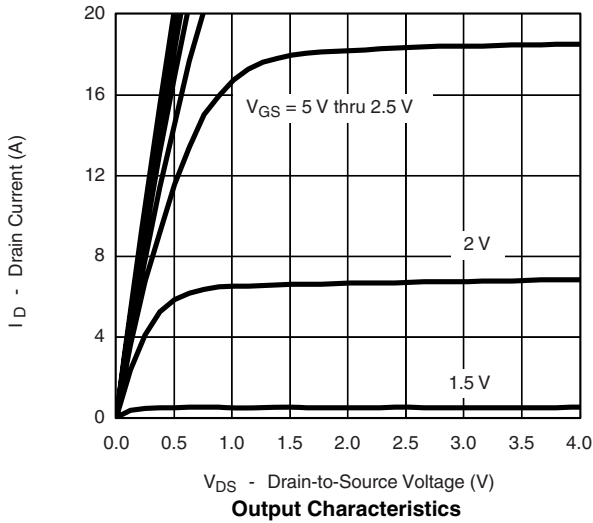
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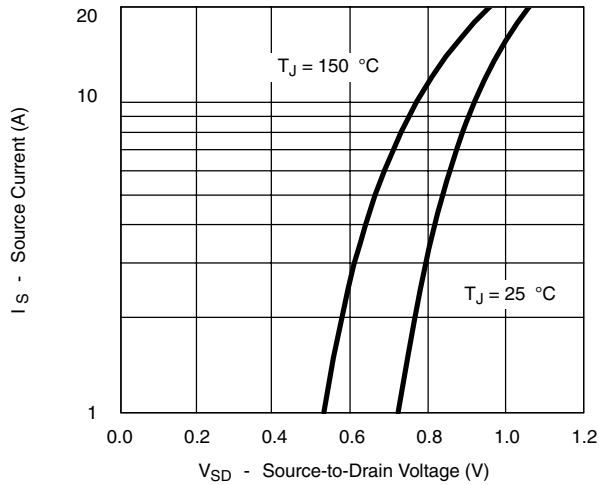
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



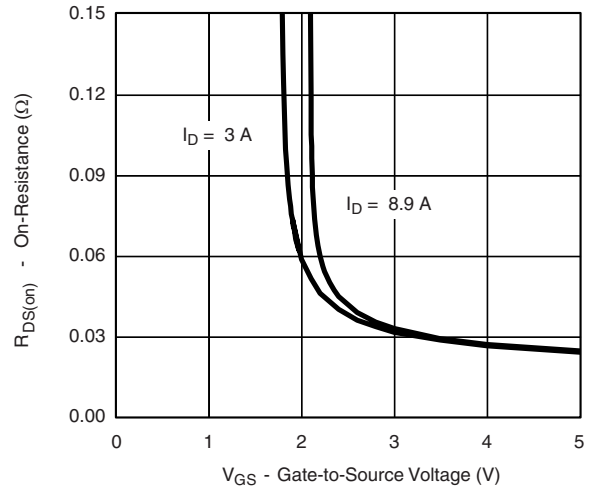
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



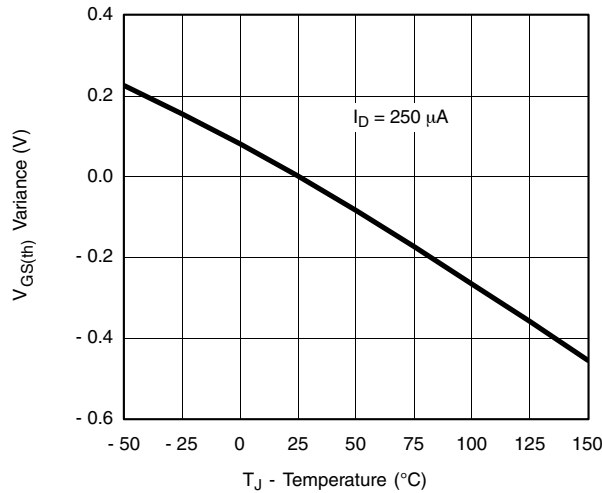
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



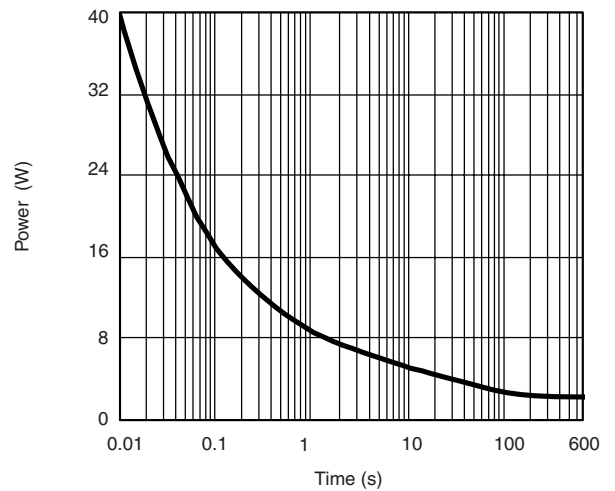
Source-Drain Diode Forward Voltage



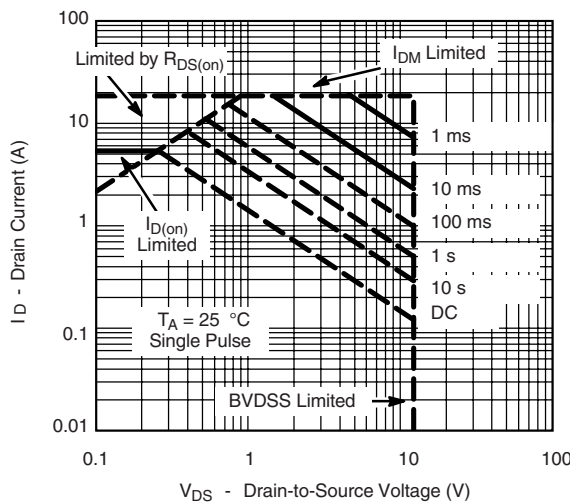
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

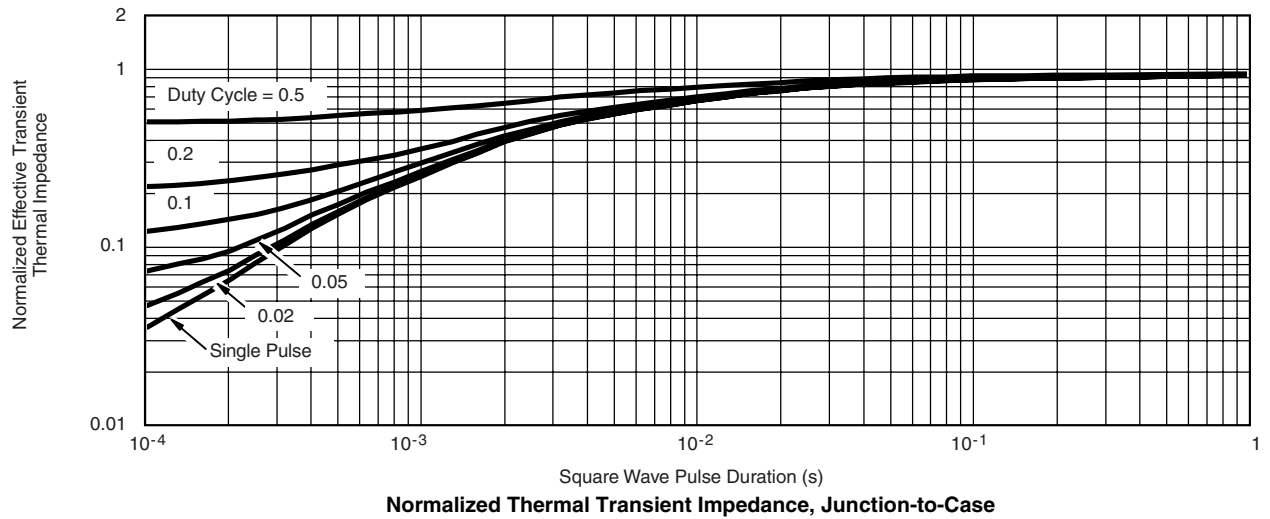
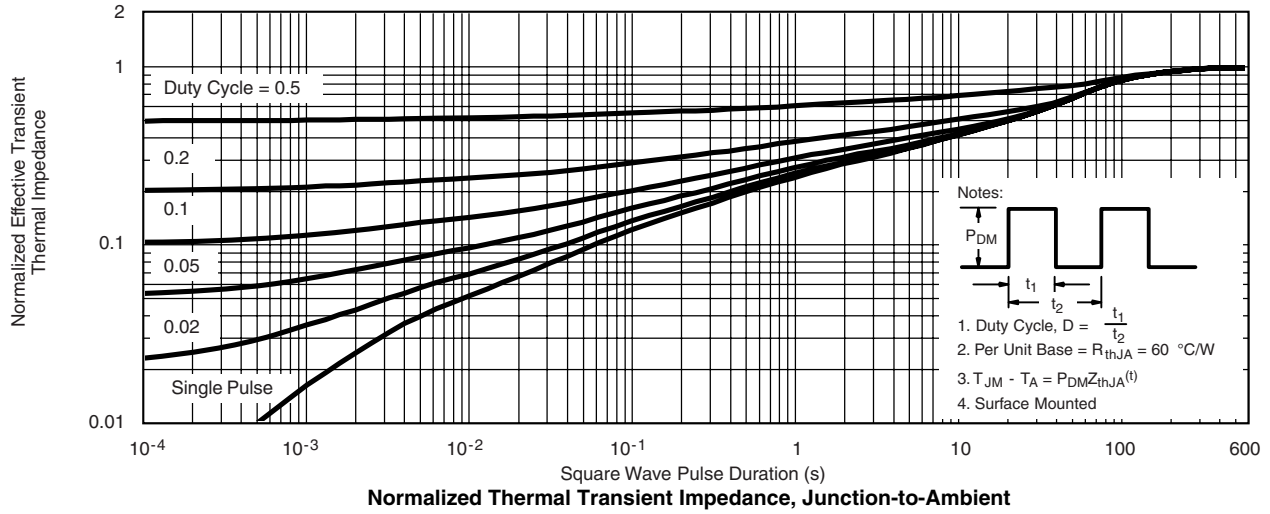


Single Pulse Power



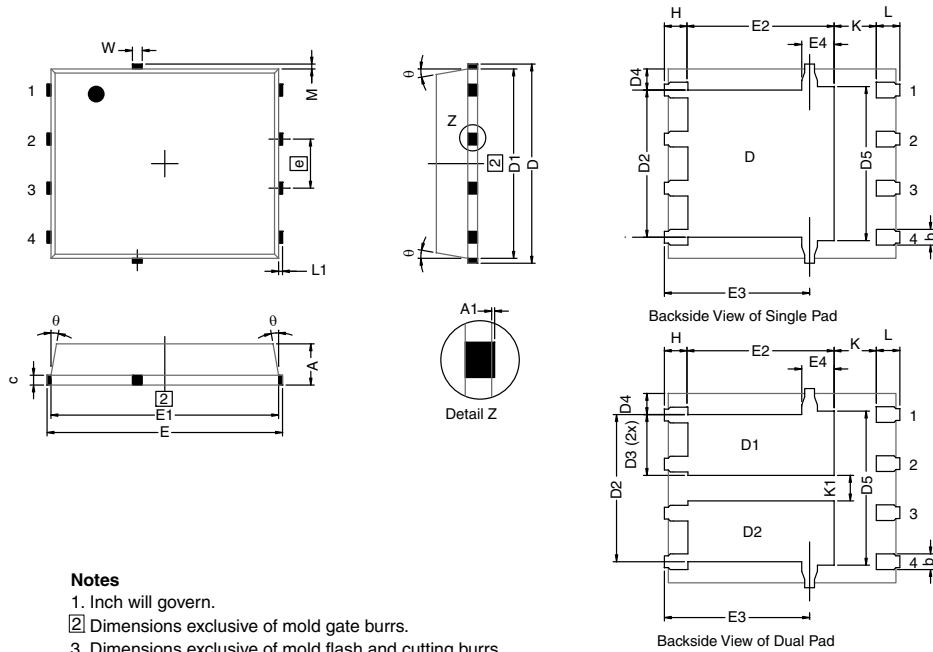
Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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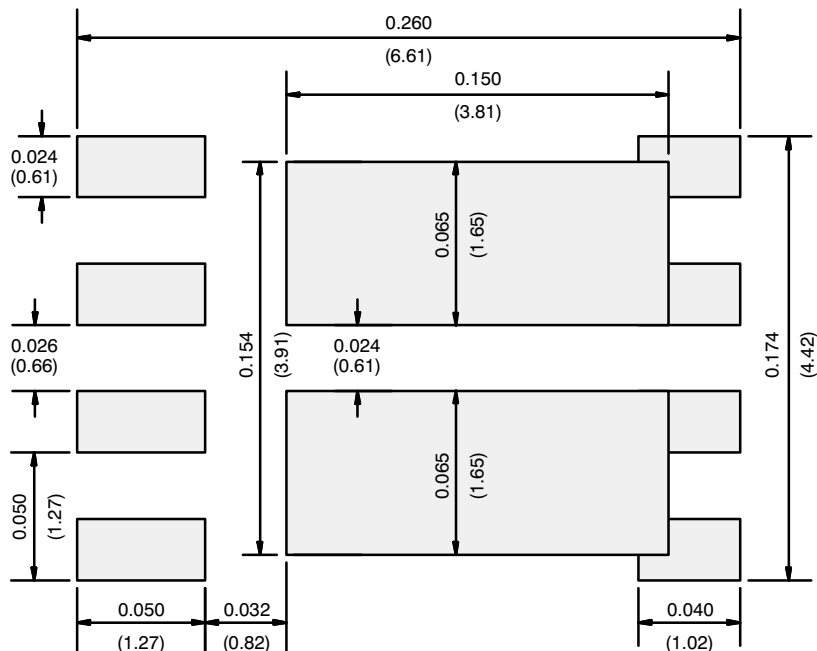
PowerPAK[®] SO-8, (Single/Dual)



- Notes**
1. Inch will govern.
 2. Dimensions exclusive of mold gate burrs.
 3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)	0.58 typ.			0.023 typ.		
E4 (for other product)	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K (for AL product)	1.45 typ.			0.057 typ.		
K (for other product)	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C13-0702-Rev. K, 20-May-13						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Dual



Recommended Minimum Pads
Dimensions in Inches/(mm)

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