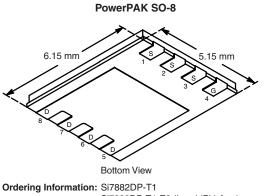


N-Channel Reduced Q_q, Fast Switching MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	
12	0.0055 at V_{GS} = 4.5 V	22	
12	0.008 at V _{GS} = 2.5 V	18	

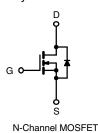


FEATURES

- Halogen-free available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- PWM Optimized for High Efficiency
- 100 % R_g Tested

APPLICATIONS

- Point-of-Load Synchronous Rectifier
- 5 V or 3.3 V BUS Step Down
- Q_a Optimized for 500 kHz Operation
- Synchronous Buck, Shoot-Thru Resistant



Bottom View	
Ordering Information: Si7882DP-T1 Si7882DP-T1-E3 (Lead (Pb)-free Si7882DP-T1-GE3 (Lead (Pb)-fr	
ABSOLUTE MAXIMUM RATINGS	$T_A = 25 ^{\circ}C$, unless otherwise noted

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	12		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _{.1} = 150 °C) ^a	T _A = 25 °C	1-	22	13	
Continuous Drain Current $(T_j = 150 \text{ C})$	T _A = 70 °C	$T_A = 70 \degree C$ I_D		11	
Pulsed Drain Current		I _{DM}	50		А
Continuous Source Current (Diode Conduction) ^a		۱ _S	4.1	1.6	
Single Pulse Avalanche Energy		I _{AS}	12		
Avalanche Energy	L = 0.1 mH		7.2		mJ
Mauinum Davier Disainational	T _A = 25 °C	PD	5	1.9	W
Maximum Power Dissipation ^a	T _A = 70 °C	' D	3.2	1.2	vv
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			2	60	50

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum lunction to Ambient (MOCEET) ⁸	t ≤ 10 s	R _{thJA}	20	25	
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State	''tnJA	55	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.0	2.6	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply.



RoHS COMPLIANT



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	0.6		1.4	V	
Gate-Body Leakage	I _{GSS}				± 100	nA	
Zana Oata Maltana Duain Ourreat		$V_{DS} = 12 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 12 V, V_{GS} = 0 V, T_{J} = 70 °C			5	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5$ V, $V_{GS} = 4.5$ V	40			А	
	Б	V _{GS} = 4.5 V, I _D = 17 A		0.0045	0.0055	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 14 \text{ A}$		0.0065	0.008	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 6 V, I_{D} = 17 A$		80		S	
Diode Forward Voltage ^a	V _{SD}	$I_{S} = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.70	1.1	V	
Dynamic ^b							
Total Gate Charge	Qg			21	30		
Gate-Source Charge	Q _{gs}	$V_{DS} = 6 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 17 \text{ A}$		4.6		nC	
Gate-Drain Charge	Q _{gd}			3.5		1	
Gate Resistance	R _g		0.8		3.5	Ω	
Turn-On Delay Time	t _{d(on)}			28	42		
Rise Time	t _r	V_{DD} = 6 V, R_L = 6 Ω		32	48		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong \text{1}$ A, V_GEN = 4.5 V, R_G = 6 Ω		82	123	ns	
Fall Time	t _f			35	53		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.7 A, di/dt = 100 A/μs		60	90		

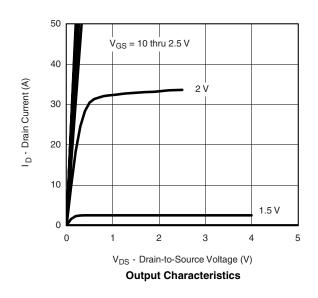
Notes:

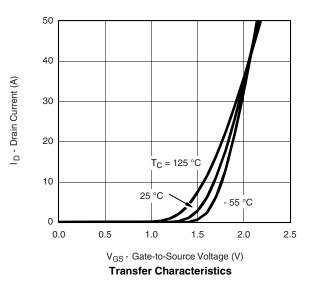
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

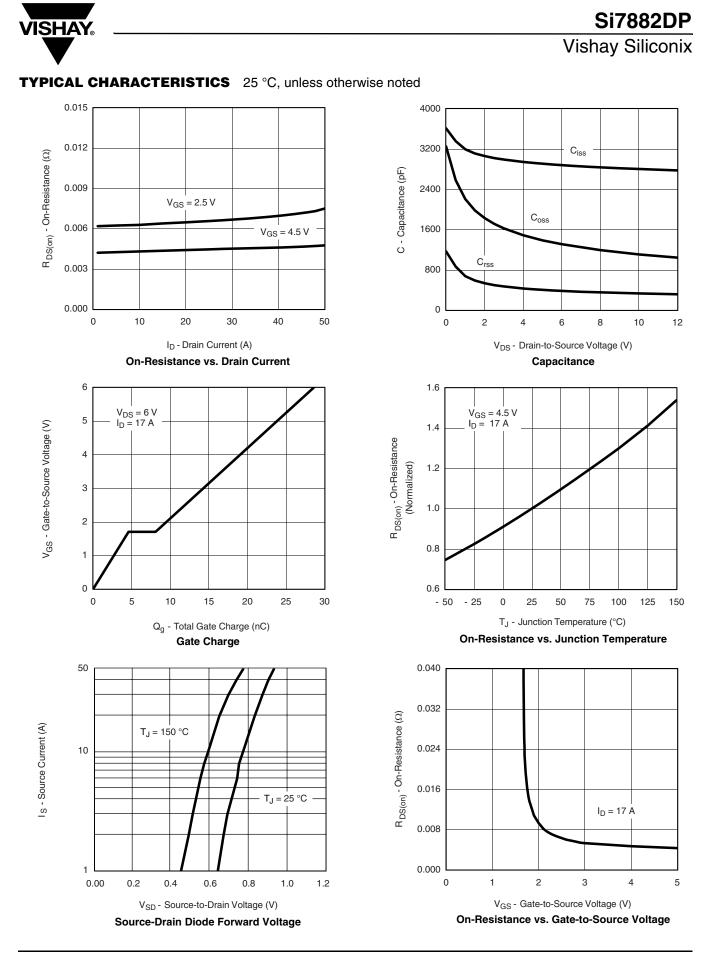
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

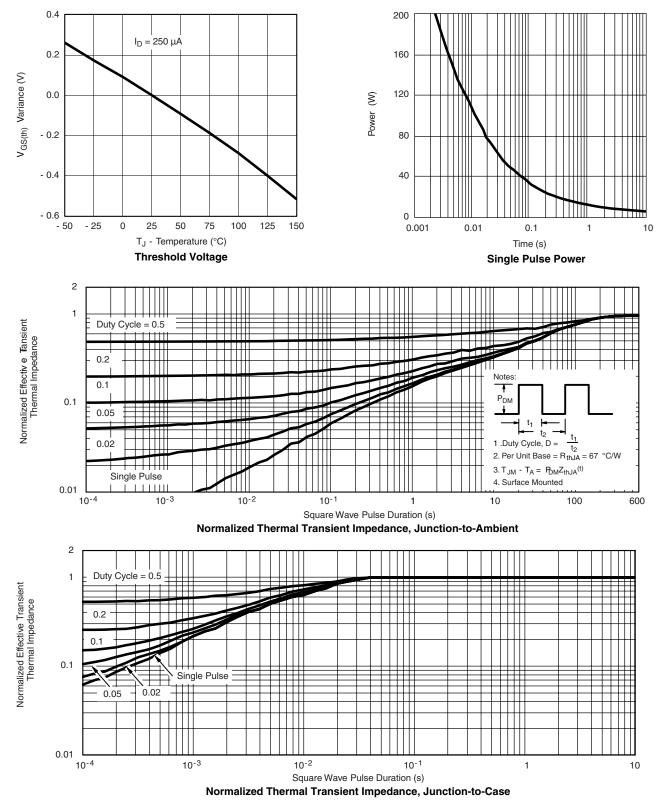






Document Number: 71858 S-80439-Rev. G, 03-Mar-08

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71858.





PowerPAK[®] SO-8, (Single/Dual)









Backside View of Dual Pad

Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4		0.57 typ.			0.0225 typ.		
D5		3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)		0.58 typ.		0.023 typ.			
E4 (for other product)		0.75 typ.		0.030 typ.			
е	1.27 BSC			0.050 BSC			
K (for AL product)		1.45 typ.		0.057 typ.			
K (for other product)		1.27 typ.		0.050 typ.			
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.			0.005 typ.			

Revison: 20-May-13

Document Number: 71655



Application Note 826

Vishay Siliconix

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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Vishay

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