ANALOG DEVICES

High Voltage Latch-Up Proof, Triple/Quad SPDT Switches

Data Sheet

ADG5233/ADG5234

FEATURES

Latch-up proof
2.8 pF off source capacitance
9 pF off drain capacitance
0.4 pC charge injection
Low on resistance: 160 Ω typical
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
48 V supply maximum ratings
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
V_{DD} to V_{SS} analog signal range
Human body model (HBM) ESD rating (TSSOP)
  8 kV input/output port to supplies
  2 kV input/output port to input/output port
  8 kV all other pins

APPLICATIONS

Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

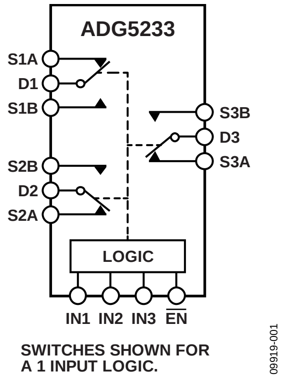

Figure 1. ADG5233 TSSOP and LFCSP_WQ

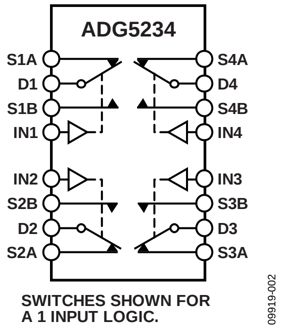

Figure 2. ADG5234 TSSOP and LFCSP_WQ

GENERAL DESCRIPTION

The ADG5233 and ADG5234 are monolithic industrial CMOS analog switches comprising three independently selectable single-pole, double throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input on the ADG5233 (LFCSP and TSSOP packages) is used to enable or disable the device. When disabled, all channels are switched off.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make these devices suitable for video signal switching.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Ultralow Capacitance and 0.4 pC Charge Injection.
3. Dual-Supply Operation.
   For applications where the analog signal is bipolar, the ADG5233/ADG5234 can be operated from dual supplies up to ±22 V.
4. Single-Supply Operation.
   For applications where the analog signal is unipolar, the ADG5233/ADG5234 can be operated from a single-rail power supply up to 40 V.
5. 3 V Logic-Compatible Digital Inputs.
   $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_L Logic Power Supply Required.

Rev. C
Document Feedback

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SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	160			Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 34
	200	250	280	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	38			Ω typ	V_S = ±10 V, I_S = −1 mA
	50	65	70	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			nA typ	V_S = V_D = ±10 V; see Figure 32
	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	160	190	215	ns max	V_S = 10 V; see Figure 39
t_{ON} ($\overline{EN}$)	145			ns typ	R_L = 300 Ω, C_L = 35 pF
	175	210	240	ns max	V_S = 10 V; see Figure 41
t_{OFF} ($\overline{EN}$)	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	155	170	180	ns max	V_S = 10 V; see Figure 41
Break-Before-Make Time Delay, t_D	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			25	ns min	V_{S1} = V_{S2} = 10 V; see Figure 40
Charge Injection, Q_{INJ}	0.4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 42
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 35
−3 dB Bandwidth	355			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 38
Insertion Loss	−6.4			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
C_S (Off)	2.8			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	9			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	13			pF typ	V_S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1] (LFCSP ONLY)					
Transition Time, $t_{TRANSITION}$	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	210	250	280	ns max	V_S = 10 V; see Figure 39
t_{ON} ($\overline{EN}$)	175			ns typ	R_L = 300 Ω, C_L = 35 pF
	215	255	290	ns max	V_S = 10 V; see Figure 41
t_{OFF} ($\overline{EN}$)	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	100	115	125	ns max	V_S = 10 V; see Figure 41
Break-Before-Make Time Delay, t_D	60			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 10 V; see Figure 40
Charge Injection, Q_{INJ}	−0.6			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 42
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 35
−3 dB Bandwidth	205			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 38
Insertion Loss	−6.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
C_S (Off)	4.5			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	10			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	15			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			μA typ	Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	140			Ω typ	V_S = ±15 V, I_S = −1 mA; see Figure 34
	160	200	230	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±15 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	33			Ω typ	V_S = ±15 V, I_S = −1 mA
	45	55	60	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = ±15 V, V_D = $\mp$15 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±15 V, V_D = $\mp$15 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			nA typ	V_S = V_D = ±15 V; see Figure 32
	±0.2	±0.3	±0.9	nA max	

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	125			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	155	180	200	ns max	$V_S = 10$ V; see Figure 39
t_{ON} ($\overline{EN}$)	145			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	170	200	220	ns max	$V_S = 10$ V; see Figure 41
t_{OFF} ($\overline{EN}$)	125			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	155	160	170	ns max	$V_S = 10$ V; see Figure 41
Break-Before-Make Time Delay, t_D	40			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
			20	ns min	$V_{S1} = V_{S2} = 10$ V; see Figure 40
Charge Injection, Q_{INJ}	0.7			pC typ	$V_S = 0$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 42
Off Isolation	−76			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−87			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 35
−3 dB Bandwidth	370			MHz typ	$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 38
Insertion Loss	−5.6			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 38
C_S (Off)	2.8			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (Off)	9			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (On), C_S (On)	13			pF typ	$V_S = 0$ V, f = 1 MHz
DYNAMIC CHARACTERISTICS[1] (LFCSP ONLY)					
Transition Time, $t_{TRANSITION}$	170			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	200	235	260	ns max	$V_S = 10$ V; see Figure 39
t_{ON} ($\overline{EN}$)	165			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	200	240	265	ns max	$V_S = 10$ V; see Figure 41
t_{OFF} ($\overline{EN}$)	80			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	95	105	115	ns max	$V_S = 10$ V; see Figure 41
Break-Before-Make Time Delay, t_D	50			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
			30	ns min	$V_{S1} = V_{S2} = 10$ V; see Figure 40
Charge Injection, Q_{INJ}	0			pC typ	$V_S = 0$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 42
Off Isolation	−75			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−80			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 35
−3 dB Bandwidth	210			MHz typ	$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 38
Insertion Loss	−5.5			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 38
C_S (Off)	4.5			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (Off)	10			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (On), C_S (On)	15			pF typ	$V_S = 0$ V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			µA typ	Digital inputs = 0 V or V_{DD}
	70		110	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	360			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA; see Figure 34
	500	610	700	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	5.5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	20	21	22	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	170			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	280	335	370	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			nA typ	V_S = V_D = 1 V/10 V; see Figure 32
	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1] (TSSOP ONLY)					
Transition Time, $t_{TRANSITION}$	165			ns typ	R_L = 300 Ω, C_L = 35 pF
	215	260	300	ns max	V_S = 8 V; see Figure 39
t_{ON} ($\overline{EN}$)	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	245	305	350	ns max	V_S = 8 V; see Figure 41
t_{OFF} ($\overline{EN}$)	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	165	180	200	ns max	V_S = 8 V; see Figure 41
Break-Before-Make Time Delay, t_D	85			ns typ	R_L = 300 Ω, C_L = 35 pF
			45	ns min	V_{S1} = V_{S2} = 8 V; see Figure 40
Charge Injection, Q_{INJ}	0			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 42
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth	260			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 38
Insertion Loss	−9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
C_S (Off)	3			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	10			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	14			pF typ	V_S = 6 V, f = 1 MHz
DYNAMIC CHARACTERISTICS[1] (LFCSP ONLY)					
Transition Time, $t_{TRANSITION}$	235			ns typ	R_L = 300 Ω, C_L = 35 pF
	295	365	410	ns max	V_S = 8 V; see Figure 39
t_{ON} ($\overline{EN}$)	240			ns typ	R_L = 300 Ω, C_L = 35 pF
	305	380	430	ns max	V_S = 8 V; see Figure 41
t_{OFF} ($\overline{EN}$)	70			ns typ	R_L = 300 Ω, C_L = 35 pF
	90	105	115	ns max	V_S = 8 V; see Figure 41
Break-Before-Make Time Delay, t_D	125			ns typ	R_L = 300 Ω, C_L = 35 pF
			65	ns min	V_{S1} = V_{S2} = 8 V; see Figure 40
Charge Injection, Q_{INJ}	0			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 42
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
−3 dB Bandwidth	172			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 38
Insertion Loss	−8.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
C_S (Off)	5			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	11			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	16			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			µA typ	Digital inputs = 0 V or V_{DD}
	50		65	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	140			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA; see Figure 34
	170	215	245	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	35			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	50	60	65	Ω max	

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 36
	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			nA typ	V_S = V_D = 1 V/30 V; see Figure 32
	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS (TSSOP ONLY)[1]					
Transition Time, $t_{TRANSITION}$	155			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	215	230	ns max	V_S = 18 V; see Figure 39
t_{ON} ($\overline{EN}$)	180			ns typ	R_L = 300 Ω, C_L = 35 pF
	215	235	250	ns max	V_S = 18 V; see Figure 41
t_{OFF} ($\overline{EN}$)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	190	190	190	ns max	V_S = 18 V; see Figure 41
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			25	ns min	V_{S1} = V_{S2} = 18 V; see Figure 40
Charge Injection, Q_{INJ}	0.5			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 42
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
−3 dB Bandwidth	275			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 38
Insertion Loss	−6.2			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
C_S (Off)	2.8			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	9			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	13			pF typ	V_S = 18 V, f = 1 MHz
DYNAMIC CHARACTERISTICS (LFCSP ONLY)[1]					
Transition Time, $t_{TRANSITION}$	205			ns typ	R_L = 300 Ω, C_L = 35 pF
	255	275	290	ns max	V_S = 18 V; see Figure 39
t_{ON} ($\overline{EN}$)	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	240	265	290	ns max	V_S = 18 V; see Figure 41
t_{OFF} ($\overline{EN}$)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	115	115	ns max	V_S = 18 V; see Figure 41
Break-Before-Make Time Delay, t_D	65			ns typ	R_L = 300 Ω, C_L = 35 pF
			35	ns min	V_{S1} = V_{S2} = 18 V; see Figure 40
Charge Injection, Q_{INJ}	−0.6			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 42
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
−3 dB Bandwidth	190			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 38

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Insertion Loss	−5.9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 38
C_S (Off)	4.5			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	10			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	15			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	80			µA typ	Digital inputs = 0 V or V_{DD}
	100		130	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5. ADG5233

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	24	16	11	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	42	26.5	15	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	26	17	11	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	46	28	15	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	17	12	7.7	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	24	17	11	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	25	17	11	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	45	28	15	mA maximum

Table 6. ADG5234

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	21	15	10	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	38	24	14	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	22	15	10	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	41	26	15	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	15	11	7	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	22	16	11	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	22	15	10	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	40	26	15	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	
ADG5233	76 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5234	67 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
20-Lead TSSOP (4-Layer Board)	143°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
20-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C
Human Body Model (HBM) ESD	
TSSOP	
Input/Output Port to Supplies	8 kV
Input/Output Port to Input/Output Port	2 kV
All Other Pins	8 kV
Human Body Model (HBM) ESD	
LFCSP	
Input/Output Port to Supplies	4 kV
Input/Output Port to Input/Output Port	1 kV
All Other Pins	4 kV

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

[2] See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

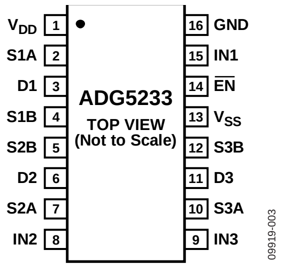
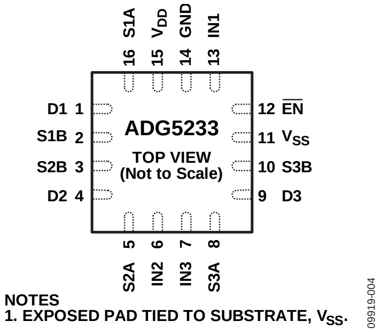


Figure 3. ADG5233 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.

Figure 4. ADG5233 LFCSP_WQ Pin Configuration

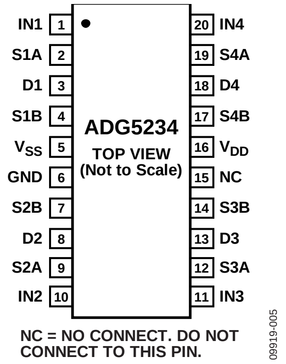
Table 8. ADG5233 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP_WQ**	**Mnemonic**	**Description**
1	15	V_{DD}	Most Positive Power Supply Potential.
2	16	S1A	Source Terminal 1A. This pin can be an input or an output.
3	1	D1	Drain Terminal 1. This pin can be an input or an output.
4	2	S1B	Source Terminal 1B. This pin can be an input or an output.
5	3	S2B	Source Terminal 2B. This pin can be an input or an output.
6	4	D2	Drain Terminal 2. This pin can be an input or an output.
7	5	S2A	Source Terminal 2A. This pin can be an input or an output.
8	6	IN2	Logic Control Input 2.
9	7	IN3	Logic Control Input 3.
10	8	S3A	Source Terminal 3A. This pin can be an input or an output.
11	9	D3	Drain Terminal 3. This pin can be an input or an output.
12	10	S3B	Source Terminal 3B. This pin can be an input or an output.
13	11	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
14	12	$\overline{\text{EN}}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches.
15	13	IN1	Logic Control Input 1.
16	14	GND	Ground (0 V) Reference.
	17	EPAD	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 9. ADG5233 Truth Table

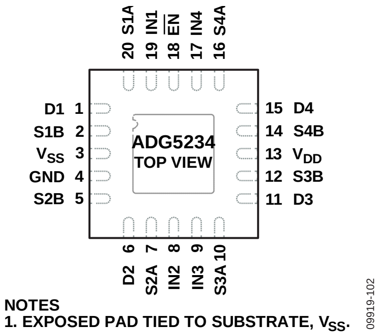
$\overline{\text{EN}}$	INx	SxA	SxB
1	X[1]	Off	Off
0	0	Off	On
0	1	On	Off

[1] X is don't care.



NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 5. ADG5234 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.

Figure 6. ADG5234 LFCSP_WQ Pin Configuration

Table 10. ADG5234 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP_WQ**	**Mnemonic**	**Description**
1	19	IN1	Logic Control Input 1.
2	20	S1A	Source Terminal 1A. This pin can be an input or an output.
3	1	D1	Drain Terminal 1. This pin can be an input or an output.
4	2	S1B	Source Terminal 1B. This pin can be an input or an output.
5	3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
6	4	GND	Ground (0 V) Reference.
7	5	S2B	Source Terminal 2B. This pin can be an input or an output.
8	6	D2	Drain Terminal 2. This pin can be an input or an output.
9	7	S2A	Source Terminal 2A. This pin can be an input or an output.
10	8	IN2	Logic Control Input 2.
11	9	IN3	Logic Control Input 3.
12	10	S3A	Source Terminal 3A. This pin can be an input or an output.
13	11	D3	Drain Terminal 3. This pin can be an input or an output.
14	12	S3B	Source Terminal 3B. This pin can be an input or an output.
15	N/A	NC	No Connect. This pin is open.
16	13	V_{DD}	Most Positive Power Supply Potential.
17	14	S4B	Source Terminal 4B. This pin can be an input or an output.
18	15	D4	Drain Terminal 4. This pin can be an input or an output.
19	16	S4A	Source Terminal 4A. This pin can be an input or an output.
20	17	IN4	Logic Control Input 4.
N/A	18	$\overline{\text{EN}}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches.
N/A	21	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG5234 Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

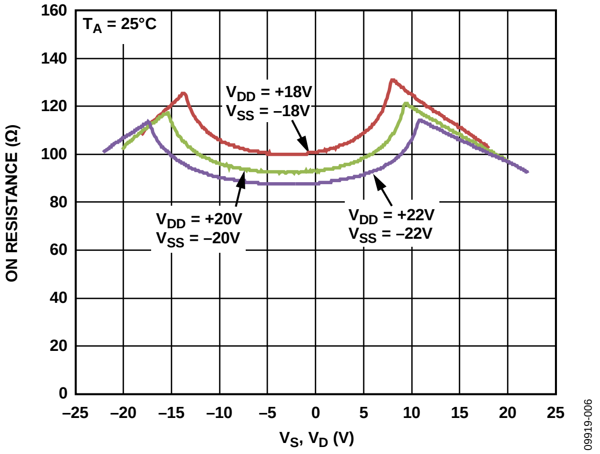


Figure 7. On Resistance as a Function of V_S, V_D (±20 V Dual Supply)

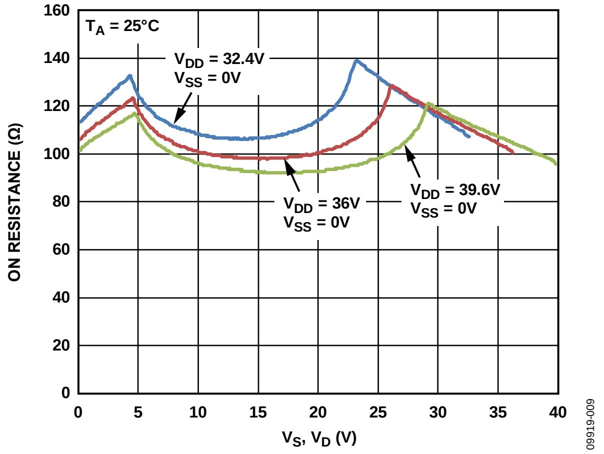


Figure 10. On Resistance as a Function of V_S, V_D (36 V Single Supply)

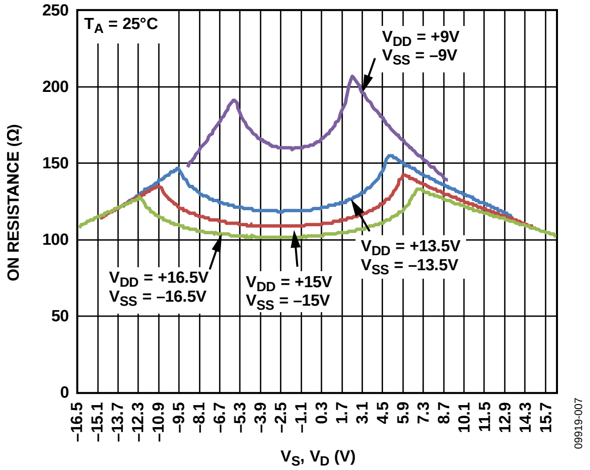


Figure 8. On Resistance as a Function of V_S, V_D (±15 V Dual Supply)

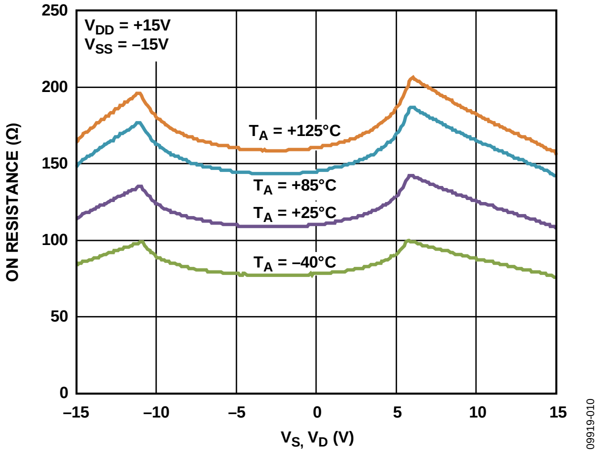


Figure 11. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

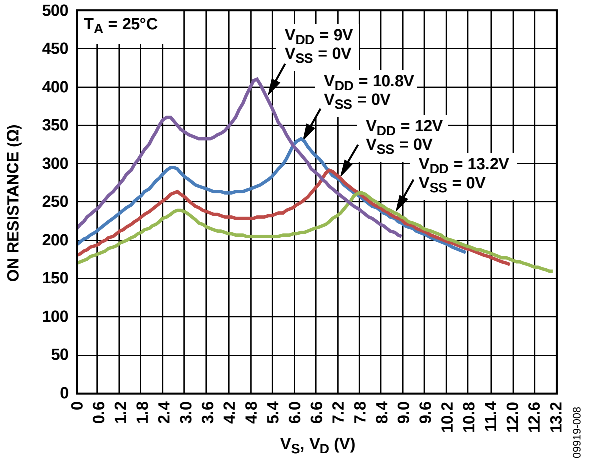


Figure 9. On Resistance as a Function of V_S, V_D (12 V Single Supply)

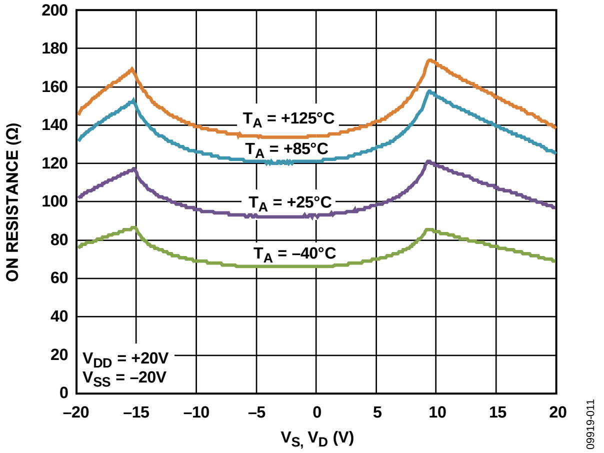


Figure 12. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

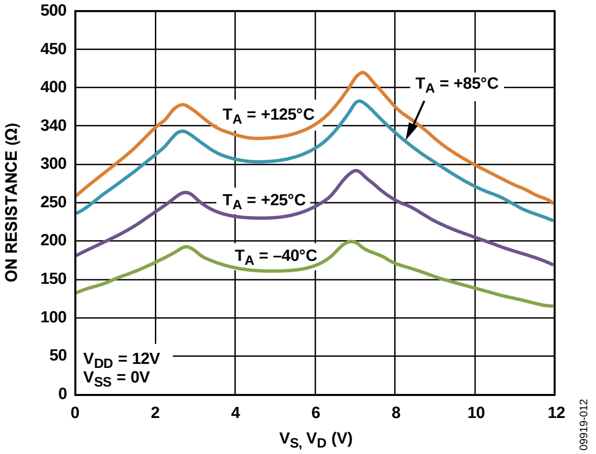


Figure 13. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

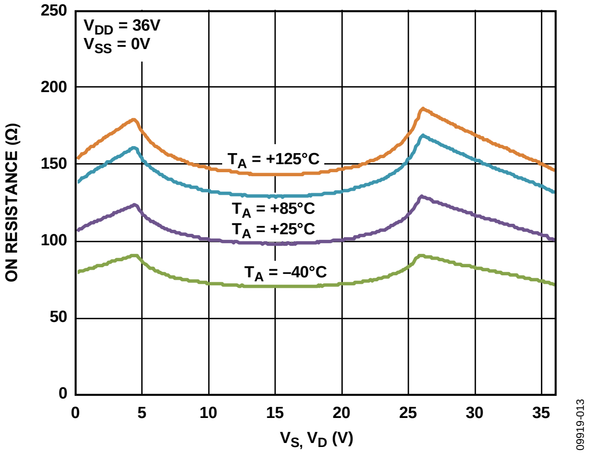


Figure 14. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

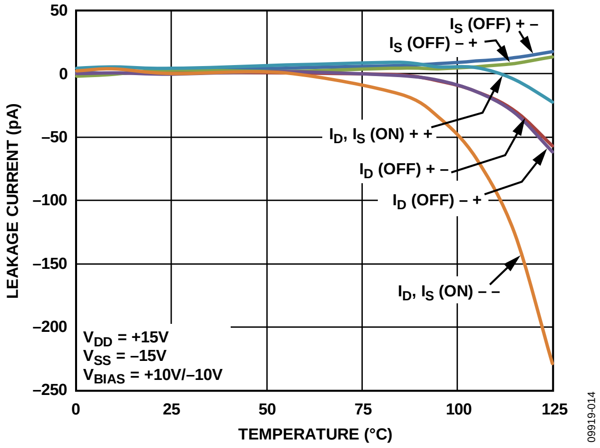


Figure 15. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

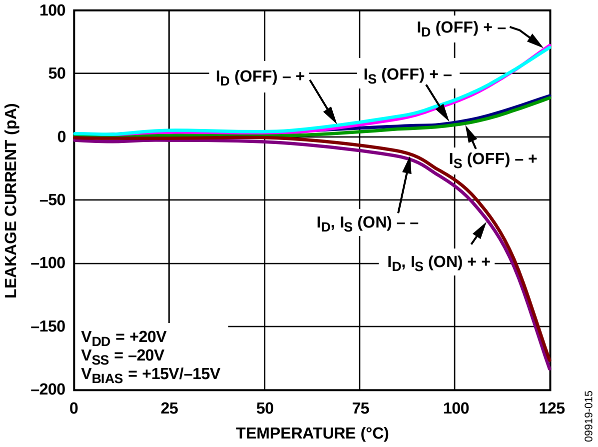


Figure 16. Leakage Currents as a Function of Temperature, ±20 V Dual Supply

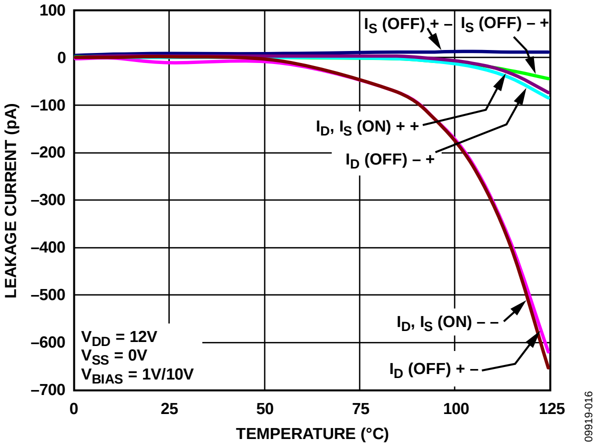


Figure 17. Leakage Currents as a Function of Temperature, 12 V Single Supply

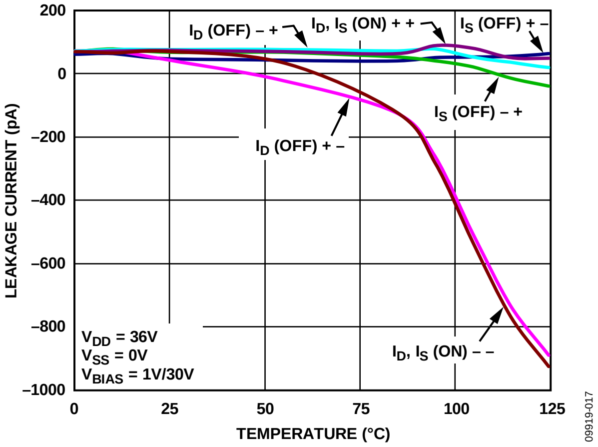


Figure 18. Leakage Currents as a Function of Temperature, 36 V Single Supply

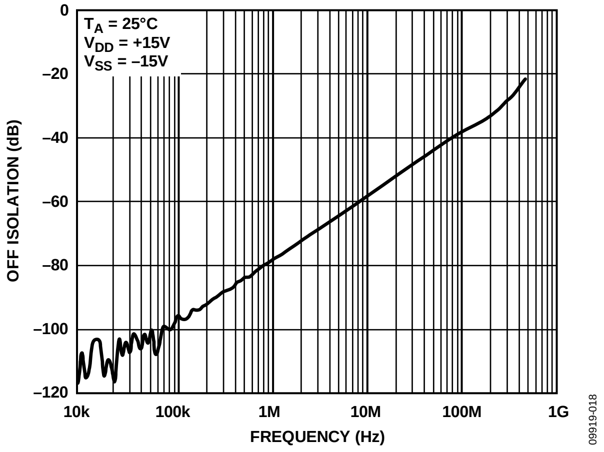


Figure 19. Off Isolation vs. Frequency, ±15 V Dual Supply

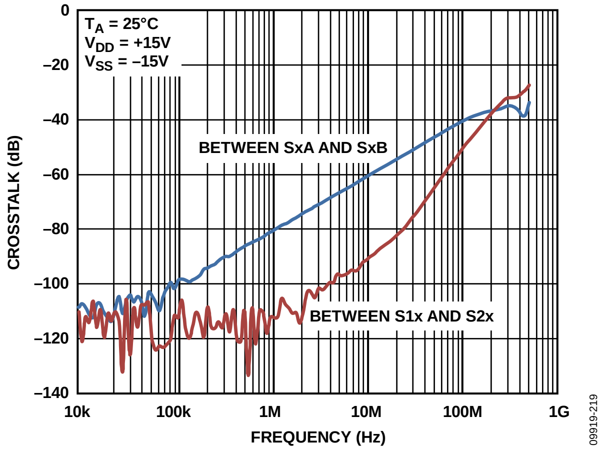


Figure 20. Crosstalk vs. Frequency, ±15 V Dual Supply (LFCSP)

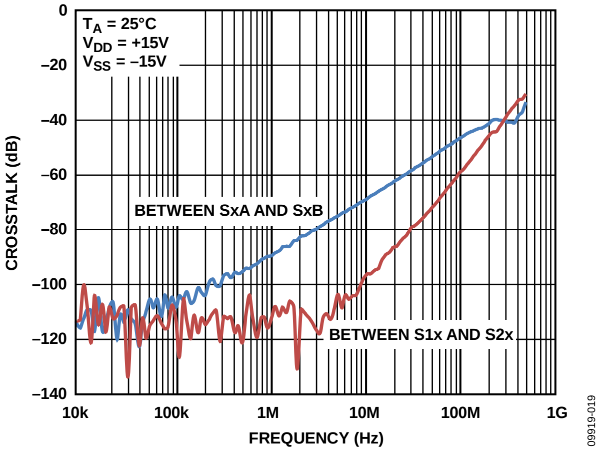


Figure 21. Crosstalk vs. Frequency, ±15 V Dual Supply (TSSOP)

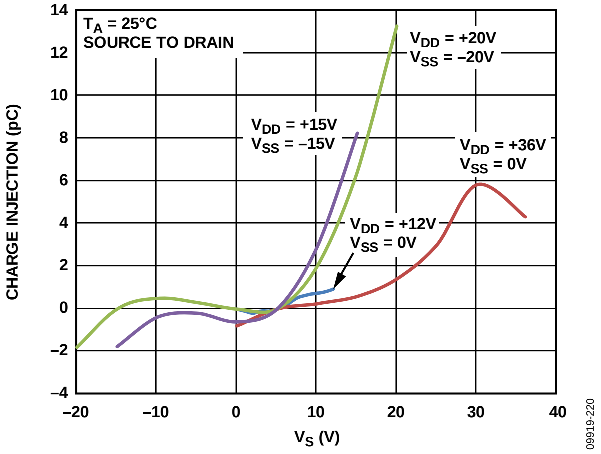


Figure 22. Charge Injection vs. Source Voltage, Source to Drain (LFCSP)

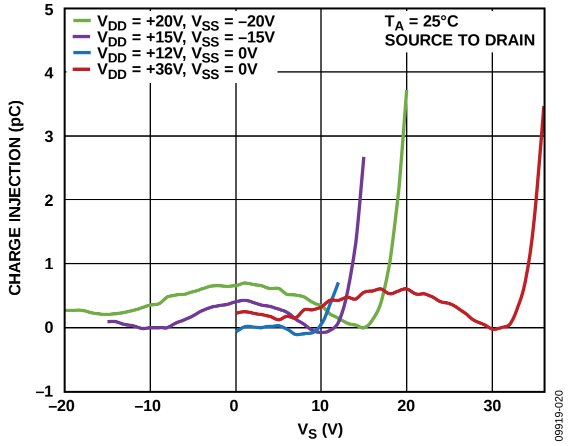


Figure 23. Charge Injection vs. Source Voltage, Source to Drain (TSSOP)

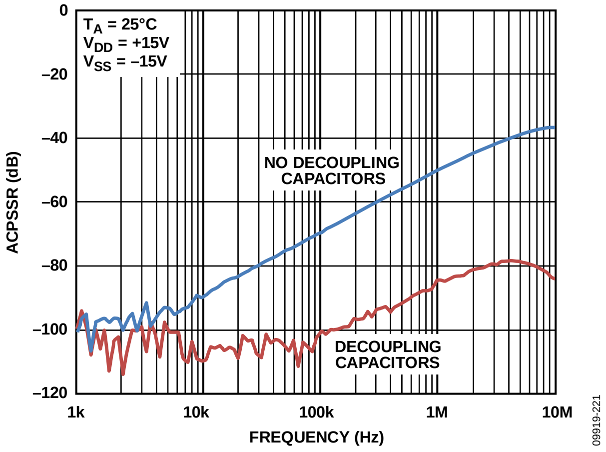


Figure 24. ACPSRR vs. Frequency, ±15 V Dual Supply (LFCSP)

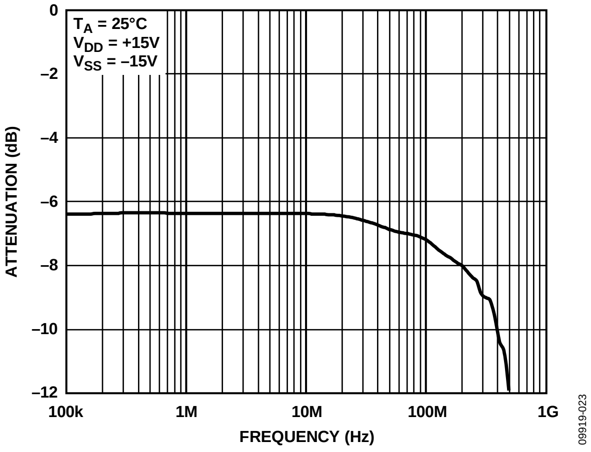


Figure 27. Bandwidth (TSSOP)

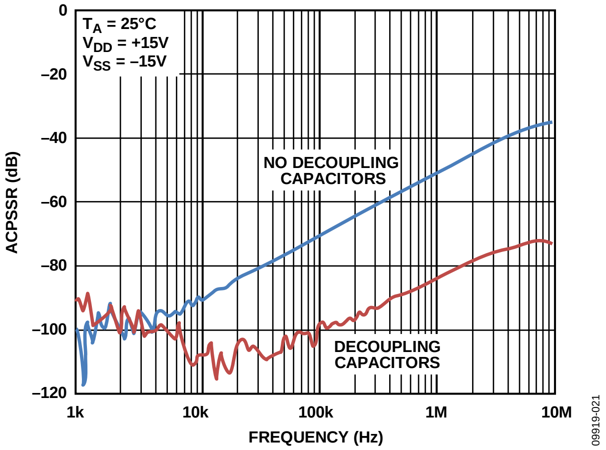


Figure 25. ACPSRR vs. Frequency, ±15 V Dual Supply (TSSOP)

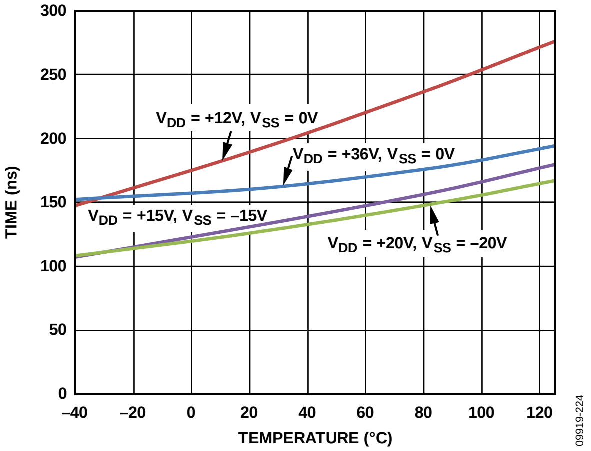


Figure 28. $t_{TRANSITION}$ Times vs. Temperature (LFCSP)

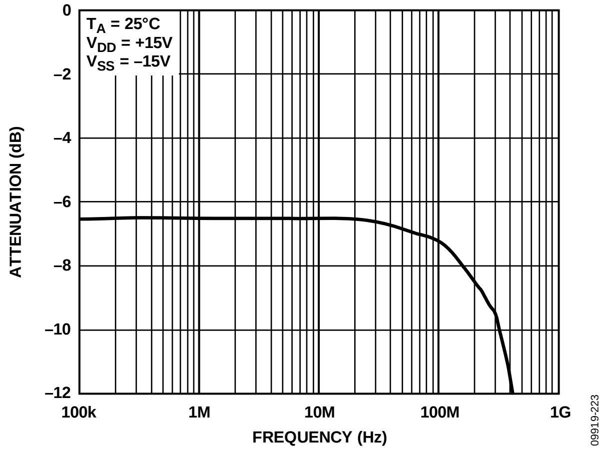


Figure 26. Bandwidth (LFCSP)

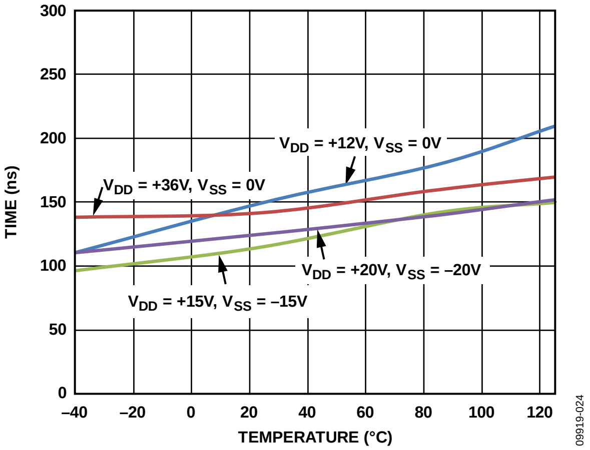


Figure 29. $t_{TRANSITION}$ Times vs. Temperature (TSSOP)

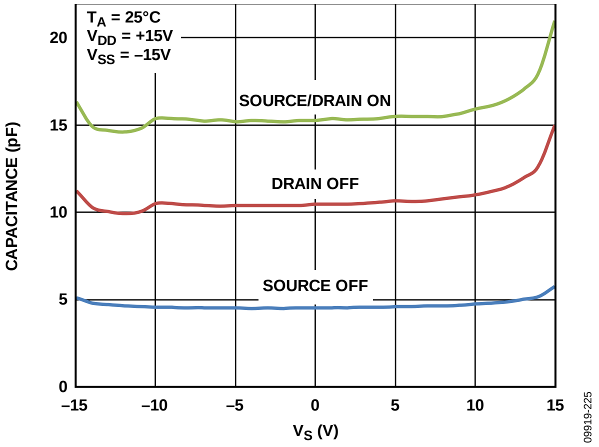


Figure 30. Capacitance vs. Source Voltage, ±15 V Dual Supply (LFCSP)

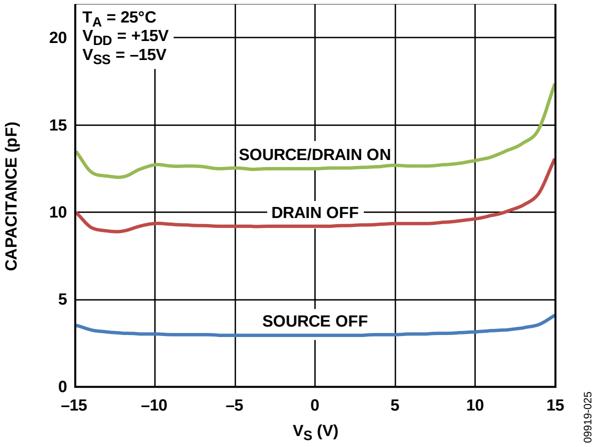


Figure 31. Capacitance vs. Source Voltage, ±15 V Dual Supply (TSSOP)

TEST CIRCUITS

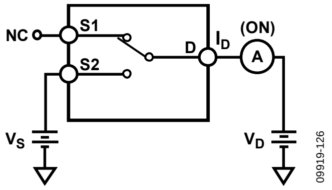


Figure 32. On Leakage

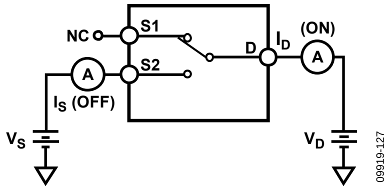


Figure 33. On and Off Leakage On and Off Leakage (ADG5234 TSSOP)

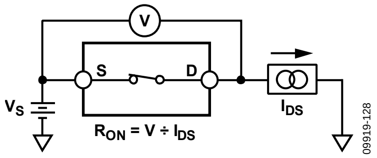


Figure 34. On Resistance

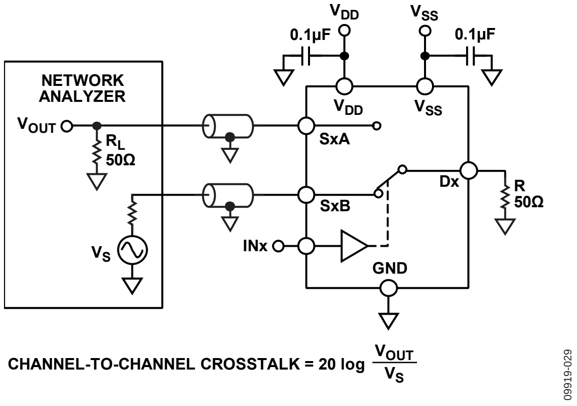


Figure 35. Channel-to-Channel Crosstalk

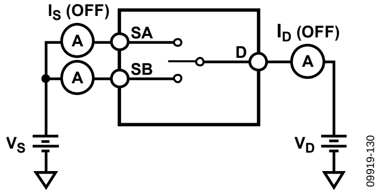


Figure 36. Off Leakage

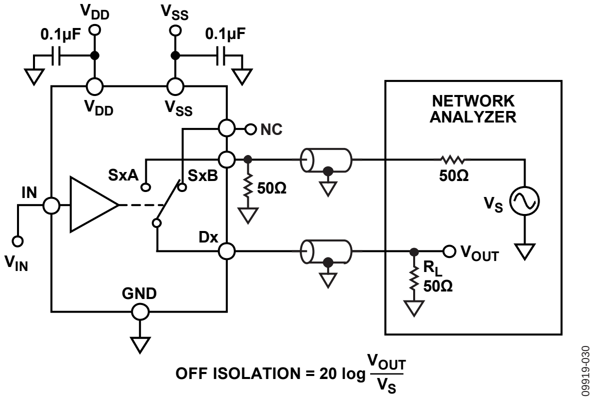


Figure 37. Off Isolation

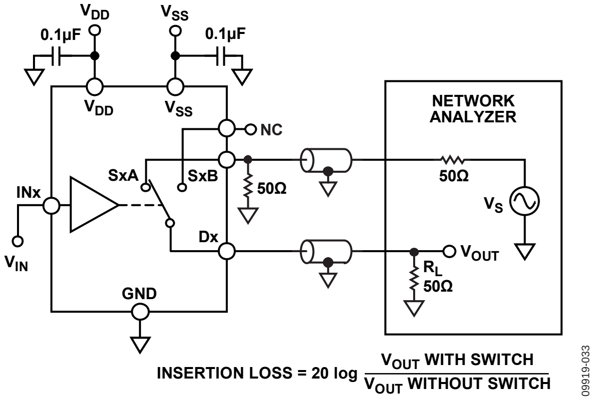


Figure 38. Bandwidth

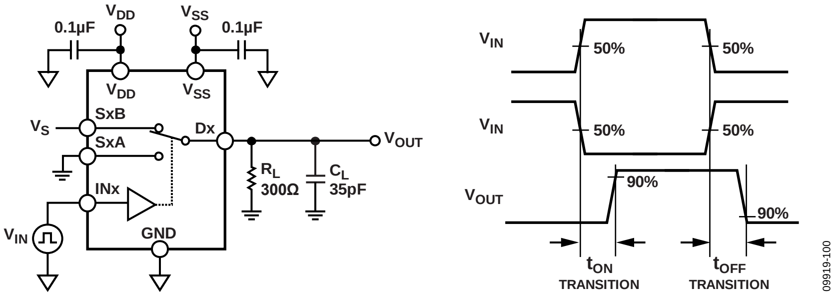


Figure 39. Switching Timing

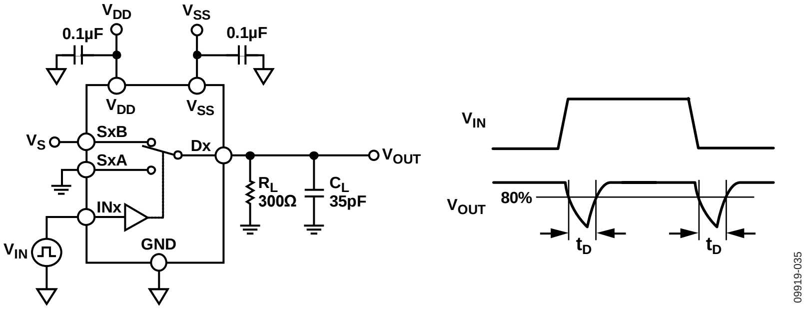


Figure 40. Break-Before-Make Delay, t_D

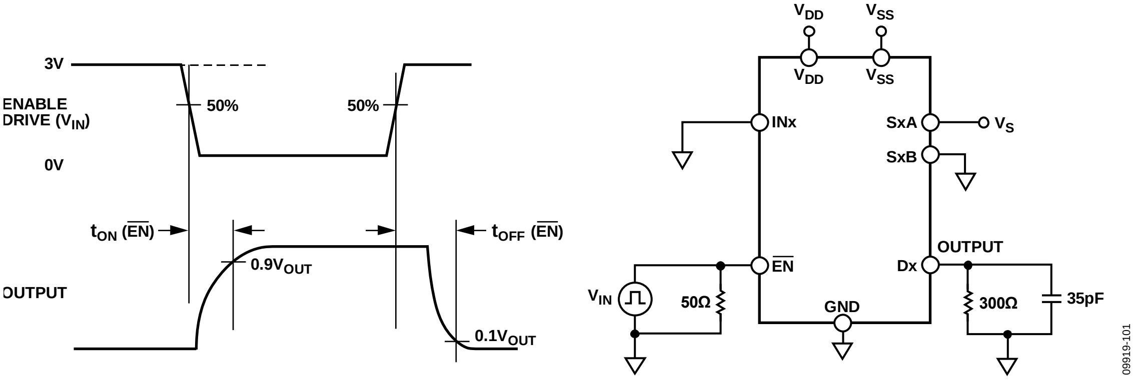


Figure 41. Enable Delay, t_{ON} $(\overline{EN})$, t_{OFF} $(\overline{EN})$

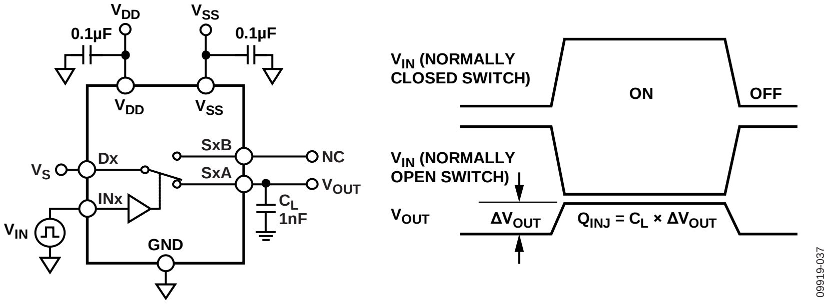


Figure 42. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal Dx and Terminal Sx, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal Dx and Terminal Sx.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

t_{ON} ($\overline{EN}$)

t_{ON} ($\overline{EN}$) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)

t_{OFF} ($\overline{EN}$) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is a measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the ADG5233/ADG5234, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

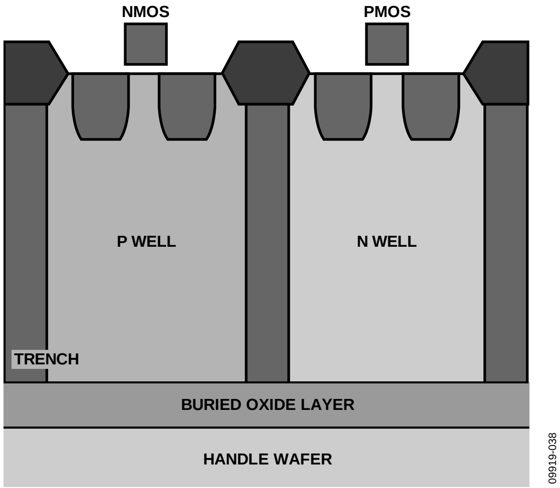


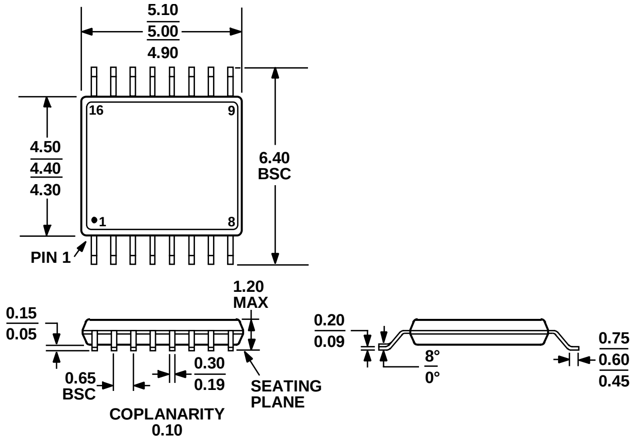
Figure 43. Trench Isolation

APPLICATIONS INFORMATION

The ADG52xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off.

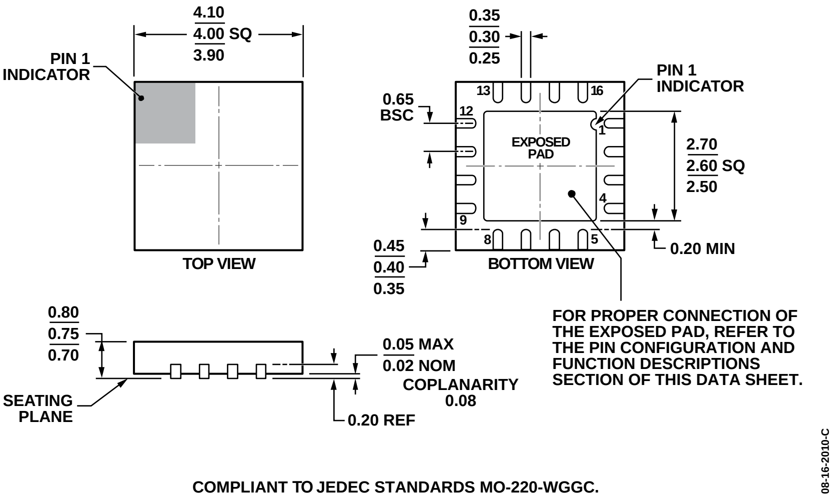
The ADG5233/ADG5234 high voltage switches allow single-supply operation from 9 V to 40 V and dual supply operation from ±9 V to ±22 V.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

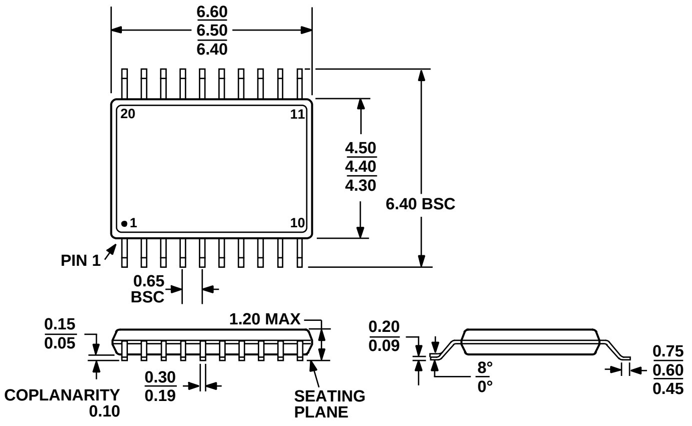
Figure 44. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

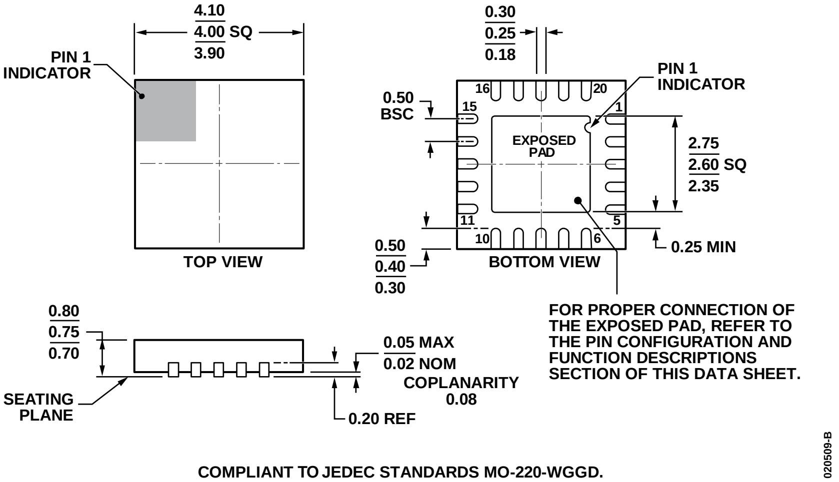
COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 45. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-17)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 46. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 47. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Description	$\overline{\text{EN}}$ Pin	Package Option
ADG5233BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG5233BRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG5233BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	Yes	CP-16-17
ADG5234BRUZ	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG5234BRUZ-RL7	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG5234BCPZ-RL7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	Yes	CP-20-8

[1] Z = RoHS Compliant Part.