DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT563

Octal D-type transparent latch; 3-state; inverting

Product specification

File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.
A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and $\overline{OE}$ are common to all latches.
When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay D_n, LE to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	14	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

    $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC   the condition is V_I = GND to V_{CC}
   for HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
20	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.
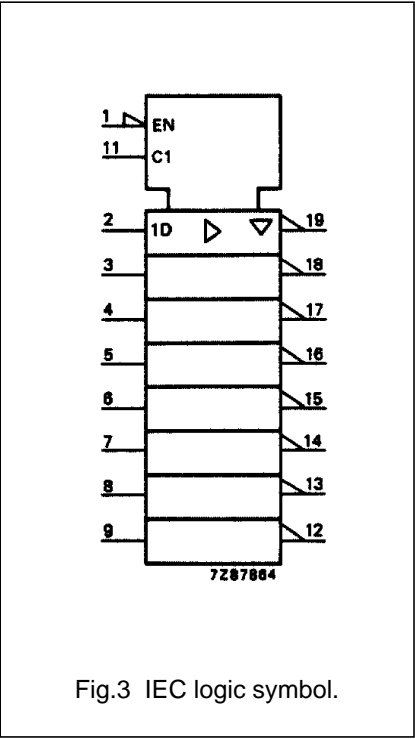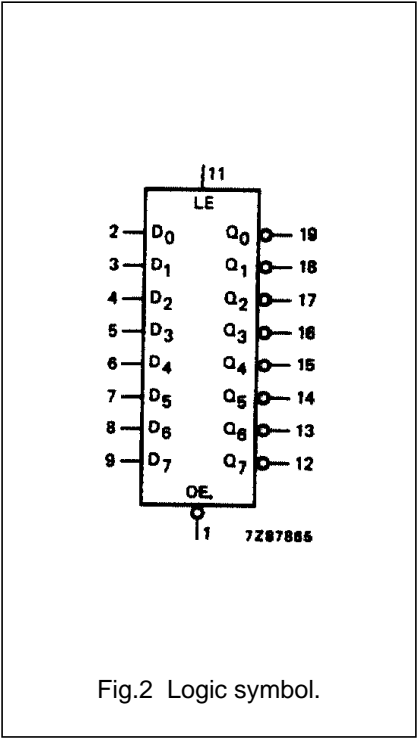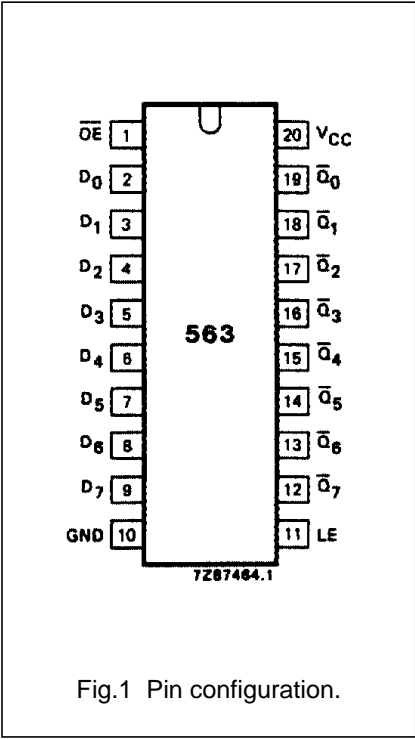
Octal D-type transparent latch; 3-state; inverting
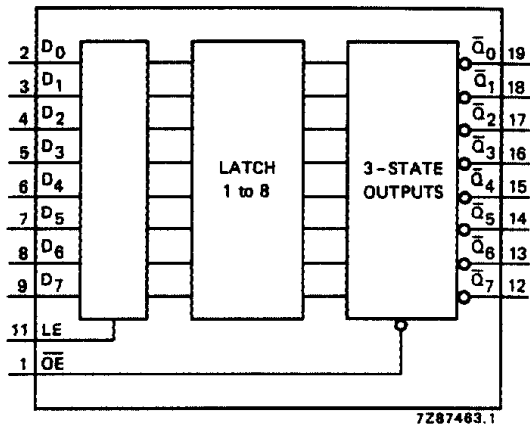
Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTER-NAL LATCHES	OUT-PUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
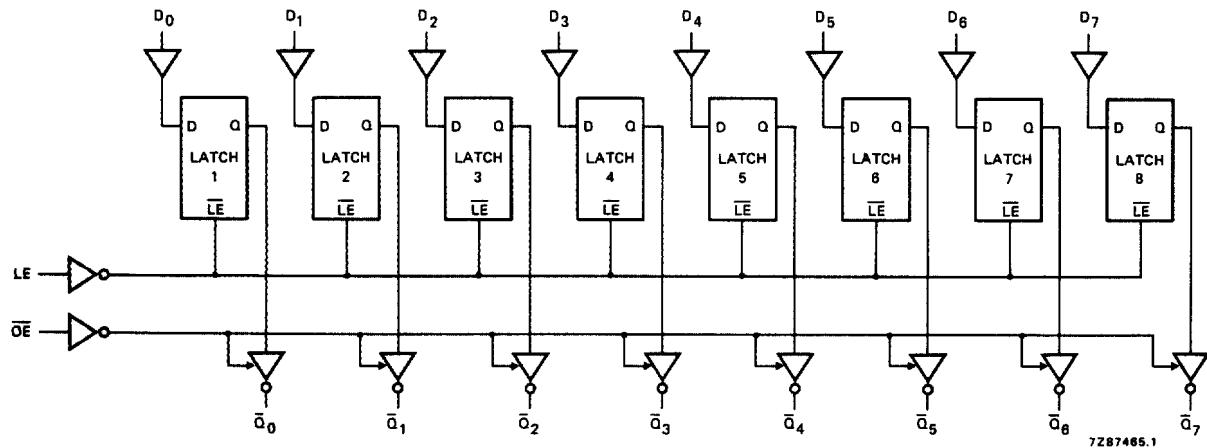   Z = high impedance OFF-state

Fig.5 Logic diagram.

Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to $\overline{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay LE to $\overline{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time D_n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t_h	hold time D_n to LE	4 4 4	−6 −2 −2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig.9

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inverting

74HC/HCT563

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
$\overline{LE}$	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		20	35		44		53	ns	4.5	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		22	35		44		53	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t_W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig.7
t_{su}	set-up time D_n to $\overline{LE}$	10	3		13		15		ns	4.5	Fig.9
t_h	hold time D_n to $\overline{LE}$	5	−1		5		5		ns	4.5	Fig.9

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74HC/HCT563

AC WAVEFORMS
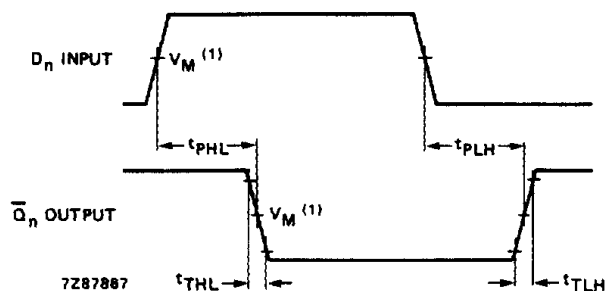
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
   HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6   Waveforms showing the data input (D_n) to
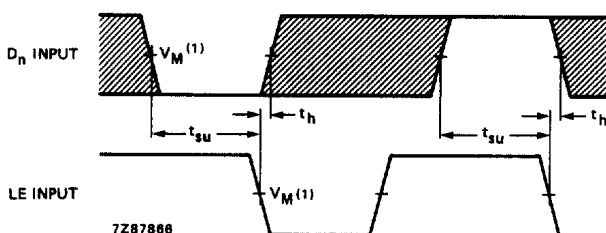output ($\overline{Q}_n$) propagation delays and the
output transition times.
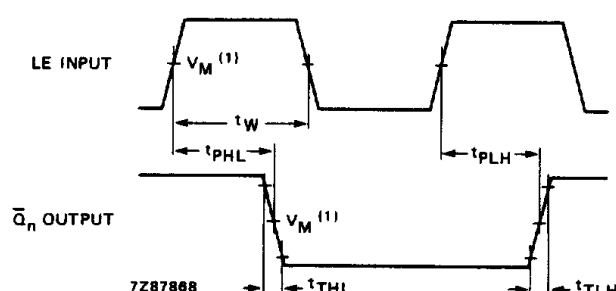
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
   HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7   Waveforms showing the latch enable input
(LE) pulse width, the latch enable input to
output ($\overline{Q}_n$) propagation delays and the
output transition times.
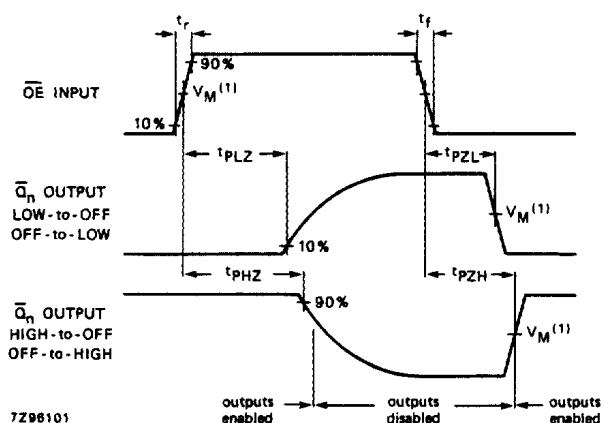
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
   HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8   Waveforms showing the 3-state enable and
disable times.

The shaded areas indicate when the input is permitted to
change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
   HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9   Waveforms showing the data set-up and
hold times for D_n input to LE input

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

74HC/HCT563 Packaging Information

Type Number	Orderable Part Number	Package Name
74HC563D	74HC563D,653	SO20
74HC563D	74HC563D,652	SO20
74HC563N	74HC563N,652	DIP20
74HCT563D	74HCT563D,652	SO20
74HCT563D	74HCT563D,653	SO20
74HCT563DB	74HCT563DB,118	SSOP20
74HCT563DB	74HCT563DB,112	SSOP20
74HCT563N	74HCT563N,652	DIP20