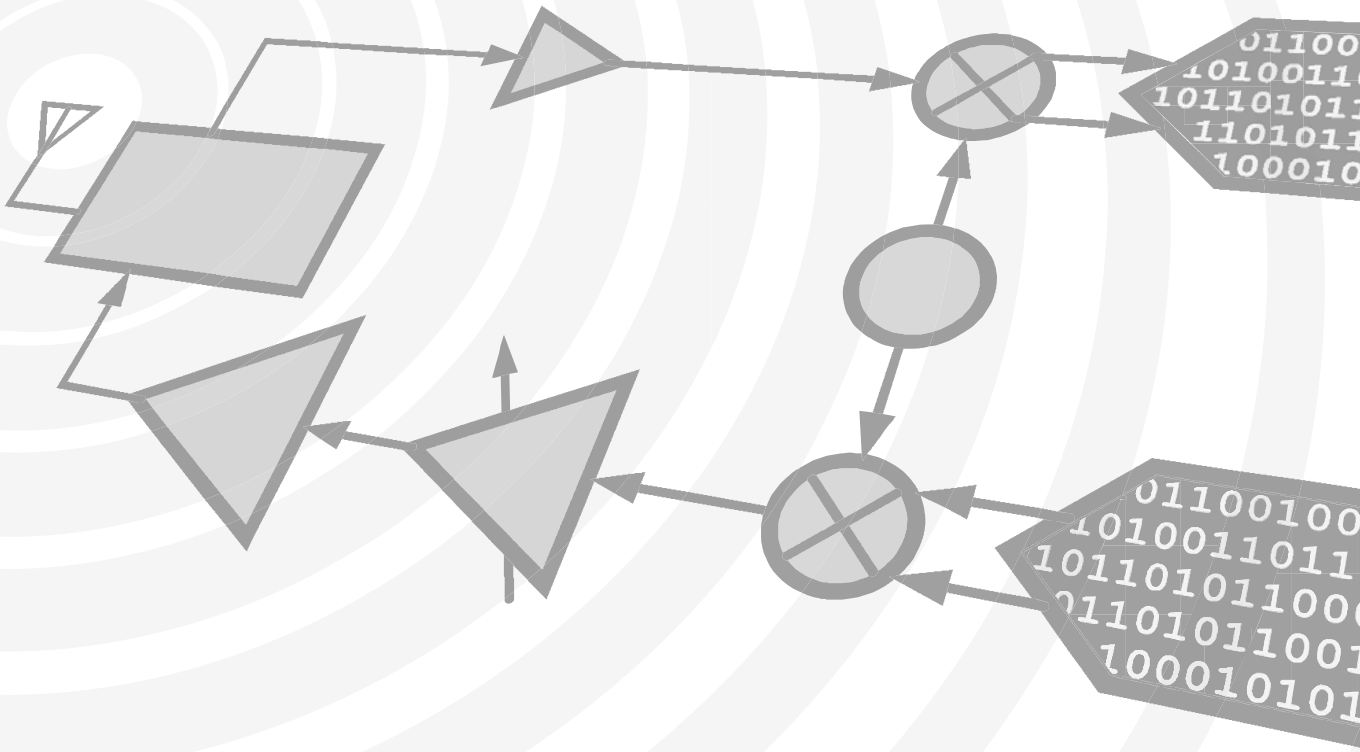
ANALOG DEVICES

Hittite MICROWAVE PRODUCTS FROM ANALOG DEVICES

Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



www.analog.com

www.hittite.com

THIS PAGE INTENTIONALLY LEFT BLANK

HMC856LC5

28 Gbps 5-BIT DIGITAL TIME DELAY WITH PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC856LC5 is ideal for:

- SONET OC-192
- High Speed Serial Logic
- Clock & Data Recovery
- Broadband Test & Measurement Equipment
- Frequency Synthesis
- Matched Timing

Features

Differential & Single-Ended Operation

Supports Data Rates up to 28 Gbps

Fast Rise and Fall Times: 20 / 18 ps

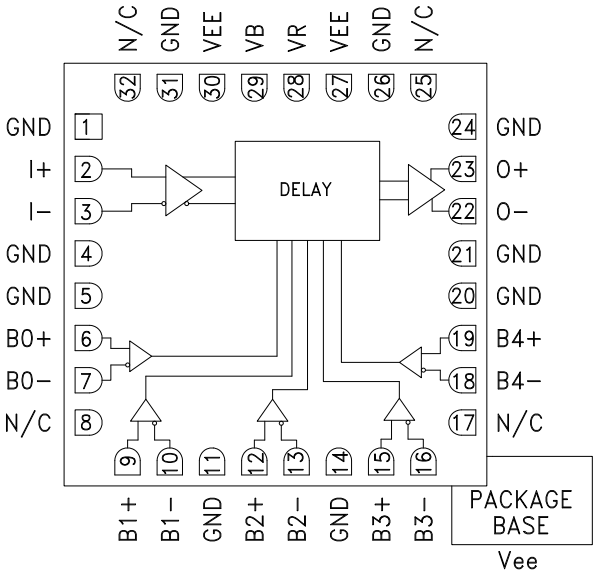
Low Power Consumption: 610 mW typ.

Programmable Differential
Output Voltage Swing: 500 - 1350 mVp-p

Single Supply: -3.3V

32 Lead Ceramic 5x5 mm SMT Package: 25 mm^2

Functional Diagram



General Description

The HMC856LC5 is a wideband time delay with a 5-bit digital control designed for timing compensation or clock skew management applications. The time delay provides nearly 100 ps of delay range with 3 ps resolution and supports 28 Gbps data. The monotonic delay is compensated for stable operation over both power supply and temperature variation.

All differential inputs to the HMC856LC5 are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be AC or DC coupled. The differential CML outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm ground terminated system or drive devices with CML logic input. The control lines B4:B0 ae differential CML inputs terminated with 600 Ohms to the positive rail, which supports lower power control options. The HMC856LC5 features an output level control pin, VR, which allows for loss compenstion or signal level optimization. The HMC856LC5 operates from a single -3.3 V supply and is available in ROHS-compliant 5x5 mm SMT package.

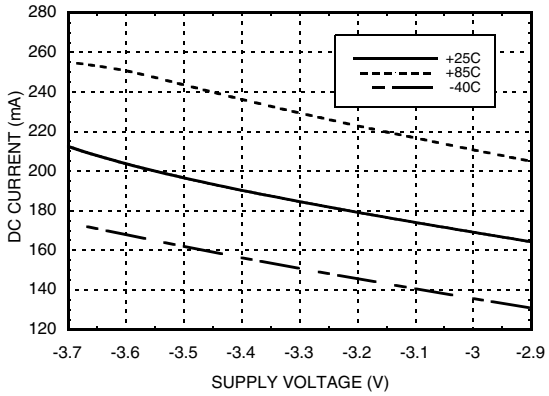
Electrical Specifications, T_A = +25 °C, Vee = -3.3 V, VR = 0 V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.7	-3.3	-2.9	V
Power Supply Current			185		mA
Maximum Data Rate			28		Gbps
Input Voltage Range, CML		-1.5		0.5	V
Input Differential Voltage		0.1		2.0	V
Output Rise / Fall Time	Differential, 20% - 80%		20 / 18		ps
Random Jitter Jr	rms		0.2		ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		<2		ps, p-p
Input Return Loss	Frequency <12 GHz		10		dB

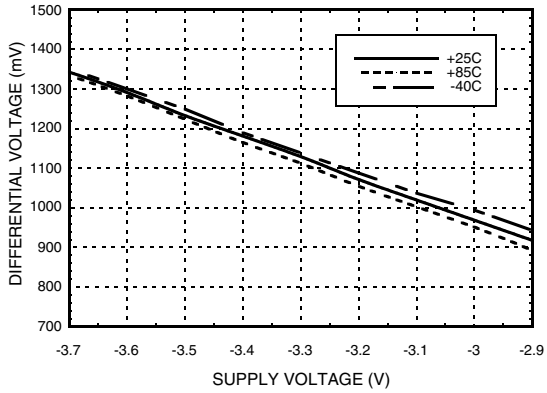
Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Output Amplitude	Single-Ended, peak-to-peak		565		mVp-p
	Differential, peak-to-peak		1130		mVp-p
Output High Voltage			-20		mV
Output Low Voltage			-585		mV
Output Return Loss	Frequency <12 GHz		10		dB
VR Pin Current	VR = 0.0 V		3.0		mA
VR Pin Current	VR = 0.4 V			4.25	mA
Propagation Delay Data to Data, Tprop			255		ps
Delay Control Range			92		ps
Delay Temperature Variation	Ta = 85 °C	9		12	ps
Delay Temperature Variation	Ta = -40 °C	4		8	ps
Delay Resolution			3		ps

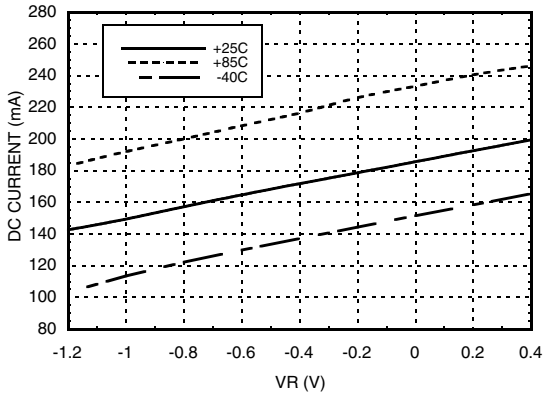
DC Current vs. Supply Voltage [1][2]



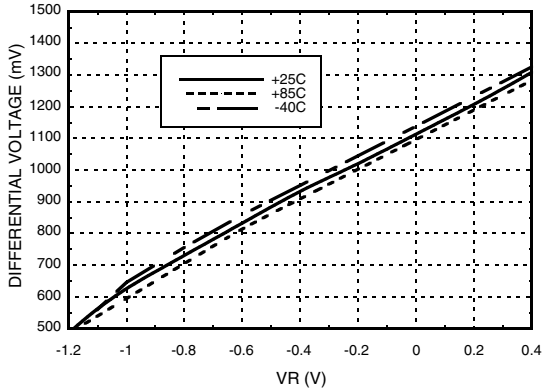
Output Differential Voltage vs. Supply Voltage [1][2]



DC Current vs. VR [2][3]



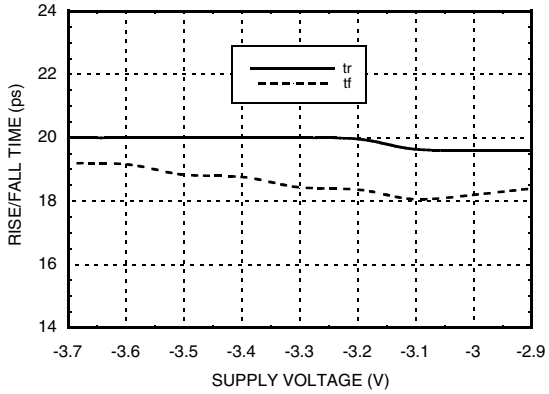
Output Differential Voltage vs. VR [2][3]



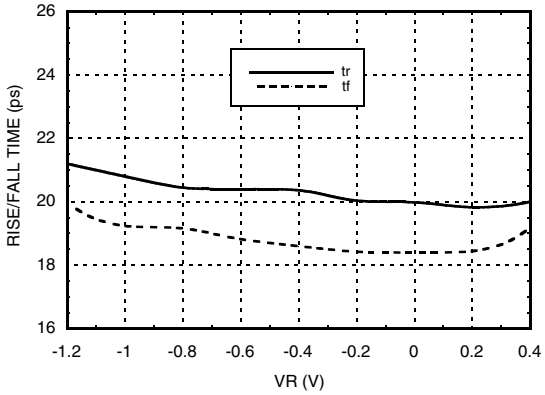
[1] VR = 0.0 V [2] Frequency = 28 Gbps [3] Vee = -3.3 V

28 Gbps 5-BIT DIGITAL TIME DELAY WITH PROGRAMMABLE OUTPUT VOLTAGE

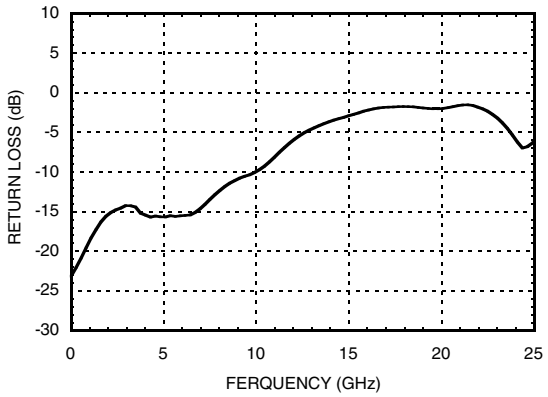
Rise / Fall Time vs. Supply Voltage [1][2]



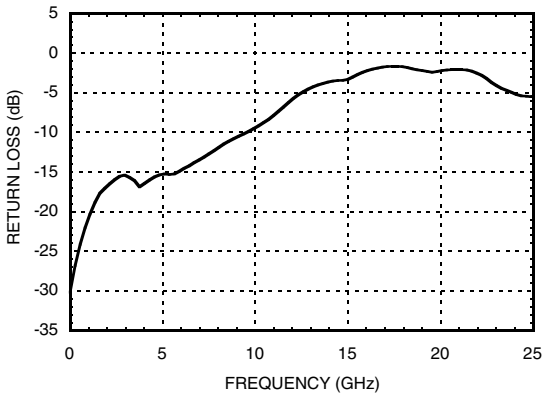
Rise / Fall Time vs. VR [2][4]



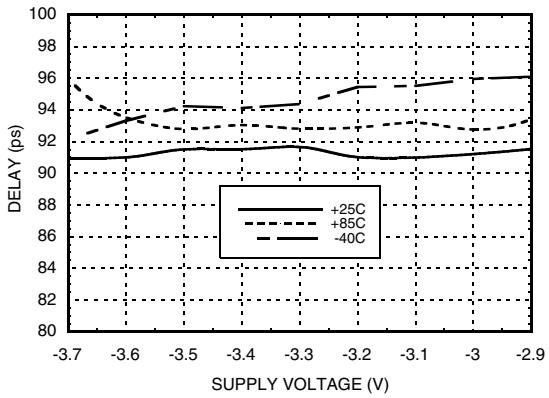
Input Return Loss vs. Frequency [1][3][4]



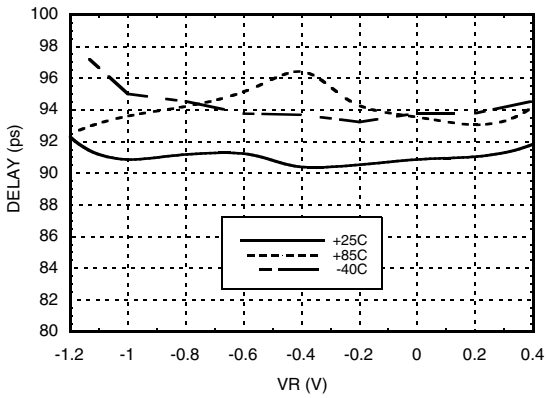
Output Return Loss vs. Frequency [1][3][4]



Delay vs. Supply Voltage [1][2]

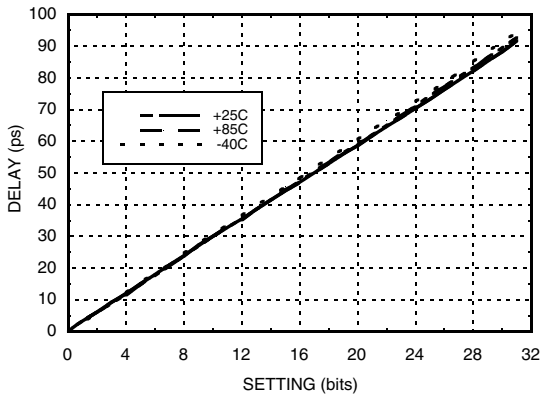


Delay vs. VR [2][4]

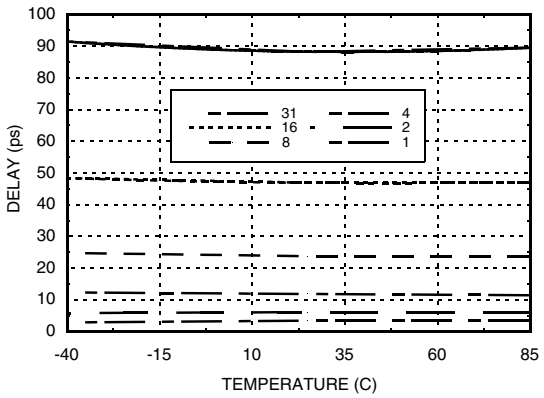


[1] VR = 0.0 V [2] Frequency = 28 Gbps [3] Device measured on evaluation board with port extensions [4] Vee = -3.3 V

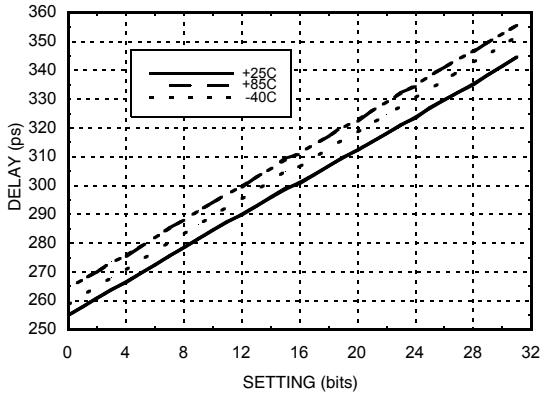
Normalized Delay vs. Setting [1][3][4][5]



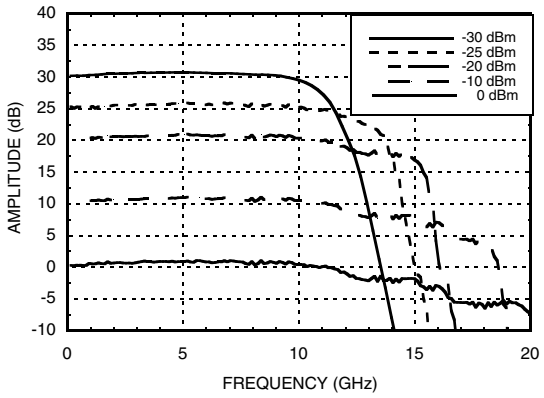
Delay vs. Setting Over Temperature [1][3][4]



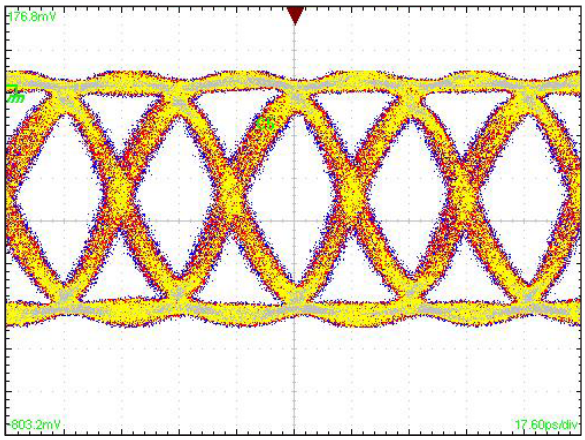
Absolute Delay vs. Setting [1][2][4][5]



Amplitude vs. Input Power [1][3][4]



Eye Diagram @ 28 Gbps

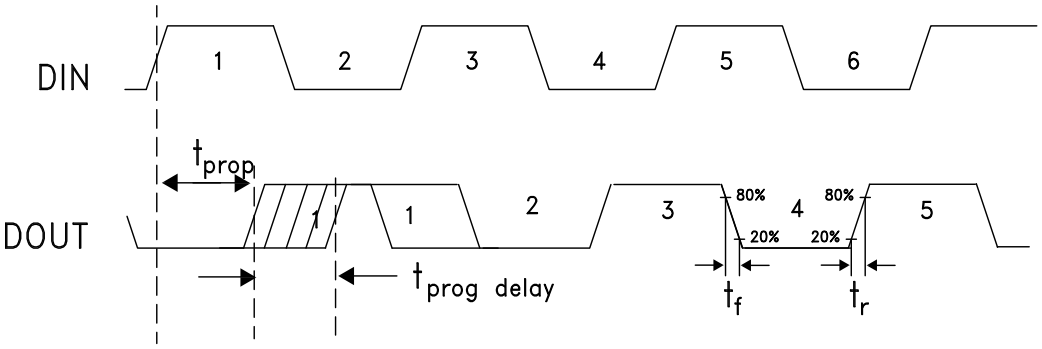


Test Conditions:

Differential 400 mV data input generated with a 2^{15} - 1 PN 28 Gbps PRBS pattern, resulting in a 28 Gbps output measured using a Tektronix CSA 8000

[1] VR = 0 V [2] Frequency = 28 Gbps [3] Device measured on evaluation board with port extensions [4] Vee = -3.3 V
[5] Normalized to 0 setting at its respective temperature

Timing Diagram

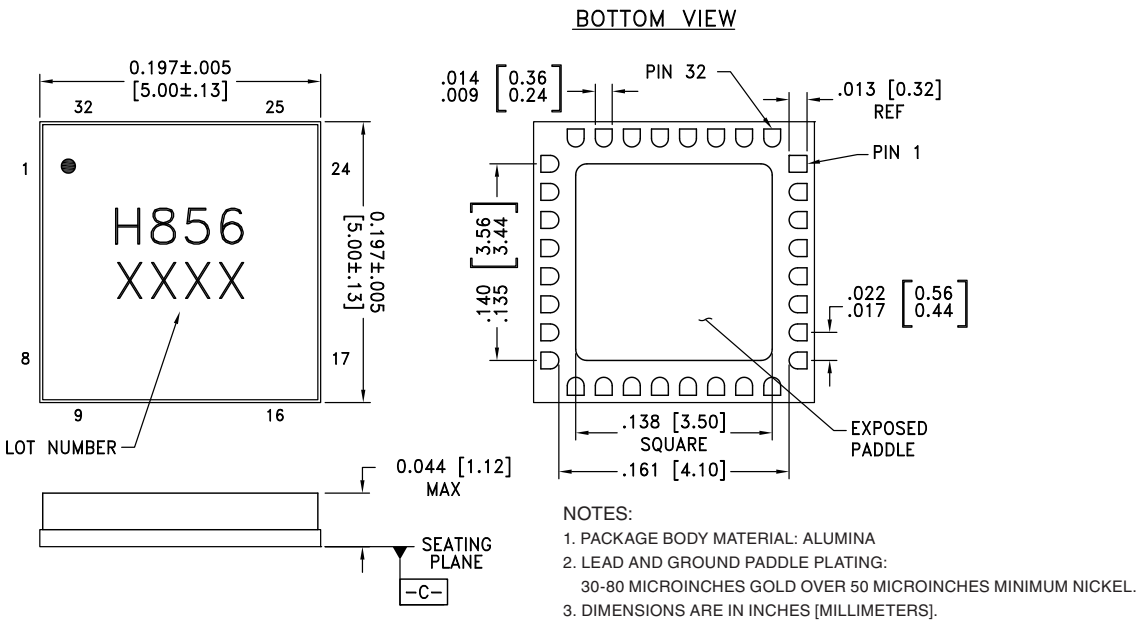


Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to 0.5 V
Maximum Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 33 mW/°C above 85 °C)	1.33 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst-case device to package paddle	30 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

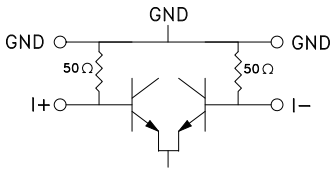
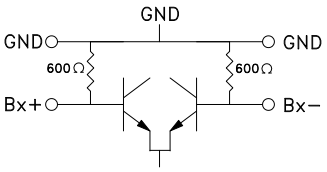
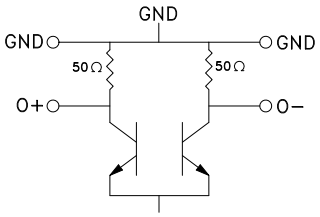
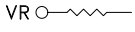
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

Package Information

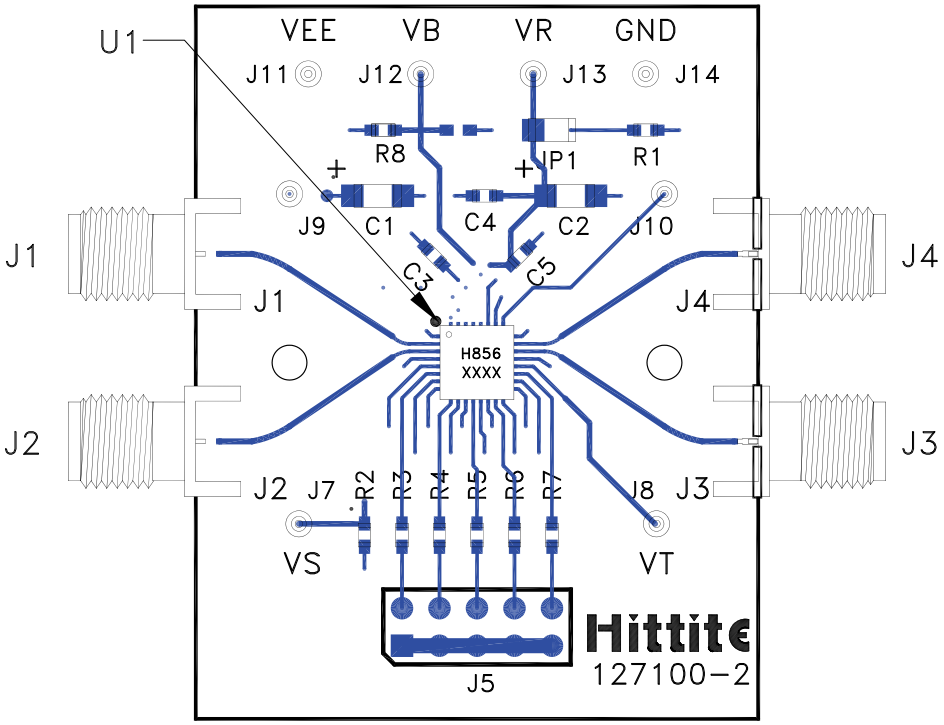
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC856LC5	Alumina, White	Gold over Nickel	MSL3 [1]	H856 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 11, 14, 20, 21, 24	GND	Signal Grounds	
2, 3	I+, I-	Differential Inputs: Current Mode Logic (CML) referenced to positive supply.	
6, 7, 9, 10, 12, 13, 15, 16, 18, 19	B0+, B0-, B1+, B1-, B2+, B2-, B3+, B3-, B4-, B4+	Differential Inputs: Current Mode Logic (CML) referenced to positive supply.	
8, 17, 25, 32	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
22, 23	O-, O+	Differential Outputs: Current Mode Logic (CML) referenced to positive supply, 600 Ohm termination.	
26, 31	GND	Supply Ground	
27, 30, Package Base	Vee	These pins and the exposed paddle must be connected to the negative voltage supply.	
28	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per “Output Differential vs. VR” plot.	
29	VB	VB Tie to ground.	

Evaluation PCB



List of Materials for Evaluation PCB 127102 [1]

Item	Description
J1, J2	PCB Mount SMA RF Connectors
J3, J4	PCN Mount K RF Connectors
J5	0.1" 2 x 5 Header
J7 - J14	0.04" DC Pin
JP1	0.1" 2 Position Header with Shunt
C1, C2	4.7 µF Capacitor, Case A.
C3 - C5	100 pF Capacitor, 0402 Pkg.
R1, R8	10 Ohm Resistor, 0603 Pkg.
R2	1.2 kOhm Resistor, 0603 Pkg.
R3 - R7	2.7 kOhm Resistor, 0603 Pkg.
U1	HMC856LC5 28 Gbps Digital Time Delay
PCB [2]	127100 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit