ANALOG DEVICES

OVP and EMI Protected, Precision, Low Noise and Bias Current Op Amp

Data Sheet

ADA4177-2

FEATURES

- **Low offset voltage: 60 μV maximum at 25°C (8-lead SOIC)**
- **Low offset voltage drift: 1 μV/°C maximum**
- **Low input bias current: 1 nA maximum at 25°C**
- **Low voltage noise density: 8 nV/$\sqrt{\text{Hz}}$ typical**
- **Large signal voltage gain (A_{VO}): 100 dB minimum over full supply voltage and operating temperature**
- **Input overvoltage protection to 32 V above and below the supply voltage rail**
- **Integrated EMI filter**
  - **70 dB typical rejection at 1000 MHz**
  - **90 dB typical rejection at 2400 MHz**
- **Rail-to-rail output swing**
- **Low supply current: 500 μA typical per amplifier**
- **Wide bandwidth**
  - **Gain bandwidth product ($A_V = +100$): 3.5 MHz typical**
  - **Unity-gain crossover: 3.5 MHz typical**
  - **−3 dB bandwidth ($A_V = +1$): 6 MHz typical**
- **Dual-supply operation**
  - **Specified at ±5 V to ±15 V**
  - **Operates over ±2.5 V to ±18 V**
- **Unity-gain stable**
- **No phase reversal**

APPLICATIONS

- **Wireless base station control circuits**
- **Optical network control circuits**
- **Instrumentation**
- **Sensors and controls**
  - **Thermocouples, resistor thermal detectors (RTDs), strain gages, shunt current measurements**
- **Precision filters**

GENERAL DESCRIPTION

The ADA4177-2 is a dual-channel amplifier featuring low offset voltage (2 μV typical) and drift (1 μV/°C maximum), and low input bias current, noise, and current consumption (500 μA typical). Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

The ADA4177-2 inputs set a new standard in precision amplifier robustness providing input protection against signal excursions 32 V beyond either supply, as well as 70 dB of rejection for electromagnetic interference (EMI) at 1000 MHz.

PIN CONNECTION DIAGRAM

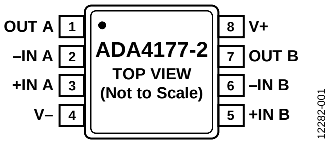

Figure 1.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, and strain gages), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The ADA4177-2 is useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

The ADA4177-2 operates over the −40°C to +125°C industrial temperature range. The ADA4177-2 is available in an 8-lead SOIC package and an 8-lead MSOP package.

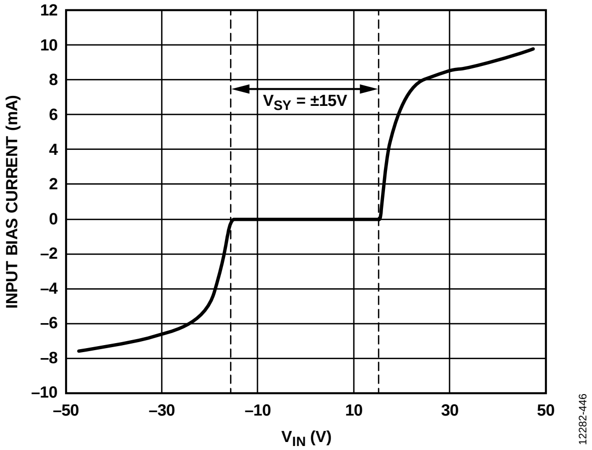

Figure 2. Overvoltage Current Limiting, Voltage Follower Configuration

Table 1. Evolution of Protected Input Op Amps by Generation[1]

Gen. 1, OVP (10 V)	Gen. 2, OVP (25 V)	Gen. 3, OVP (32 V)	Gen. 4 EMI Filters	Gen. 5, OVP (32 V) + EMI
OP291	ADA4091-2	ADA4096-2	AD8657	ADA4177-2
OP491	ADA4091-4	ADA4096-4	AD8659	
	ADA4092-4		AD8546	
			AD8548	
			ADA4661-2	
			ADA4666-2	

[1] Gen. stands for Generation.

Rev. A

Document Feedback

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REVISION HISTORY

10/14—Rev. 0 to Rev. A

Changes to Large Signal Voltage Gain Parameter, Test Conditions/Comments Column, Table 3 ... 5

10/14—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5 V

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
8-Lead SOIC				2	60	µV
		−40°C < T_A < +125°C			120	µV
8-Lead MSOP				2.2	120	µV
		−40°C < T_A < +125°C			200	µV
Offset Voltage Drift (8-Lead SOIC/8-Lead MSOP)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C			1	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−40°C < T_A < +125°C	−2		+2	nA
Input Offset Current	I_{OS}		−0.75	0.1	+0.75	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Voltage Range	IVR		−3.5		+3.5	V
Overvoltage Current Limit[1]	I_{OVP}	5 V < V_{CM} < 37 V		12		mA
		−37 V < V_{CM} < −5 V		10		mA
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.5 V to +3.5 V	122	130		dB
		−40°C < T_A < +125°C	120			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −4.5 V to +4.5 V	108	110		dB
		−40°C < T_A < +125°C	100			dB
		R_L = 10 kΩ, V_{OUT} = −4.5 V to +4.5 V	115	120		dB
		−40°C < T_A < +125°C	110			dB
Input Capacitance	C_{INDM}	Differential mode		1		pF
	C_{INCM}	Common mode		1		pF
Input Resistance	R_{DIFF}	Differential mode		4		MΩ
	R_{CM}	Common mode		100		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{LOAD} = 1 mA	4.95			V
		−40°C < T_A < +125°C	4.90			V
		I_{LOAD} = 7 mA	4.80			V
		−40°C < T_A < +125°C	4.75			V
Output Voltage Low	V_{OL}	I_{LOAD} = 1 mA			−4.95	V
		−40°C < T_A < +125°C			−4.90	V
		I_{LOAD} = 7 mA			−4.80	V
		−40°C < T_A < +125°C			−4.75	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		25		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		70		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.11		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	125	145		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V		500	560	µA
		−40°C < T_A < +125°C			600	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.5		V/μs
Settling Time	t_S					
To 0.1%		V_{IN} = 1 V step, R_L = 2 kΩ, A_V = −1		1.8		μs
To 0.01%		V_{IN} = 1 V step, R_L = 2 kΩ, A_V = −1		3.5		μs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		6		MHz
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, R_L = 2 kΩ, A_V = +1, f = 1 kHz		0.003		%
EMI Rejection of +IN x	EMIRR	V_{IN} = 200 mV p-p				
f = 1000 MHz				70		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		175		nV p-p
Voltage Noise Density	e_n	f = 10 Hz		10		nV/√Hz
		f = 1 kHz		8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		200		pA/√Hz

[1] All inputs are stressed to 32 V beyond supplies for 500 ms. See Figure 64 for the typical input bias current vs. the input voltage over the overvoltage protected input range.

ELECTRICAL CHARACTERISTICS, ±15 V

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
8-Lead SOIC				2	60	µV
		$-40°C < T_A < +125°C$			120	µV
8-Lead MSOP				2.2	120	µV
		$-40°C < T_A < +125°C$			200	µV
Offset Voltage Drift (8-Lead SOIC/8-Lead MSOP)	$\Delta V_{OS}/\Delta T$	$-40°C < T_A < +125°C$			1	µV/°C
Input Bias Current	I_B		−1	−0.3	+1	nA
		$-40°C < T_A < +125°C$	−2		+2	nA
Input Offset Current	I_{OS}		−0.75	0.1	+0.75	nA
		$-40°C < T_A < +125°C$	−1.5		+1.5	nA
Input Voltage Range	IVR		−13.5		+13.5	V
Overvoltage Current Limit[1]	I_{OVP}	$15\text{ V} < V_{CM} < 47\text{ V}$		12		mA
		$-47\text{ V} < V_{CM} < -15\text{ V}$		10		mA
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.5 V to +13.5 V	128	130		dB
		$-40°C < T_A < +125°C$	125			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −14.2 V to +14.2 V	110	114		dB
		$-40°C < T_A < +125°C$	105			dB
		R_L = 10 kΩ, V_{OUT} = −14.5 V to +14.5 V	118	120		dB
		$-40°C < T_A < +125°C$	110			dB
Input Capacitance	C_{INDM}	Differential mode		1		pF
	C_{INCM}	Common mode		1		pF
Input Resistance	R_{DIFF}	Differential mode		4		MΩ
	R_{CM}	Common mode		130		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{LOAD} = 1 mA	14.95			V
		$-40°C < T_A < +125°C$	14.90			V
		I_{LOAD} = 7 mA	14.80			V
		$-40°C < T_A < +125°C$	14.75			V
Output Voltage Low	V_{OL}	I_{LOAD} = 1 mA			−14.95	V
		$-40°C < T_A < +125°C$			−14.90	V
		I_{LOAD} = 7 mA			−14.80	V
		$-40°C < T_A < +125°C$			−14.75	V
Output Current	I_{OUT}	$V_{DROPOUT} < 1\text{ V}$		25		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		70		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.08		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	125	145		dB
		$-40°C < T_A < +125°C$	120			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V		500	580	µA
		$-40°C < T_A < +125°C$			620	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.5		V/µs
Settling Time	t_S					
To 0.01%		V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		5.5		µs
To 0.1%		V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		7.5		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\,dB}$	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		6		MHz
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A_V = +1, R_L = 2 kΩ, f = 1 kHz		0.002		%
EMI Rejection of +IN x	EMIRR	V_{IN} = 200 mV p-p				
f = 1000 MHz				70		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		175		nV p-p
Voltage Noise Density	e_n	f = 100 Hz		10		nV/√Hz
		f = 1 kHz		8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		200		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz		127		dB

[1] All inputs are stressed to 32 V beyond supplies for 500 ms. See Figure 67 for the typical input bias current vs. the input voltage over the overvoltage protected input range.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_{SY} ± 32 V
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Refer to the Maximum Power Dissipation section
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)[1]	300°C
ESD	
Human Body Model (HBM)[2]	4 kV
Field Induced Charged Device Model (FICDM)[3]	1250 V
Machine Model (MM)	200 V

[1] IPC/JEDEC J-STS-020D applicable standard.
[2] ESDA/JEDEC JS-001-2011 applicable standard.
[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The ADA4177-2 is capable of driving a short-circuit output current up to 70 mA. However, the usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the ADA4177-2 is 150°C (see Table 4). The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A$$

where:
T_J is the die junction temperature.
P_D is the power dissipated in the package.
θ_{JA} is the thermal resistance of the package.
T_A is the ambient temperature.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated by the output stage transistor. It is calculated as follows:

$$P_D = (V_{SY} \times I_{SY}) + (V_{SY} - V_{OUT}) \times I_{LOAD}$$

where:
V_{SY} is the power supply rail.
I_{SY} is the quiescent current.
V_{OUT} is the output of the amplifier.
I_{LOAD} is the output load.

Do not exceed the 150°C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device. Refer to Technical Article MS-2251, *Data Sheet Intricacies—Absolute Maximum Ratings and Thermal Resistances*, for more information.

THERMAL RESISTANCE

Thermal resistance between junction and ambient (θ_{JA}) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

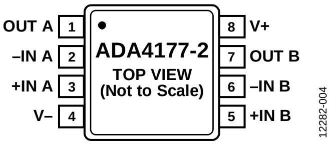


Figure 3. 8-Lead MSOP Pin Configuration

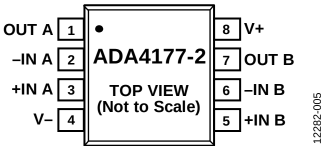


Figure 4. 8-Lead SOIC Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A
2	–IN A	Inverting Input Channel A
3	+IN A	Noninverting Input Channel A
4	V–	Negative Supply Voltage
5	+IN B	Noninverting Input Channel B
6	–IN B	Inverting Input Channel B
7	OUT B	Output Channel B
8	V+	Positive Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

Ambient temperature (T_A) = 25°C unless otherwise noted.

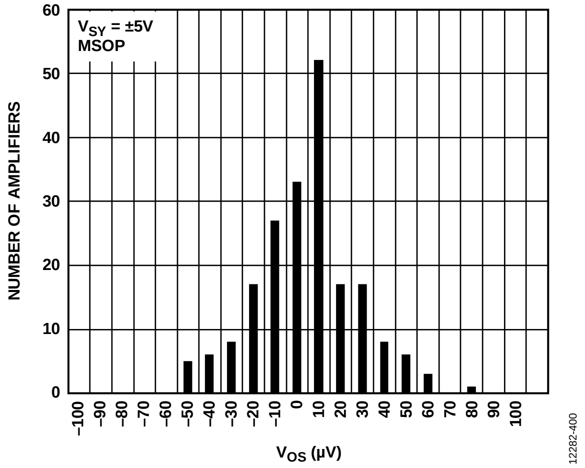


Figure 5. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V, 8-Lead MSOP

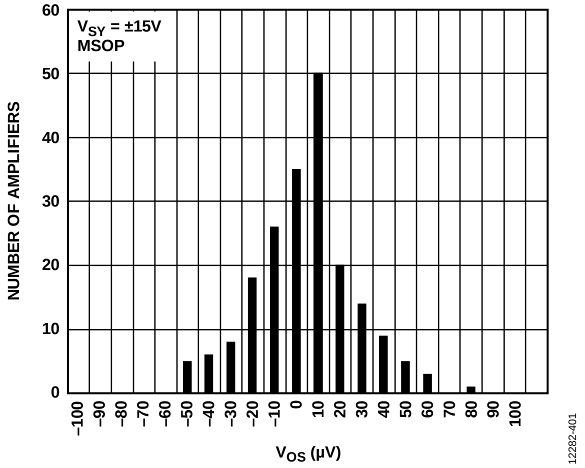


Figure 8. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V, 8-Lead MSOP

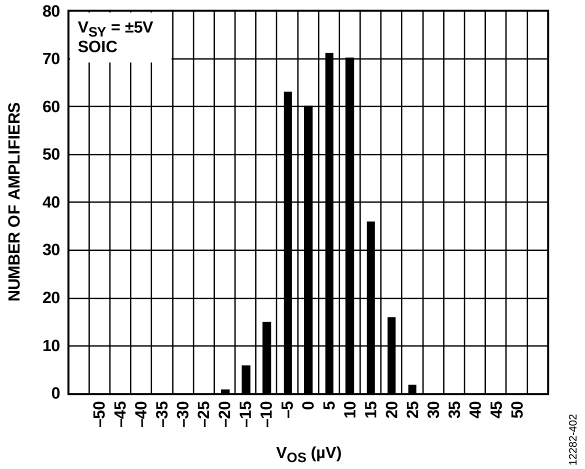


Figure 6. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V, 8-Lead SOIC

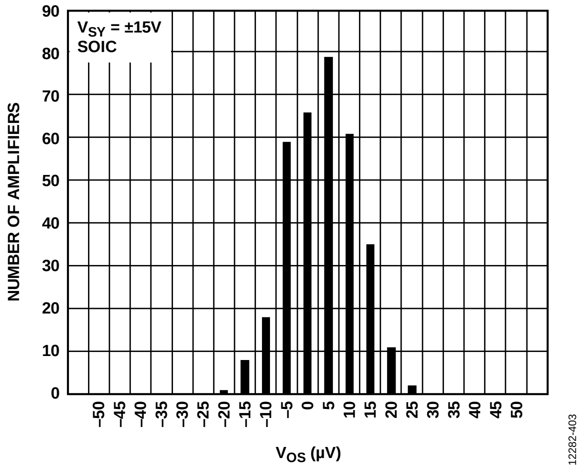


Figure 9. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V, 8-Lead SOIC

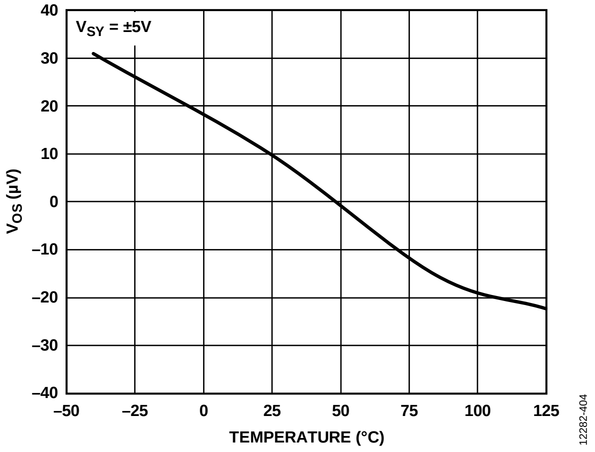


Figure 7. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±5 V

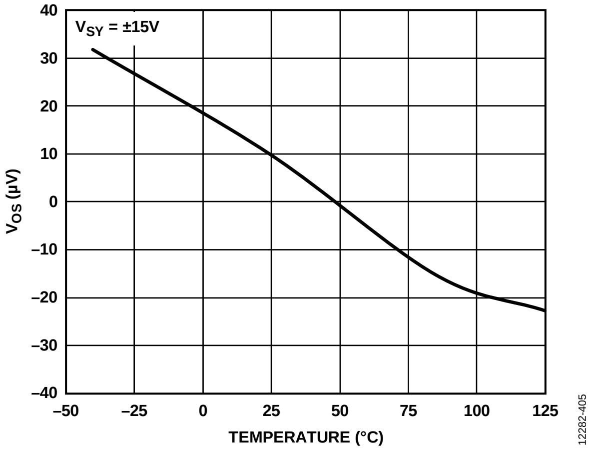


Figure 10. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±15 V

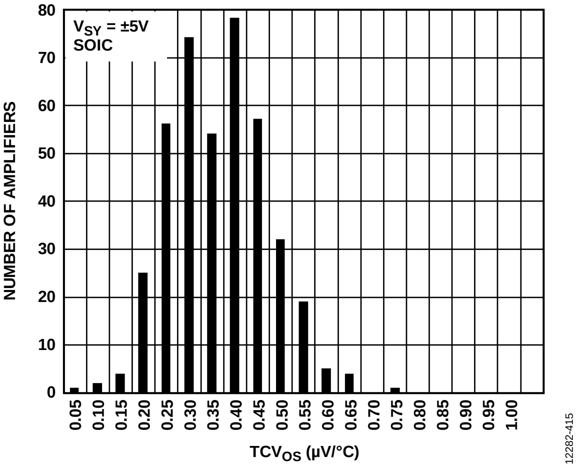


Figure 11. Temperature Coefficient of Offset Voltage (TCV$_{OS}$), V$_{SY}$ = ±5 V, 8-Lead SOIC

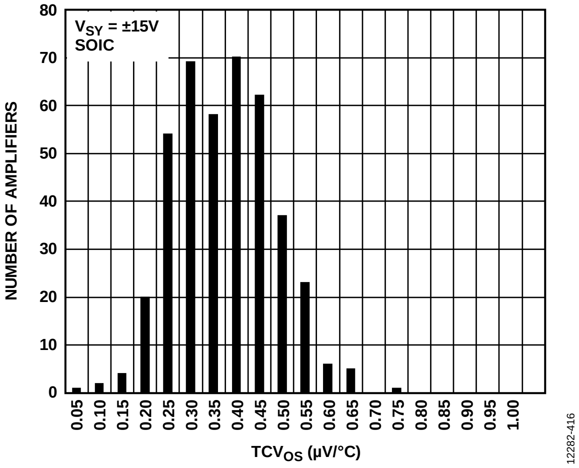


Figure 14. Temperature Coefficient of Offset Voltage (TCV$_{OS}$), V$_{SY}$ = ±15 V, 8-Lead SOIC

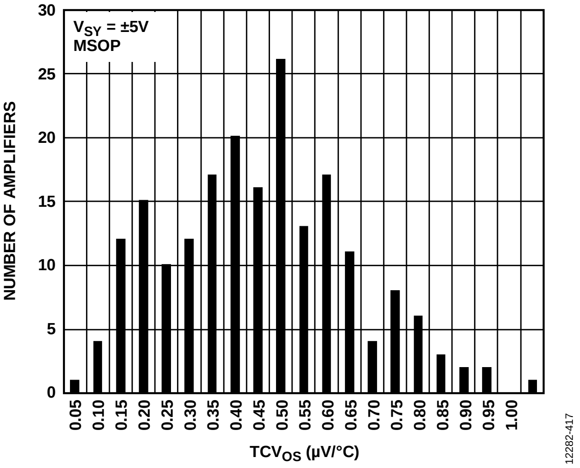


Figure 12. Temperature Coefficient of Offset Voltage (TCV$_{OS}$), V$_{SY}$ = ±5 V, 8-Lead MSOP

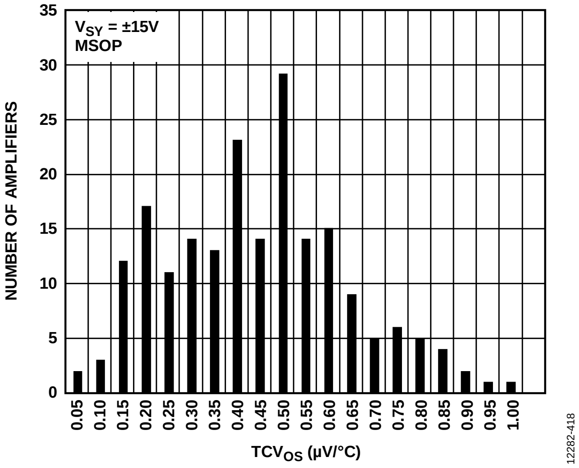


Figure 15. Temperature Coefficient of Offset Voltage (TCV$_{OS}$), V$_{SY}$ = ±15 V, 8-Lead MSOP

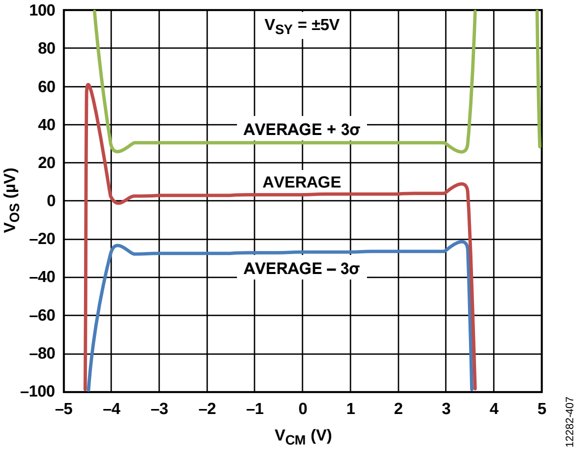


Figure 13. Offset Voltage (V$_{OS}$) vs. Common-Mode Voltage (V$_{CM}$), V$_{SY}$ = ±5 V

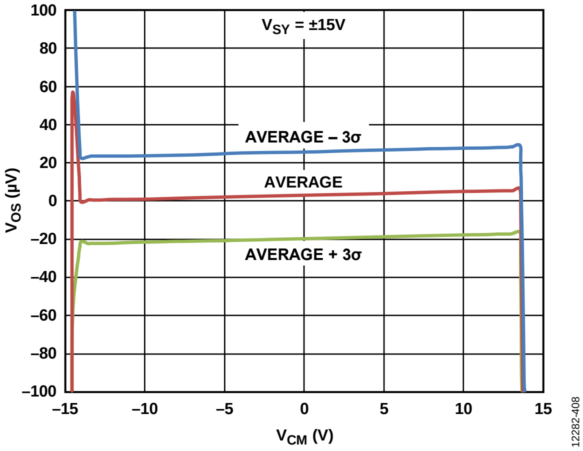


Figure 16. Offset Voltage (V$_{OS}$) vs. Common-Mode Voltage (V$_{CM}$), V$_{SY}$ = ±15 V

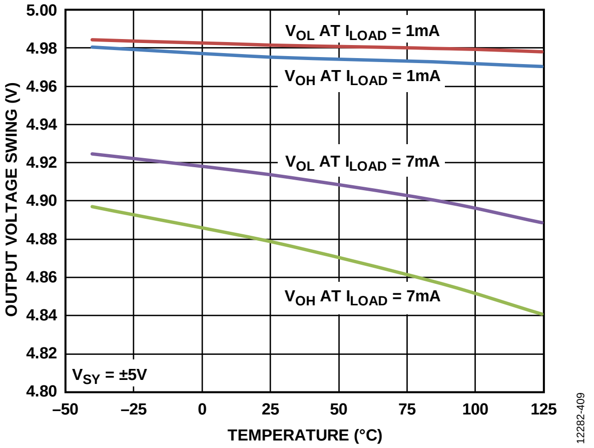


Figure 17. Output Voltage Swing vs. Temperature, V_{SY} = ±5 V

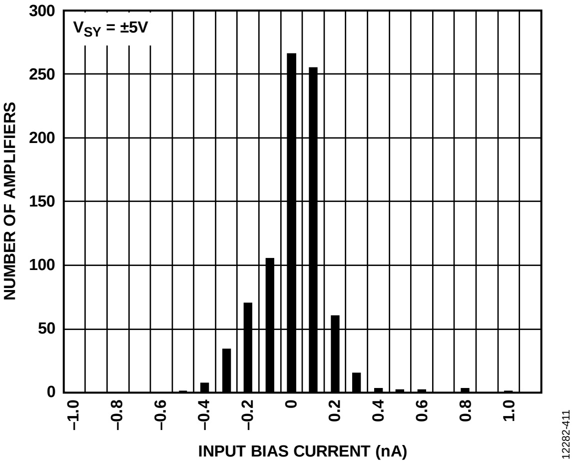


Figure 18. Input Bias Current Distribution, V_{SY} = ±5 V

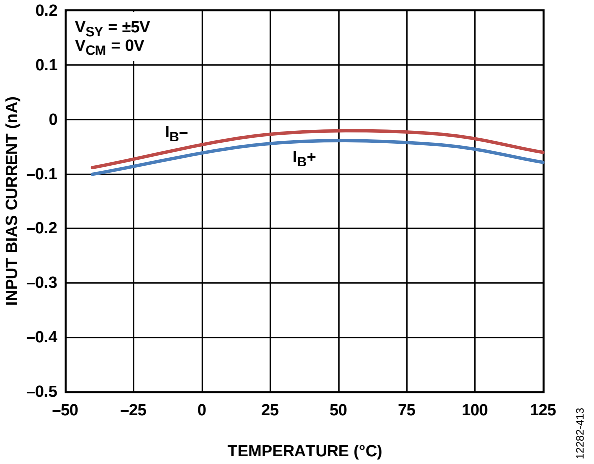


Figure 19. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±5 V

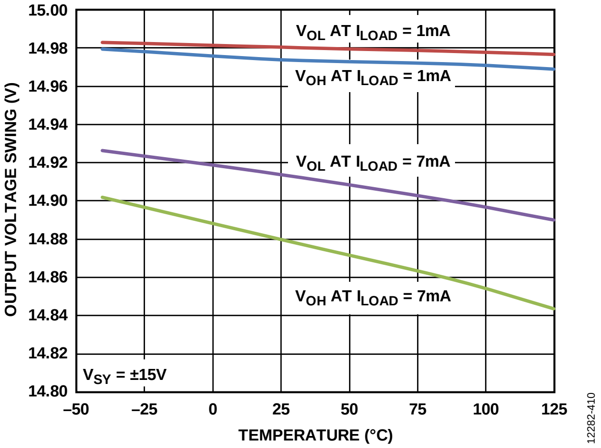


Figure 20. Output Voltage Swing vs. Temperature, V_{SY} = ±15 V

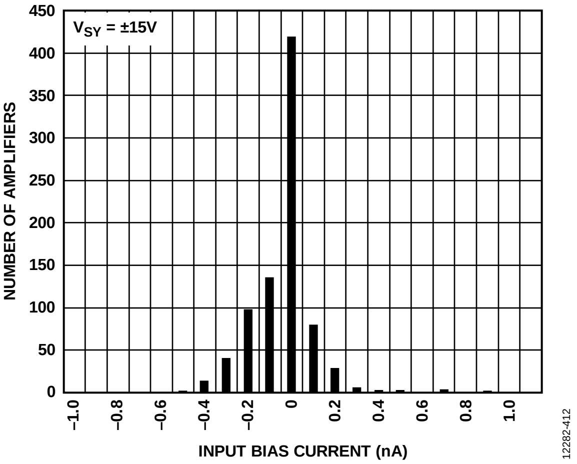


Figure 21. Input Bias Current Distribution, V_{SY} = ±15 V

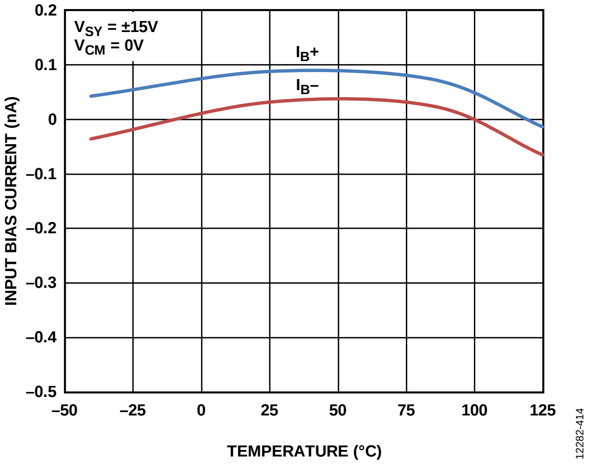


Figure 22. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±15 V

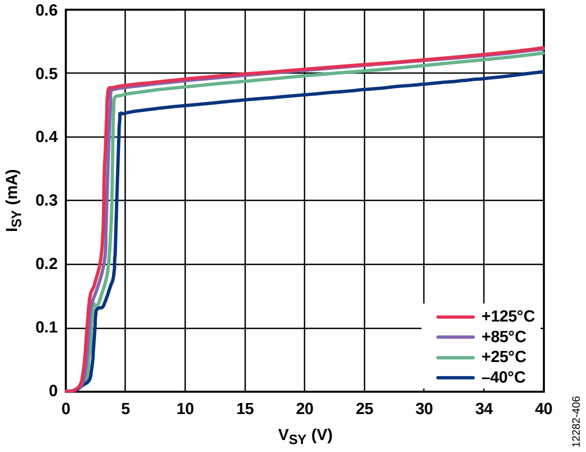


Figure 23. Supply Current per Amplifier (I_{SY}) vs. Power Supply Voltage (V_{SY})

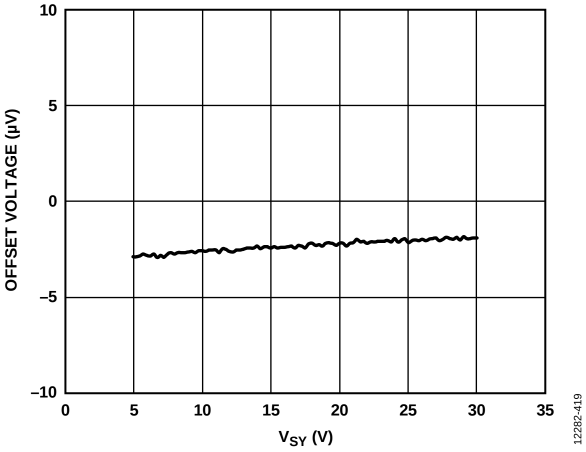


Figure 26. Offset Voltage (V_{OS}) vs. Power Supply Voltage (V_{SY})

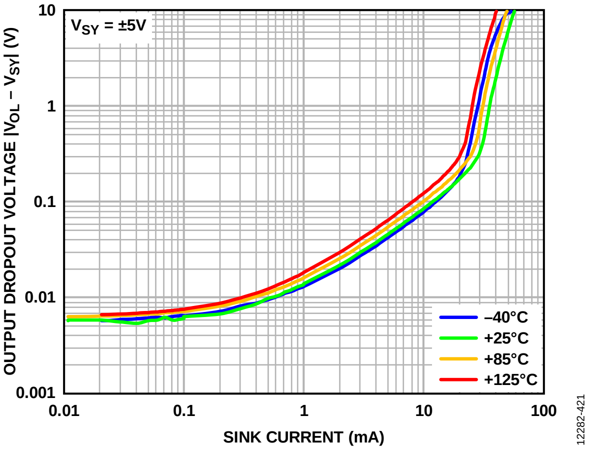


Figure 24. Output Dropout Voltage vs. Sink Current, V_{SY} = ±5 V

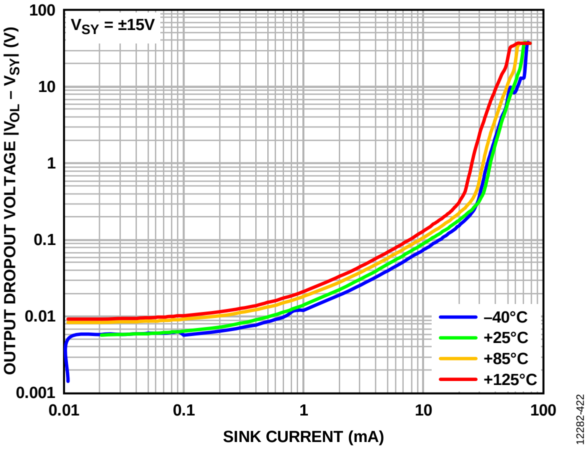


Figure 27. Output Dropout Voltage vs. Sink Current, V_{SY} = ±15 V

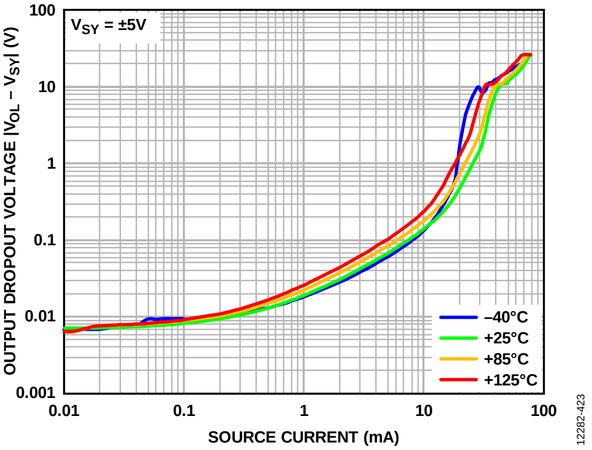


Figure 25. Output Dropout Voltage vs. Source Current, V_{SY} = ±5 V

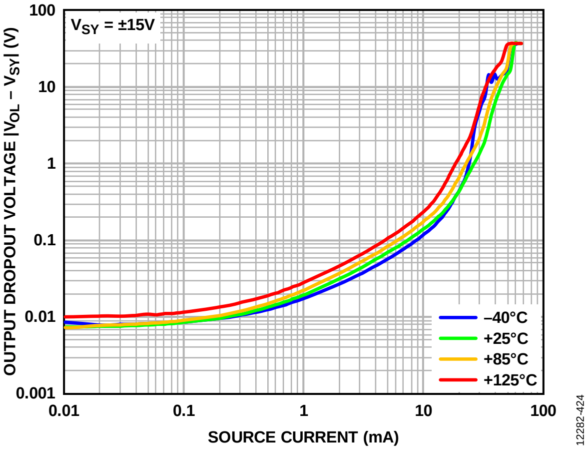


Figure 28. Output Dropout Voltage vs. Source Current, V_{SY} = ±15 V

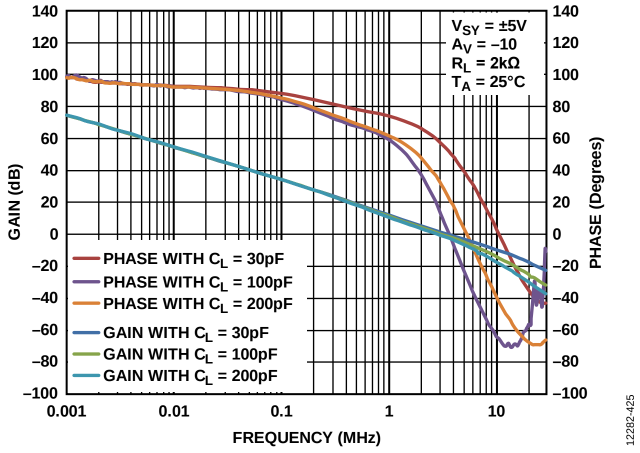


Figure 29. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±5 V

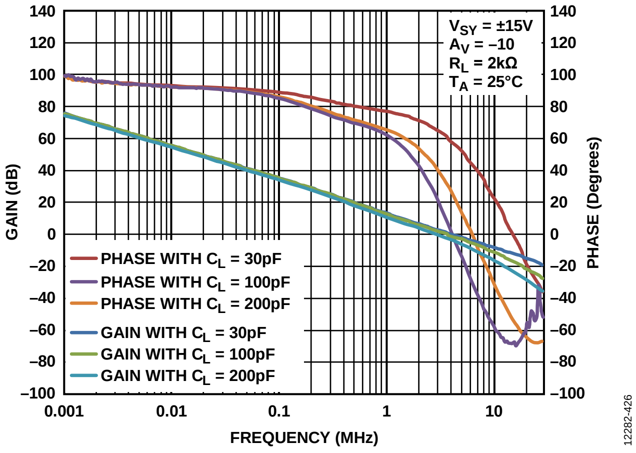


Figure 32. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±15 V

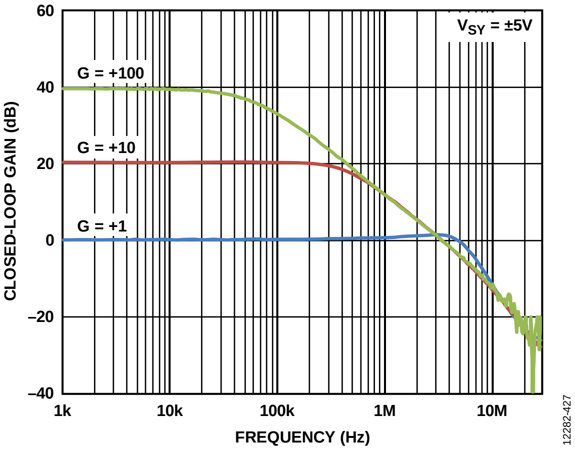


Figure 30. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

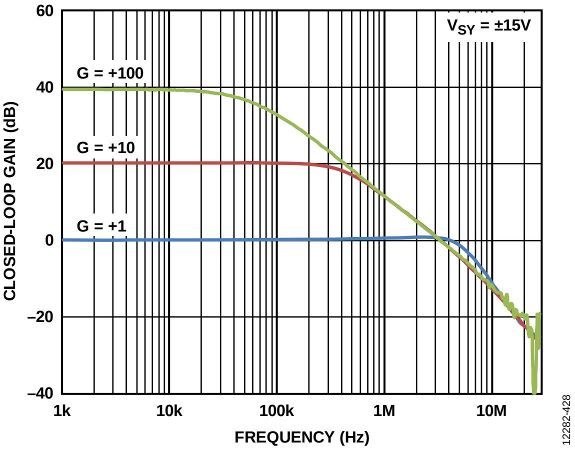


Figure 33. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

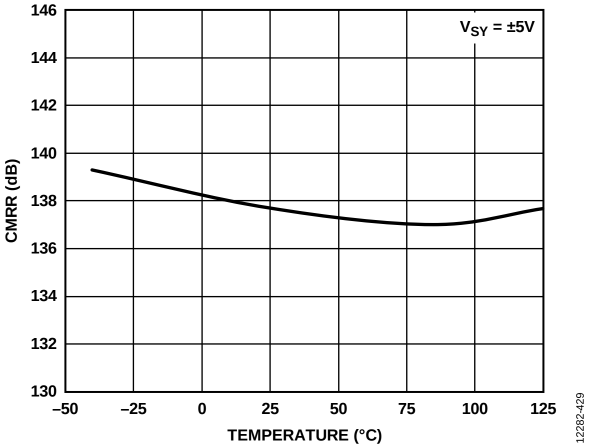


Figure 31. Common-Mode Rejection Ratio (CMRR) vs. Temperature, V_{SY} = ±5 V

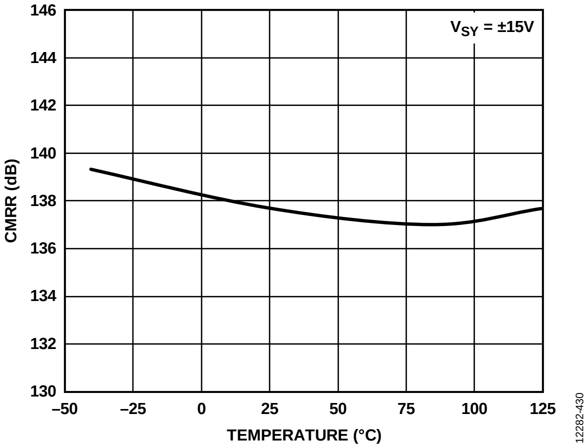


Figure 34. Common-Mode Rejection Ratio (CMRR) vs. Temperature, V_{SY} = ±15 V

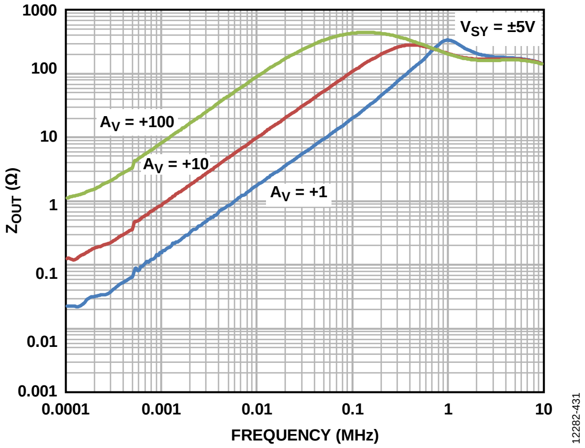


Figure 35. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

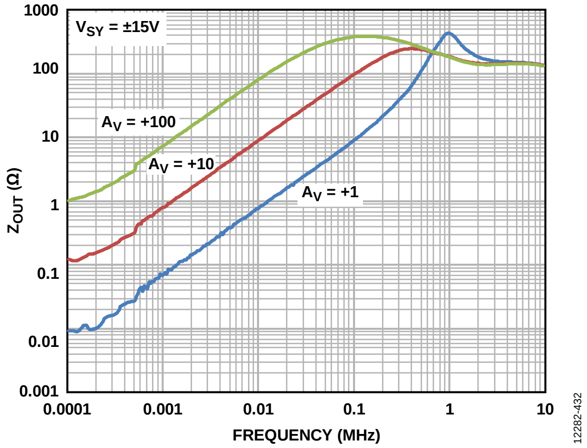


Figure 38. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±15 V

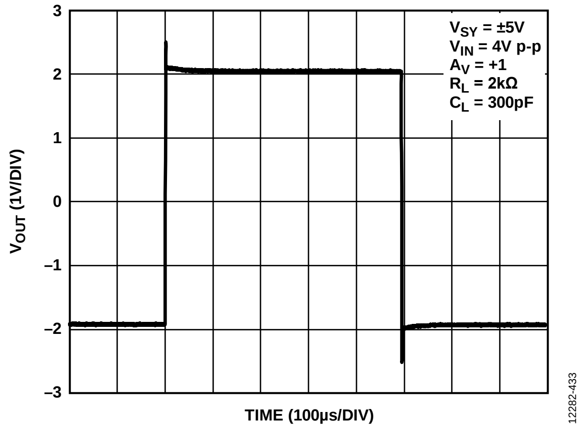


Figure 36. Large Signal Transient Response, V_{SY} = ±5 V

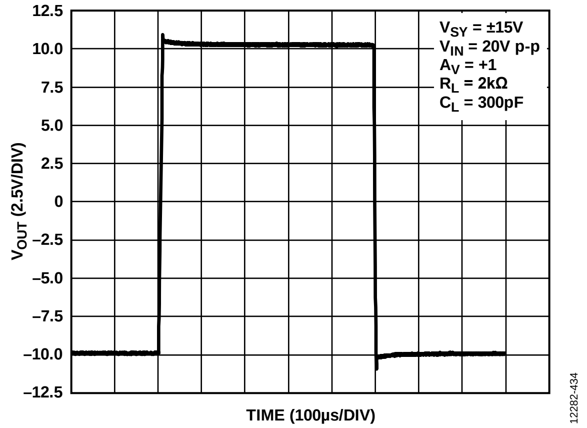


Figure 39. Large Signal Transient Response, V_{SY} = ±15 V

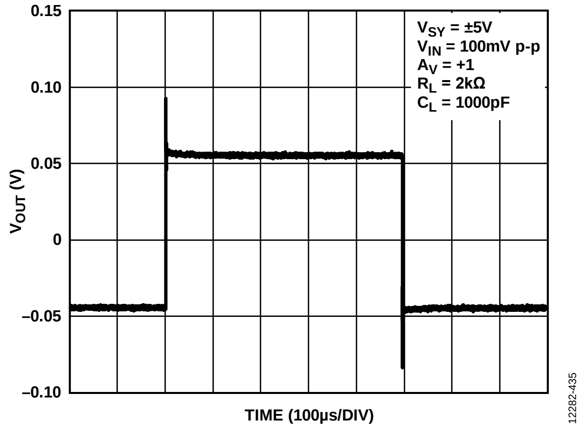


Figure 37. Small Signal Transient Response, V_{SY} = ±5 V

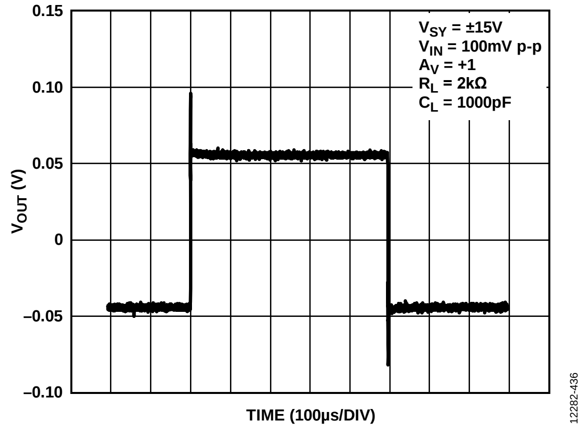


Figure 40. Small Signal Transient Response, V_{SY} = ±15 V

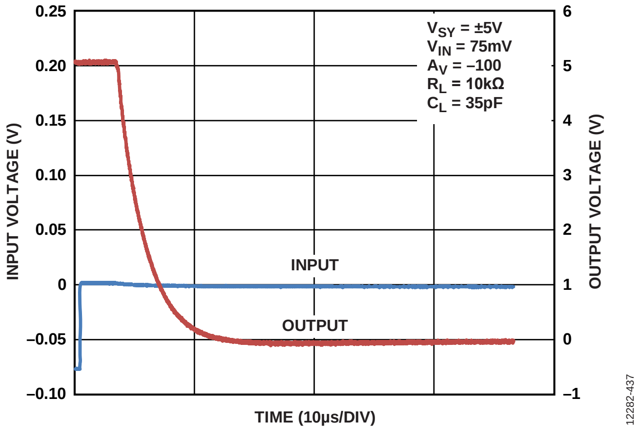


Figure 41. Positive Overload Recovery, V_{SY} = ±5 V

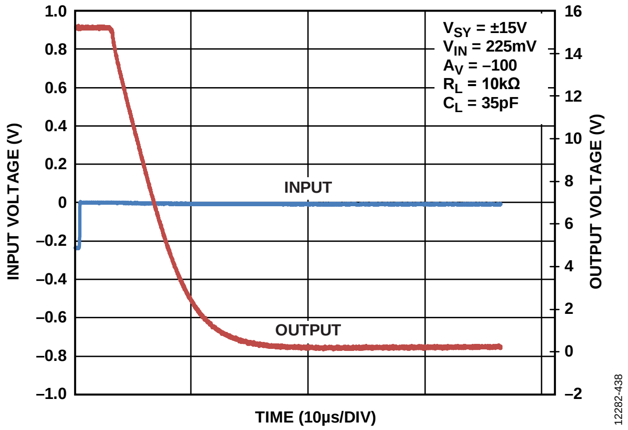


Figure 44. Positive Overload Recovery, V_{SY} = ±15 V

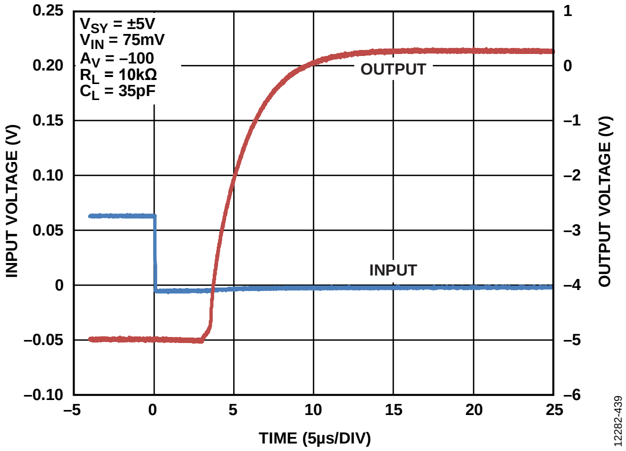


Figure 42. Negative Overload Recovery, V_{SY} = ±5 V

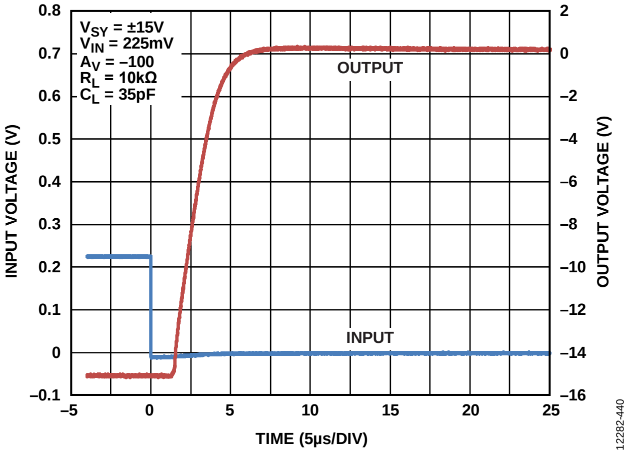


Figure 45. Negative Overload Recovery, V_{SY} = ±15 V

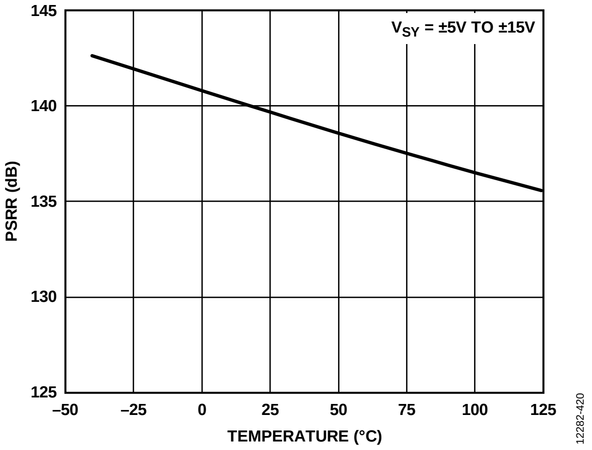


Figure 43. Power Supply Rejection Ratio (PSRR) vs. Temperature, V_{SY} = ±5 V to ±15 V

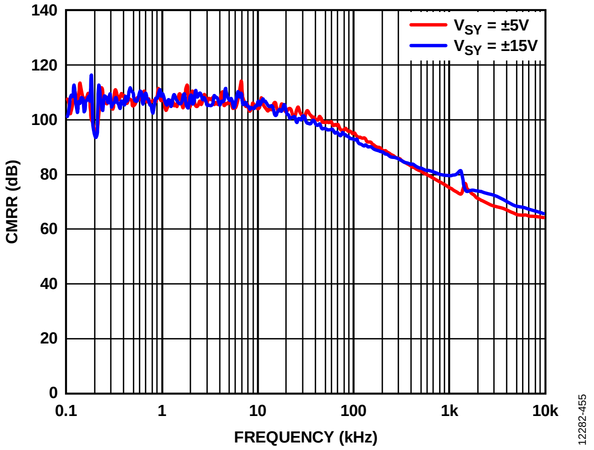


Figure 46. Common-Mode Rejection Ratio (CMRR) vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

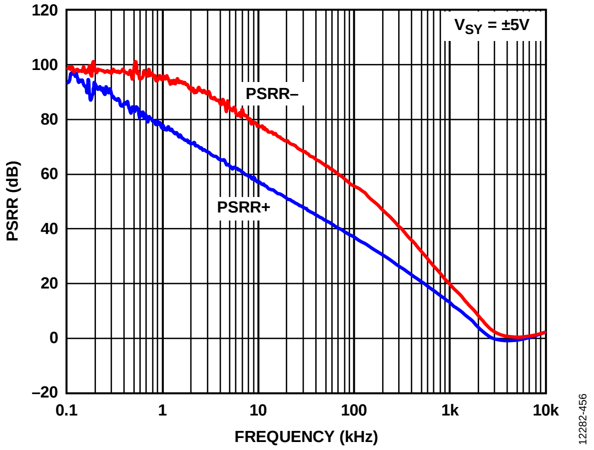


Figure 47. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{SY} = ±5 V

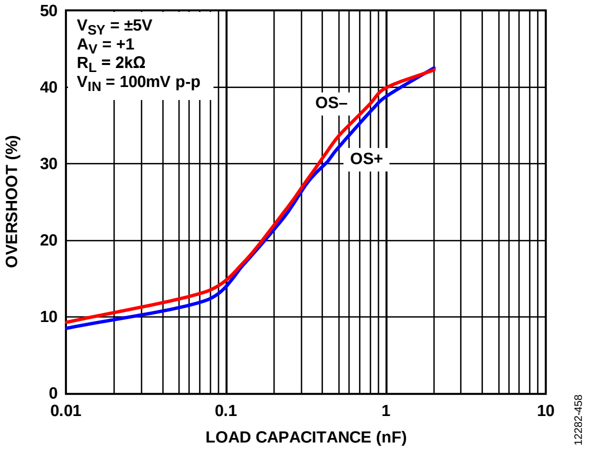


Figure 48. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±5 V

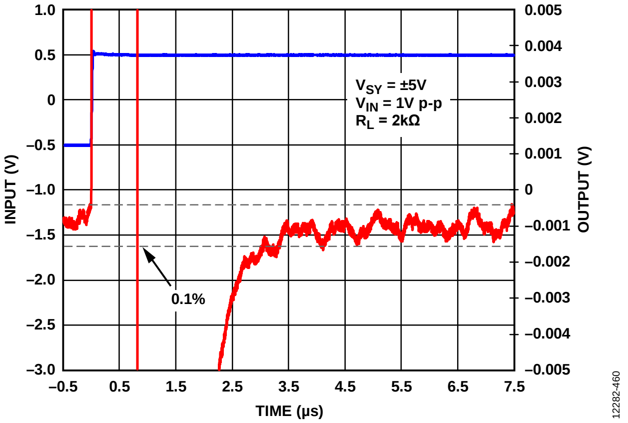


Figure 49. Positive Settling Time to 0.1%, V_{SY} = ±5 V

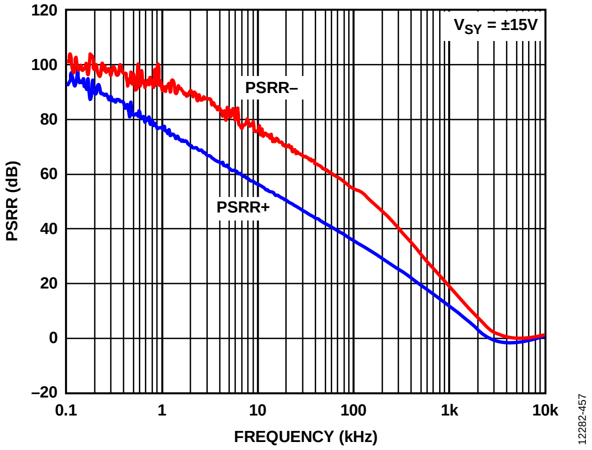


Figure 50. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{SY} = ±15 V

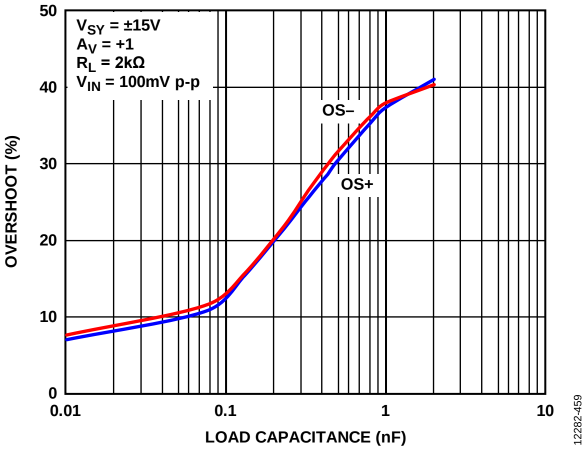


Figure 51. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±15 V

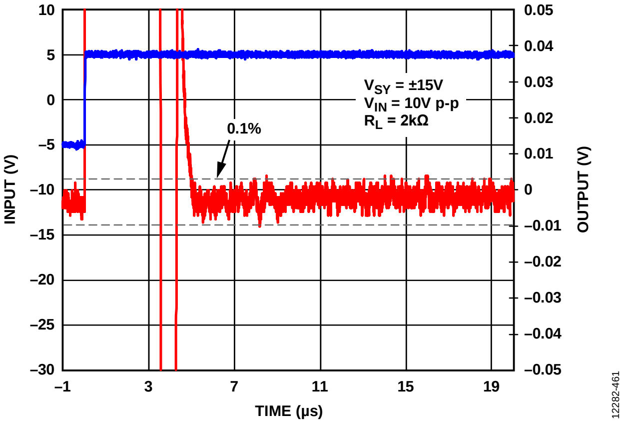


Figure 52. Positive Settling Time to 0.1%, V_{SY} = ±15 V

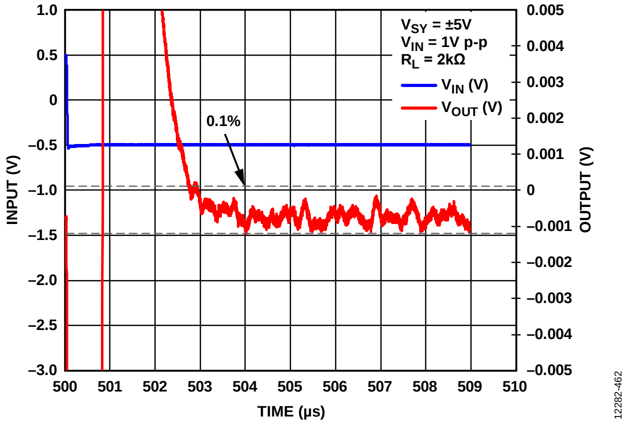


Figure 53. Negative Settling Time to 0.1%, V_{SY} = ±5 V

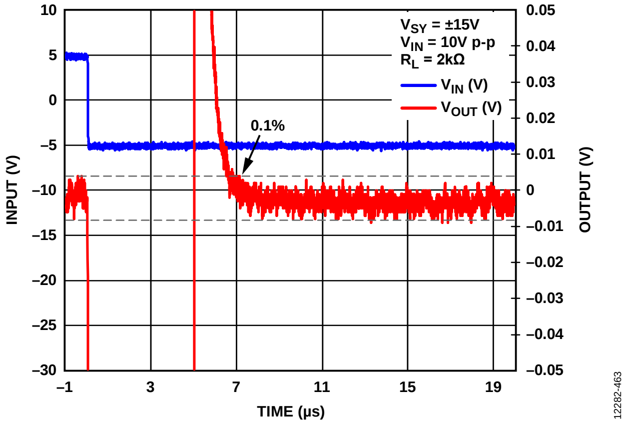


Figure 56. Negative Settling Time 0.1%, V_{SY} = ±15 V

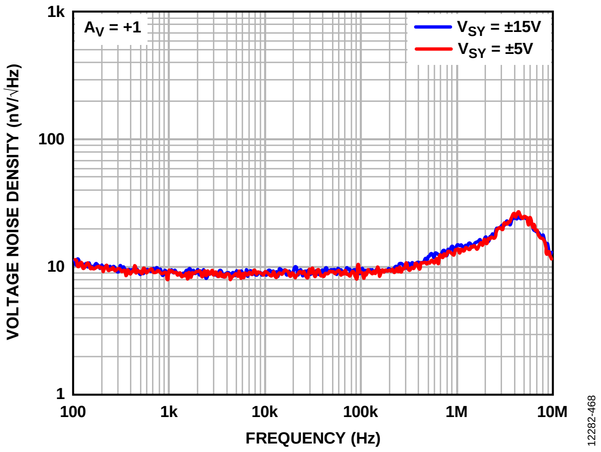


Figure 54. Voltage Noise Density vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

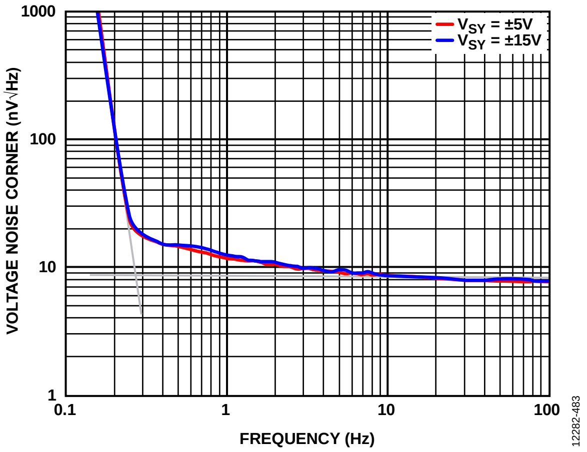


Figure 57. Voltage Noise Corner vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

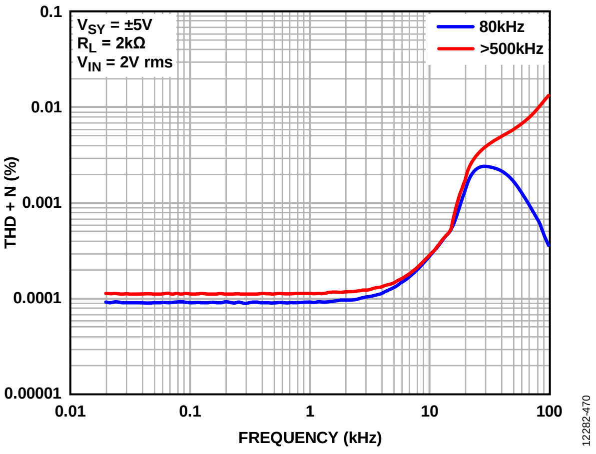


Figure 55. THD + N vs. Frequency, V_{SY} = ±5 V

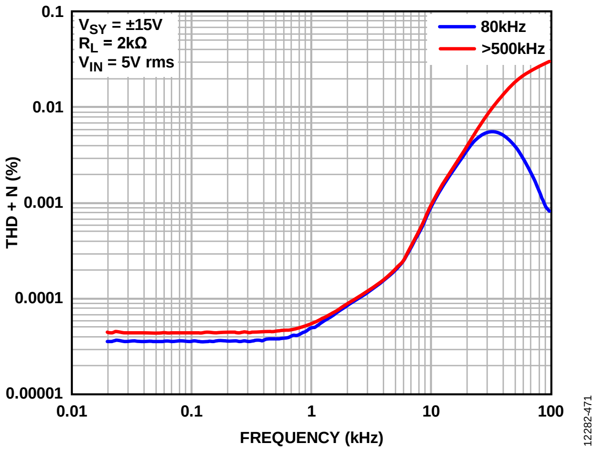


Figure 58. THD + N vs. Frequency, V_{SY} = ±15 V

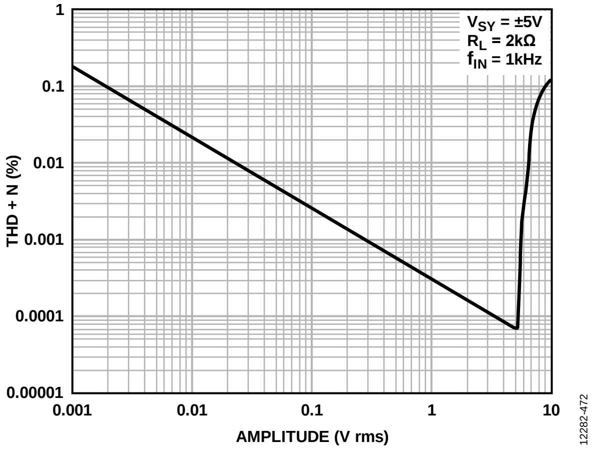


Figure 59. THD + N vs. Amplitude, V_{SY} = ±5 V

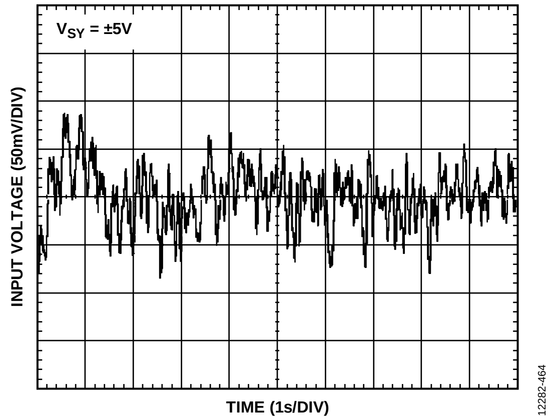


Figure 60. 0.1 Hz to 10 Hz Noise, V_{SY} = ±5 V

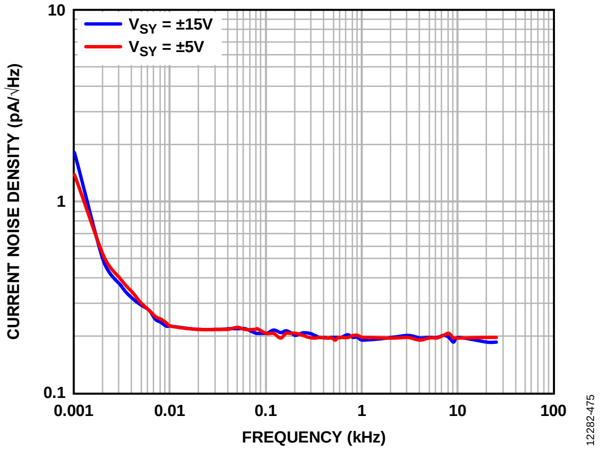


Figure 61. Current Noise Density vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

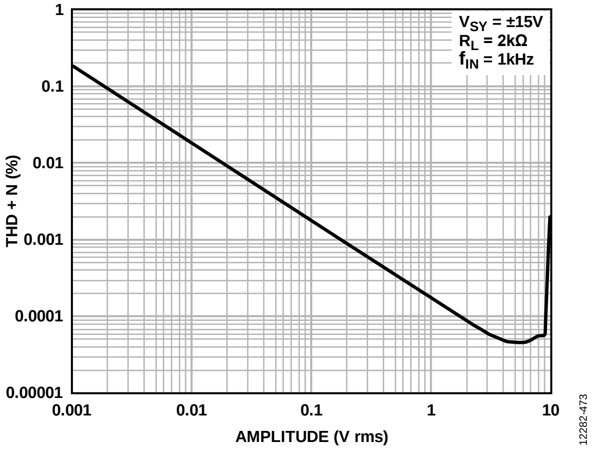


Figure 62. THD + N vs. Amplitude, V_{SY} = ±15 V

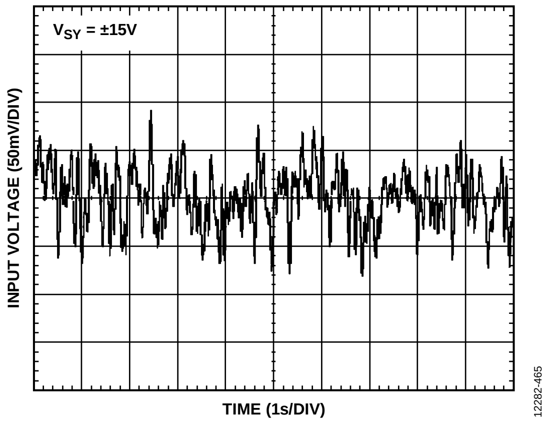


Figure 63. 0.1 Hz to 10 Hz Noise, V_{SY} = ±15 V

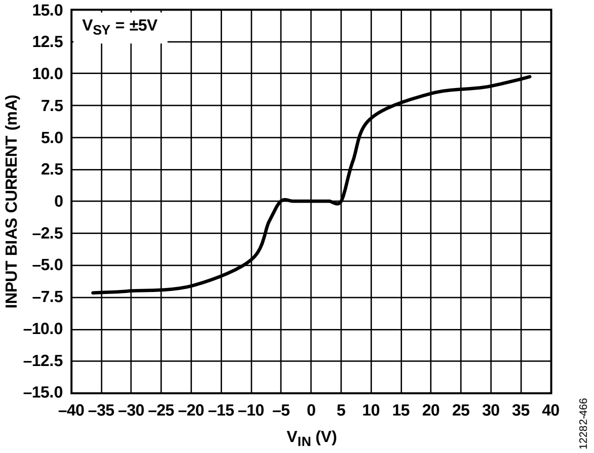


Figure 64. Input Bias Current vs. Input Voltage Including Input Overvoltage Range (Beyond V_{SY} = ±5 V)

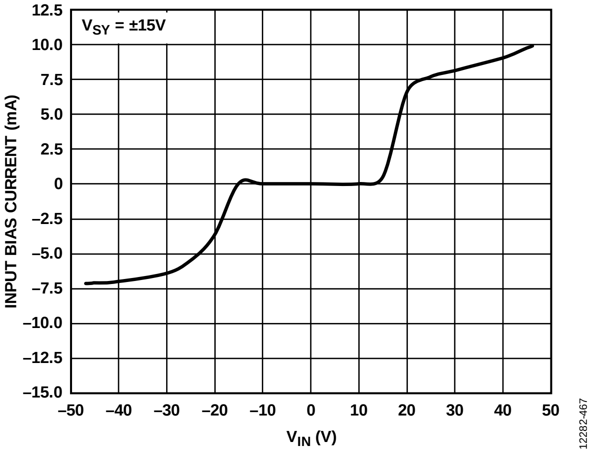


Figure 67. Input Bias Current vs. Input Voltage Including Input Overvoltage Range (Beyond V_{SY} = ±15 V)

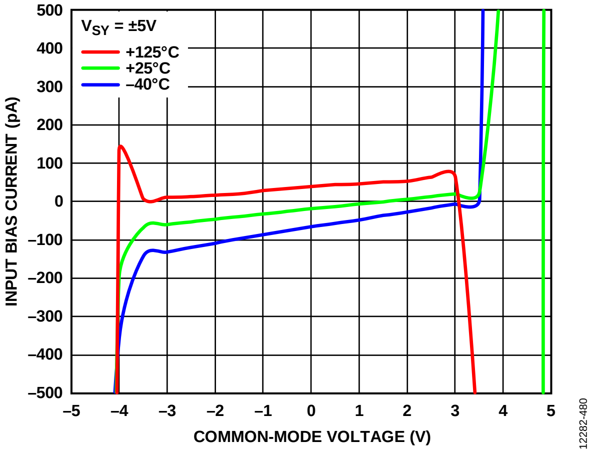


Figure 65. Input Bias Current vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±5 V

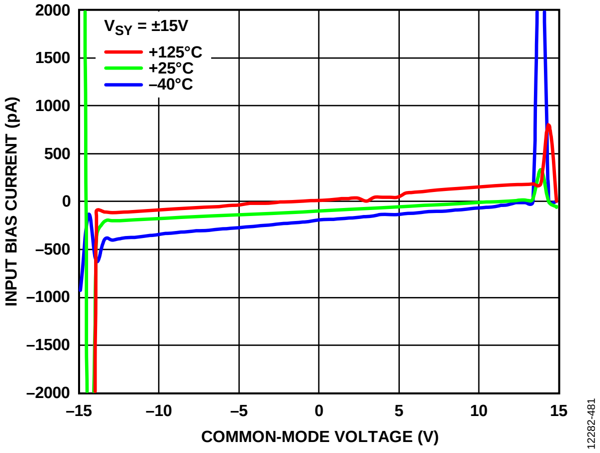


Figure 68. Input Bias Current vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±15 V

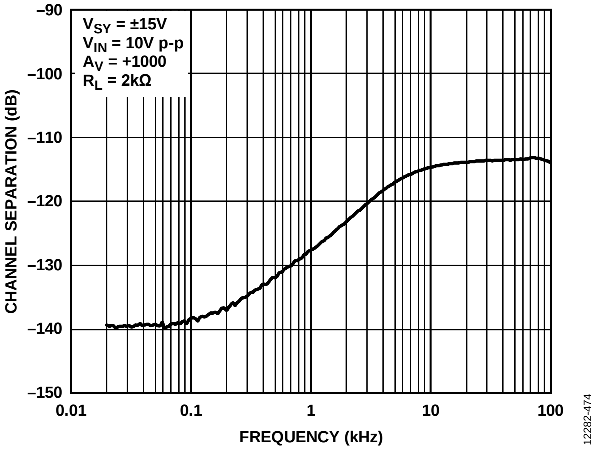


Figure 66. Channel Separation vs. Frequency, V_{SY} = ±15 V

THEORY OF OPERATION

The ADA4177-2 is a precision, bipolar op amp that integrates both input overvoltage protection (OVP) and input EMI filtering while maintaining a low 2 nA maximum bias current and a rail-to-rail output operation. Figure 69 shows a conceptual schematic of the main amplifier that uses super beta, bipolar input transistors and bias current cancellation to minimize the input bias current. The inputs are cascoded to protect the super beta input devices from damage during overvoltage conditions. The cascoded inputs feed into an active load which makes up the primary gain stage. A buffered transconductance (g_m) stage converts a differential voltage to a differential current to drive the output stage. The rail-to-rail output can swing to 50 mV maximum with a 1 mA load at 25°C.

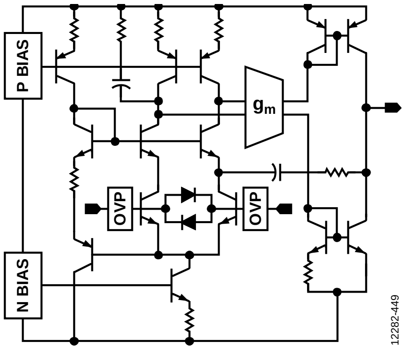


Figure 69. Conceptual Schematic

APPLICATIONS INFORMATION

ACTIVE OVERVOLTAGE PROTECTION

The ADA4177-2 uses active overvoltage protection to protect the device from damage when the inputs are driven to a voltage up to 32 V above the positive supply voltage or 32 V below the negative supply voltage. The ADA4177-2 not only protects the input from damage, but it also reduces the input noise.

Common Protection Methods

Add an External Series Input Resistor

When an op amp does not have input overvoltage protection, moving the input voltage above or below the supply voltage can cause excessive input current, which can damage the op amp. To avoid this, add a series resistor at the input. To protect the op amp from a 30 V transient beyond either rail, limit the input current to 5 mA, and add a 6 kΩ series resistor to the input. However, a trade-off of adding the series resister is that it adds thermal noise. The 6 kΩ series resistor exhibits 10 nV/√Hz of thermal noise, which adds in quadrature thermal noise from the resistor with the op amp noise.

$$N_{TOTAL} = \sqrt{N_{OP\ AMP}^{2} + N_{RESISTOR}^{2}}$$

where:

$N_{OP\ AMP}$ is the op amp noise.

$N_{RESISTOR}$ is the thermal noise generated by the resistor.

When the additional thermal noise is added to the thermal noise (8 nV/√Hz) of the ADA4177-2, the 6 kΩ series resistor brings the total thermal noise to 12 nV/√Hz, which is a 70% increase in thermal noise. Figure 70 shows how noise from the additional source resistance adds to the total noise at the amplifier input; the higher the source resistance, the higher the total noise. Because the ADA4177-2 has integrated input protection for overvoltage conditions, the noise trade-off is avoided.

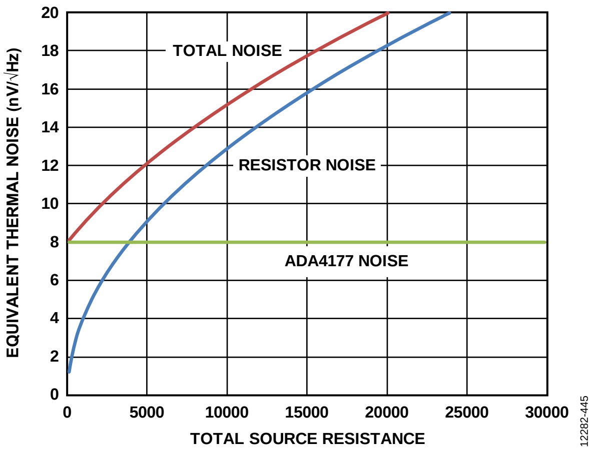


Figure 70. Equivalent Thermal Noise vs. Total Source Resistance

Add External Clamping Diodes

System designers purchase precision op amps because they have a low offset voltage (V_{OS}) and a high common-mode rejection ratio (CMRR). Both of these characteristics simplify system calibration and minimize dynamic error. To maintain these specifications in the presence of electrostatic discharge (ESD) events, bipolar op amps often have internal clamp diodes and small limiting resistors in series with their inputs; however, these do not address fault conditions where the inputs exceed the rails. In these cases, the system designer commonly adds clamping diodes (D1 and D2) along with a series resistor (R_{OVP}), as shown in Figure 71.

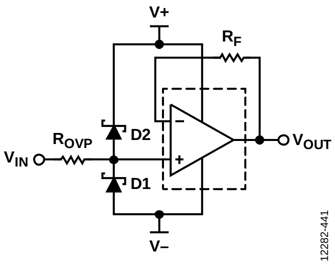


Figure 71. Common Scheme for Protecting Precision Amplifier Inputs from Overvoltage Conditions

If the signal source at V_{IN} is driven to one diode voltage beyond the op amp supplies, the fault current is limited by R_{OVP}. Schottky diodes have a low forward knee voltage of 200 mV less than a typical small signal diode. Therefore, all overvoltage currents are shunted through the external diodes (D1 and D2). The reverse leakage current for a typical Schottky diode is extremely variable with the reverse voltage level. Therefore, as the noninverting input of the op amp swings, the D1 and D2 leakage currents do not match, and the differences pass through R_{OVP}, creating a voltage drop. The voltage drop on R_{OVP} appears as a variation in V_{OS}, which can drastically reduce the CMRR performance. Because the ADA4177-2 has integrated input protection during overvoltage conditions, the degradation in performance is avoided.

Input Protection Circuit

The ADA4177-2 input provides overvoltage protection without the trade-offs encountered in the common design methods. The conceptual schematic of the input is shown in Figure 72.

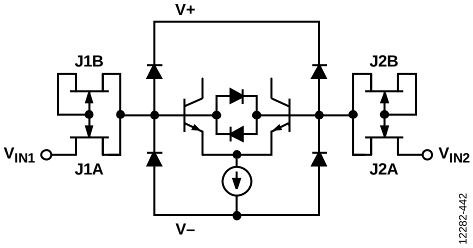


Figure 72. Conceptual Schematic of the Inputs of the ADA4177-2

J1A, J1B, J2A, and J2B are depletion mode junction field effect transistors (JFETs) that replace the series resistance in the conventional protection scheme. Under normal operation, the input bias current of the ADA4177-2 flows through the J1A and J2A transistors without pinching off the channel. To achieve excellent noise performance with the ADA4177-2, J1A and J2A must have a low on resistance (R_{DSON}) of approximately 300 Ω.

When either input exceeds the rail by more than a diode, large currents flow through either J1A or J2A, which causes the channels to pinch off and effectively raises their resistance. Figure 73 shows the overvoltage and undervoltage characteristics as the FET channel pinches.

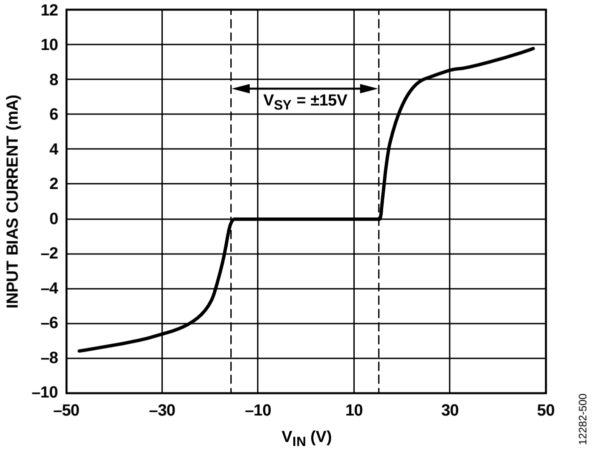


Figure 73. Input Bias Current During Overvoltage and Undervoltage Characteristics, V_{SY} = ±15 V, Voltage Follower Configuration

Figure 74 shows how the JFET effective resistance increases exponentially as shown by the measurements at 2 V, 20 V, and 40 V overvoltage. Note that as the overvoltage increases from 2 V to 40 V, the resistance increases from 300 Ω to 3.5 kΩ (a factor of 11).

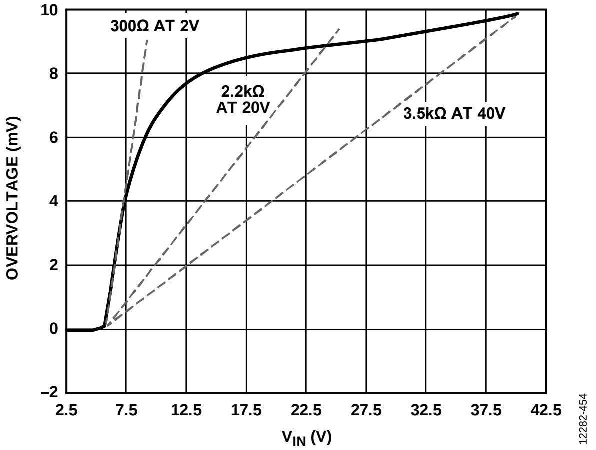


Figure 74. Overvoltage vs. Input Voltage (V_{IN}), Voltage Follower Configuration

LIMITING OVERVOLTAGE CURRENT OUT OF THE POSITIVE SUPPLY PIN

Because the positive power supply of the system may be incapable of sinking the large overvoltage current of 8 mA, care was taken to divide down this current into the positive rail during an overvoltage event. As shown in Figure 75, Q1L is a lateral PNP transistor that serves two purposes. First, the emitter base acts as a clamping diode to route the overvoltage current away from the V+ pin and to the V− pin. Second, it divides down this current via the beta of Q1L. At an emitter current of 8 mA, the beta of Q1L is approximately 8, which reduces the current injected into the positive supply by a factor of 8.

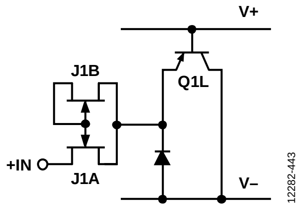


Figure 75. Overvoltage Protection Circuitry

Figure 76 shows the positive and negative supply currents when the input voltage exceeds the supply voltages (and overvoltage condition). The current at the V+ terminal does not reverse direction during an overvoltage event because the current is directed to V− via the collector of Q1L.

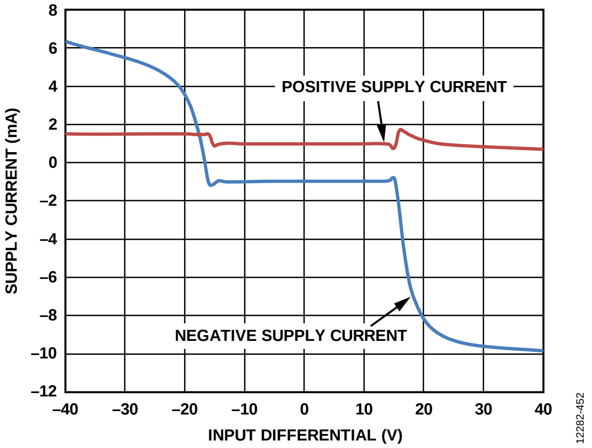


Figure 76. Supply Current vs. Input Differential, Circuit Configured at Unity Gain with V+ = +15 V and V− = −15 V

If undervoltage transients are expected, ensure that the negative voltage source driving V− can handle sourcing current without pumping up the supply voltage.

EMI PROTECTION

The ADA4177-2 inputs are also protected from high frequency EMI. In an op amp with no EMI protection, signals not within the bandwidth of the op amp couple into sensitive amplifier inputs and become rectified as they travel through the amplifier, eventually appearing as ac feedthrough riding on a dc offset. When an input filter is not provided, these offsets can be quite large. These offsets are referred to as the electromagnetic interference rejection ratio (EMIRR). The amplifier EMIRR is defined as

$$EMIRR = 20 \times \log\left(\frac{100\text{ mV}}{\Delta V_{OS}}\right)$$

where:
100 mV is generally the peak-to-peak input used for the test.
ΔV_{OS} is the change in the op amp offset as a result of the input signal.

Figure 77 shows the input EMI protection of the ADA4177-2.

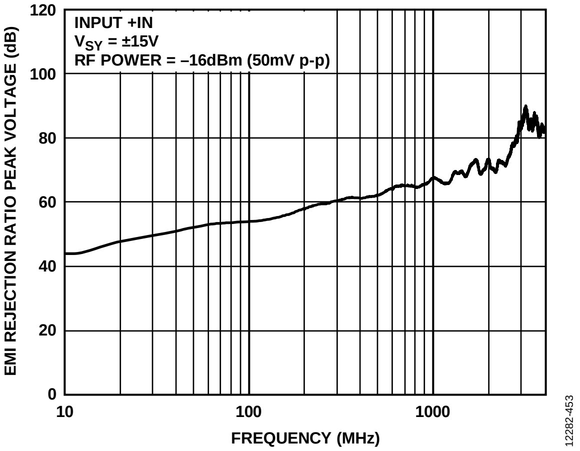


Figure 77. EMI Rejection Ratio Peak Voltage vs. Frequency

SELF HEATING

During an overvoltage condition, the ADA4177-2 dissipates heat according to the thermal resistance (θ_{JA}) of the package it is in, which, in turn, heats up the die. Ensure that the specified operating junction temperature does not exceed 150°C for device protection. Extended overtemperature exposure can cause some operating specifications to shift outside of their guaranteed limits.

As shown in Figure 73, the ADA4177-2 inputs sink by approximately 8 mA at 15 V overvoltage. In that condition, the ADA4177-2 dissipates 120 mW of power. If the package has a θ_{JA} of 100°C/W, the junction temperature rises by approximately 12°C over the ambient temperature of the package and junction. In such a case, derate the ambient operating temperature by 12°C (125°C minus 12°C) for an absolute maximum operating temperature of 113°C. When the junction temperature exceeds the absolute maximum junction temperature of 125°C, add an additional series resistance to the inputs to further decrease the overvoltage current. Figure 78 shows the maximum ambient temperature vs. the continuous overvoltage at θ_{JA} = 150°C/W.

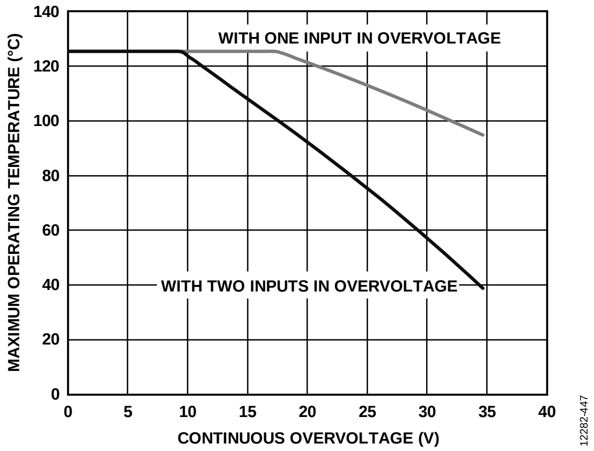


Figure 78. Maximum Ambient Temperature vs. Continuous Overvoltage for One Input and Two Inputs (θ_{JA} = 150°C/W)

USING THE ADA4177-2 AS A COMPARATOR

The ADA4177-2 can be used as a comparator as long as relatively small input impedance can be tolerated. That is, the input differential pair is diode clamped but the overvoltage protection circuitry limits the differential. Figure 79 shows the ADA4177-2 input current vs. the input differential voltage with ±15 V supplies.

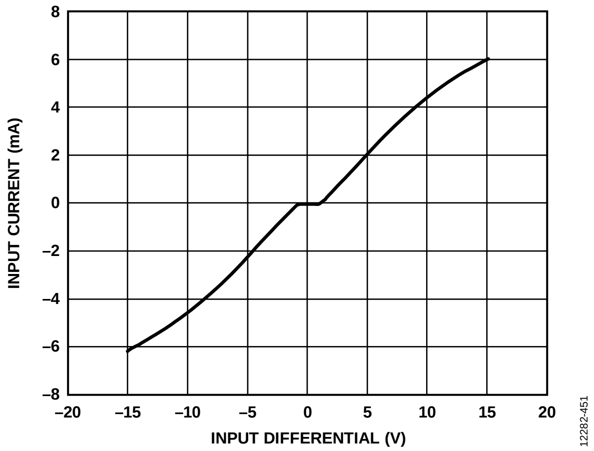


Figure 79. Input Current vs. Input Differential with ±15 V Supplies

Figure 80 shows a comparator circuit referenced to ground using the ADA4177-2. The supply voltages are ±5 V. The −IN input is grounded and a positive input is stepped to ±1 V. Both the positive and negative recovery is approximately 4 µs.

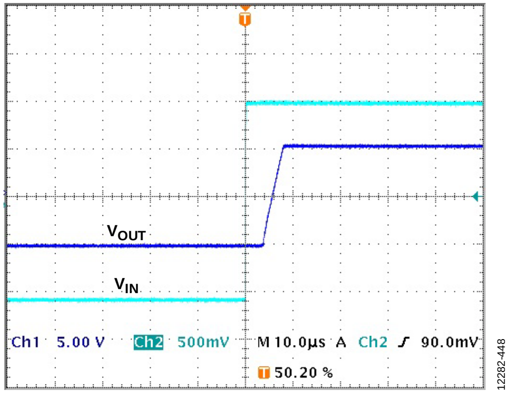


Figure 80. ADA4177-2 Used as a Comparator with ±5 V Supplies and a ±1 V Input Step, Voltage Follower Configuration

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change in polarity in the amplifier transfer function. Many op amps exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this phase reversal can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ADA4177-2 is immune to phase reversal problems even at input voltages beyond the power supply settings.

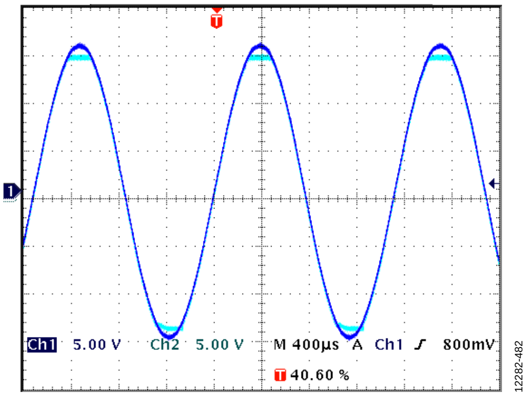


Figure 81. Output Showing No Phase Reversal in Overvoltage Condition

PROPER PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADA4177-2 is a high precision device. To ensure optimum performance at the PCB level, take care in the design of the board layout.

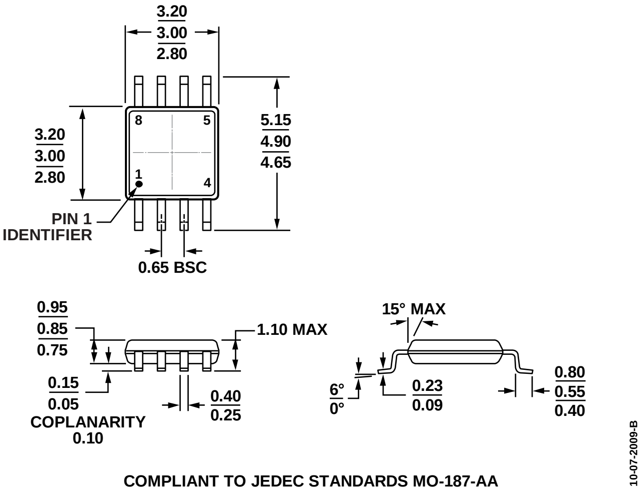
To avoid leakage currents, maintain a clean and moisture free board surface. Coating the surface creates a barrier to moisture accumulation and reduces parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes the power supply disturbances caused by the output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. Keep the signal traces at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Ensure, where possible, that input signal paths contain matching numbers and types of components, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other, and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

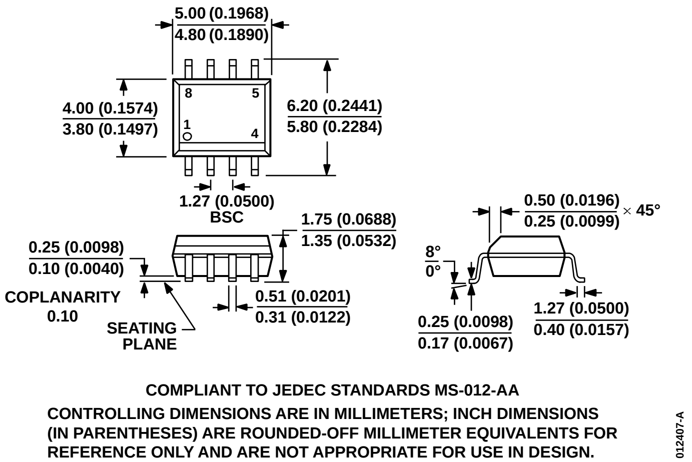
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and maintains a constant temperature across the circuit board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 82. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 83. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4177-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A36
ADA4177-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A36
ADA4177-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A36
ADA4177-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4177-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4177-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Compliant Part.

D12282-0-10/14(A)