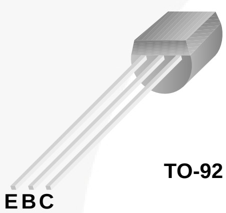
October 2014

2N3904 / MMBT3904 / PZT3904
NPN General-Purpose Amplifier

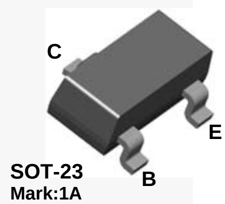
Description

This device is designed as a general-purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

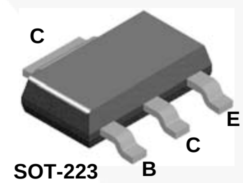
2N3904



MMBT3904



PZT3904



Ordering Information

Part Number	Marking	Package	Packing Method	Pack Quantity
2N3904BU	2N3904	TO-92 3L	Bulk	10000
2N3904TA	2N3904	TO-92 3L	Ammo	2000
2N3904TAR	2N3904	TO-92 3L	Ammo	2000
2N3904TF	2N3904	TO-92 3L	Tape and Reel	2000
2N3904TFR	2N3904	TO-92 3L	Tape and Reel	2000
MMBT3904	1A	SOT-23 3L	Tape and Reel	3000
PZT3904	3904	SOT-223 4L	Tape and Reel	2500

© 2002 Fairchild Semiconductor Corporation

Absolute Maximum Ratings[1], [2]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C

Notes:

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

Thermal Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Maximum			Unit
		2N3904	**MMBT3904**[3]	**PZT3904**[4]	
P_D	Total Device Dissipation	625	350	1,000	mW
	Derate Above 25°C	5.0	2.8	8.0	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

Notes:

3. Device is mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.
4. Device is mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm, mounting pad for the collector lead minimum 6 cm^2.

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	6.0		V
I_{BL}	Base Cut-Off Current	V_{CE} = 30 V, V_{EB} = 3 V		50	nA
I_{CEX}	Collector Cut-Off Current	V_{CE} = 30 V, V_{EB} = 3 V		50	nA
ON CHARACTERISTICS[5]					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V	40		
		I_C = 1.0 mA, V_{CE} = 1.0 V	70		
		I_C = 10 mA, V_{CE} = 1.0 V	100	300	
		I_C = 50 mA, V_{CE} = 1.0 V	60		
		I_C =100 mA, V_{CE} = 1.0V	30		
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA		0.2	V
		I_C = 50 mA, I_B = 5.0 mA		0.3	
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA	0.65	0.85	V
		I_C = 50 mA, I_B = 5.0 mA		0.95	
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 100 kHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 100 kHz		8.0	pF
NF	Noise Figure	I_C = 100 μA, V_{CE} = 5.0 V, R_S = 1.0 kΩ, f = 10 Hz to 15.7 kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA		200	ns
t_f	Fall Time			50	ns

Note:

5. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

Typical Performance Characteristics

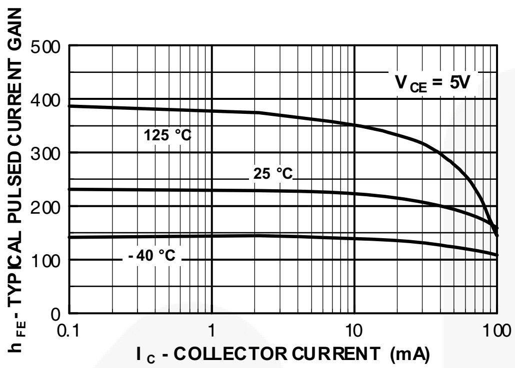


Figure 1. Typical Pulsed Current Gain vs. Collector Current

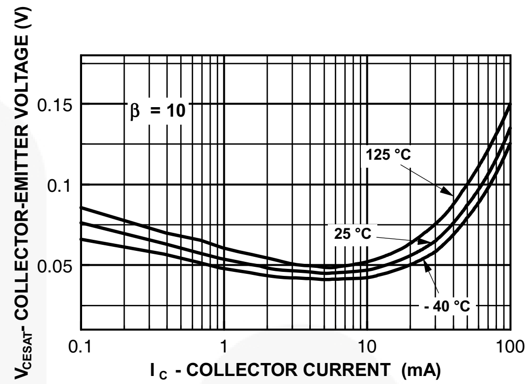


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

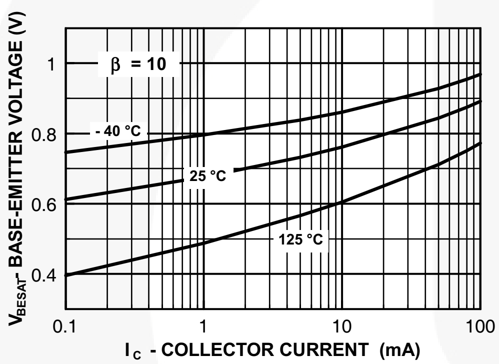


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

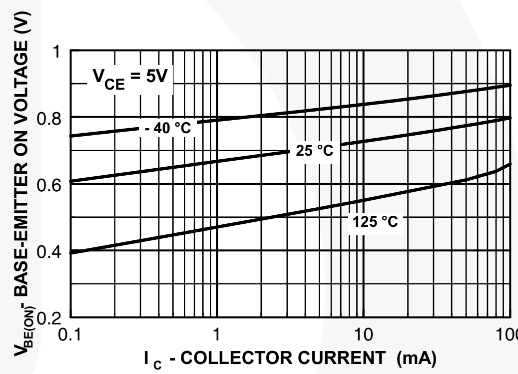


Figure 4. Base-Emitter On Voltage vs. Collector Current

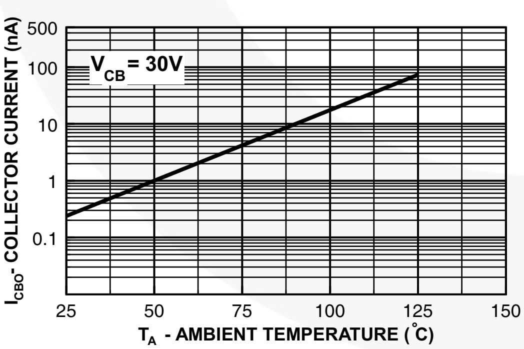


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

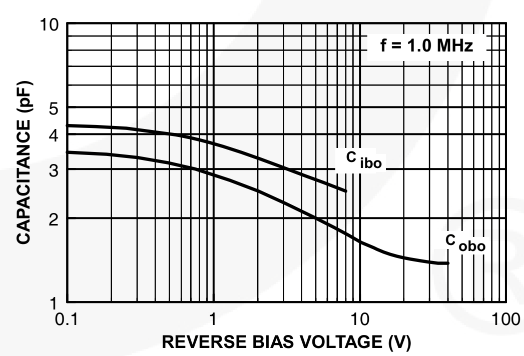


Figure 6. Capacitance vs. Reverse Bias Voltage

Typical Performance Characteristics (Continued)

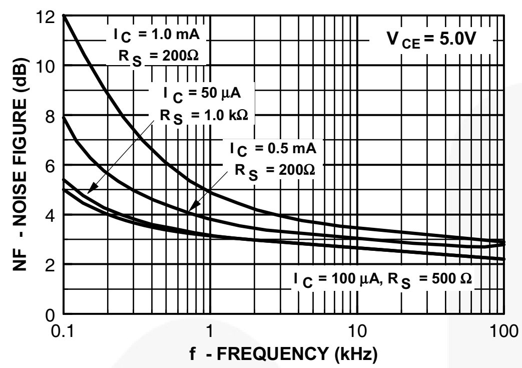


Figure 7. Noise Figure vs. Frequency

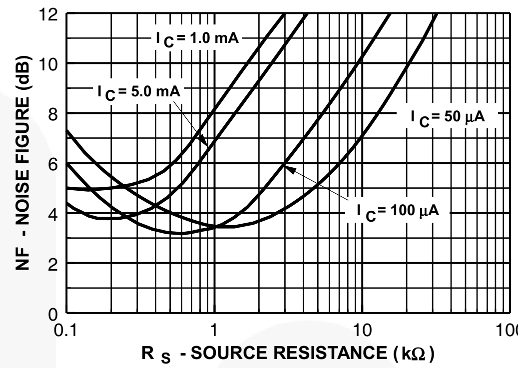


Figure 8. Noise Figure vs. Source Resistance

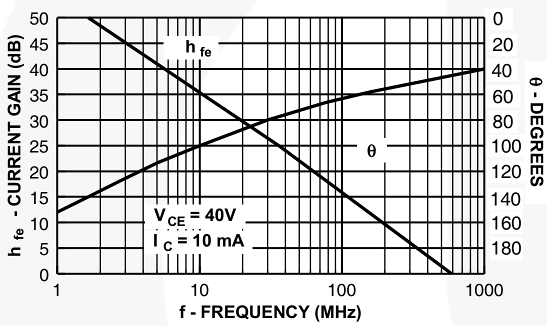


Figure 9. Current Gain and Phase Angle vs. Frequency

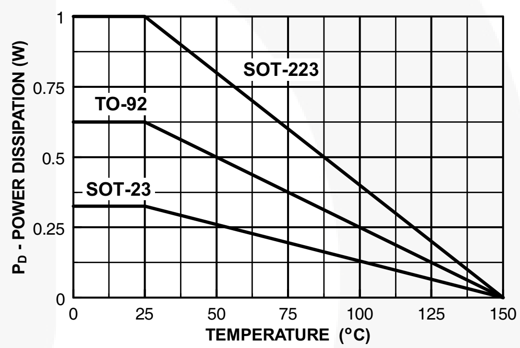


Figure 10. Power Dissipation vs. Ambient Temperature

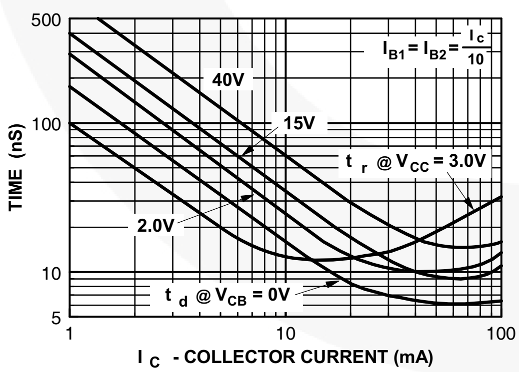


Figure 11. Turn-On Time vs. Collector Current

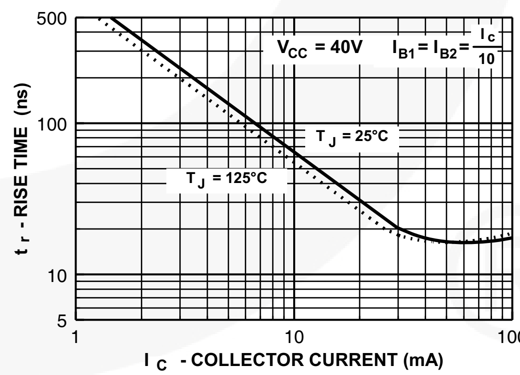


Figure 12. Rise Time vs. Collector Current

Typical Performance Characteristics (Continued)

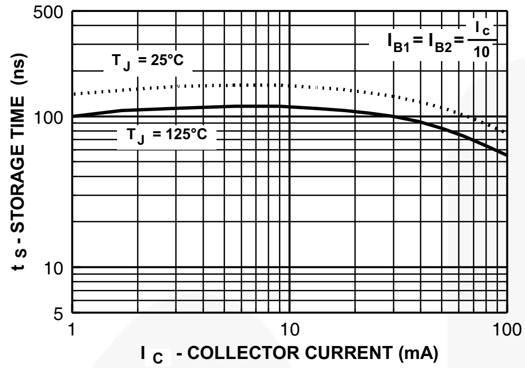


Figure 13. Storage Time vs. Collector Current

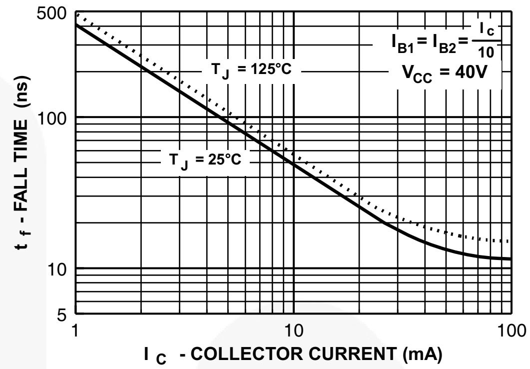


Figure 14. Fall Time vs. Collector Current

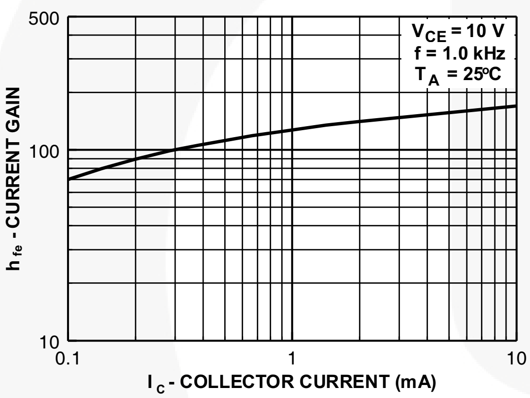


Figure 15. Current Gain

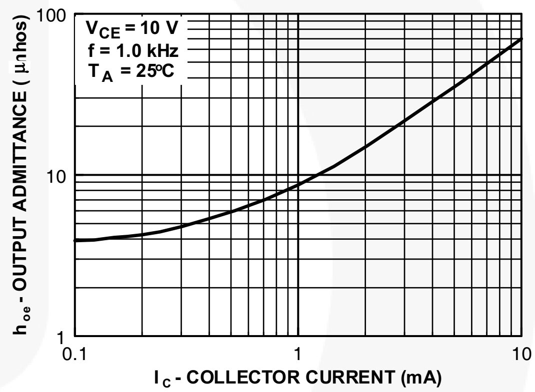


Figure 16. Output Admittance

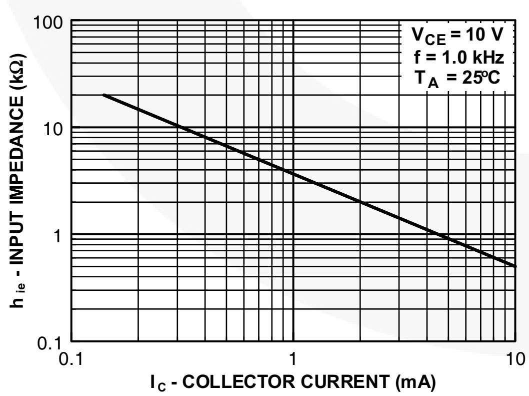


Figure 17. Input Impedance

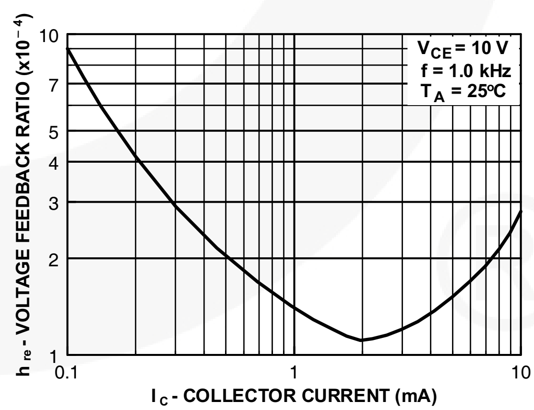


Figure 18. Voltage Feedback Ratio

Test Circuits

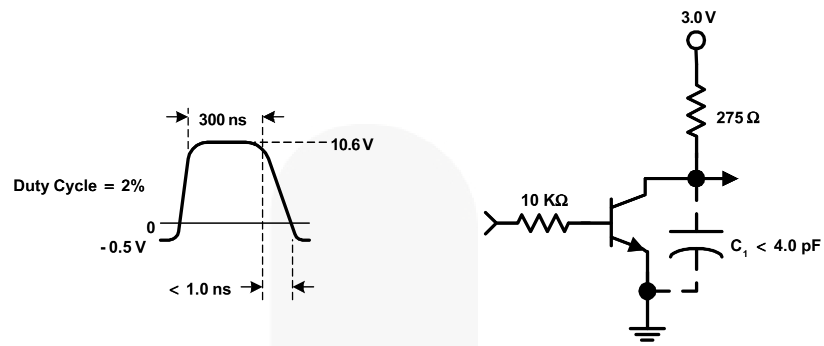


Figure 19. Delay and Rise Time Equivalent Test Circuit

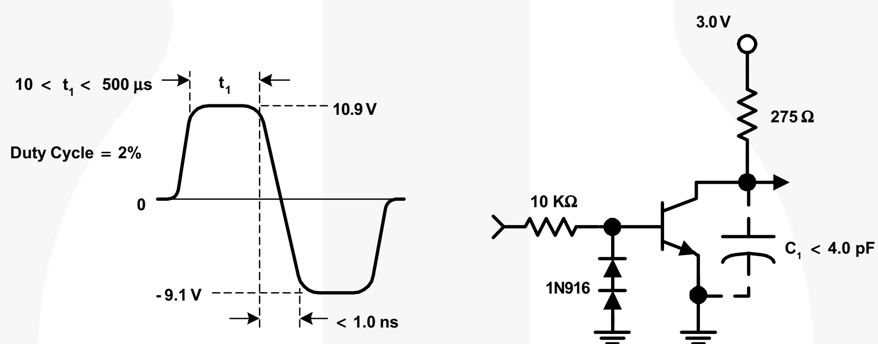
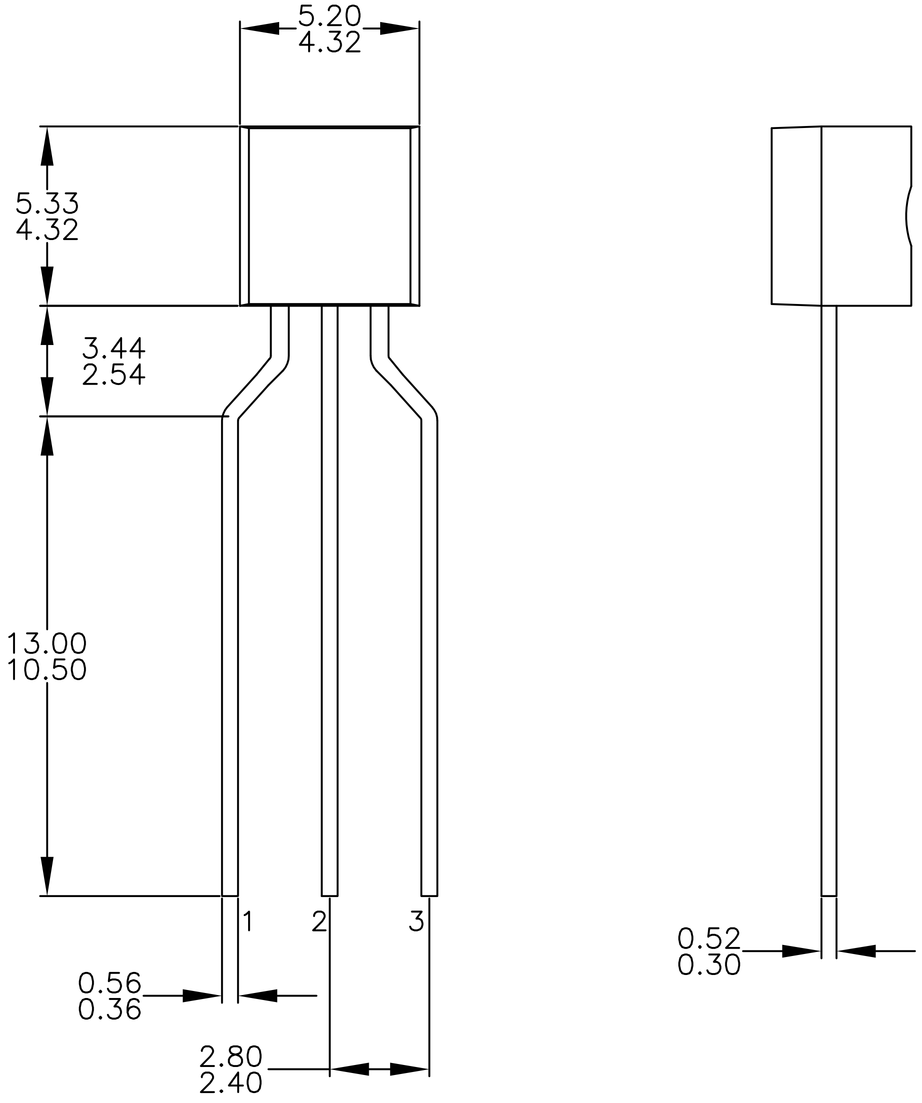
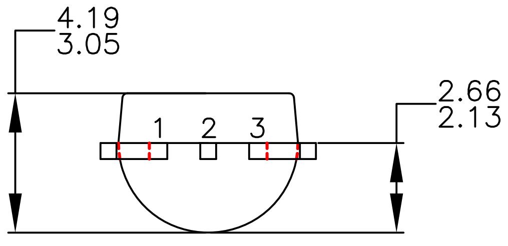


Figure 20. Storage and Fall Time Equivalent Test Circuit





NOTES: UNLESS OTHERWISE SPECIFIED

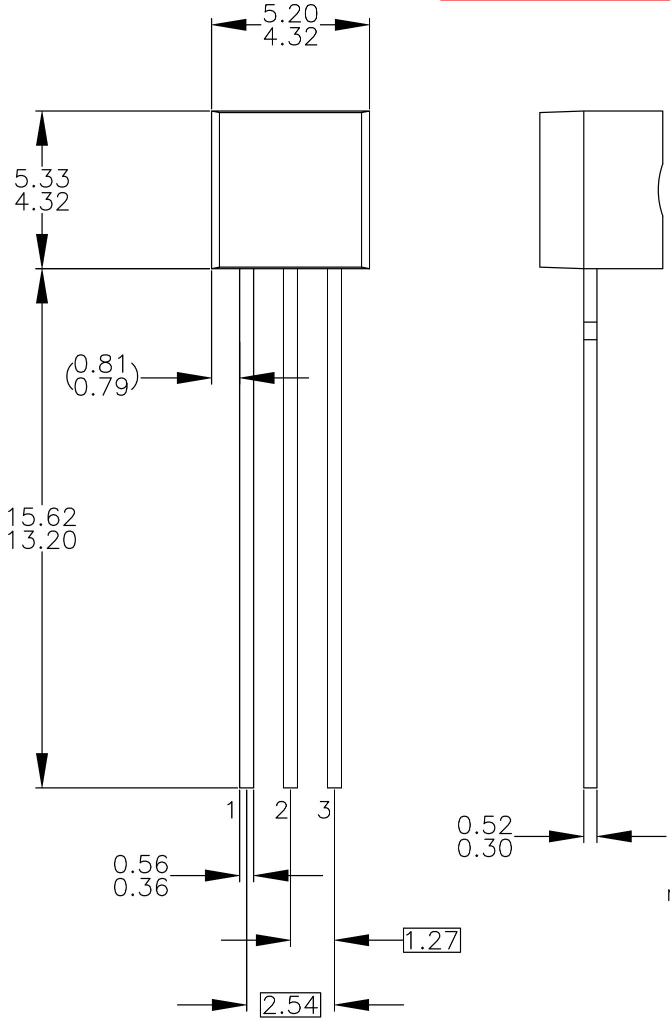
A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5M-2009.
D. DRAWING FILENAME: MKT-ZA03FREV3.
E. FAIRCHILD SEMICONDUCTOR.

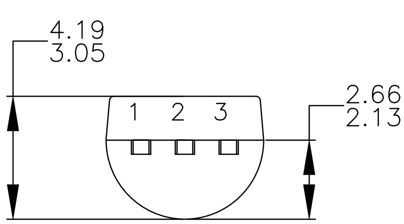
THIS DRAWING IS THE PROPERTY OF FAIRCHILD SEMICONDUCTOR CORPORATION. NO USE THEREOF SHALL BE MADE OTHER THAN AS A REFERENCE FOR PROPOSALS AS SUBMITTED TO FAIRCHILD SEMICONDUCTOR CORPORATION FOR JOBS TO BE EXECUTED IN CONFORMITY WITH SUCH PROPOSALS UNLESS THE CONSENT OF SAID FAIRCHILD SEMICONDUCTOR CORPORATION HAS PREVIOUSLY BEEN OBTAINED. NO PART OF THIS DRAWING SHALL BE COPIED OR DUPLICATED OR ITS CONTENTS DISCLOSED. THE INFORMATION CONTAINED ON THIS DRAWING IS CONFIDENTIAL AND PROPRIETARY.

REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14–1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32– 4.70 TO 4.32–4.83; CHG PKG HEIGHT DIM FR 4.32–4.70 TO 4.32–4.78; CHG LD THICK DIM FR 0.30– 0.48 TO 0.30–0.52; DAMBAR–PKG DIM FR 1.27–1.65 TO 0.90–1.65; LD LGH DIM FR 14.47–15.64 TO 14.47–15.62; PKG DIM: 1.02–1.52 TO 0.92–1.52, 3.81–4.45 TO 3.40–4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C; MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	4OCT1999	RCM/MRG
3	CHG LD LEN FR 15.61/14.07 TO 15.62/13.20; CHG MOLD BODY HT FR 4.78/4.32 TO 5.33/4.32; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO (0.81/0.79); CHG MOLD BODY WIDTH FR 4.83/4.32 TO 5.20/4.32; ADD PKG THICKNESS DIM 'E'; CHG 's' DIM FR 2.41/2.13 TO 2.66/2.13; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M–1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP

APPROVED
July-14-2008





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO–92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M–1994.
D) TO–92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT–ZA03DREV3.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	03APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

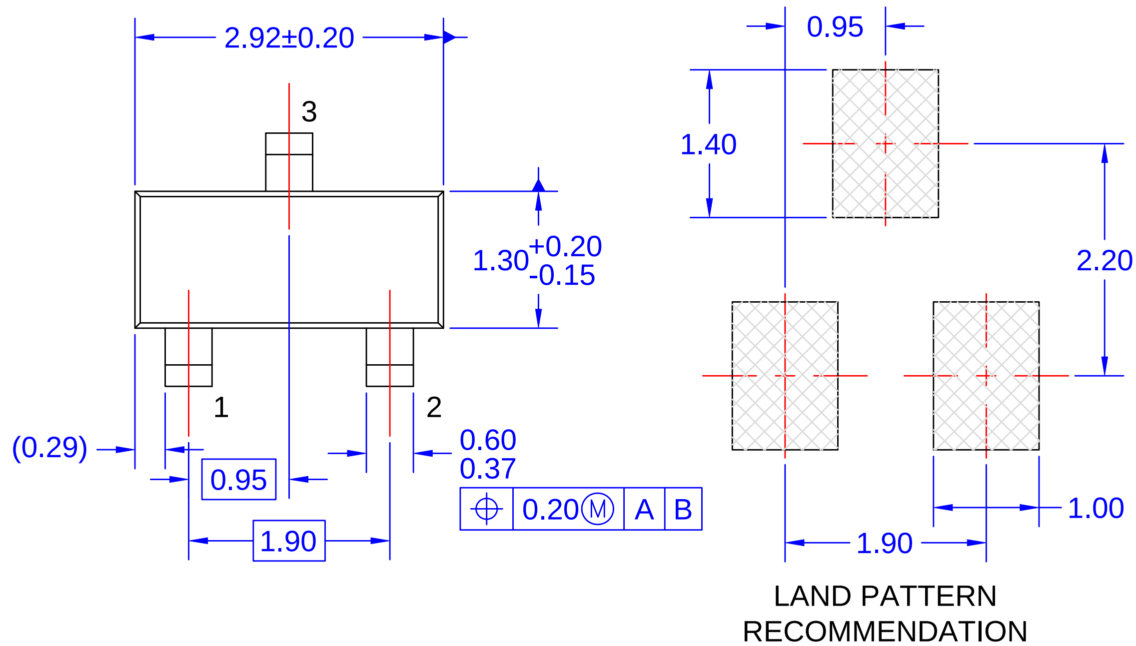
PROJECTION
INCH
[MM]

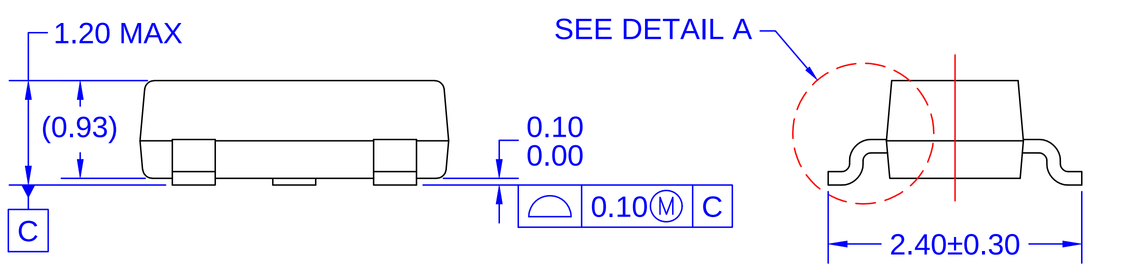
FAIRCHILD SEMICONDUCTOR™

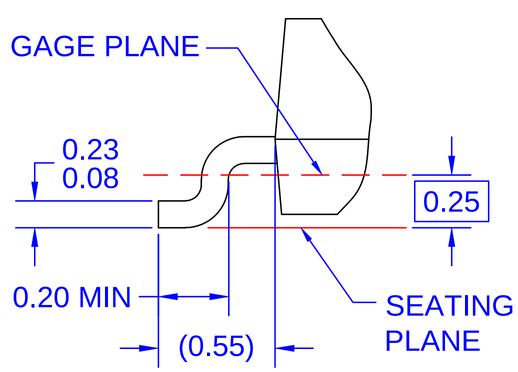
3LD,TO–92,MOLDED
STD STRAIGHT LD
(NO EOL CODE)

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT–ZA03D	3

FORMERLY: N/A
SHEET : 1 OF 1







DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

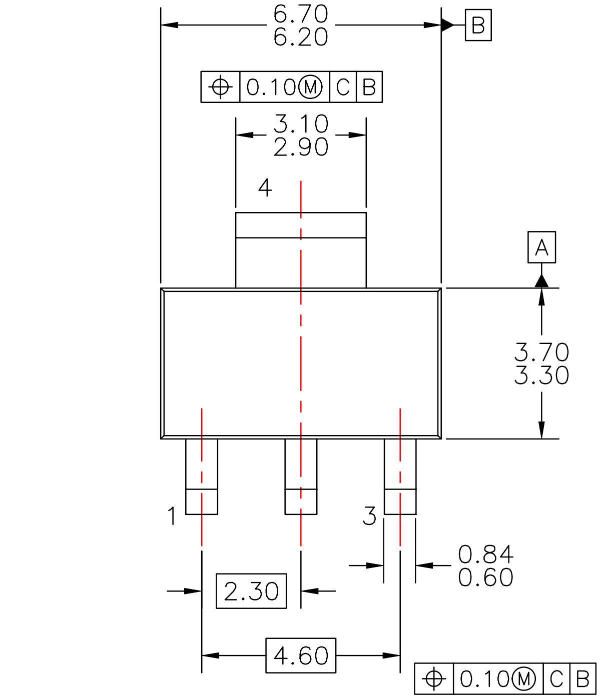
A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
E) DRAWING FILE NAME: MA03DREV10

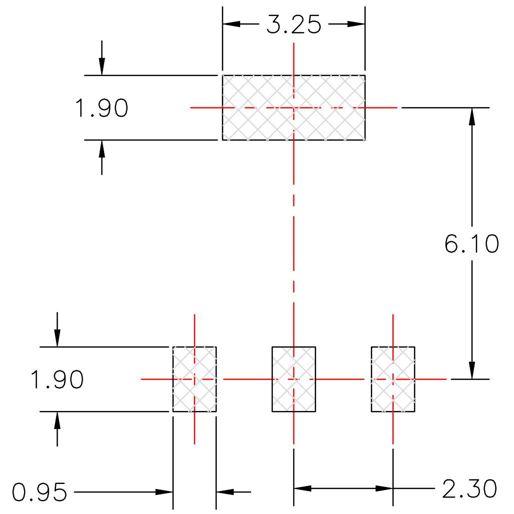
THIS DRAWING IS THE PROPERTY OF FAIRCHILD SEMICONDUCTOR CORPORATION. NO USE THEREOF SHALL BE MADE OTHER THAN AS A REFERENCE FOR PROPOSALS AS SUBMITTED TO FAIRCHILD SEMICONDUCTOR CORPORATION FOR JOBS TO BE EXECUTED IN CONFORMITY WITH SUCH PROPOSALS UNLESS THE CONSENT OF SAID FAIRCHILD SEMICONDUCTOR CORPORATION HAS PREVIOUSLY BEEN OBTAINED. NO PART OF THIS DRAWING SHALL BE COPIED OR DUPLICATED OR ITS CONTENTS DISCLOSED. THE INFORMATION CONTAINED ON THIS DRAWING IS CONFIDENTIAL AND PROPRIETARY.

APPROVED
July-14-2008

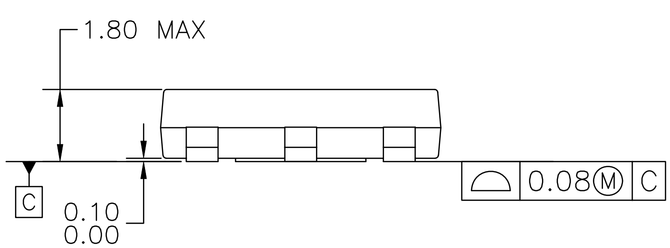
REVISIONS

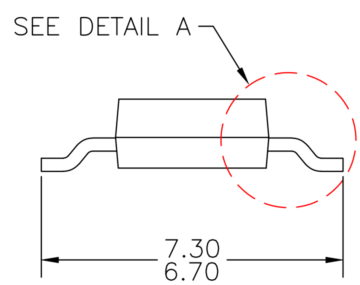
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR $0.74^{+0.05}_{-0.07}$ TO 0.60–0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR $^{1.80}_{1.55}$ TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR $0.3^{+0.02}_{-0.07}$ TO 0.20–0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC: CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR $3.56^{+0.15}_{-0.25}$ TO $^{3.70}_{3.30}$; CHG BODY LN FR $6.5^{+0.2}_{-0.2}$ TO $^{6.70}_{6.20}$; CHG TOTAL PKG WID FR $6.96^{+0.33}_{-0.25}$ TO $^{7.30}_{6.70}$; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP

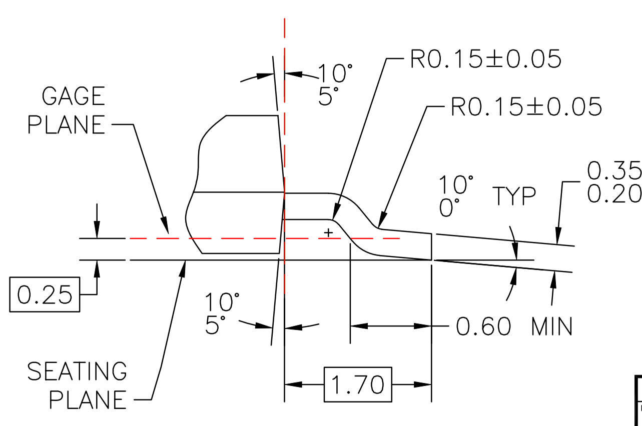




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING BASED ON JEDEC REGISTRATION TO–261, VARIATION AA.
B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
C) ALL DIMENSIONS ARE IN MILLIMETERS.
D) DRAWING CONFORMS TO ASME Y14.5M–1994.
E) LANDPATTERN NAME: SOT230P700X180–4BN
F) DRAWING FILENAME: MKT–MA04AREV2

APPROVALS	DATE	
DRAWN: J.U. COMPARATIVO JR.	26FEB2008	FAIRCHILD SEMICONDUCTOR™
CHECKED: L.Z. STA CRUZ		MOLDED PACKAGE SOT–223, 4 LEAD
APPROVED: M.R. GESTOLE		
G.S. BAJE		
PROJECTION INCH [MM]		SCALE 1:1 · SIZE A3 · DRAWING NUMBER MKT–MA04A · REV 2
		FORMERLY: N/A · SHEET : 1 OF 1

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AttitudeEngine™
Awinda®
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
MTi®
MTx®
MVN®
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™
Xsens™
仙童™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT HTTP://WWW.FAIRCHILDSEMI.COM. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I73