



May 2014

# FDMS7602S

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

Q1: 30 V, 30 A, 7.5 mΩ Q2: 30 V, 30 A, 5.0 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 7.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 12$  A
- Max  $r_{DS(on)}$  = 12 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 10$  A

Q2: N-Channel

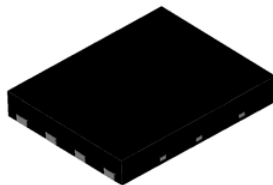
- Max  $r_{DS(on)}$  = 5.0 mΩ at  $V_{GS} = 10$  V,  $I_D = 17$  A
- Max  $r_{DS(on)}$  = 6.8 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 14$  A
- RoHS Compliant

### General Description

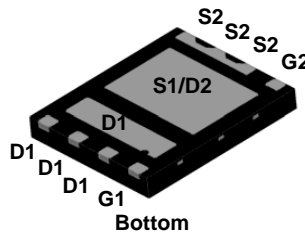
This device includes two specialized N-Channel MOSFETs in a dual MLP package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET<sup>™</sup> (Q2) have been designed to provide optimal power efficiency.

### Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCore

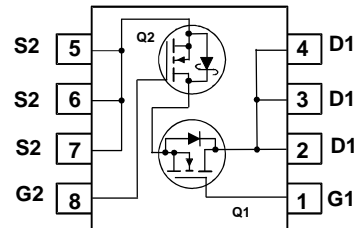


Top



Bottom

Power 56



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	30	30	A
	-Continuous $T_A = 25$ °C	12 <sup>1a</sup>	17 <sup>1b</sup>	
	-Pulsed	40	60	
$P_D$	Power Dissipation for Single Operation $T_A = 25$ °C	2.2 <sup>1a</sup>	2.5 <sup>1b</sup>	W
	Power Dissipation for Single Operation $T_A = 25$ °C	1.0 <sup>1c</sup>	1.0 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 <sup>1a</sup>	50 <sup>1b</sup>	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 <sup>1c</sup>	120 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	2	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7602S	FDMS7602S	Power 56	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 1\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		15 15		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			100 100	nA nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$ , $I_D = 1\text{ mA}$	Q1 Q2	1 1	1.8 1.8	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 1\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-6 -5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q1		6.0 8.5 8.3	7.5 12 12	m $\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 17\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 14\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 17\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q2		4.2 5.4 4.9	5.0 6.8 7.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 12\text{ A}$ $V_{DS} = 5\text{ V}$ , $I_D = 17\text{ A}$	Q1 Q2		63 87		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1: $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		1315 2020	1750 2690	pF
$C_{oss}$	Output Capacitance	Q2: $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		445 860	600 1145	pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		45 95	70 145	pF
$R_g$	Gate Resistance		Q1 Q2		0.9 0.7		$\Omega$

**Switching Characteristics**

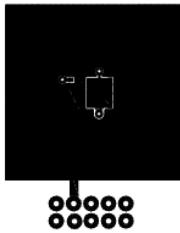
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}$ , $I_D = 12\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$ Q2: $V_{DD} = 15\text{ V}$ , $I_D = 17\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		8.6 11	18 20	ns	
$t_r$	Rise Time		Q1 Q2		2.5 3.8	10 10	ns	
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		20 27	32 43	ns	
$t_f$	Fall Time		Q1 Q2		2.3 3.2	10 10	ns	
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V}$ to $10\text{ V}$ $V_{GS} = 0\text{ V}$ to $4.5\text{ V}$	Q1 $V_{DD} = 15\text{ V}$ , $I_D = 12\text{ A}$	Q1 Q2		20 33	28 46	nC
				Q1 Q2		9.3 16	13 22	
$Q_{gs}$	Gate to Source Gate Charge	Q2 $V_{DD} = 15\text{ V}$ , $I_D = 17\text{ A}$	Q1 Q2		4.3 5.8		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		2.2 4.6			

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 17\text{ A}$ (Note 2)	Q2		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		27	43	ns
			Q2		29	46	
$Q_{rr}$	Reverse Recovery Charge	$I_F = 17\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		10	18	nC
			Q2		31	50	

**Notes:**

1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



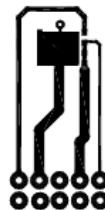
a. 57 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3: As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

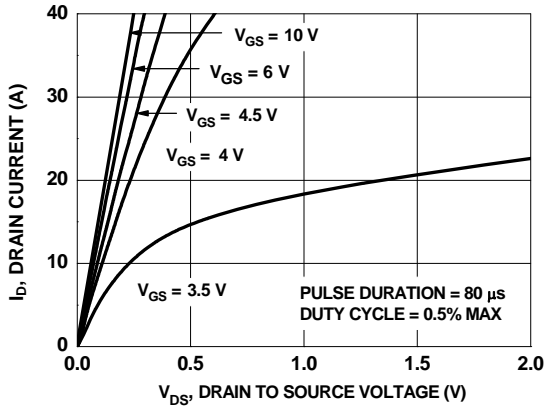


Figure 1. On Region Characteristics

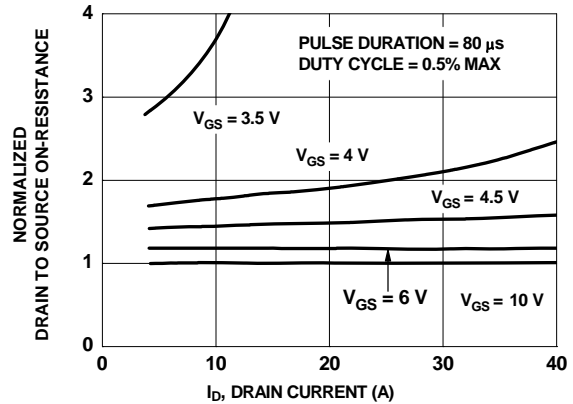


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

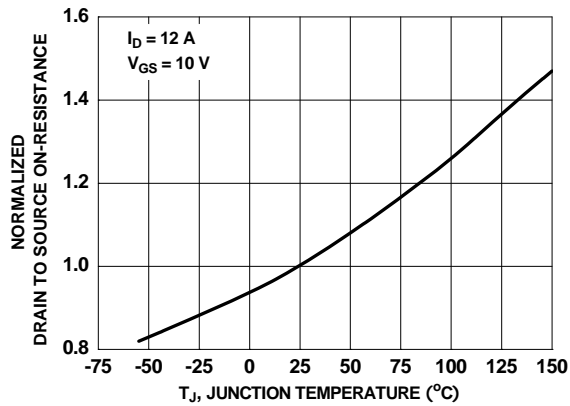


Figure 3. Normalized On Resistance vs Junction Temperature

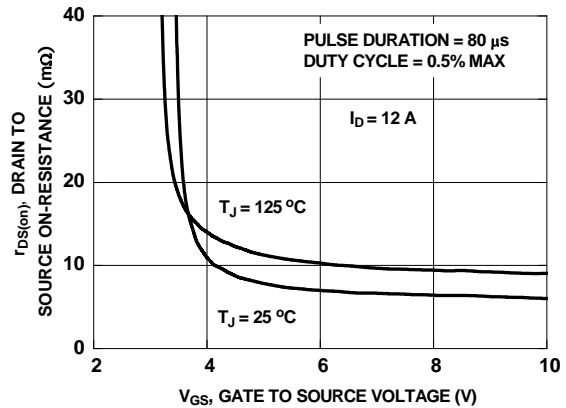


Figure 4. On-Resistance vs Gate to Source Voltage

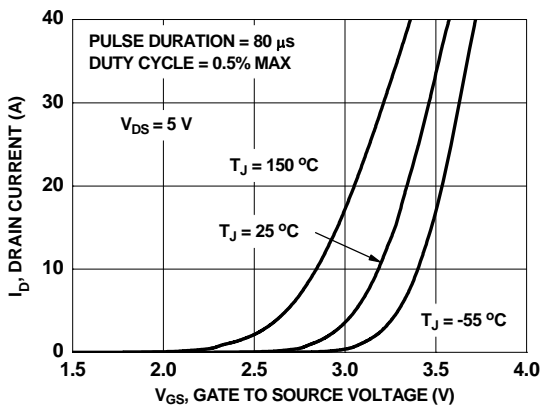


Figure 5. Transfer Characteristics

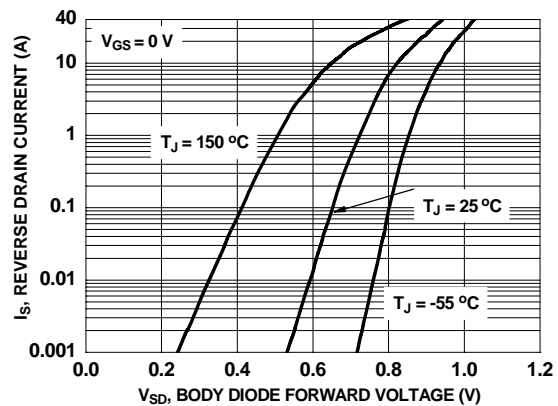
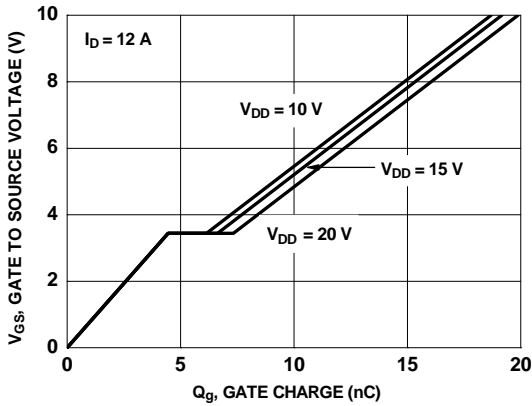
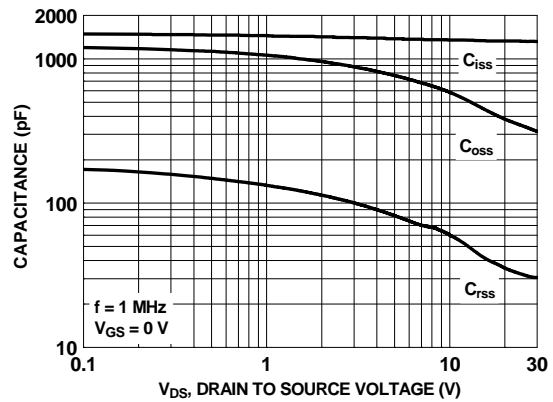


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

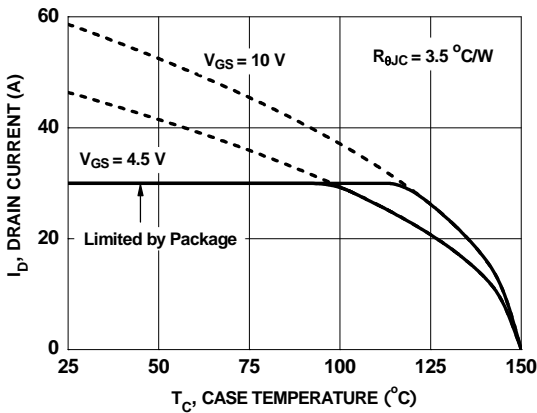
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



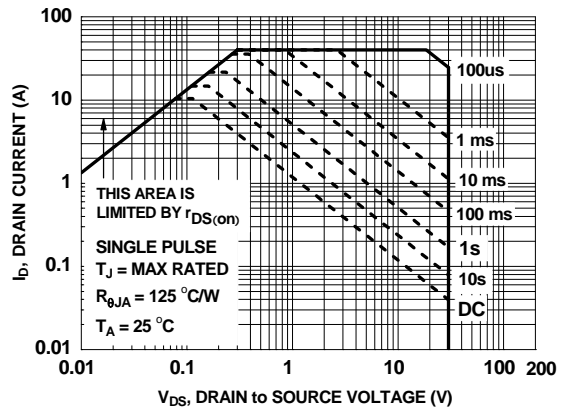
**Figure 7. Gate Charge Characteristics**



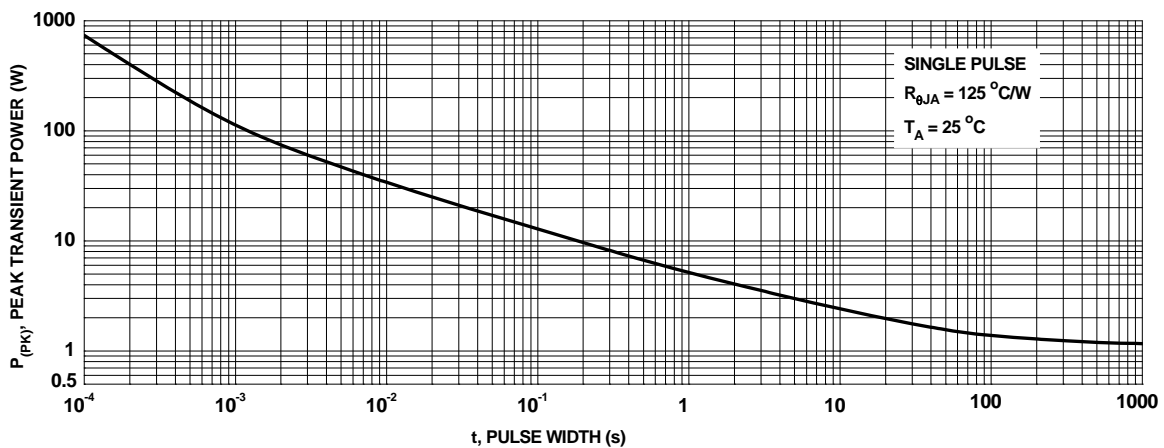
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Maximum Continuous Drain Current vs Case Temperature**

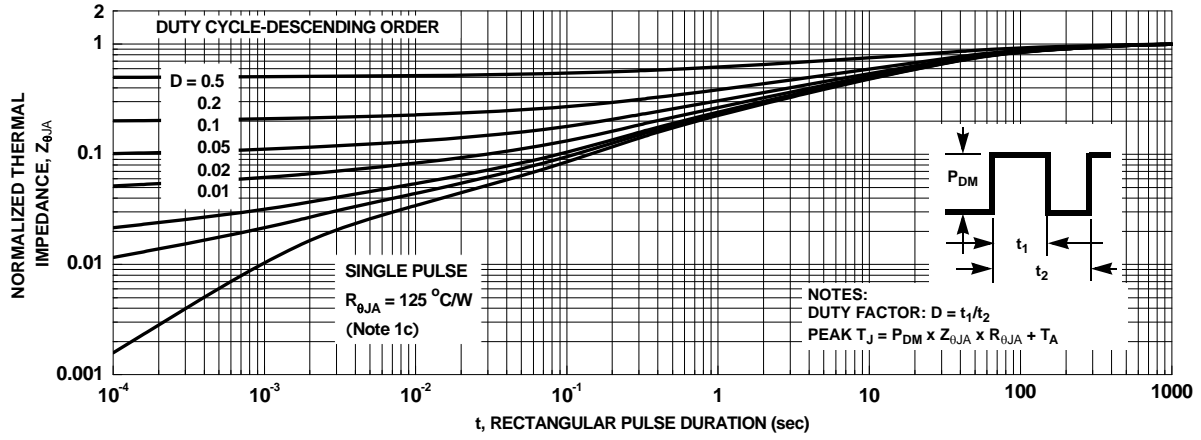


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

### Typical Characteristics (Q2 SyncFET)

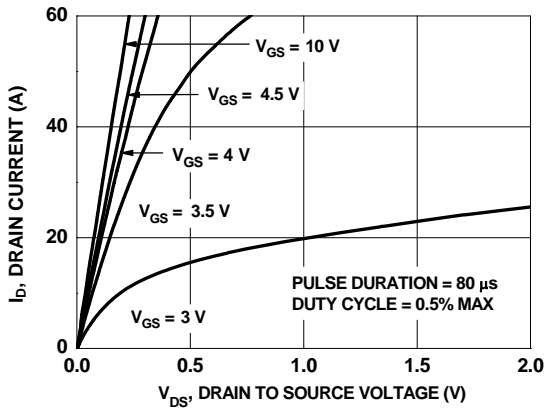


Figure 13. On-Region Characteristics

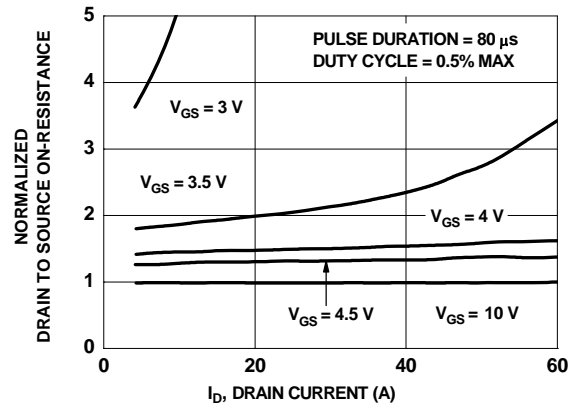


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

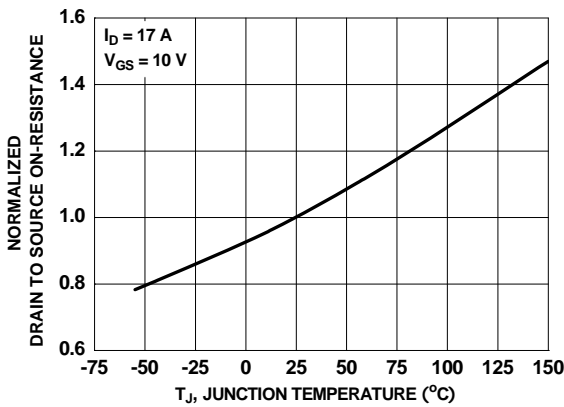


Figure 15. Normalized On-Resistance vs Junction Temperature

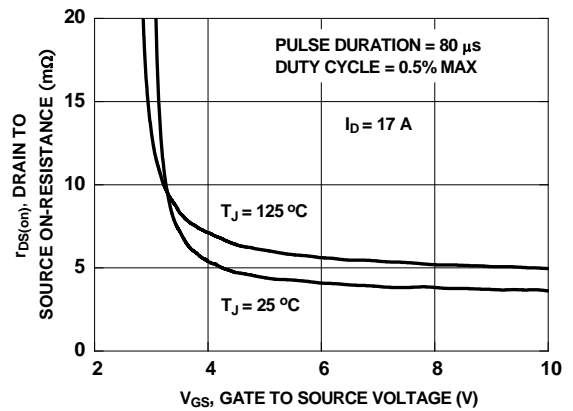


Figure 16. On-Resistance vs Gate to Source Voltage

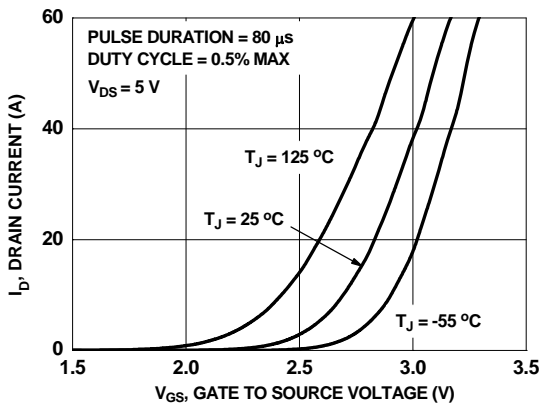


Figure 17. Transfer Characteristics

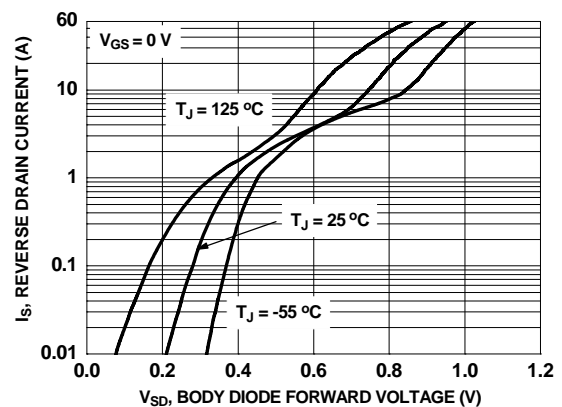


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

### Typical Characteristics (Q2 SyncFET)

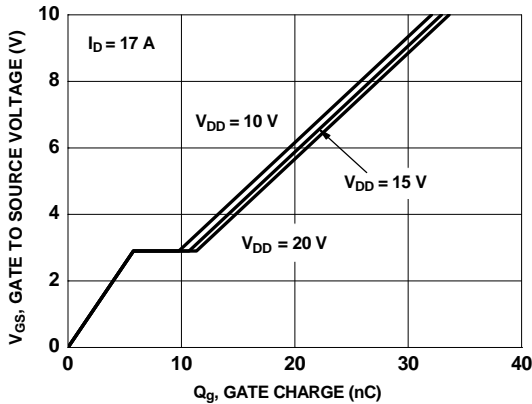


Figure 19. Gate Charge Characteristics

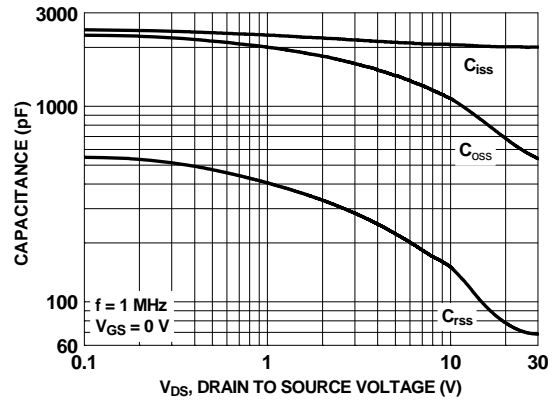


Figure 20. Capacitance vs Drain to Source Voltage

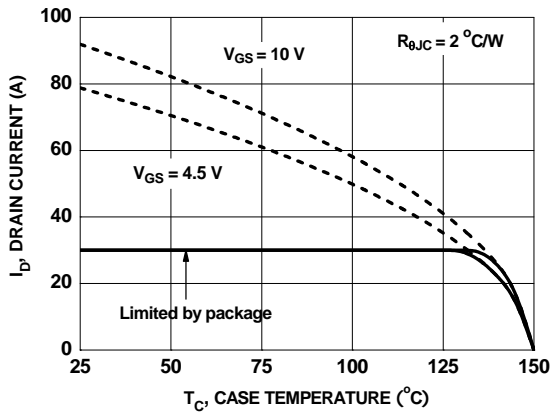


Figure 21. Maximum Continuous Drain Current vs Case Temperature

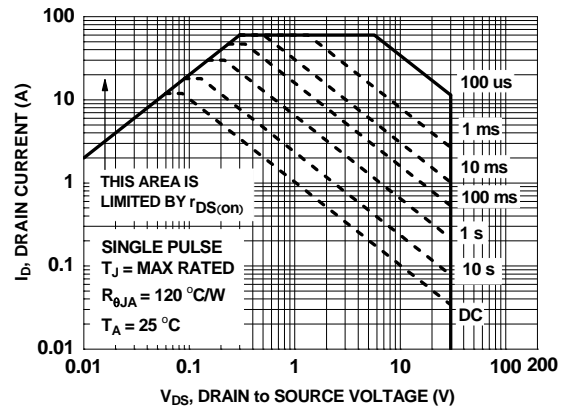


Figure 22. Forward Bias Safe Operating Area

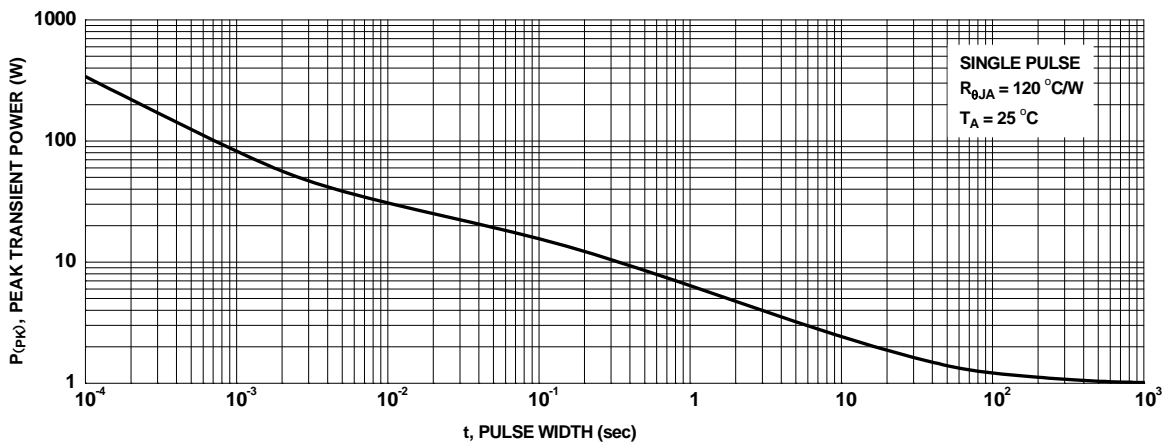


Figure 23. Single Pulse Maximum Power Dissipation



### Typical Characteristics (Q2 SyncFET)

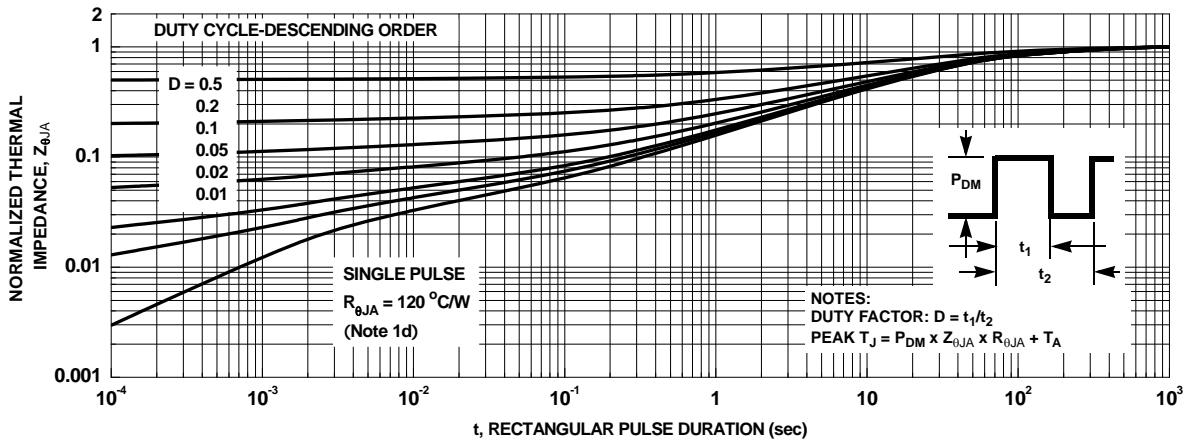


Figure 24. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

### SyncFET<sup>™</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>™</sup> process embeds a Schottky diode in parallel with PowerTrench<sup>®</sup> MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 25 shows the reverse recovery characteristic of the FDMS7602S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

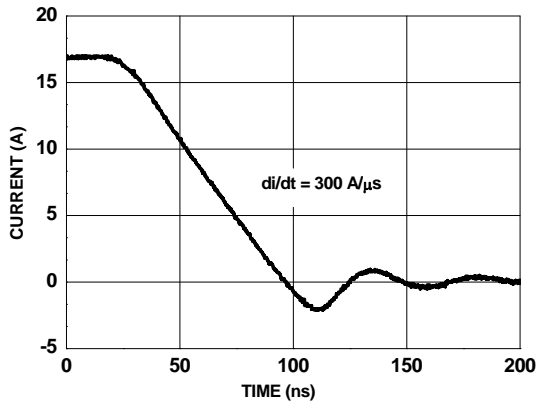


Figure 25. FDMS7602S SyncFET<sup>™</sup> Body Diode Reverse Recovery Characteristic

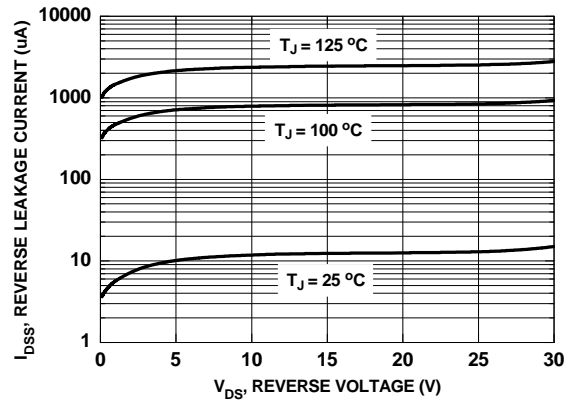
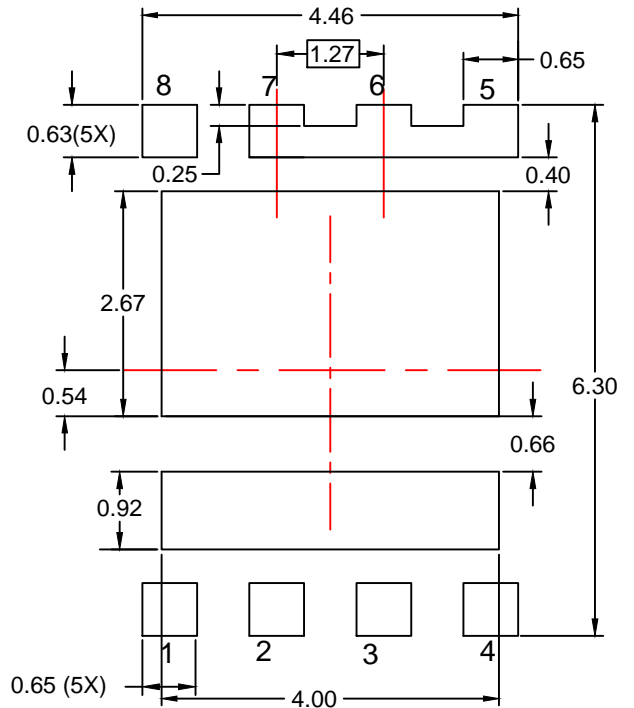
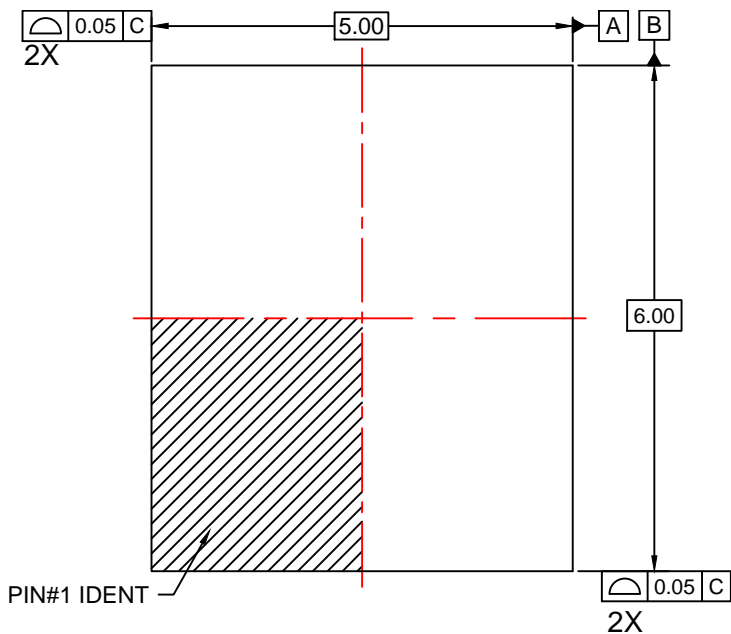
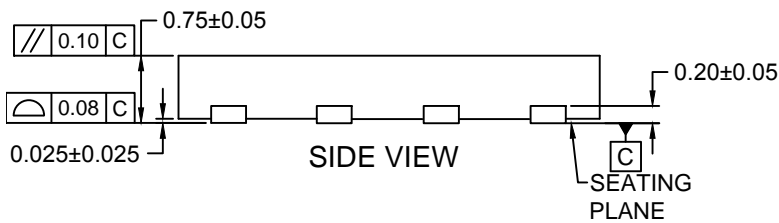


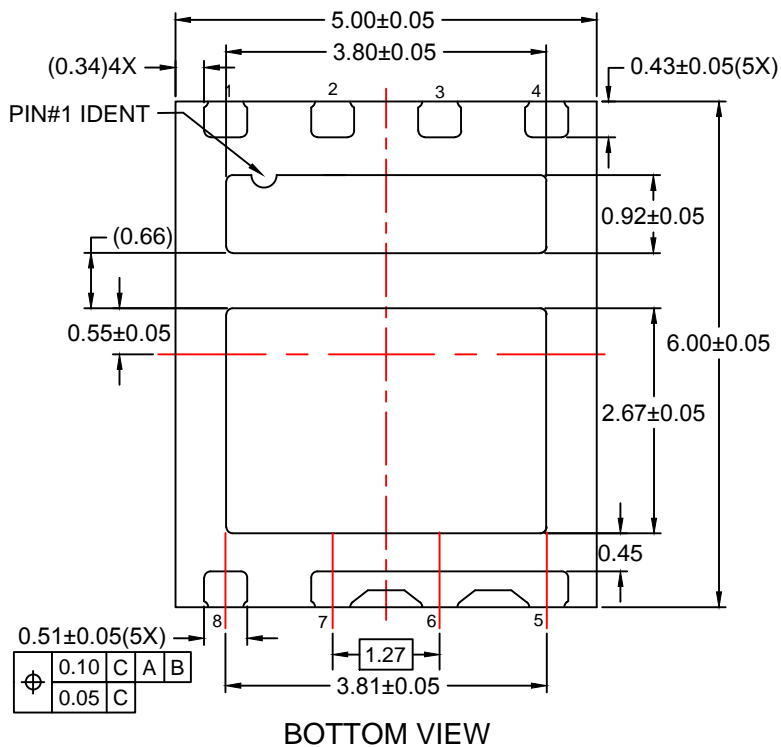
Figure 26. SyncFET<sup>™</sup> Body Diode Reverse Leakage vs. Drain-Source Voltage



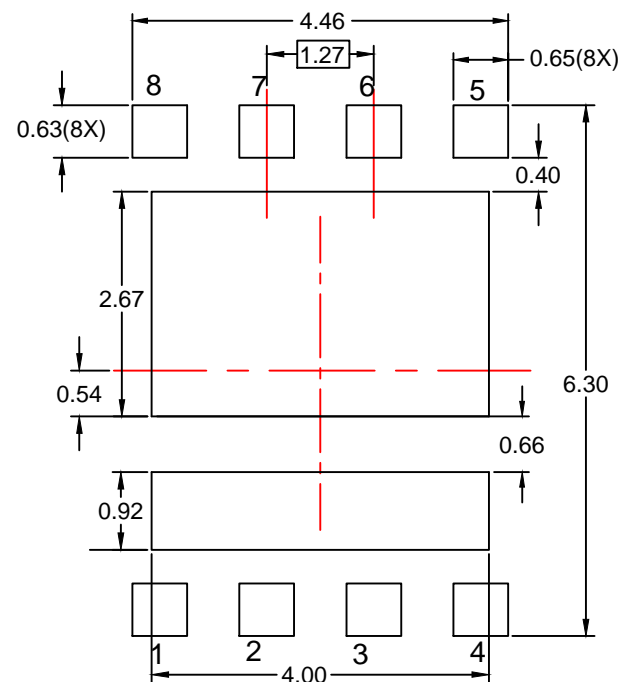
RECOMMENDED LAND PATTERN  
(OPTION 1 - FUSED LEADS 5,6,7)



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN  
(OPTION 2 - ISOLATED LEADS)

**NOTES:**

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Prev2.





### TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	F-PFS™	OPTOPLANAR®	
AttitudeEngine™	FRFET®		TinyBoost®
Awinda®	Global Power Resource™	PowerXS™	TinyBuck®
AX-CAP®*	GreenBridge™	Programmmable Active Droop™	TinyCalc™
BitSiC™	Green FPS™	QFET®	TinyLogic®
Build it Now™	Green FPS™ e-Series™	QS™	TINYOPTO™
CorePLUS™	Gmax™	Quiet Series™	TinyPower™
CorePOWER™	GTO™	RapidConfigure™	TinyPWM™
CROSSVOLT™	IntelliMAX™		TinyWire™
CTL™	ISOPLANAR™	Saving our world, 1mW/W/kW at a time™	TranSiC™
Current Transfer Logic™	Making Small Speakers Sound Louder and Better™	SignalWise™	TriFault Detect™
DEUXPEED®	MegaBuck™	SmartMax™	TRUECURRENT®*
Dual Cool™	MICROCOUPLER™	SMART START™	μSerDes™
EcoSPARK®	MicroFET™	Solutions for Your Success™	
EfficientMax™	MicroPak™	SPM®	UHC®
ESBC™	MicroPak2™	STEALTH™	Ultra FRFET™
	MillerDrive™	SuperFET®	UniFET™
Fairchild®	MotionMax™	SuperSOT™-3	Vcx™
Fairchild Semiconductor®	MotionGrid®	SuperSOT™-6	VisualMax™
FACT Quiet Series™	MTI®	SuperSOT™-8	VoltagePlus™
FACT®	MTX®	SupreMOS®	XST™
FAST®	MVN®	SyncFET™	Xsens™
FastvCore™	mWSaver®	Sync-Lock™	仙童™
FETBench™	OptoHiT™		
FPS™	OPTOLOGIC®		

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I73