

# NL17SZ00

## Single 2-Input NAND Gate

The NL17SZ00 is a single 2-input NAND Gate in three tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

### Features

- Tiny SOT-353, SOT-553 and SOT-953 Packages
- 2.7 ns  $T_{PD}$  at 5 V (typ)
- Source/Sink 24 mA at 3.0 V
- Over-Voltage Tolerant Inputs
- Pin For Pin with NC7SZ00P5X, TC7SZ00FU and TC7SZ00AFE
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- These Devices are Pb-Free and are RoHS Compliant

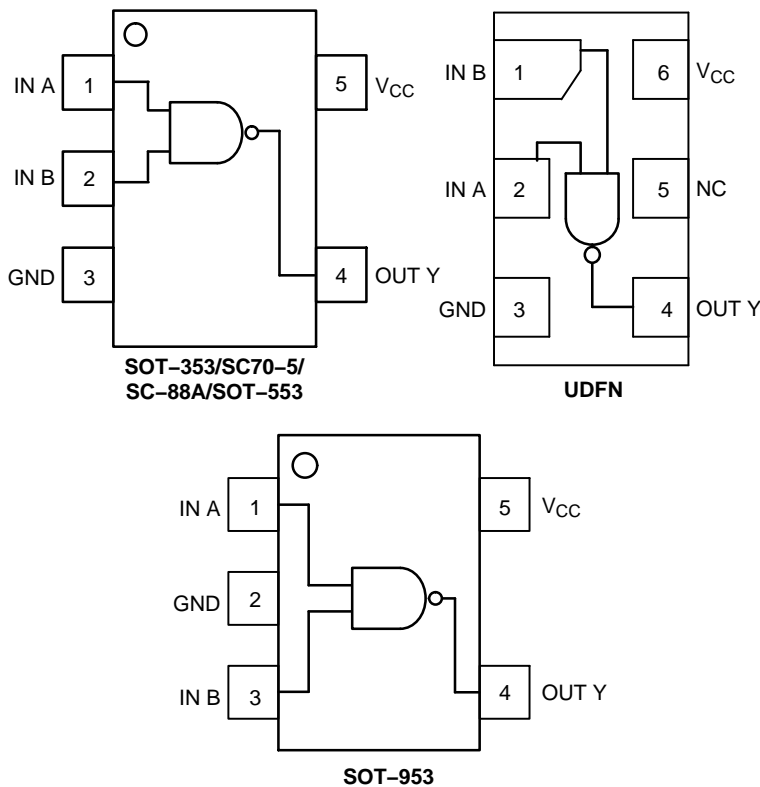


Figure 1. Pinouts (Top View)

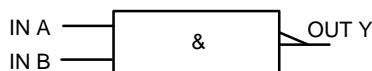


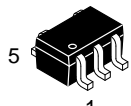
Figure 2. Logic Symbol

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



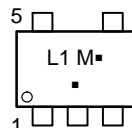
ON Semiconductor®

<http://onsemi.com>




**SOT-353/SC70-5/SC-88A**  
DF SUFFIX  
CASE 419A

### MARKING DIAGRAMS

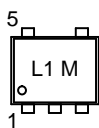



L1 = Specific Device Marking  
M = Date Code\*  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)  
\*Date Code orientation and/or position may vary depending upon manufacturing location.




**SOT-553**  
XV5 SUFFIX  
CASE 463B


L1 = Specific Device Marking  
M = Date Code






**UDFN6**  
1.45 x 1.0  
CASE 517AQ






**UDFN6**  
1.0 x 1.0  
CASE 517BX


X = Specific Device Marking  
M = Date Code





**SOT-953**  
CASE 527AE

T = Specific Device Code  
M = Month Code



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# NL17SZ00

## PIN ASSIGNMENT (SOT-353/ SC70-5/SC-88A/SOT-553/ UDFN)

Pin	Function
1	IN A
2	IN B
3	GND
4	OUT Y
5	V <sub>CC</sub>

## PIN ASSIGNMENT (SOT-953)

Pin	Function
1	IN A
2	GND
3	IN B
4	OUT Y
5	V <sub>CC</sub>

## FUNCTION TABLE

Input		Output Y = AB
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to + 7.0	V
V <sub>IN</sub>	DC Input Voltage	-0.5 to + 7.0	V
V <sub>OUT</sub>	DC Output Voltage (SOT-353/SC70-5/SC-88A/SOT-553/UDFN Packages) Power-Down Mode	-0.5 to + 7.0	V
V <sub>OUT</sub>	DC Output Voltage (SOT-953 Package)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	-50	mA
I <sub>OK</sub>	DC Output Diode Current (SOT-953 Package) V <sub>OUT</sub> < GND, V <sub>OUT</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	DC Output Diode Current (SOT-353/SC70-5/SC-88A/SOT-553 Packages) V <sub>OUT</sub> < GND	-50	mA
I <sub>OUT</sub>	DC Output Current	±50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance SOT-353 (Note 1) SOT-553	350 496	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C SOT-353 SOT-553	186 135	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
ESD	ESD Classification Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	2000 200 N/A	
I <sub>LATCHUP</sub>	Latchup Performance Above V <sub>CC</sub> and Below GND at 125°C (Note 5)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A, rated to EIA/JESD22-A114-B.
3. Tested to EIA/JESD22-A115-A, rated to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

# NL17SZ00

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	1.65	5.5	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage (SOT-353/SC70-5/SC-88A/SOT-553/UDFN Packages)	0	5.5	V
$V_{OUT}$	DC Output Voltage (SOT-953 Package)	0	$V_{CC}$	V
$T_A$	Operating Temperature Range	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 3.0 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	100 20	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$V_{IH}$	High-Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 $V_{CC}$ 0.7 $V_{CC}$			0.75 $V_{CC}$ 0.7 $V_{CC}$		V
$V_{IL}$	Low-Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.25 $V_{CC}$ 0.3 $V_{CC}$		0.25 $V_{CC}$ 0.3 $V_{CC}$	V
$V_{OH}$	High-Level Output Voltage $V_{IN} = V_{IL}$ or $V_{IH}$	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -3 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -16 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	$V_{CC} - 0.1$ 1.29 1.9 2.2 2.4 2.3 3.8	$V_{CC}$ 1.4 2.1 2.4 2.7 2.5 4.0		$V_{CC} - 0.1$ 1.29 1.9 2.2 2.4 2.3 3.8		V
$V_{OL}$	Low-Level Output Voltage $V_{IN} = V_{IH}$ or $V_{OH}$	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 3 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 32 \text{ mA}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
$I_{IN}$	Input Leakage Current	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage Current	$V_{IN} = 5.5 \text{ V}$ or $V_{OUT} = 5.5 \text{ V}$	0			1		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$V_{IN} = 5.5 \text{ V}$ or GND	5.5			1		10	$\mu\text{A}$

## AC ELECTRICAL CHARACTERISTICS $t_R = t_F = 3.0 \text{ ns}$

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay (Figure 3 and 4)	$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	1.65	2.0	5.4	11.4	2.0	12	ns
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	1.8	2.0	4.5	9.5	2.0	10.0	
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	2.5 to 0.2	0.8	3.0	6.5	0.8	7.0	
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	$3.3 \pm 0.3$	0.5	2.4	4.5	0.5	4.7	
		$R_L = 500 \Omega, C_L = 50 \text{ pF}$		1.5	2.4	5.0	1.5	5.2	
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$ $R_L = 500 \Omega, C_L = 50 \text{ pF}$	$5.0 \pm 0.5$	0.5 0.8	2.0 2.4	3.9 4.3	0.5 0.8	4.1 4.5	

# NL17SZ00

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0 \text{ V}$ or $V_{CC}$	> 4	pF
$C_{PD}$	Power Dissipation Capacitance (Note 6)	10 MHz, $V_{CC} = 3.3 \text{ V}$ , $V_I = 0 \text{ V}$ or $V_{CC}$ 10 MHz, $V_{CC} = 5.5 \text{ V}$ , $V_I = 0 \text{ V}$ or $V_{CC}$	25 30	pF

6.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

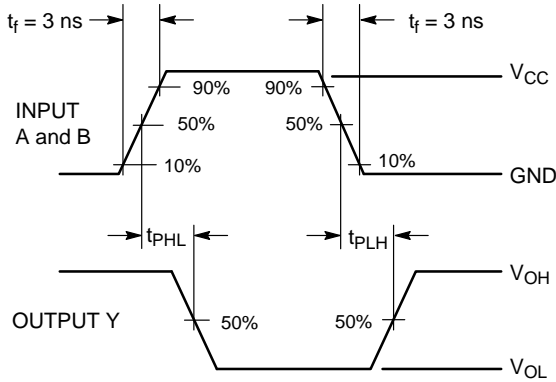
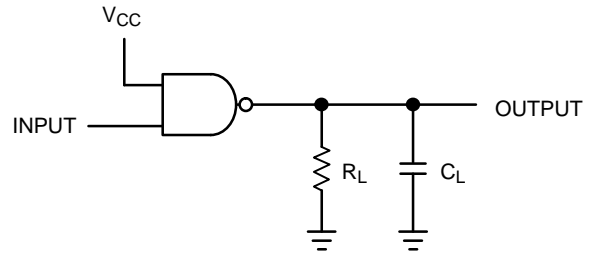


Figure 3. Switching Waveform



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

## DEVICE ORDERING INFORMATION

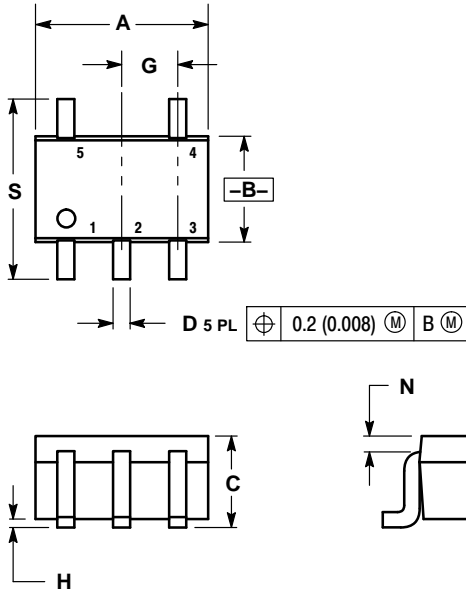
Device Order Number	Package Type	Shipping†
NL17SZ00DFT2G	SOT-353 (Pb-Free)	3000 / Tape & Reel
NL17SZ00XV5T2G	SOT-553 (Pb-Free)	4000 / Tape & Reel
NL17SZ00AMUTCG (In Development)	UDFN6, 1.45 x 1.0 (Pb-Free)	3000 / Tape & Reel
NL17SZ00CMUTCG (In Development)	UDFN6, 1.0 x 1.0 (Pb-Free)	3000 / Tape & Reel
NL17SZ00P5T5G	SOT-953 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NL17SZ00

## PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)  
CASE 419A-02  
ISSUE L

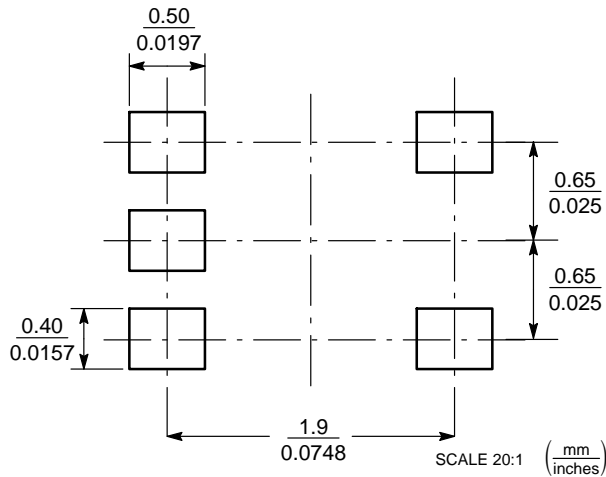


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

### SOLDER FOOTPRINT\*

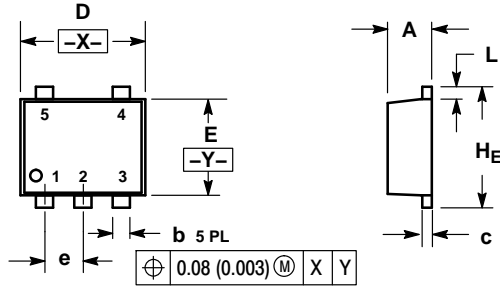


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NL17SZ00

## PACKAGE DIMENSIONS

SOT-553  
XV5 SUFFIX  
CASE 463B  
ISSUE B

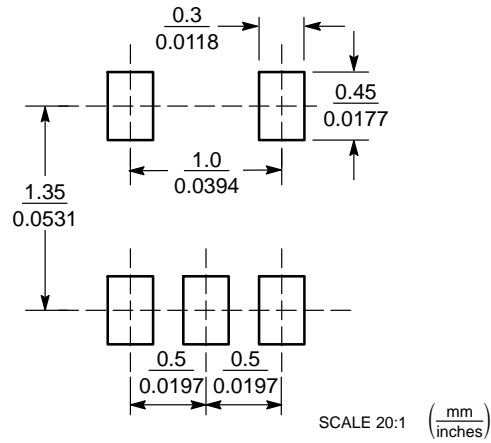


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

### SOLDERING FOOTPRINT\*

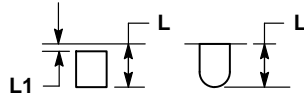
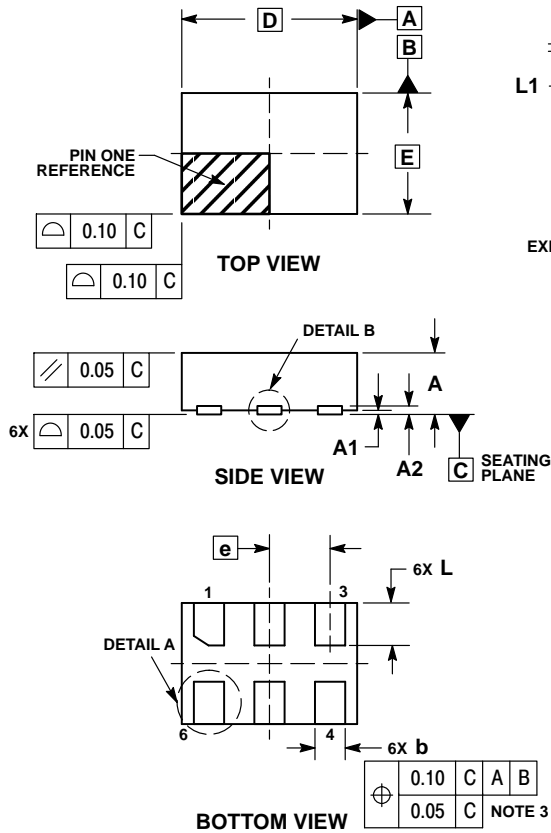


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

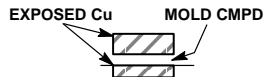
# NL17SZ00

## PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P  
CASE 517AQ  
ISSUE O



**DETAIL A**  
OPTIONAL  
CONSTRUCTIONS



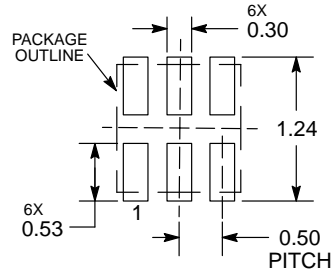
**DETAIL B**  
OPTIONAL  
CONSTRUCTIONS

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

### MOUNTING FOOTPRINT



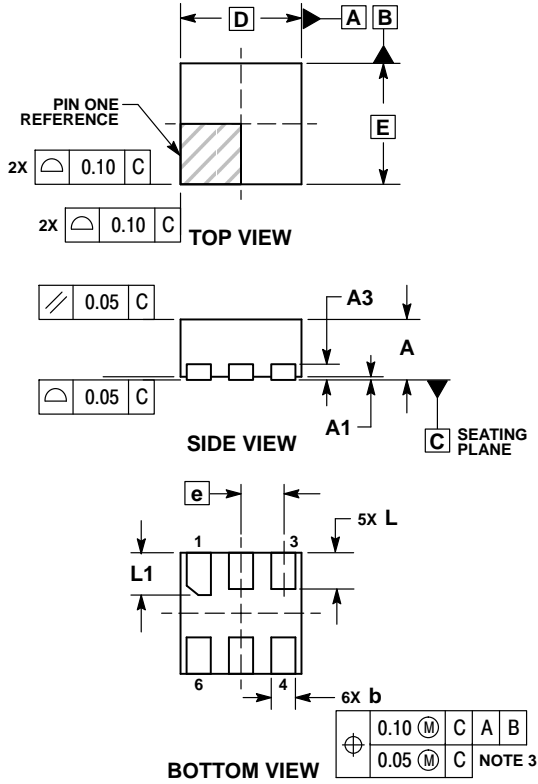
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NL17SZ00

## PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P  
CASE 517BX  
ISSUE O

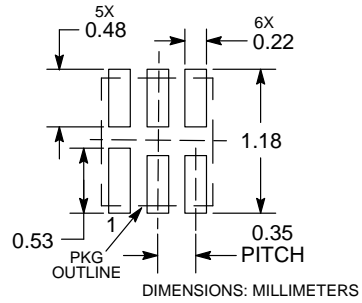


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***



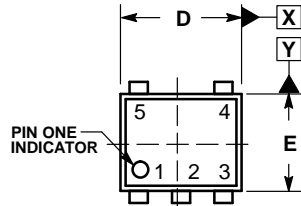
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



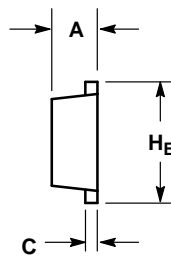
# NL17SZ00

## PACKAGE DIMENSIONS

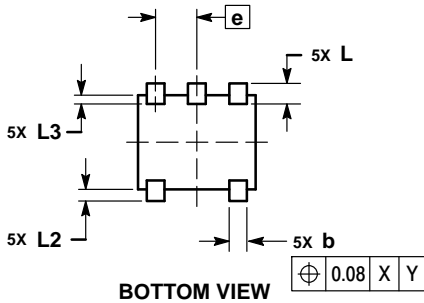
**SOT-953**  
CASE 527AE  
ISSUE E



TOP VIEW



SIDE VIEW



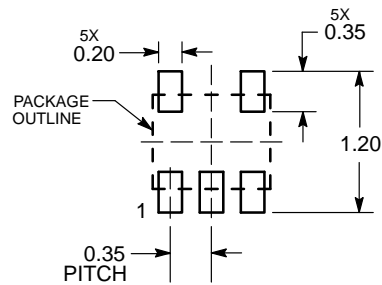
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H <sub>E</sub>	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative