

XMC4500 Satellite-kit: Standard Human Machine Interface Kit

Part Number: KIT_XMC4X_HMI_OLED_001



Features

- Connection to CPU Board via HMI Satellite Connector (80-pin)
- Micro SD Card Slot – 4 bit SD card mode
- Passive Matrix OLED Display, size: 1.54", 160x128 pixel
- 2.5 mm stereo receptacle for audio headsets
- Stereo audio codec TLV320AIC3204
- 2 touch buttons with LED's
- I2C based IO expander with 8 channels
- Single side assembly of all parts
- 2 LEDs indicating power (3.3 Volt, 13 Volt)
- Power supply from CPU-Board via HMI Satellite Connector (80-pin)

PLEASE SEE THE FOLLOWING PAGES FOR USERS MANUAL



Hexagon Application Kit

For XMC4000 Family

CPU_44A-V2

CPU Board XMC4400 General Purpose

Board User's Manual

Revision 1.0, 2013-02-19

Microcontroller

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Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 1.0, 2013-02-19	Initial release

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Introduction

This document describes the features and hardware details of the CPU Board XMC4400 General Purpose (CPU_44A-V2) designed to work with Infineon's XMC4400 Microcontroller. This board is part of Infineon's Hexagon Application Kits.

1 Overview

The CPU board CPU_44A-V2 houses the XMC4400 Microcontroller and three satellite connectors (HMI, COM, ACT) for application expansion. The board along with satellite cards (e.g. HMI_OLED-V1, COM_ETH-V1, AUT_ISO-V1 boards) demonstrates the capabilities of the XMC4400. The main use case for this board is to demonstrate the generic features of the XMC4400 device including tool chain. The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1.1 Key Features

The CPU_44A-V2 board is equipped with the following features

- XMC4400 (ARM® Cortex™-M4-based) Microcontroller, 512 kByte on-chip Flash, LQFP-100
- Connection to satellite cards via the satellite connectors COM, HMI and ACT
- USB OTG Host/Device support via micro USB connector
- Debug options
 - On-board Debugger via the Debug USB connector
 - Cortex Debug connector 10-pin (0.05")
 - Cortex Debug+ETM connector 20-pin (0.05")
- Reset push button
- RGB LED connected to GPIOs P1.10, P1.11 and P5.7
- Boot option switch
- PowerScale Connector: Ready for power consumption analysis
- 7 LED's
 - 3 Power indicating LEDs
 - 2 User LEDs (P5.2 and P1.8)
 - 1 RESET LED
 - 1 Debug LED
- Two User Buttons connected to HIB_IO_0 and P0.10
- Potentiometer, connected to analog input P14.1
- Power supply
 - Via Micro-USB connector in USB device mode
 - Via satellite connector pins (COM/ACT satellites cards can supply power to CPU board)
 - Via Debug USB connector
 - RTC backup battery

1.2 Block Diagram

Figure 1 shows the functional block diagram of the CPU_44A-V2 board. For more information about the power supply please refer to chapter 2.1.

The CPU board has got the following building blocks:

- 3 Satellite Connectors (COM, HMI ACT)
- 2 User LEDs connected to GPIOs P5.2 and P1.8
- 2 User Buttons connected to HIB_IO_0 and P0.10
- RGB LED connected to GPIOs P1.10, P1.11 and P5.7
- 2 Cortex Debug Connectors
- Variable resistor (POTI) connected to GPIO P14.1
- USB On-The-Go Connector (Micro-USB)
- On-board Debugger via Debug USB connector (Micro-USB)

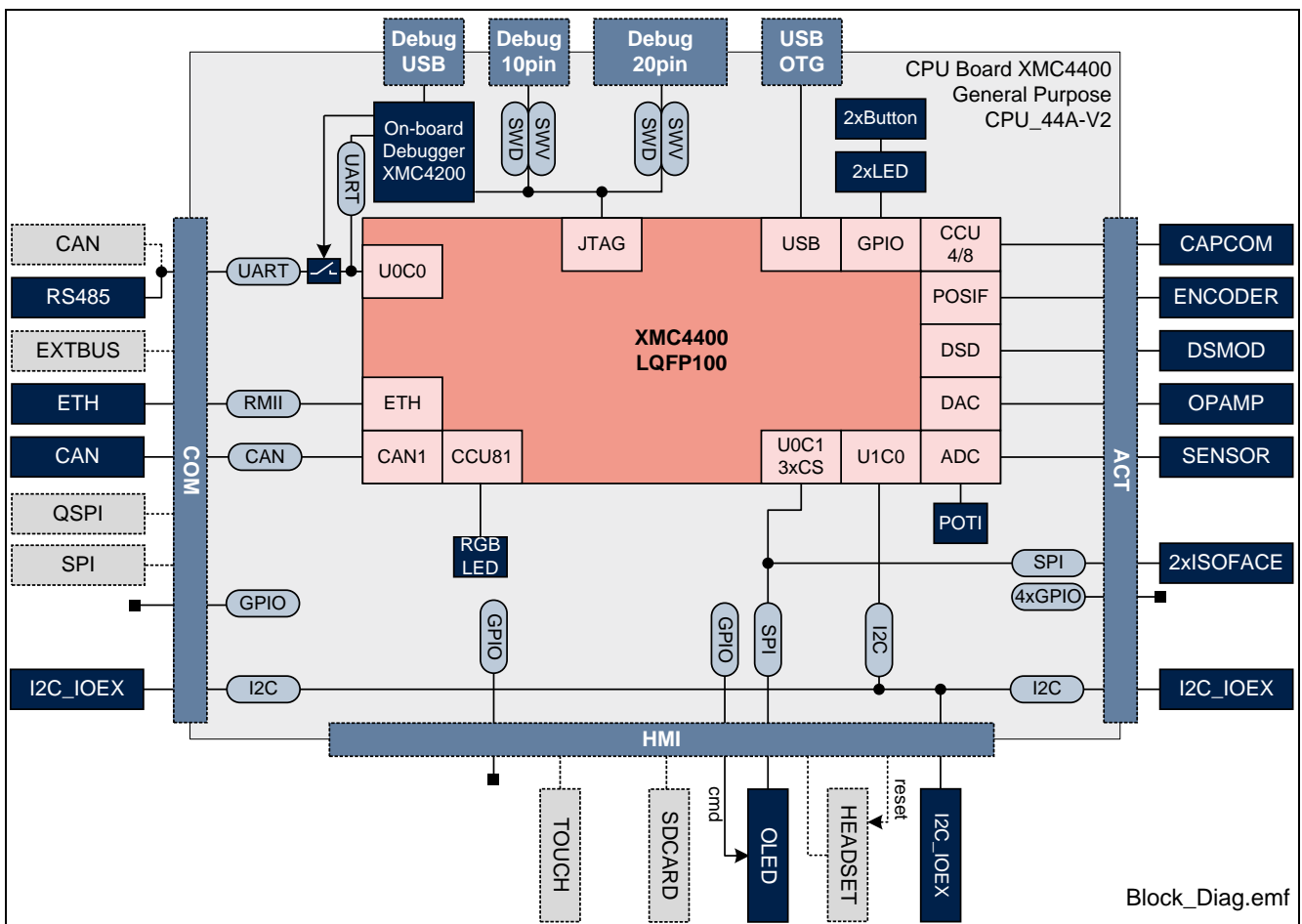


Figure 1 CPU_44A-V2 Board Block Diagram

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

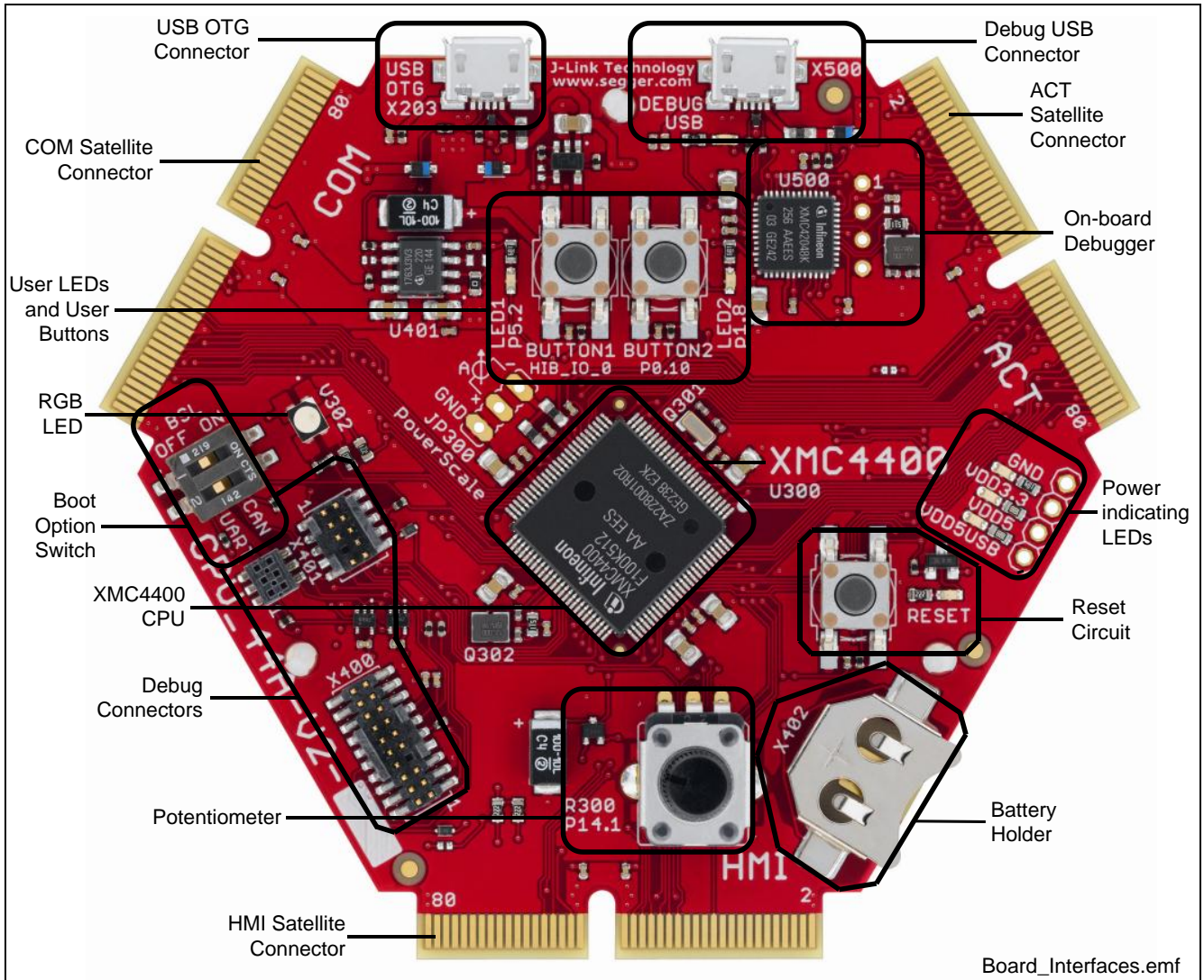


Figure 2 CPU Board XMC4400 General Purpose (CPU_44A-V2)

2.1 Power Supply

The CPU_44A-V2 board can be powered via either of the USB plugs (5 V); however, there is a current limit that can be drawn from the host PC through USB. If the CPU_44A-V2 board is used to drive other satellite cards e.g. MOT_GPDLV-V2 and the total system current required exceeds 500 mA, then the CPU_44A-V2 board needs to be powered by a satellite cards. These satellite cards support external power supply.

The typical current drawn by the CPU board without any satellite cards connected is about 190 mA (@5 V).

For powering the board through an USB interface, connect the USB cable provided with the kit to either of the Micro-USB connector on board as shown in Figure 3.

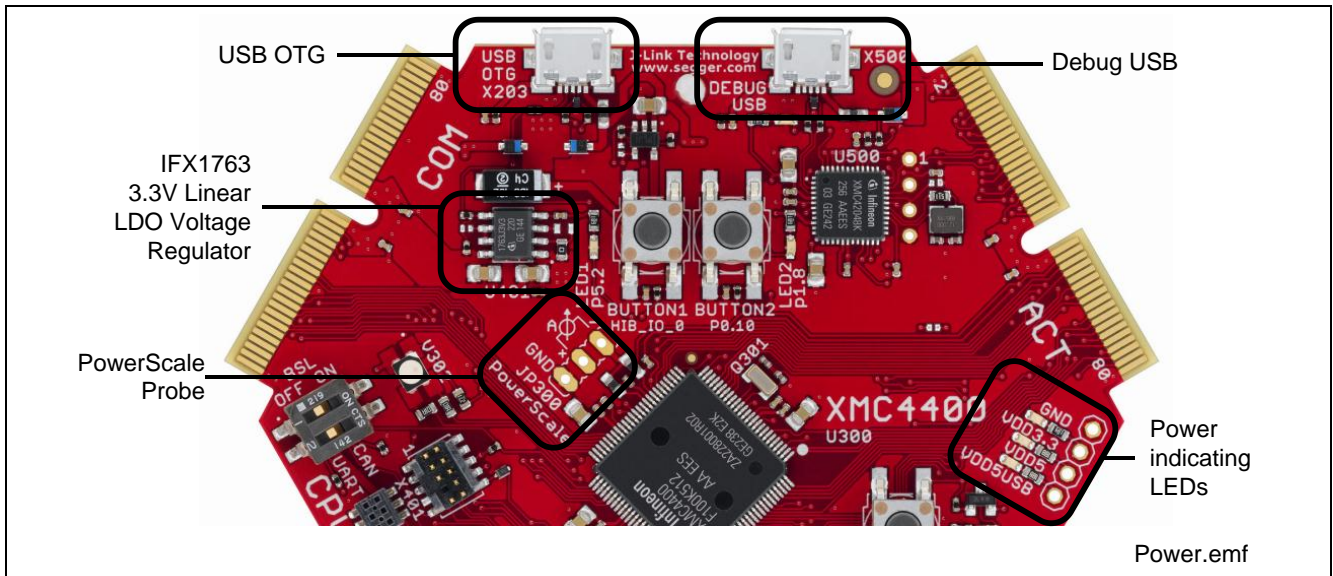


Figure 3 Powering Option

To indicate the power status of the CPU_44A-V2 board three power indicating LED's are provided on board (see Figure 3). The LED will be "ON" when the corresponding power rail is powered.

Table 1 Power status LED's

LED Reference	Power Rail	Voltage	Note
V401	VDD5	5 V	Must always be "ON"
V402	VDD5USB	5 V	"ON" if powered by USB OTG connector X203 "OFF" in all other supply cases
V403	VDD3.3	3.3 V	Must always be "ON"

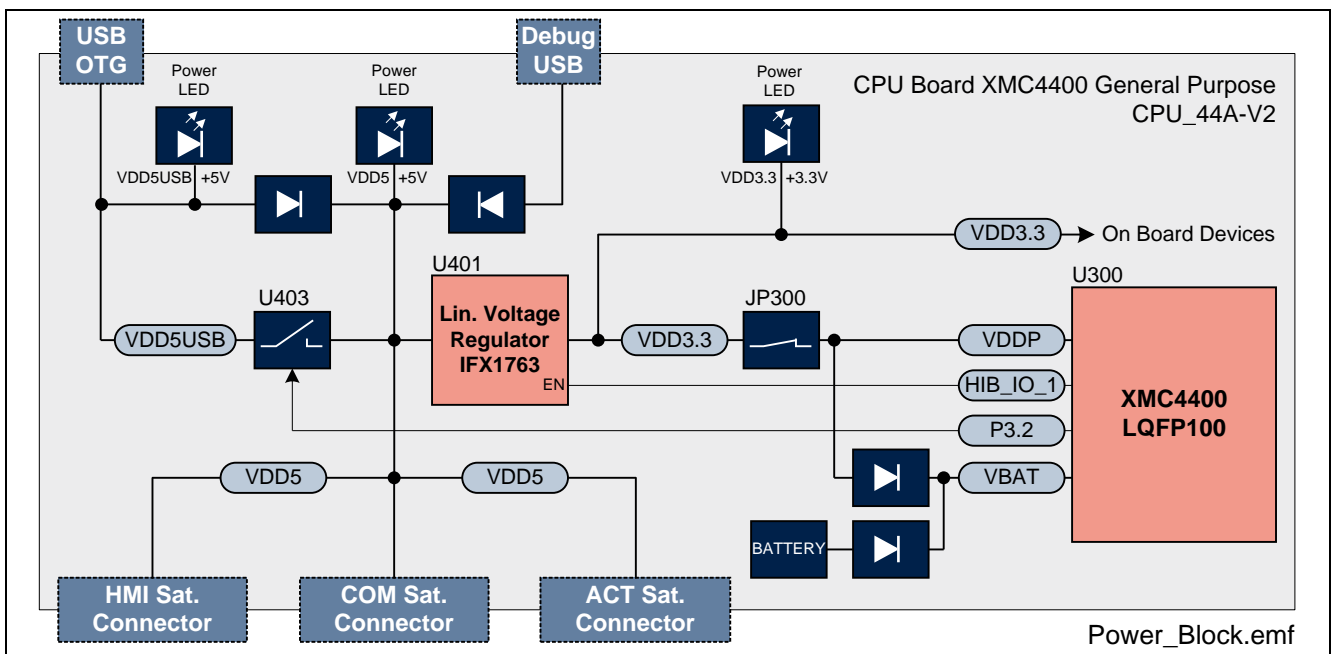


Figure 4 Block Diagram Of Power Supply

Hitex PowerScale probe is provided on the CPU_44A-V2 board to measure the power consumption of the XMC4400 device.

Table 2 Power Measurement

Jumper	Function	Description
JP300	PowerScale	A Hitex PowerScale probe can be connected for current sensing the VDD3.3 (CPU power source). Default: pos. 1-2 (closed) <i>Note: On the PCB there is a shorting trace between pin 1-2. This trace has to be cut first, before using PowerScale. Pin 3 is GND.</i>

2.2 Reset

A reset signal connected to the low-active PORST# pin of the target CPU (U300) can be issued by

- an on-board Reset Button (SW400, RESET)
- an on-board debug device (U500)
- an external debugger connected to either Cortex Debug connector X400 or X401

The RESET signal is routed to all satellite connectors. The reset circuit includes a red LED (V407) to indicate the reset status: The Reset LED (V407) will be "ON" during active reset state and will be "OFF" if reset is not active.

Be aware that PORST# is a bidirectional reset pin of the XMC4000 family which can also be pulled low by the XMC4000 device itself.

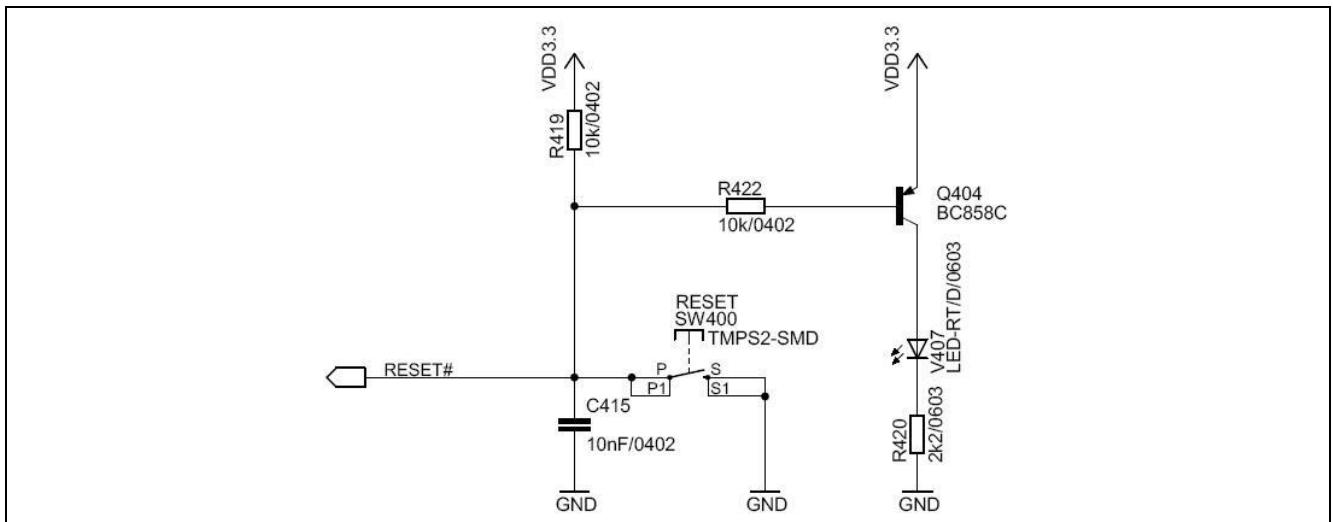


Figure 5 Reset Circuit

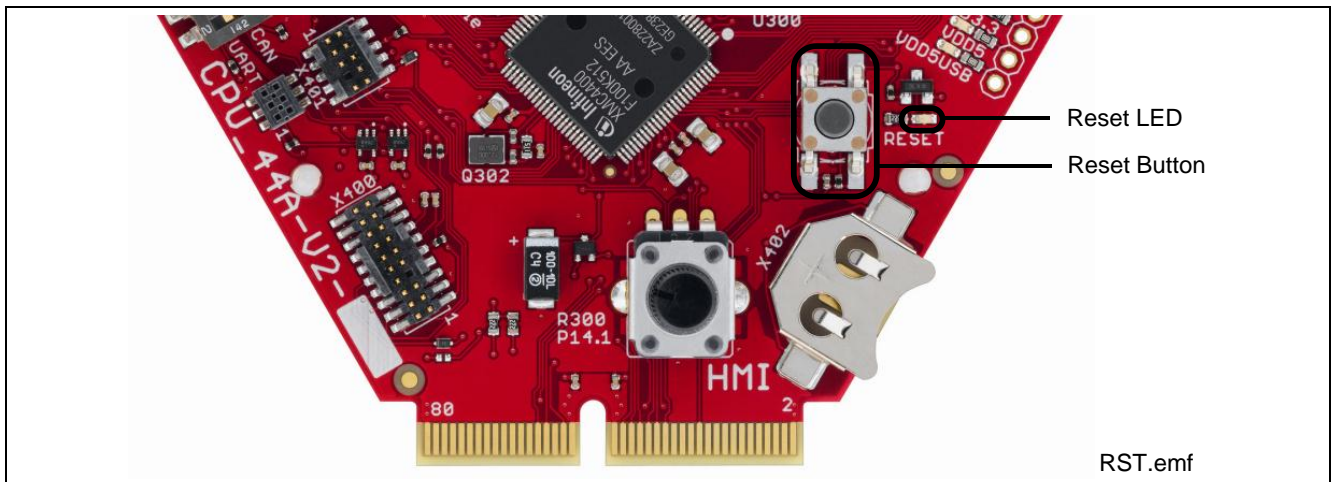


Figure 6 Reset LED and Reset Button

2.3 Clock Generation

An external 12 MHz crystal provides the clock signal to the XMC4400 microcontroller. The drive strength of the oscillator is set to maximum by software, in order to ensure a safe start-up of the oscillator even under worst case conditions. Therefore a serial 510 Ohm resistor will attenuate the oscillations during operations.

For the RTC clock a separate external 32.768 kHz crystal is used on board.

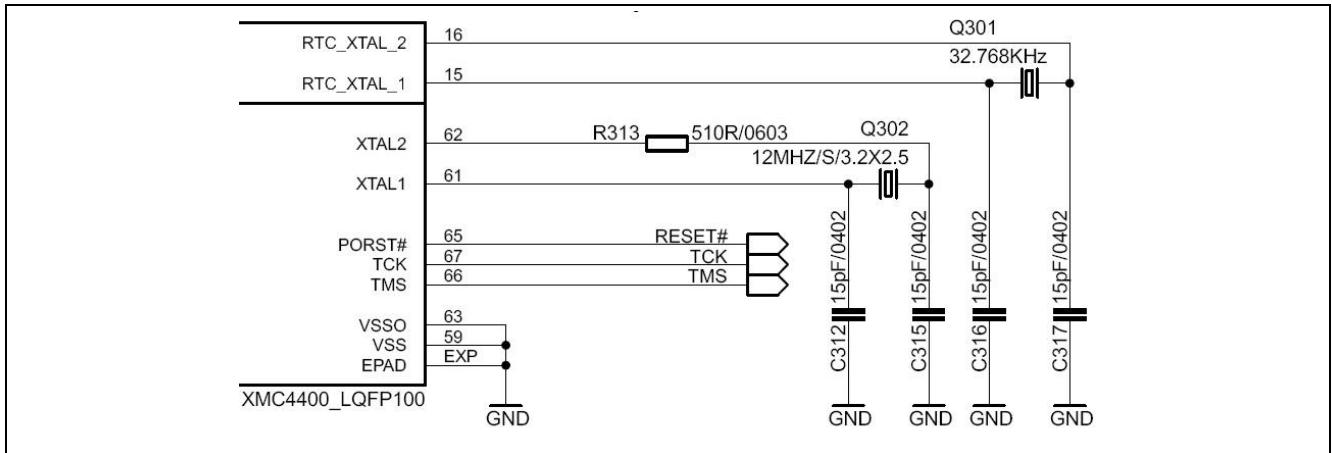


Figure 7 Clock Generation

2.4 Boot Option

During power-on-reset the XMC4400 latches the dip switch SW300 settings via the TCK and the TMS pin. Based on the values latched different boot options are possible.

Table 3 Boot Options Settings

BSL (TMS)	CAN/UART (TCK)	Boot Option
OFF (1)	UART (0)	Normal Mode (Boot from flash)
ON (0)	UART (0)	ASC BSL Enabled (Boot from UART)
OFF (1)	CAN (1)	BMI Customized Boot Enabled
ON (0)	CAN (1)	CAN BSL Enabled (Boot from CAN)

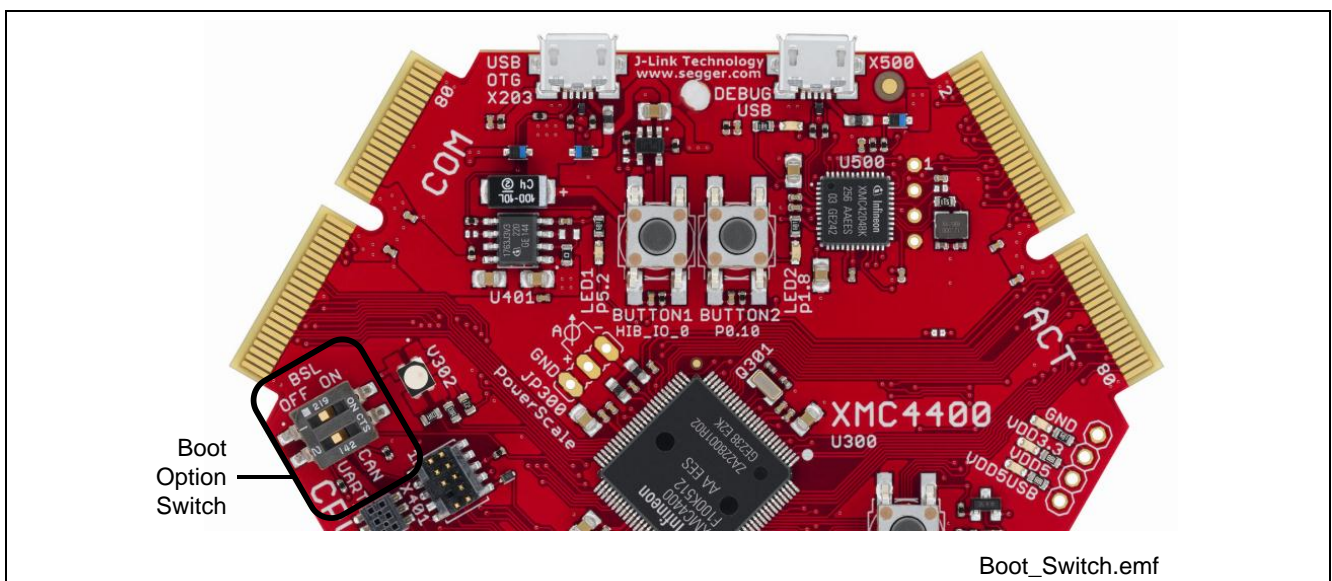


Figure 8 Boot Options Switch

2.5 Debug Interface

The CPU_44A-V2 board supports debugging via 3 different channels:

- On-board Debugger
- Cortex Debug Connector (10-pin)
- Cortex Debug+ETM Connector (20-pin)

The Hexagon Application Boards are designed to use “Serial Wire Debug” as debug interface. JTAG debug is not supported by default because the GPIO P0.7, where the required TDI function is mapped to also, is used by various Actuator boards connected to the ACT satellite connector.

Note: It is strongly recommended not to use JTAG debug mode, especially if satellites boards are connected, which uses the GPIO 0.7. For the same reason also do not use the on-board debugger in JTAG mode.

If you want to use the JTAG debug mode through the cortex debug connectors (X400, X401) anyway, enable the JTAG interface of the XMC device by assembling the pull-up resistor R427 (4k7 Ohm) and the resistor R410 (0 - 33 Ohm).

2.5.2 Cortex Debug Connector (10-pin)

The CPU_44A-V2 board supports Serial Wire Debug operation and Serial Wire Viewer operation (via the SWO signal when Serial Wire Debug mode is used) through the 10-pin Cortex Debug Connector.

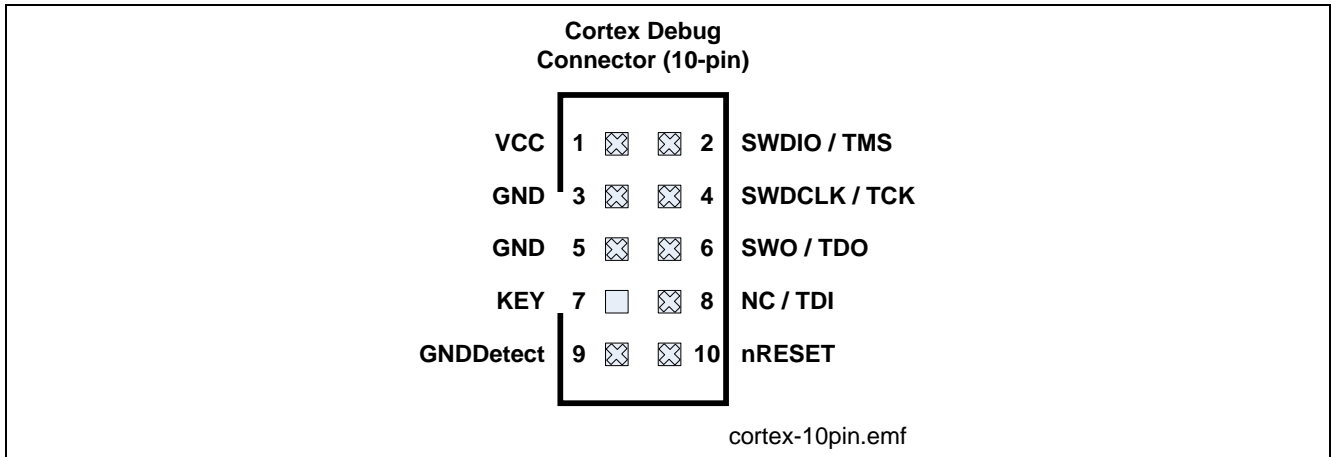


Figure 11 Cortex Debug Connector (10-pin)

Table 4 Cortex Debug Connector (10 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)

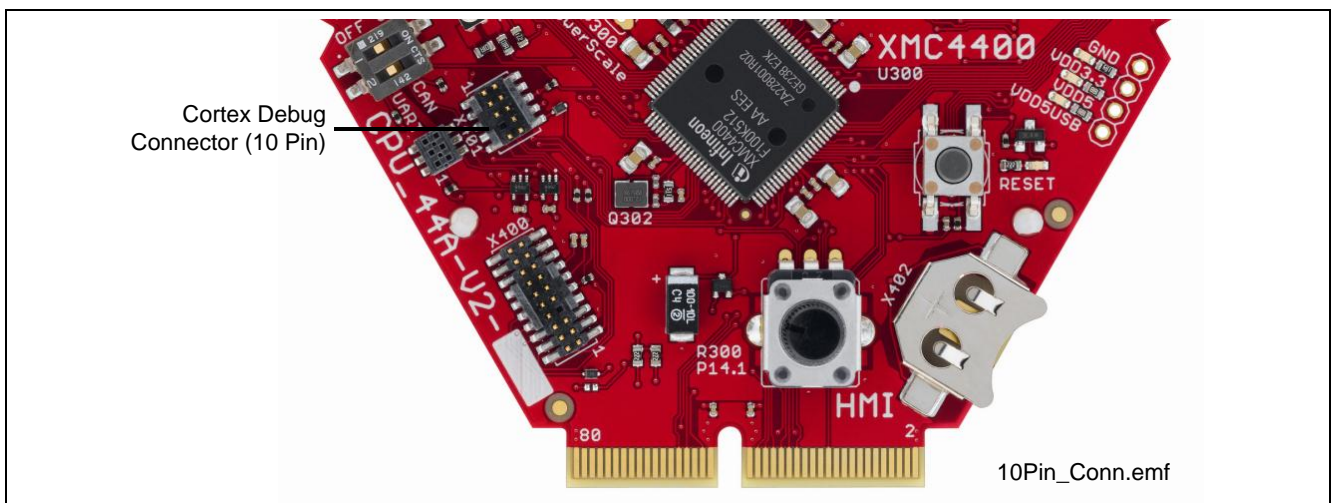


Figure 12 Cortex Debug Connector (10-pin) Layout

2.5.3 Cortex Debug+ETM Connector (20-pin)

The CPU_44A-V2 board supports Serial Wire Debug operation, Serial Wire Viewer operation (via SWO connection when Serial Wire Debug mode is used) through the 20-pin Cortex Debug+ETM Connector. The board does not support the Instruction Trace operation.

JTAG Debug operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the pin P0.7 is used by some Actuator boards connected to the ACT satellite connector.

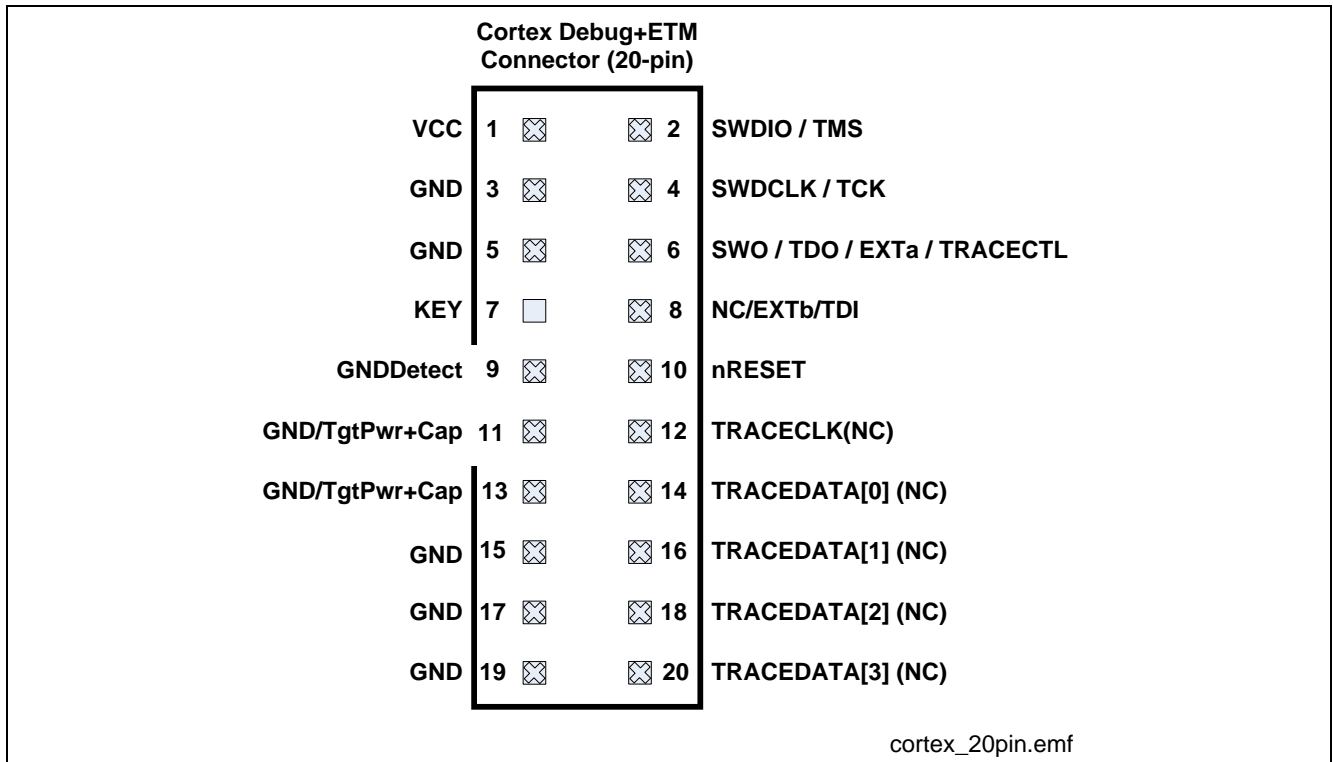


Figure 13 Cortex Debug+ETM Connector (20-pin)

Table 5 Cortex Debug+ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)
11	GND/TgtPwr+Cap	Ground	Ground
12	TRACECLK*	TRACECLK*	TRACECLK*
13	GND/TgtPwr+Cap	Ground	Ground
14	TRACEDATA[0]*	TRACEDATA[0]*	TRACEDATA[0]*
15	GND	Ground	Ground

Table 5 Cortex Debug+ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
16	TRACEDATA[1]*	TRACEDATA[1]*	TRACEDATA[1]*
17	GND	Ground	Ground
18	TRACEDATA[2]*	TRACEDATA[2]*	TRACEDATA[2]*
19	GND	Ground	Ground
20	TRACEDATA[3]*	TRACEDATA[3]*	TRACEDATA[3]*

Note: * Not connected on the CPU_44A-V2 board.

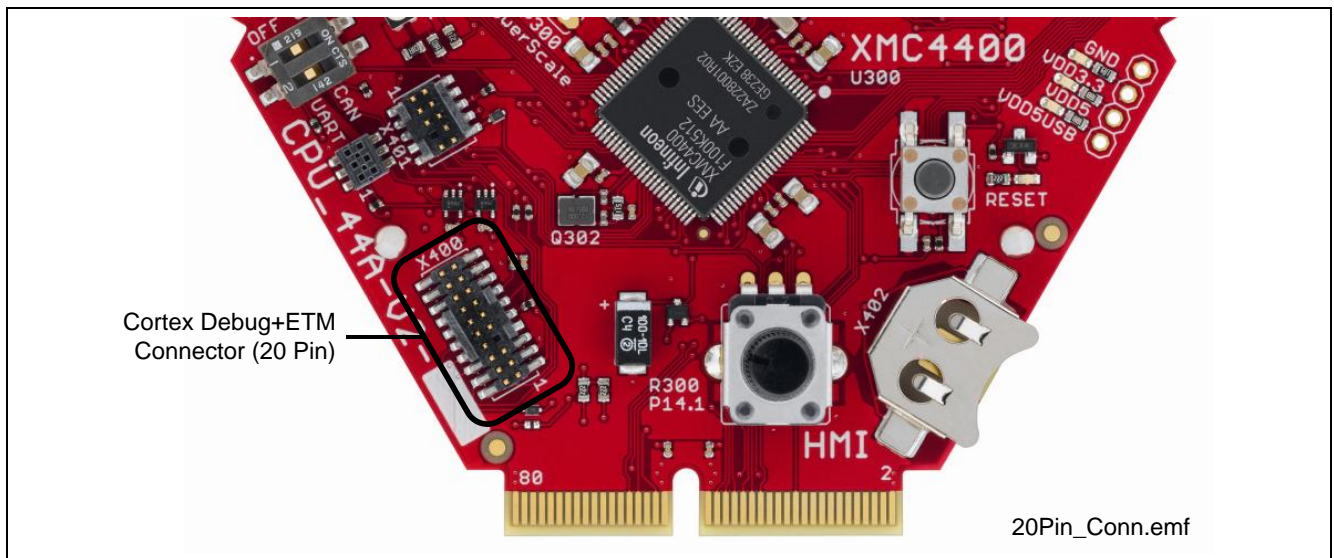


Figure 14 Cortex Debug+ETM Connector (20-pin) Layout

2.6 RGB LED

The CPU_44A-V2 board has a tricolored LED. The LED glows with either Red/Blue/Green colors as controlled by the GPIO pins given below.

Table 6 RGB LED Connections

Pin No. / Function	LED Color
P5.7 / CCU81.OUT02	RED
P1.11 / CCU81.OUT11	GREEN
P1.10 / CCU81.OUT21	BLUE

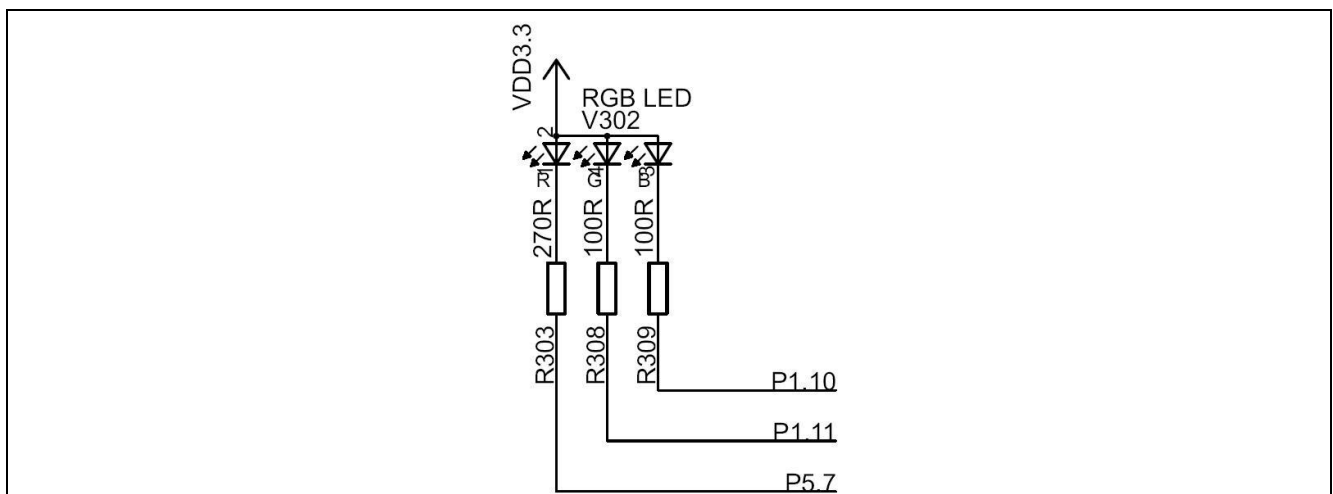


Figure 15 RGB LED

2.7 USB

The XMC4400 supports USB interface in host only mode, device only mode or as an OTG Dual Role Device (DRD). In USB device mode, power is expected through VBUS (pin 1 of X203C) from an external host (e.g. PC). When the current consumption of the application running on the Hexagon Application system is higher than 500 mA, power from an external source through satellite cards shall be used.

Note: Some PCs, notebooks or hubs have a weak USB supply which is not sufficient for proper supply. In this case use an external 5 Volt power supply or a powered USB hub.

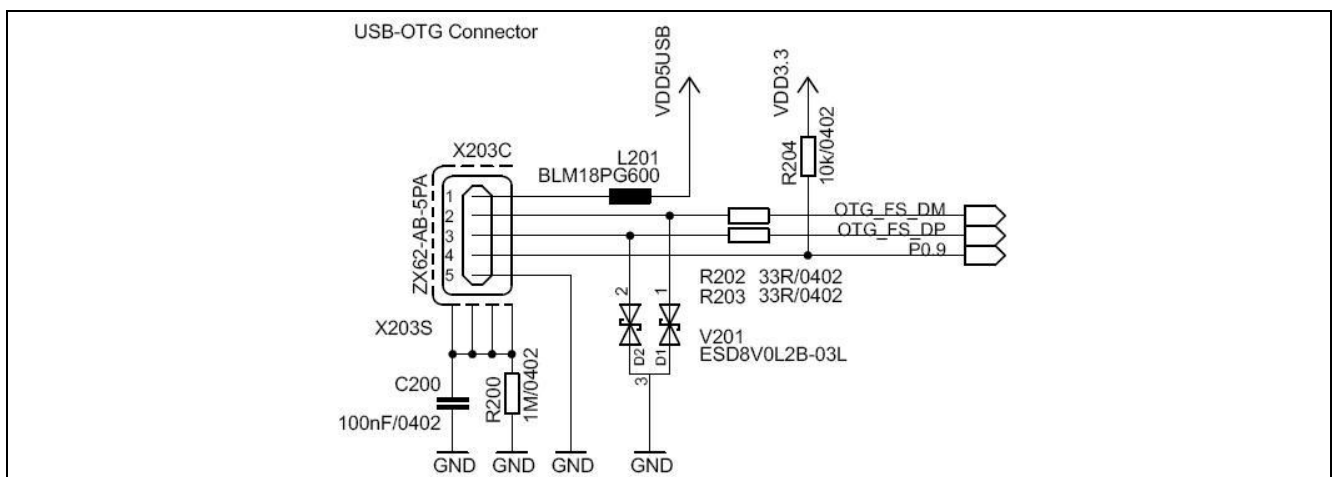


Figure 16 USB Connector

USB ID pin of the USB connector (pin 4 of X203C) is connected to the port pin P0.9 of the XMC4400. On this port pin the USD identification signal (USB.ID) of XMC4000 USB module is mapped to. An OTG device will detect whether a USB Micro-A or Micro-B plug is inserted by checking the ID pin. When the ID = FALSE a Micro-A connector is plugged in and when ID = TRUE a Micro-B connector is plugged in. When the ID is true the XMC4400 acts as a USB host else as a USB device.

Table 7 USB micro AB connector Pinot

Pin No.	Pin Name	Pin Description
1	VBUS	5 V
2	D-	Data Minus
3	D+	Data Plus
4	ID	Identification
5	GND	Ground

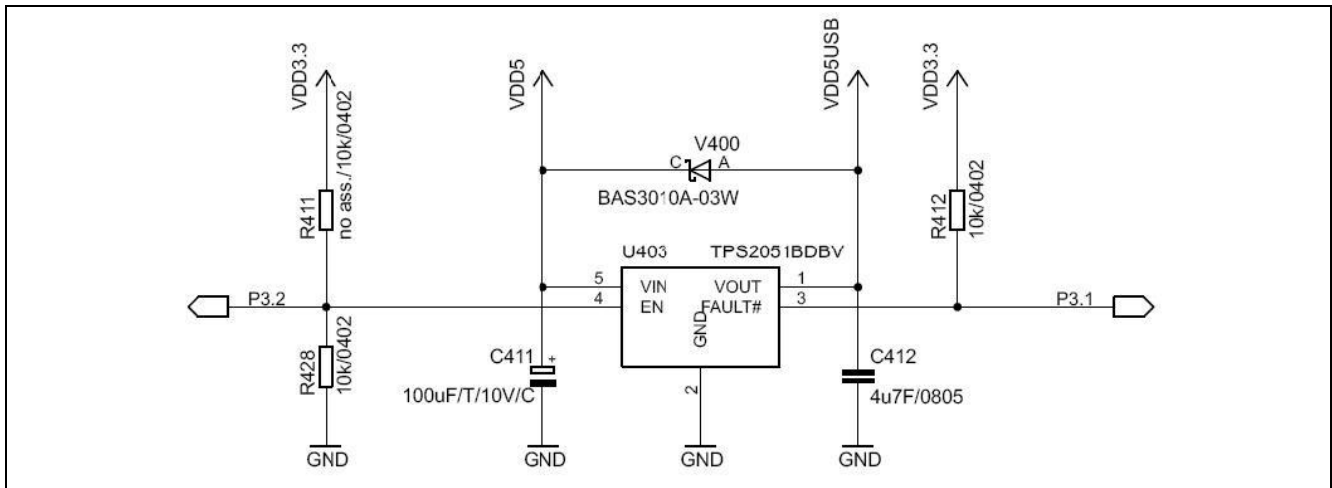


Figure 17 USB power generation - Host/OTG mode

In the host only mode and OTG mode the CPU_44A-V2 board is capable of supplying power to the connected device (e.g. USB mouse). The board has a power-switch which is controlled by the USB.BUSDRIVE signal of the XMC4400. The USB.BUSDRIVE signal is mapped to port pin P3.2 (active high).

In the Host/OTG mode a low active FAULT signal indicates to the port pin P3.1 of the XMC4400, if more than 500 mA current is drawn by the external device.

Diode V400 will allow powering the board through USB in all USB modes via e.g. a PC.

2.8 RTC

The XMC4400 CPU has two power domains, the Core Domain and Hibernate Domain.

The Core Domain (VDDP pins) is connected to the VDD3.3 rail. An on-board LDO voltage regulator generates VDD3.3 (3.3 V) from VDD5 (5 V).

The Hibernate Domain is powered via the auxiliary supply pin VBAT, which is supplied by either a 3 V coin cell (size 1216, 1220, 1225) plugged into the battery holder or 3.3 V (VDD3.3) generated by the on-board voltage regulator.

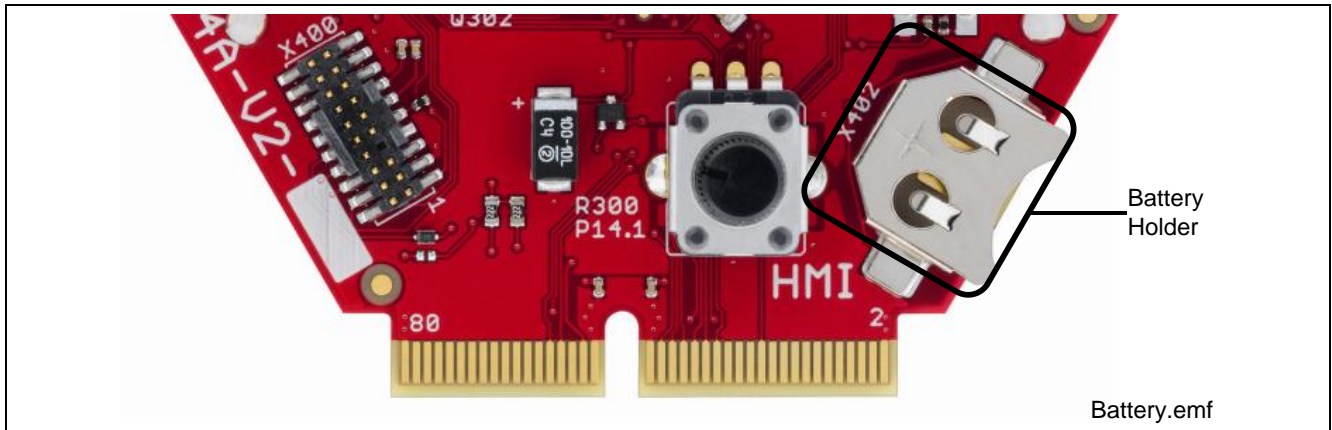


Figure 18 Battery Holder for Coin Cells

The Real Time Clock (RTC) is located in the hibernate domain. The XMC4400 uses the HIB_IO_1 signal (active low) to shut down the external LDO voltage regulator which generates the VDD3.3 (Core Domain). Even if the Core Domain is not powered the Hibernate Domain will operate if VBAT is available. The RTC keeps running as long as the Hibernate Domain is powered via the auxiliary supply VBAT. The RTC is capable to wake-up the whole system from Hibernate mode by setting HIB_IO_1 to high.

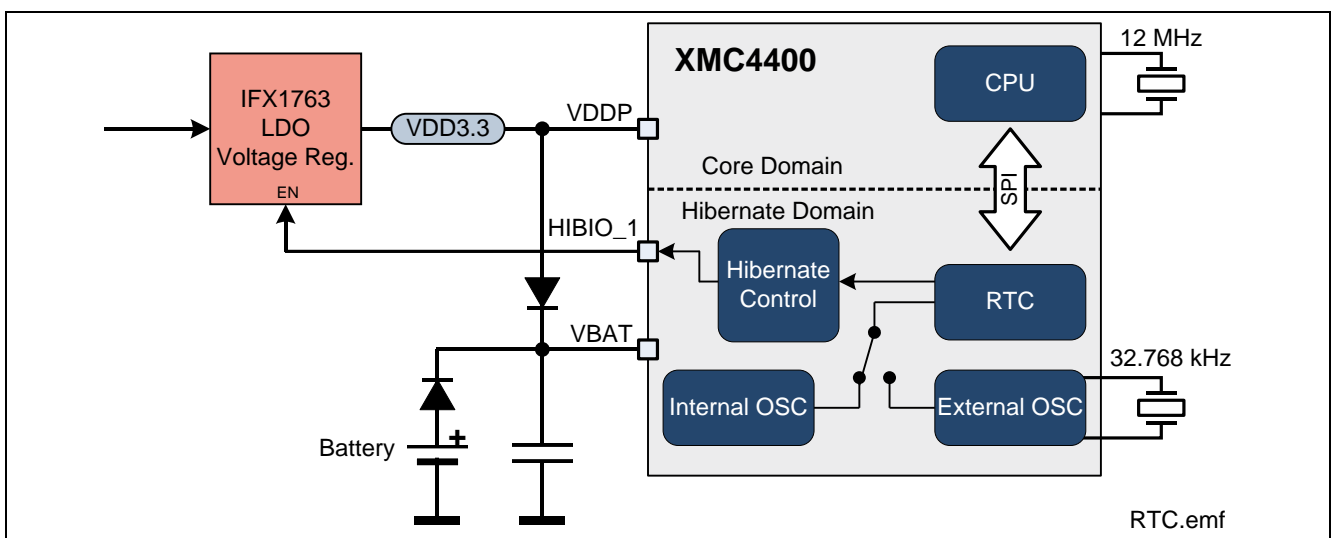


Figure 19 XMC4400 Power Domains and Real Time Clock

2.9 User LEDs and User Buttons

The port pins P5.2 and P1.8 of the XMC4400 are connected to the LEDs V300 and V301 respectively. More User LED's are available through the I2C GPIO expander on most of the satellite cards.

Table 8 User LEDs

LED	Connected to Port Pin
V300	GPIO P5.2
V301	GPIO P1.8

Two User Buttons, SW301 and SW302 are connected to P0.10 and HIB_IO_0 of XMC4400.

Table 9 User Buttons

Button	Connected to Port Pin
BUTTON1 / SW301	HIB_IO_0
BUTTON2 / SW302	P0.10

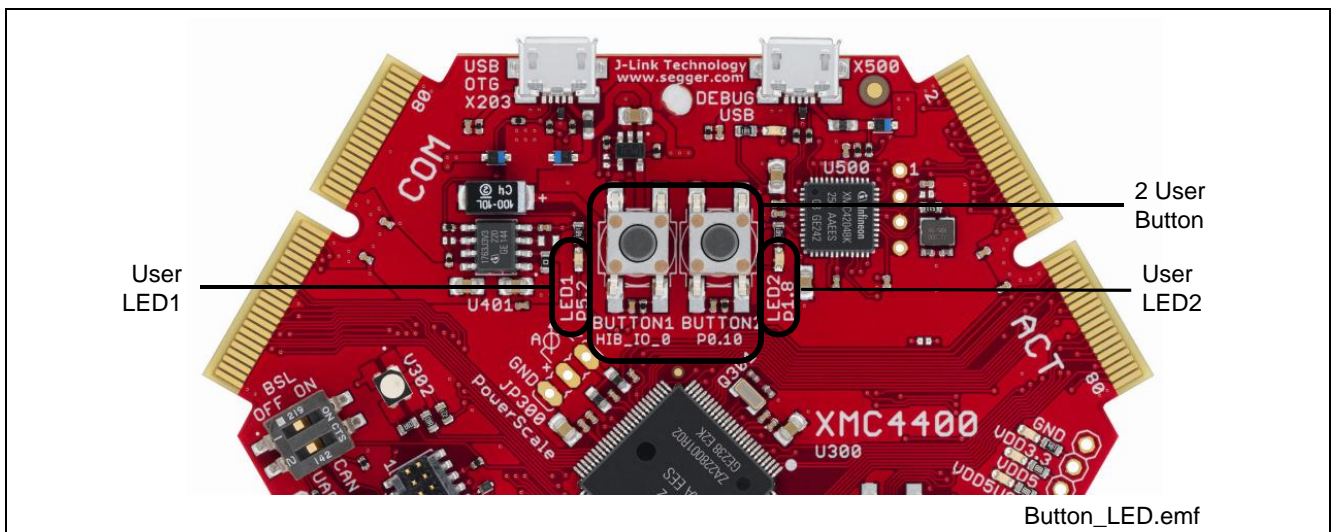


Figure 20 User LEDs and User Buttons

2.10 Potentiometer

The CPU_44A-V2 board provides a potentiometer POT1 for ease of use and testing of the on-chip analog to digital converter. The potentiometer is connected to the analog input G0_CH1 (P14.1). The analog output of the potentiometer ranges from 0 V to 3.3 V.

Table 10 Potentiometer

Potentiometer	Connected to Port Pin
R300	P14.1 / G0_CH1 (Group 0, channel 1)

2.11 Satellite Connectors

The CPU_44A-V2 board provides three satellite connectors for application extension by satellite cards:

- COM satellite connector (Communication)
- HMI satellite connector (Human Machine Interface)
- ACT satellite connector (Actuator)

Note: Satellite cards shall be connected to their matching satellite connectors only. (For e.g. COM satellite cards shall be connected to COM satellite connector only)

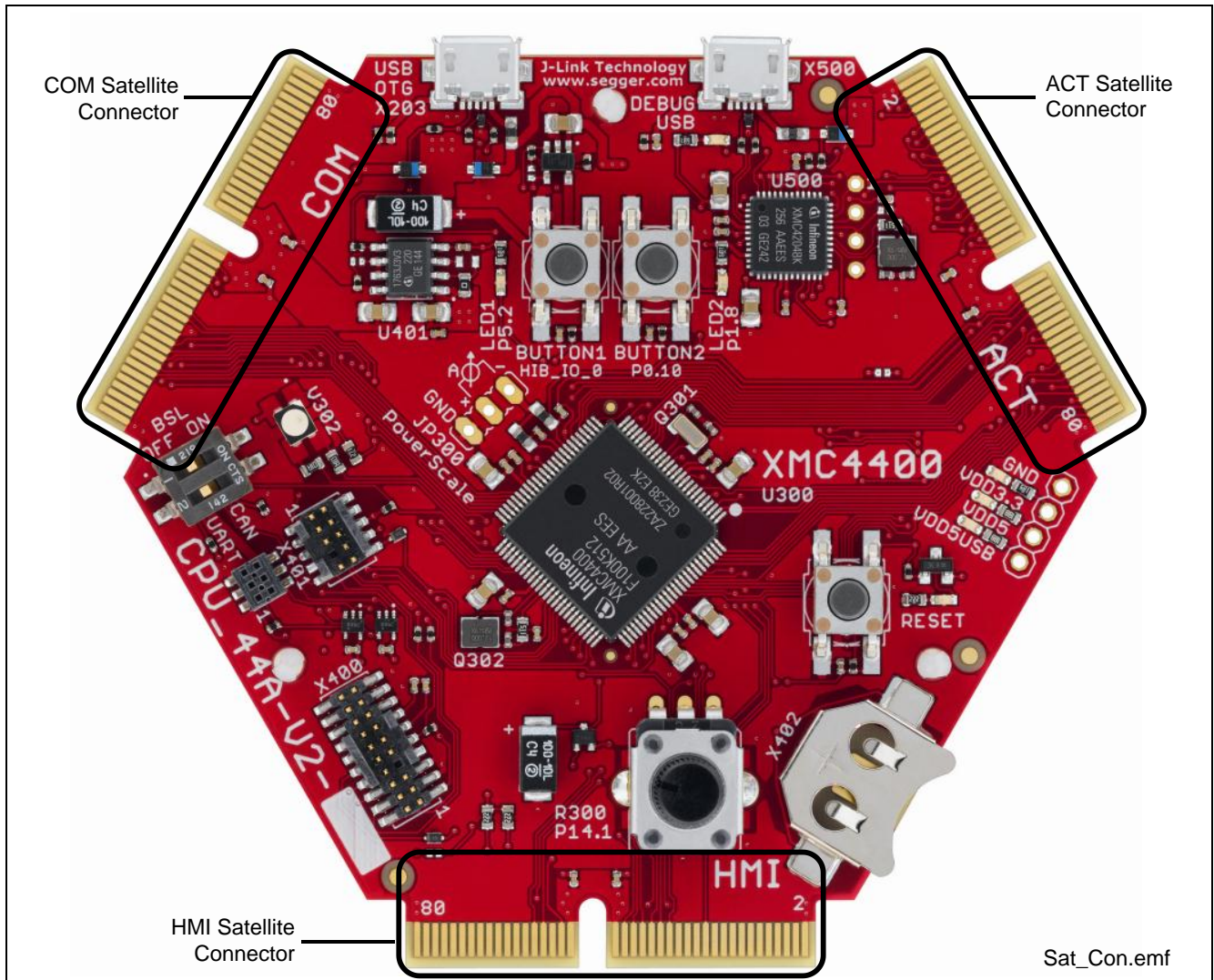


Figure 21 Satellite Connectors

2.11.1 COM Connector

The COM satellite connector on the CPU_44A-V2 board allows interface expansion through COM satellite cards (e.g. COM_ETH-V1)

CPU_44A-V2		Satellite Connector		CPU_44A-V2	
XMC Pin	XMC Function	Pin	Function	XMC Pin	XMC Function
		COM			
		1	GND		VSS
		2	GND		GND
		3	qSPI_D0		nc
		4	qSPI_D1		nc
		5	qSPI_CS		nc
		6	qSPI_D2		nc
		7	qSPI_D3		nc
		8	qSPI_CS		nc
		9	RSVD		nc
		10	RSVD		nc
		11	RSVD		nc
		12	RSVD		nc
		13	ETH_RMII		P2.3
		14	ETH_RMII		P2.2
		15	ETH_RMII		P2.0
		16	ETH_RMII		P2.7
		17	ETH_RMII		P2.5
		18	ETH_RMII		nc
		19	ETH_RMII		nc
		20	ETH_RMII		nc
		21	ETH_RMII		nc
		22	ETH_RMII		nc
		23	ETH_RMII		nc
		24	GND		VSS
		25	RSVD		nc
		26	RSVD		nc
		27	CAN_TXD		P1.12
		28	CAN_TXD		P1.4
		29	CAN_RXD		nc
		30	CAN_RXD		nc
		31	SPI_MTSR		nc
		32	SPI_MTSR		nc
		33	SPI_MRST		nc
		34	SPI_MRST		nc
		35	SPI_SCLK		nc
		36	SPI_SCLK		nc
		37	I2C_SCL		P0.11
		38	I2C_SCL		P0.6
		39	GPIO		RESET#
		40	GPIO		RESET#
		41	RESET		RESET#
		42	RESET		RESET#
		43	VDD5		VDD5
		44	VDD5		VDD5
		COM			
		45	VDD5		nc
		46	VDD5		nc
		47	EBU_ADV		nc
		48	EBU_ADV		nc
		49	EBU_WR		nc
		50	EBU_RD		nc
		51	EBU_RD		nc
		52	EBU_AD		nc
		53	EBU_AD		nc
		54	EBU_AD		nc
		55	EBU_AD		nc
		56	EBU_AD		nc
		57	EBU_CS		nc
		58	EBU_CS		nc
		59	EBU_CS		nc
		60	EBU_CS		nc
		61	GND		VSS
		62	GND		GND
		63	EBU_A		nc
		64	EBU_A		nc
		65	EBU_A		nc
		66	EBU_A		nc
		67	EBU_A		nc
		68	EBU_A		nc
		69	EBU_A		nc
		70	EBU_A		nc
		71	EBU_A		nc
		72	EBU_A		nc
		73	EBU_A		nc
		74	EBU_A		nc
		75	EBU_A		nc
		76	EBU_A		nc
		77	EBU_A		nc
		78	EBU_A		nc
		79	GND		VSS
		80	GND		GND
		COM			

Figure 22 Satellite Connector Type COM

2.11.2 HMI Connector

The HMI satellite connector on the CPU_44A-V2 board allows interface expansion through HMI satellite cards.

CPU_44A-V2		Satellite Connector		CPU_44A-V2	
XMC Pin	XMC Function	Pin	Function	XMC Pin	XMC Function
VSS	GND	HMI 1	GND	VSS	VSS
nc	nc	2	MMC_CLK	nc	nc
nc	nc	3	MMC_rRST	nc	nc
nc	nc	4	MMC_DATA0	nc	nc
nc	nc	5	MMC_DATA1	nc	nc
nc	nc	6	MMC_DATA2	nc	nc
nc	nc	7	MMC_DATA3	nc	nc
nc	nc	8	MMC_DATA4	nc	nc
nc	nc	9	MMC_DATA5	nc	nc
nc	nc	10	MMC_DATA6	nc	nc
nc	nc	11	MMC_DATA7	nc	nc
nc	nc	12	MMC_CMD	nc	nc
nc	nc	13	MMC_BUSPOW	nc	nc
nc	nc	14	MMC_nSDCD	nc	nc
nc	nc	15	MMC_LED	nc	nc
nc	nc	16	MMC_SDWC	nc	nc
nc	nc	17	RSVD	nc	nc
nc	nc	18	RSVD	nc	nc
nc	nc	19	RSVD	nc	nc
nc	nc	20	RSVD	nc	nc
nc	nc	21	RSVD	nc	nc
nc	nc	22	RSVD	nc	nc
nc	nc	23	AudioRST	P0.12/OLED_RS	P0.12/OLED_RS
nc	nc	24	OLED_CMD	nc	nc
nc	nc	25	I2S_WA	I2S_MTSR	nc
nc	nc	26	I2S_MCLK	I2S_MTSR	nc
nc	nc	27	I2S_SYNCCLK	I2S_MRST	nc
nc	nc	28	I2S_SYNCCLK	I2S_SCLK	nc
P1.13	U0C1_SEL03	29	SPI_CSH0	SPI_MTSR	U0C1_DOUT0 P3.5
nc	nc	30	SPI_CSH1	SPI_MTSR	U0C1_DX0E P4.0
nc	nc	31	SPI_CSH2	SPI_SCLK	U0C1_SCLKOUT P3.6
nc	nc	32	I2C_SDA	I2C_SCL	U1CO_SCLKOUT P0.11
P2.14	U1CO_DX0D/DOUT0	33	HMI_GPIO1	GPIO	P0.6
nc	nc	34	HMI_GPIO0	RESET	RESET#
nc	nc	35	VDD5	VDD5	PORST
VAGND	AGND	HMI 45	VDD5	VDD5	VAREF
nc	nc	46	AGND	AREF	VAREF
nc	nc	47	DAC0/ADC1	DAC1/ADCO	nc
nc	nc	48	ADC3/ORCO	ADC2/DACREF	nc
nc	nc	49	ADC15	ADC14	VADC_G0CH4 P14.4
P14.12	VADC_G1CH4	50	ADC17	ADC16	VADC_G0CH3 P14.3
nc	nc	51	ADC19	ADC18	nc
nc	nc	52	RSVD	RSVD	nc
nc	nc	53	RSVD	RSVD	nc
nc	nc	54	RSVD	RSVD	nc
nc	nc	55	TPx1	TP7	nc
nc	nc	56	TPx0	TP6	nc
nc	nc	57	COL3	TP5	nc
nc	nc	58	COL2	TP4	nc
nc	nc	59	COL1	TP3	nc
nc	nc	60	COLA	TP2	nc
nc	nc	61	GND	TP1	nc
VSS	GND	62	GND	TP0	nc
		63	GND		nc
		64	GND		nc
		65	GND		nc
		66	GND		nc
		67	GND		nc
		68	GND		nc
		69	GND		nc
		70	GND		nc
		71	GND		nc
		72	GND		nc
		73	GND		nc
		74	GND		nc
		75	GND		nc
		76	GND		nc
		77	GND		nc
		78	GND		nc
		79	GND		nc
		80	GND		nc
		HMI 80	GND		VSS

Figure 23 Satellite Connector Type HMI

2.11.3 ACT Satellite Connector

The ACT satellite connector on the CPU_44A-V2 board allows interface expansion through ACT satellite cards.

CPU_44A-V2		Satellite Connector		CPU_44A-V2	
XMC Pin	XMC Function	Function	Pin	Function	XMC Pin
VSS	GND	GND	1	GND	VSS
nc	nc	PIF0IN0	2	GND	P14.7
nc	nc	PIF0IN1	3	PIF0IN1	P14.7
nc	nc	PIF0IN2	4	PIF0IN2	P14.6
nc	nc	PIF0IN3	5	PIF0IN3	P14.5
P5.0	PWMN	PWMN	6	nc	nc
P5.1	PWMP	PWMP	7	DSDIN0	nc
nc	nc	DSDCLK0	8	DSDIN1	P2.6
P1.9	DSD_MCLK0	DSDCLK1	9	DSDIN2	P1.6
nc	nc	DSDCLK1	10	DSDIN3	P0.8(2)
nc	nc	RSVD	11	RSVD	nc
nc	nc	CC_IN3	12	CC_IN0	nc
nc	nc	CC_IN4	13	CC_IN1	HRPWM_COINA
nc	nc	CC_IN5	14	CC_IN2	HRPWM_CIINA
P0.7 (L16)	CCU80_IN0A	TRAP_A	15	ENA_A	HRPWM_C1INA
P1.3	CCU40_IN0A	TRAP_B	16	ENA_B	P1.15
P3.4	CCU42_IN2A	TRAP_X	17	ENA_X	P2.15
P1.14	U0C1_SELO2	SPI_CSA0	18	SPI_MTSR	P2.10
P4.1	U0C1_SELO0	SPI_CSA1	19	SPI_MRST	P3.5
nc	nc	SPI_CSA2	20	SPI_SCLK	P4.0
P2.14	U1C0_DX0C/DOU0	I2C_SDA	21	I2C_SCL	P3.6
nc	nc	ACT_GPI01	22	GPIO	P0.11
nc	nc	ACT_GPI00	23	RESET	P0.6
nc	nc	VDD5	24	VDD5	PORST
VAGND	AGND	VDD5	25	VDD5	VAREF
P14.9	VADC_G1CH1	AGND	26	AREF	VAREF
nc	nc	DAC0/ADC1	27	DAC1/ADC0	VADC_G1CH0
P14.0	VADC_G0CH0(4)	ADC3/ORC0	28	ADC2/DACREF	P14.8
P14.14	VADC_G1CH6	ADC5/ORC2	29	ADC4/ORC1	P14.4
P15.3	VADC_G2CH3	ADC7	30	ADC6/ORC3	nc
P14.13	VADC_G1CH5	ADC9	31	ADC8	P14.15
nc	nc	ADC11	32	ADC10	P14.2
nc	nc	ADC13	33	ADC12	P15.2
nc	nc	PWM80_H	34	PWMA0_H	nc
nc	nc	PWM80_L	35	PWMA0_L	CCU80_OUT00
nc	nc	PWM81_H	36	PWMA1_H	CCU80_OUT01
nc	nc	PWM81_L	37	PWMA1_L	CCU80_OUT10
nc	nc	PWM82_H	38	PWMA2_H	CCU80_OUT11
nc	nc	PWM82_L	39	PWMA2_L	CCU80_OUT20
nc	nc	PWM83	40	PWMA3	CCU80_OUT21
nc	nc	PWMX2	41	PWMA2	CCU42_OUTF3
nc	nc	PWMX3	42	PWMA3	CCU42_OUT0
VSS	GND	VDD5	43	VDD5	GND
		VDD5	44	VDD5	VSS

Figure 24 Satellite Connector Type ACT

- (1) P0.7 can also be used for JTAG Debugging (TDI)
- (2) P0.8 is used as TRST in order to enable JTAG Debug
- (3) This pin is connected with the satellite connector via an analog switch
- (4) This ADC input does not support "Out of Range Detection"
- (5) This pin must be "enabled" by a solder jump.
- (6) Support High Resolution PWM

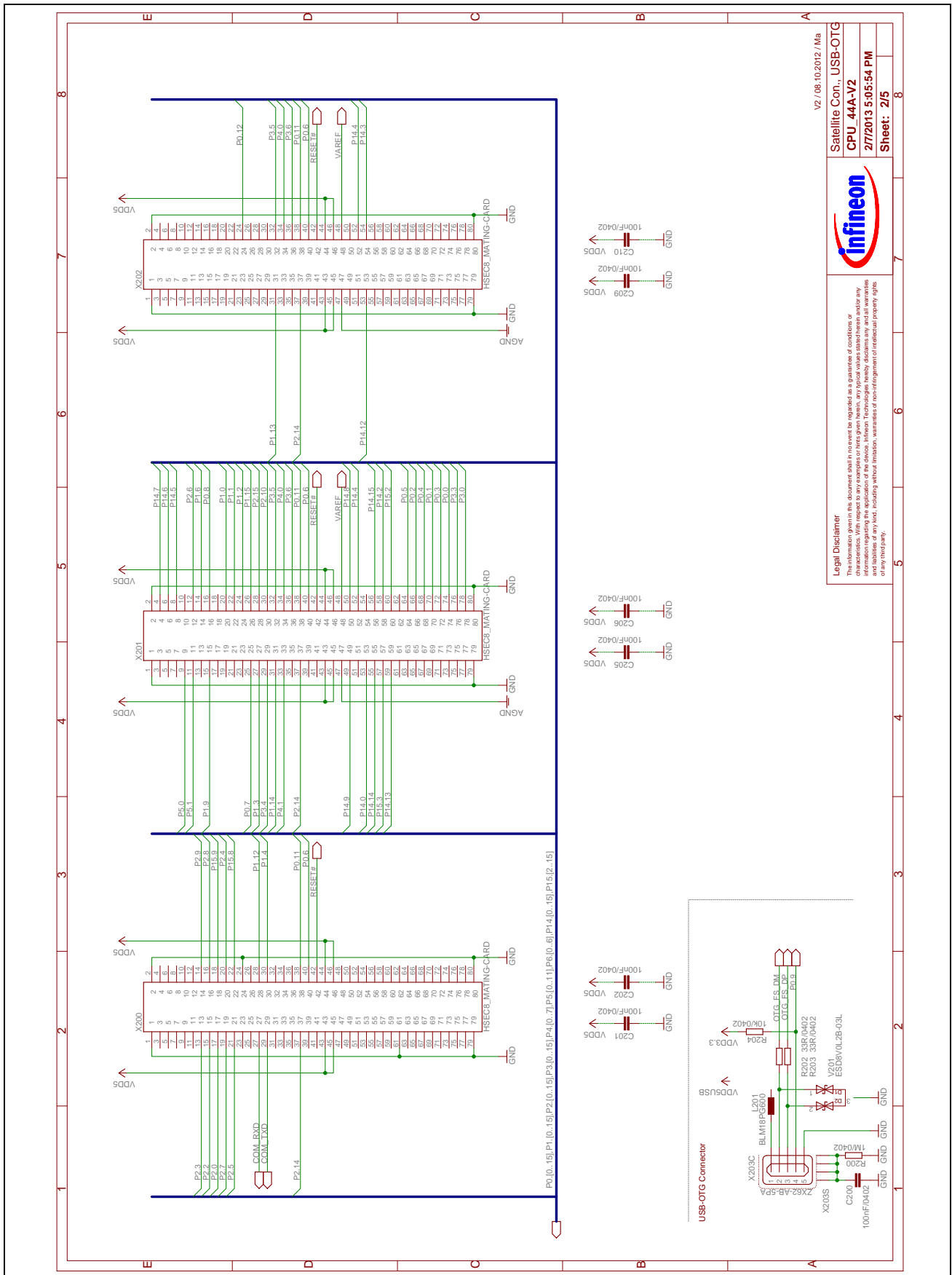
3 Production Data

3.1 Schematics

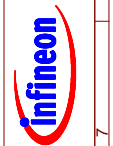
This chapter contains the schematics for the CPU board:

- Satellite Connectors, USB-OTG
- XMC4400
- Power, Debug Connectors, Reset
- On-board Debugger

The board has been designed with Eagle. The full PCB design data of this board can also be downloaded from www.infineon.com/xmc-dev.

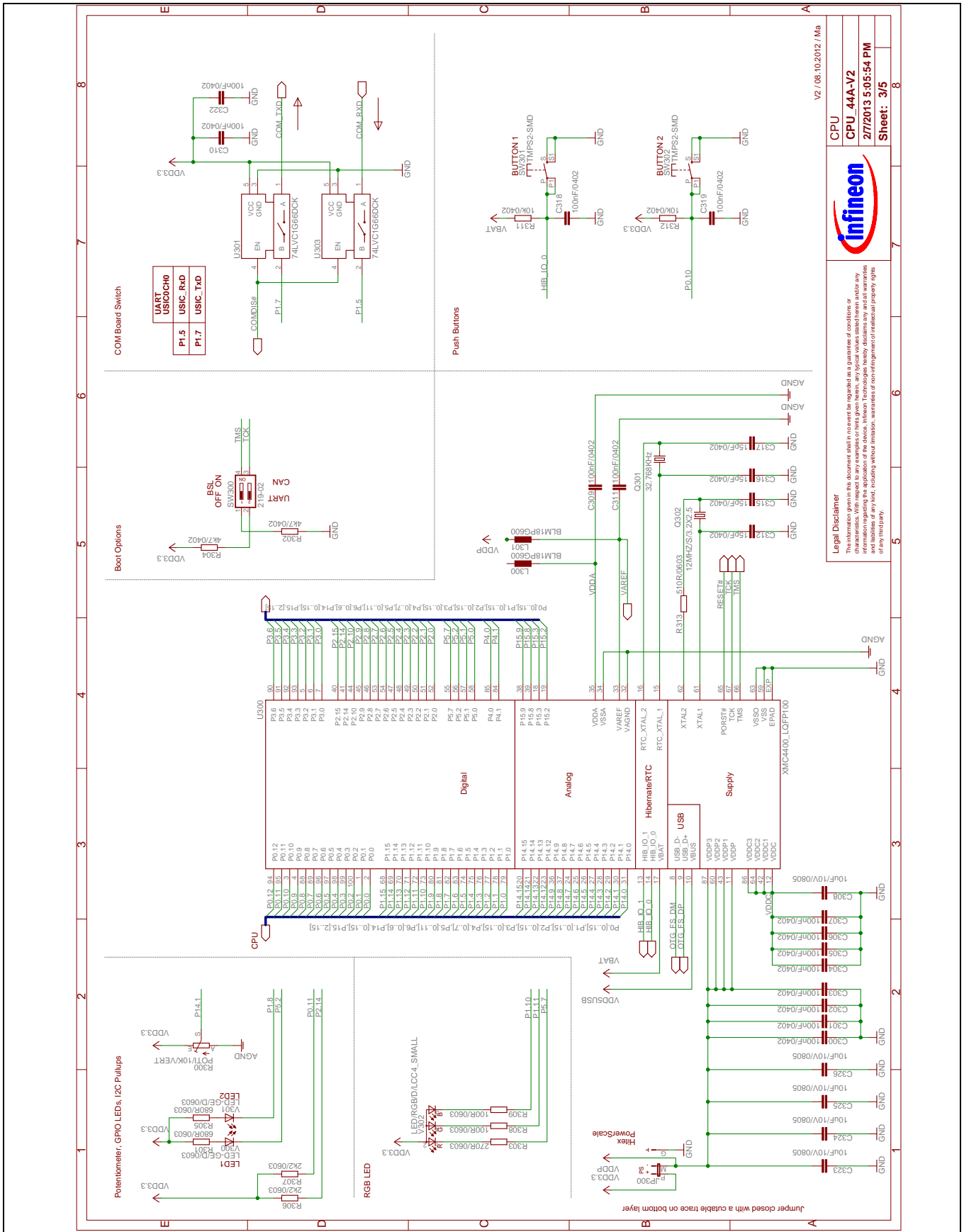


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Figure 25 Satellite Connectors, USB-OTG



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Figure 26 XMC4400

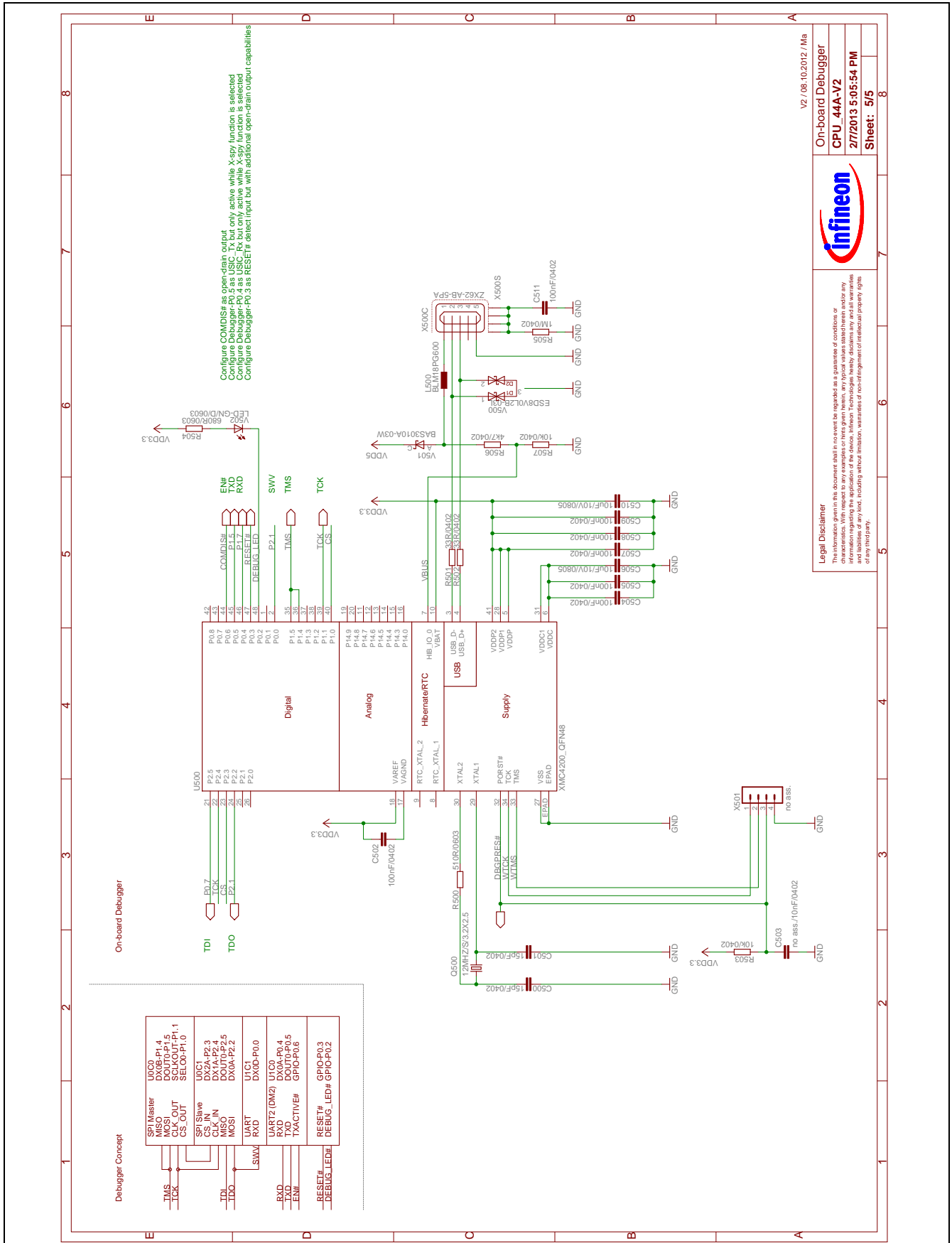


Figure 28 On-board Debugger

3.3 Bill of Material (BOM)

Table 11 BOM of CPU_44A-V2 Board

Pos. No.	Qty	Value	Device	Reference Des.
1	1	0R/0603	Resistor	R416
2	2	1M/0402	Resistor	R200, R505
3	2	1k5/0603	Resistor	R405, R406
4	3	2k2/0603	Resistor	R306, R307, R420
5	3	4k7/0402	Resistor	R302, R304, R506
6	1	4u7F/0805	Capacitor, ceramic	C412
7	11	10k/0402	Resistor	R204, R311, R312, R401, R412, R414, R419, R422, R428, R503, R507
8	2	10nF/0402	Capacitor	C406, C415
9	9	10uF/10V/0805	Capacitor, ceramic	C308, C323, C324, C325, C326, C405, C407, C506, C510
10	2	12MHZ/S/3.2X2.5	Crystal, NX3225GD, NDK	Q302, Q500
11	6	15pF/0402	Capacitor	C312, C315, C316, C317, C500, C501
12	1	32.768KHz	Crystal, NX3215SA, NDK	Q301
13	5	33R/0402	Resistor	R402, R403, R404, R501, R502
14	2	33R/0402	Resistor	R202, R203
15	2	74LVC1G66DCK	IC, Single Analog Switch	U301, U303
16	2	100R/0603	Resistor	R308, R309
17	31	100nF/0402	Capacitor	C200, C201, C202, C205, C206, C209, C210, C300, C301, C302, C303, C304, C305, C306, C307, C309, C310, C311, C318, C319, C322, C400, C401, C413, C502, C504, C505, C507, C508, C509, C511
18	2	100uF/T/10V/C	Capacitor, bipolar	C411, C414
19	1	219-02	Dual DIP-Switch, 0.1" SMD	SW300
20	1	270R/0603	Resistor	R303
21	1	270k/0402	Resistor	R415
22	2	510R/0603	Resistor	R313, R500
23	4	680R/0603	Resistor	R301, R305, R407, R504
24	3	BAS3010A-03W	Diode, SOD323, Infineon	V400, V408, V501
25	2	BAT54-02V	Diode, SC79, Infineon	V404, V405
26	1	BAV70W	Diode, SOT323, Infineon	V406
27	1	BC858C	Transistor, SOT23-3, Infineon	Q404
28	1	BK-885	Battery Holder, 12mm Coin Cell	X402
29	4	BLM18PG600	Ferrite Bead, 0603, Murata	L201, L300, L301, L500
30	2	ESD8V0L2B-03L	Diode, TSLP-3-1, Infineon	V201, V500
31	3	FIDUCIAL	FIDUCIAL	ADJ_1, ADJ_2, ADJ_3
32	3	HSEC8_MATING-CARD	Connector, Edgecard, Samtec	X200, X201, X202
33	1	IFX1763-3.3	Voltage Regulator, 3.3V LDO, Infineon	U401
34	2	LED-GE/D/0603	LED, yellow	V300, V301
35	4	LED-GN/D/0603	LED, green	V401, V402, V403, V502
36	1	LED-RT/D/0603	LED, red	V407
37	1	LED/RGB/D/LCC4_SMALL	LED, RGB, LCC4_SMALL	V302
38	1	POTI/10K/VERT	Potentiometer, K09K1130A8G, ALPS	R300
39	1	S2*10/1.27SO	Connector, FTSH-110-01-L-DV-K-P, Samtec	X400

Table 11 BOM of CPU_44A-V2 Board

Pos. No.	Qty	Value	Device	Reference Des.
40	3	TMPS2-SMD	Switch, tactile	SW301, SW302, SW400
41	1	TPS2051BDBV	IC, Power Switch	U403
42	1	XE3K_DM2+CTX	Connector, FTSH-105-01-LM-DV-K, without pin 7, Samtec Connector, FLE-103-01-G-DV, Samtec	X401
43	1	XMC4200_QFN48	IC, XMC4200, QFN48, Infineon	U500
44	1	XMC4400_LQFP100	IC, XMC4400, LQFP100, Infineon	U300
45	2	ZX62-AB-5PA	Connector, Micro-USB, Hirose	X203, X500
46	1	no ass.	Pinheader, 4-pin, 0.1" TH	X501
47	4	no ass.	Pinheader, 1-pin, 0.1" TH	TP404, TP405, TP406, TP407
48	1	no ass./0R/0603	Resistor	R417
49	1	no ass./4k7/0402	Resistor	R427
50	2	no ass./10k/0402	Resistor	R411, R413
51	1	no ass./10nF/0402	Capacitor	C503
52	1	no ass./33R/0402	Resistor	R410
53	1	no ass.	Pinheader, 3-pin, 0.1" TH, Hitex PowerScale	JP300

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Hexagon Application Kit

For XMC4000 Family

MOT_GPDLV-V2

General Purpose Motor Drive Card

Board User's Manual

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Page or Item	Subjects (major changes since previous revision)
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Introduction

This document describes the features and hardware details of the General Purpose Motor Drive Card (MOT_GPDLV-V2) designed to work with Infineon's CPU boards of the XMC4000 family. This board is a member of Infineon's Hexagon Application Kits.

1 Overview

The MOT_GPDLV-V2 board is an application expansion satellite card of the Hexagon Application Kits. The satellite card along with a CPU board (e.g. CPU_45A-V2 board) demonstrates the motor control capabilities of XMC4000 family. The main use case for this satellite card is proofing software algorithms and methods for motor control. The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1.1 Key Features

The MOT_GPDLV-V2 satellite card is equipped with following features

- Seamless connection to the CPU board (e.g. CPU_45A-V2) via the ACT satellite connector
- 3 phase low voltage half-bridge inverter using Infineon's N-channel OptiMOS™3 power transistors
- Gate Driver IC (6ED003L02-F2) with over-current detection circuit (ITRIP)
- Current measurement by using single or triple shunts (amplified)
- Position sensing via
 - Inductive resolver interface using delta-sigma modulator and pattern generator for resolver excitation
 - Quadrature encoder interface for both single ended and differential signals
 - Hall sensor interface
- Input voltage range: 24 V +/-20%
- Power supply
 - Switch mode power supply for 5V power generation
 - Low drop voltage regulators (15 V) for MOSFET gate driver and resolver excitation
 - Low drop voltage regulators (3.3V) for logic
- Maximum DC-link current: 7.5 A, nominal DC-link current 5 A

1.2 Block Diagram

Figure 1 shows the block diagram of the MOT_GPDLV-V2 satellite card. There are following building blocks:

- Connectors to CPU Board, power supply, motor and position interfaces
- Analog signal measurement
- Position sensing

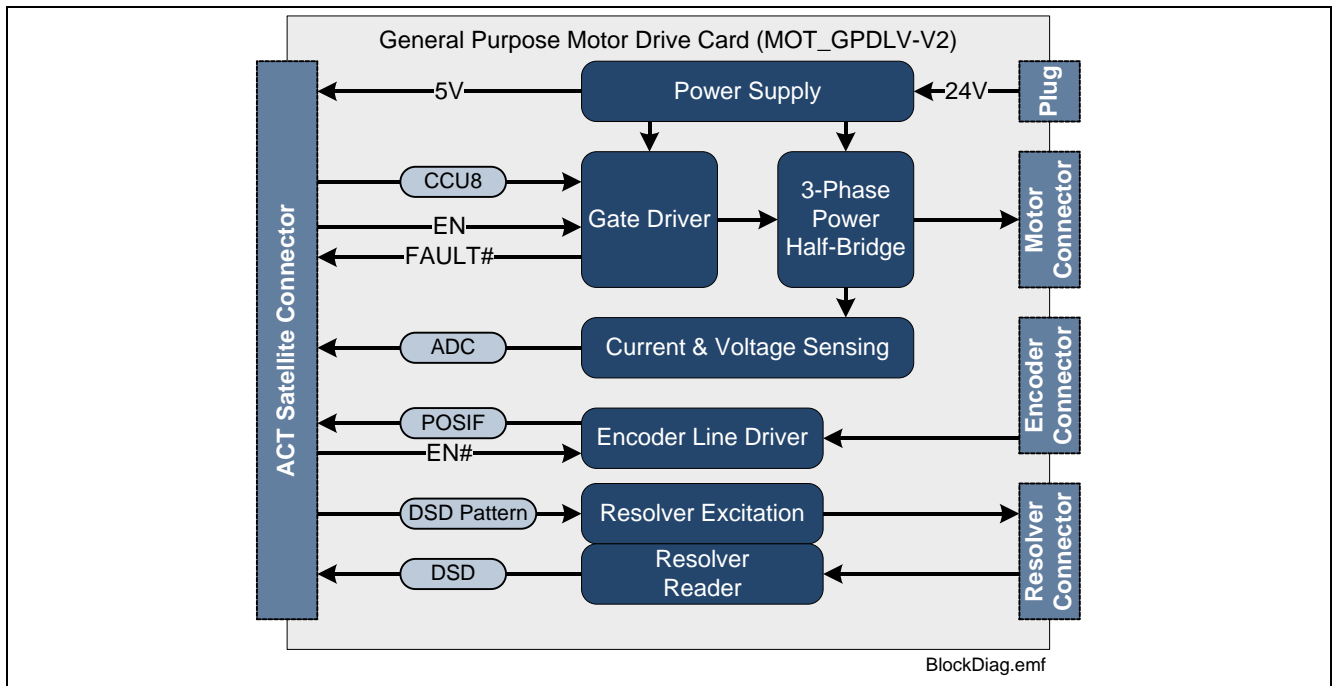


Figure 1 Block Diagram of the General Purpose Motor Drive Card

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

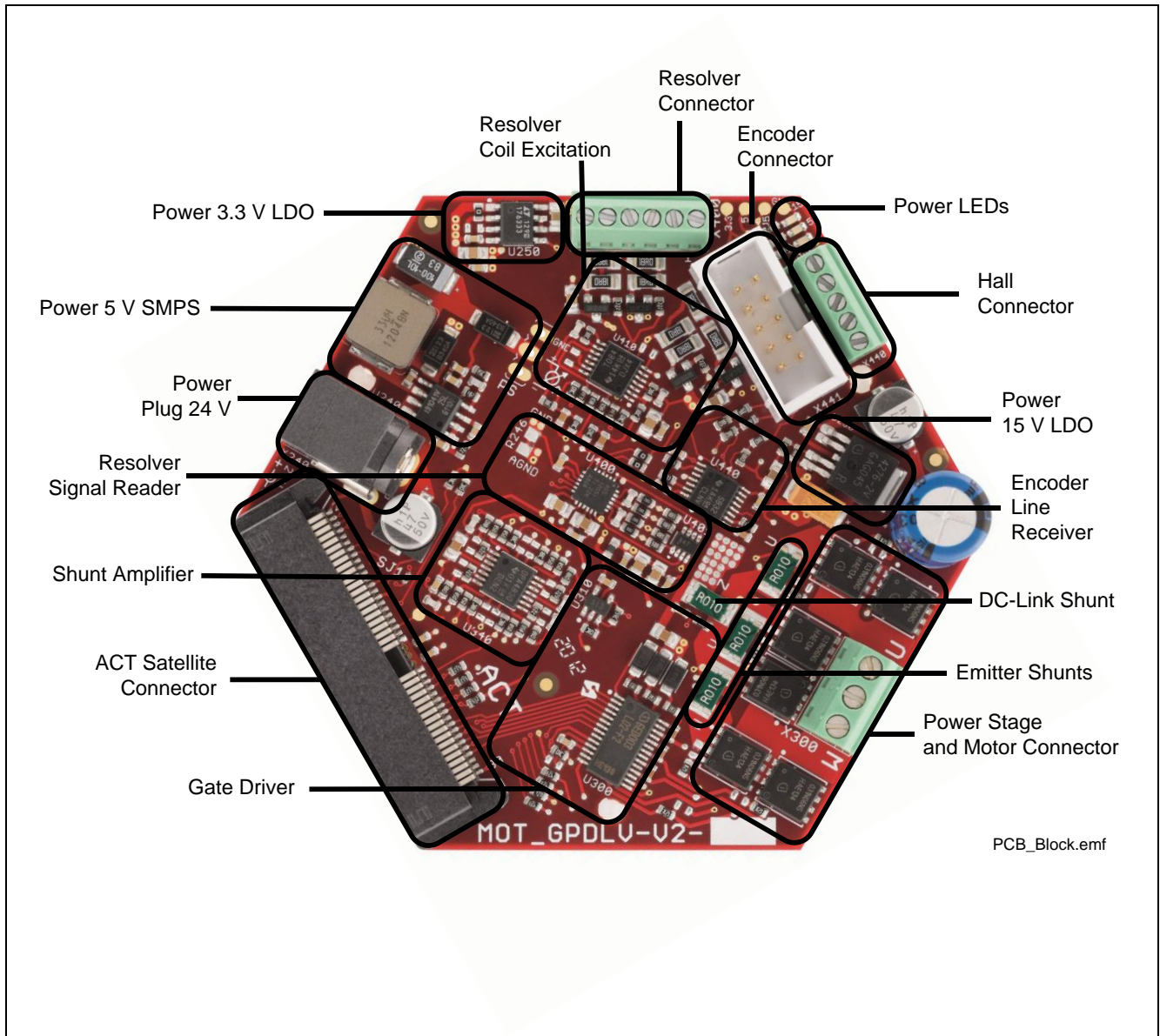


Figure 2 General Purpose Motor Drive Card

2.1 Power Supply

The General Purpose Motor Drive Card must be supplied by an external 24 Volt DC power supply connected to its power jack X240. The power to be delivered by the external power supply depends on the overall load mainly defined by the power consumption of the motor. The power supply unit (24V / 2A) delivered with the motor control kit is sufficient to drive the enclosed motor as well as other satellite cards connected to the CPU board. The power supply concept is shown in Figure 3.

A diode protects the power supply units and the circuit if more than one power supply is connected to the system via other satellite cards or via the CPU board (USB). The General Purpose Motor Drive Card is able to supply all other boards with 5V (VDD5) via the ACT satellite connector.

An on-board DC-DC converter (U240) steps down the 24 V input voltage from the power jack to 5 V (VDD5). The input voltage VDD24 must be 24 V +/-20%. The 5 Volt supply for analog circuits VDDA5 is derived from VDD5 filtered by a low pass. A LDO voltage regulator generates 3.3 V (VDD3.3) out of VDD5 and another voltage regulator generates 15 V (VDD15) power supply out of the 24 V input voltage.

Three power LEDs indicate the presence of the generated supply voltages.

Table 1 Power LED

LED	Power Rail	Voltage	Note
V210	VDD5	5.0 V	Must always be "ON"
V211	VDD3.3	3.3 V	Must always be "ON"
V212	VDD15	15.0V	Must always be "ON"

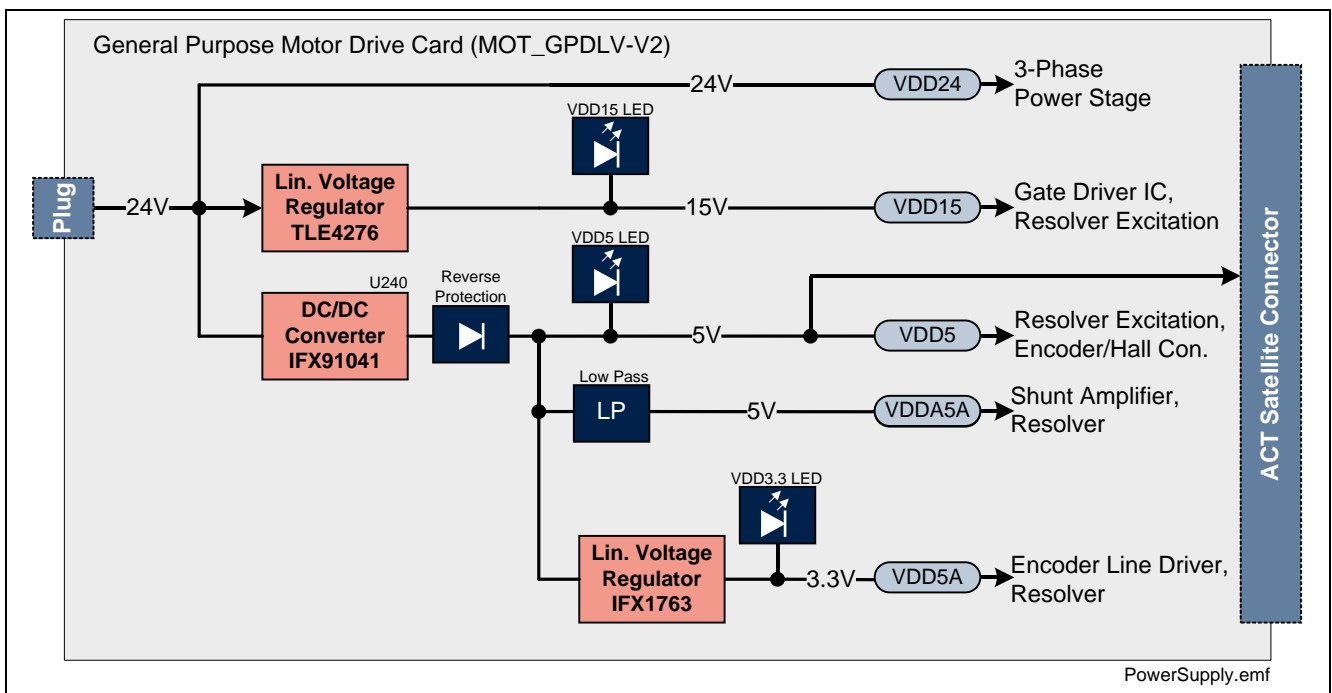


Figure 3 Block Diagram of the Power Circuit

Table 2 shows the connection of the power rails to the ACT satellite connector.

Table 2 Power rail connection to the ACT Satellite Connector

Pin No.	Power rail	Description
43,44,45,46	VDD5	5 V
1,2,79,80	GND	Ground

2.2 Satellite Connector

The satellite connector of the General Purpose Motor Drive Card is the interface to the CPU board e.g. CPU_45A-V2. Take care to connect the General Purpose Motor Drive Card always to the corresponding ACT satellite connector of the CPU board only as shown in Figure 4.

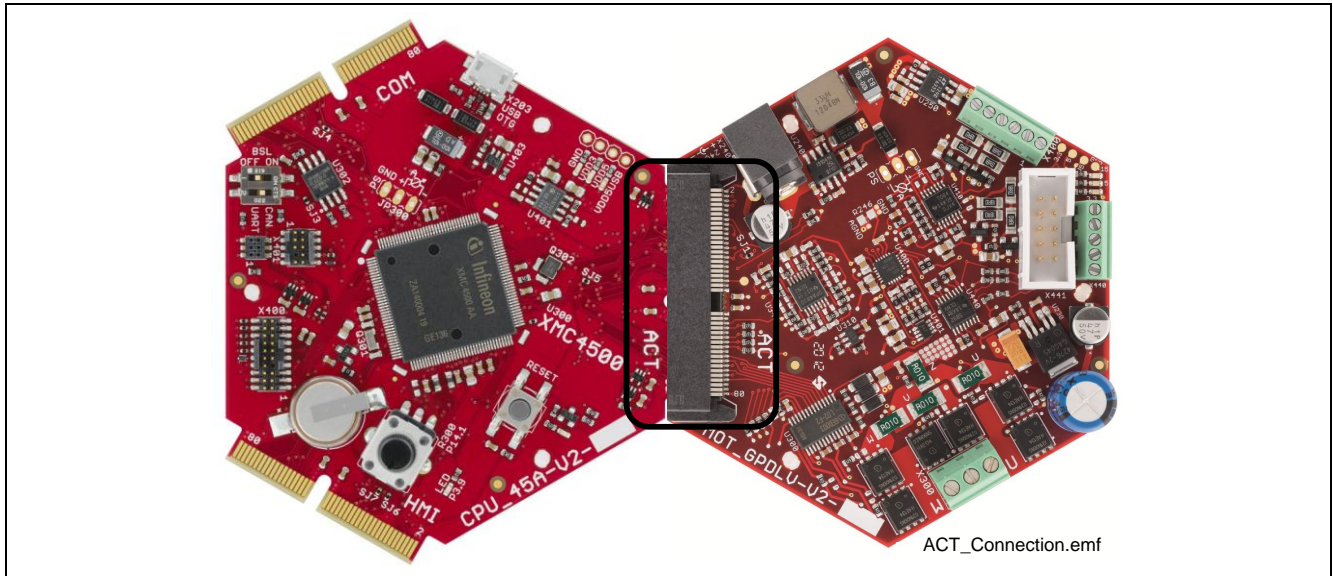


Figure 4 Connection to the CPU Board

The signal mapping details of the ACT satellite connector and the General Purpose Motor Drive Card are provided in Figure 5. The inner rows show the general function of the 80 pins of the ACT connector, which is common for all ACT satellites cards. The outer rows show the signals of the General Purpose Motor Drive Card.

The General Purpose Motor Drive Card provides 5 functional groups of signals (marked by color code) at its pins of the satellite connector:

- The encoder signals (ENCA, ENCB, ENCI): pin 4, 6 and 8
- Resolver signals (PWMN/P, MCLK, MCOS, MSIN): pin 9, 11, 13, 14, 15, 16
- Control and TRAP signals (FAULT#, ENPOW, ENENC#): pin 25, 26, 30
- Voltage and current measurement signals: (UU, UV, UW, UZ, AMP_IW...) located from pin 49 to 60
- PWM signals for the 3-Phase power stage (HIN1#, LIN1#, HIN2 ...): pin 64, 66, 68,70, 72, 74

MOT_GPDLV-V2	Function	ACT		Function	MOT_GPDLV-V2
GND	GND	1	2	GND	GND
nc	PIF0IN1	3	4	PIF0IN1	nc
nc	PIF1IN1	5	6	PIF1IN1	nc
nc	PIF1IN2	7	8	PIF0IN3	nc
PWMN	PWMN	9	10	DSDIN0	nc
MCLK	DSDCLK0	11	12	DSDIN1	nc
MCLK	DSDCLK1	13	14	DSDIN2	nc
nc	RSVD	15	16	DSDIN3	nc
nc	CC_IN3	17	18	RSVD	nc
nc	CC_IN4	19	20	CC_IN0	nc
nc	CC_IN5	21	22	CC_IN1	nc
nc	TRAP_A	23	24	CC_IN2	nc
nc	TRAP_B	25	26	ENA_A	ENPOW
nc	TRAP_X	27	28	ENA_B	nc
nc	SPL_CSA0	29	30	ENA_X	ENENCH
nc	SPL_CSA1	31	32	SPL_MTR	nc
nc	I2C_SDA	33	34	SPL_MTR	nc
nc	ACT_GPI01	35	36	SPL_SCLK	nc
VDD5	ACT_GPI00	37	38	I2C_SCL	nc
VDD5	VDD5	39	40	GPIO	nc
VDD5	VDD5	41	42	RESET	nc
VDD5	VDD5	43	44	VDD5	VDD5
VDD5	VDD5	45	46	VDD5	VDD5
AMP_IW	AGND	47	48	AREF	nc
AMP_IU	DAC0/ADCL	49	50	DACL/ADCO	OFFS
UZ	ADC3/ORC0	51	52	ADC2/DACREF	UV
AMP_IV	ADC5/ORC7	53	54	ADC4/ORCL	nc
AMP_IZ	ADC7	55	56	ADC5/ORC3	UU
UZ	ADCL3	57	58	ADC8	UZ
nc	PWMB0_H	59	60	ADCL0	UW
nc	PWMB0_L	61	62	ADCL2	nc
nc	PWMB1_H	63	64	PWMA0_H	HIN1#
nc	PWMB1_L	65	66	PWMA0_L	LIN1#
nc	PWMB2_H	67	68	PWMA1_H	HIN2#
nc	PWMB2_L	69	70	PWMA1_L	LIN2#
nc	PWMX2	71	72	PWMA2_H	HIN3#
nc	PWMX3	73	74	PWMA2_L	LIN3#
GND	GND	75	76	PWMX0	nc
GND	GND	77	78	PWMX1	nc
GND	GND	79	80	GND	GND

Figure 5 Pin Mapping on ACT Satellite Connector

Figure 6 is an extended view of the signal mapping between the General Purpose Motor Drive Card (MOT_GPDV-V2) and the “XMC4500 CPU Board General Purpose” (CPU_45A-V2). It shows in details which pin of the XMC4500 is mapped to which signal on the motor drive card.

MOT_GPDV-V2		CPU_45A-V2		Satellite Connector		CPU_45A-V2		MOT_GPDV-V2	
Function	XMC Pin	XMC Function	XMC Pin	Pin	Function	XMC Function	XMC Pin	Function	XMC Pin
GND	VSS	GND	GND	1	GND	GND	VSS	GND	VSS
nc	nc	nc	nc	2	PIF0IN1	PIF0_IN0A	P1.3	ENCA	P1.3
nc	nc	nc	nc	3	PIF1IN1	PIF0_IN1A	P1.2	ENCB	P1.2
nc	nc	nc	nc	4	PIF0IN2	PIF0_IN2A	P1.1	ENCI	P1.1
PWMN	P1.0	DSD_PWMN	DSD_DIN0A	5	PIF1IN2	P0.8(2)	P2.6	nc	P0.8(2)
PWMP	P5.1	DSD_PWMP	DSD_DIN1	6	PWMN	DSD_DIN2A	P1.6	MCOS	P1.6
MCLK	P1.7	DSD_MCLK2A	DSDCLK0	7	PWMP	DSD_DIN3A	P6.5 (3)	MSIN	P6.5 (3)
MCLK	P3.4	DSD_MCLK3B	DSDCLK1	8	PIF1IN3	RSVD	nc	nc	nc
nc	nc	nc	RSVD	9	PWMN	CC_IN0	P4.6	nc	P4.6
nc	P4.3	CCU43_IN3A	CC_IN3	10	PWMP	CC_IN1	P4.5	nc	P4.5
nc	P5.2	CCU81_IN1B	CC_IN4	11	PWMP	CC_IN2	P4.4	nc	P4.4
nc	P5.4	CCU81_IN3B	CC_IN5	12	MCLK	ENA_A	P2.13	ENPOW	P2.13
nc	P0.7 (1)	CCU80_IN0A	TRAP_A	13	MCLK	ENA_B	P2.12	nc	P2.12
nc	P5.0	CCU81_IN0A/1A/2A/3A	TRAP_B	14	MCLK	ENA_X	P6.4	ENENC#	P6.4
nc	P4.7	CCU43_IN0C	TRAP_X	15	nc	CCU43_OUT1	P3.13	nc	P3.13
nc	P3.11	U0C1_SELO2	SPL_CSA0	16	nc	U0C1_DOUT0	P2.5	nc	P2.5
nc	P3.8	U0C1_SELO3	SPL_CSA1	17	nc	U0C1_DX0B	P3.0	nc	P3.0
nc	nc	nc	SPL_CSA2	18	nc	U0C1_SCLKOUT	P5.8	nc	P5.8
nc	P2.14	U1C0_DX0D/DOUT0	I2C_SDA	19	nc	V1C0_SCLKOUT	P0.6	nc	P0.6
nc	P15.4	P15.4 Input	ACT_GPI01	20	nc	RESET	PORST	nc	PORST
nc	P4.2	P4.2	ACT_GPI00	21	nc	VDD5	VDD5	nc	VDD5
VDD5	VSS	GND	VDD5	22	nc	VDD5	VDD5	nc	VDD5
VDD5	VAGND	AGND	VDD5	23	nc	VDD5	VDD5	nc	VDD5
AMP_IW	P14.9	VADC_61CH1	AGND	24	nc	AREF	VAREF	nc	VAREF
nc	P14.6	VADC_60CH6	DAC0/ADC1	25	nc	DAC1/ADC0	VADC_61CH0	OFFS	P14.8
AMP_IU	P14.7	VADC_60CH7	ADC3/ORC0	26	nc	ADC2/DACREF	VADC_60CH4	UV	P14.4
UZ	P14.0	VADC_60CH0	ADC5/ORC2	27	nc	ADC4/ORC1	VADC_61CH6	nc	P14.14
AMP_IV	P14.5	VADC_62CH1	ADC7	28	nc	ADC6/ORC3	VADC_61CH7	UU	P14.15
AMP_IJ	P15.14	VADC_63CH6	ADC9	29	nc	ADC8	VADC_60CH2	UZ	P14.2
UZ	P15.15	VADC_63CH7	ADC11	30	nc	ADC10	VADC_62CH6	UW	P15.6
nc	P1.15	CCU81_OUT00	ADC13	31	nc	ADC12	VADC_62CH7	nc	P15.7
nc	P1.12	CCU81_OUT01	PWMB0_H	32	nc	PWMA0_H	CCU80_OUT00	HIN1#	P0.5
nc	P1.14	CCU81_OUT10	PWMB0_L	33	nc	PWMA0_L	CCU80_OUT01	LIN1#	P0.2
nc	P1.11	CCU81_OUT11	PWMB1_H	34	nc	PWMA1_H	CCU80_OUT10	LIN2#	P0.4
nc	P1.13	CCU81_OUT20	PWMB1_L	35	nc	PWMA1_L	CCU80_OUT11	LIN2#	P0.1
nc	P1.10	CCU81_OUT31	PWMB2_H	36	nc	PWMA2_H	CCU80_OUT20	HIN3#	P0.3
nc	P6.0 (3)	CCU81_OUT30	PWMB2_L	37	nc	PWMA2_L	CCU80_OUT21	LIN3#	P0.0
nc	P6.1 (3)	CCU81_OUT30	PWMX2	38	nc	PWMX1	CCU43OUT2	P6.3	nc
GND	VSS	GND	PWMX3	39	nc	GND	CCU43OUT3	P6.2	nc
GND	VSS	GND	VDD5	40	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	41	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	42	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	43	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	44	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	45	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	46	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	47	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	48	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	49	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	50	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	51	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	52	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	53	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	54	nc	VDD5	VSS	VSS	VSS
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GND	VSS	GND	VDD5	56	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	57	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	58	nc	VDD5	VSS	VSS	VSS
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GND	VSS	GND	VDD5	62	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	63	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	64	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	65	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	66	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	67	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	68	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	69	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	70	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	71	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	72	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	73	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	74	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	75	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	76	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	77	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	78	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	79	nc	VDD5	VSS	VSS	VSS
GND	VSS	GND	VDD5	80	nc	VDD5	VSS	VSS	VSS

Figure 6 Pin Mapping to XMC4500 on CPU Board CPU_45A-V2

2.3 Gate Driver and Power Stage

The power stage consists of three half-bridges using Infineon's N-channel OptiMOS™ power transistors. They are selected for a safe operation area with huge headroom, hence no cooling is needed when using at nominal current of 5 Ampere.

The gate driver (6ED003L02-F2) is Infineon's full bridge driver in SOI-technology offering an excellent ruggedness on transient voltages. The external bootstrap circuitry has been dimensioned according to the formula (see Infineon application note AN-EICEDRIVER-6EDL04-1):

$$C_{BS} = \frac{i_{QBS} \cdot t_P + Q_G}{\Delta V_{BS}} \cdot 1.2$$

$$\frac{C_{BS} \cdot \Delta V_{BS}}{1.2} = i_{QBS} \cdot t_P + Q_G$$

$$(0.833 \cdot C_{BS} \cdot \Delta V_{BS}) - Q_G = i_{QBS} \cdot t_P$$

$$t_P = \frac{(0.833 \cdot C_{BS} \cdot \Delta V_{BS}) - Q_G}{i_{QBS}}$$

With

C_{BS} : Bootstrap Capacity (1 uF)

i_{QBS} : highside driver quiescent current (max. 100 uA)

Q_G : Gate charge (max. 130 nC)

ΔV_{BS} : max. allowed voltage drop at the bootstrap capacitor (5 V)

Factor 1.2: 20% margin for capacitor

the minimum switching period t_p is 40 ms:

$$t_p = \frac{(0.833 \cdot 1 \mu F \cdot 5 V) - 130 \text{ nC}}{100 \mu A}$$

$$t_p = 40 \text{ ms}$$

The gate driver offers several protection features like under-voltage lockout, signal interlocking of every phase to prevent cross-conduction and overcurrent detection.

In an error situation a FAULT# signal is generated and must be handled by the microcontroller. The FAULT# signal changes to low state if an over-current condition has been detected by the ITRIP circuit. The ITRIP current level is measured as the amplified voltage drop over the DC-link shunt (see Figure 7). The minimum input voltage level to trigger an over-current event is specified at 380 mV. With an amplifier gain of $1 + (40.2/10) = 5.02$ and a DC-Link shunt with 10 mΩ the ITRIP will be triggered at a DC-Link current higher than 7.57 A:

$$I = U / R,$$

$$I = (0.38 \text{ V} / 5.02) / 10 \text{ m}\Omega,$$

$$I = 7.57 \text{ A}.$$

The overcurrent condition must be present for longer than about 100 us ($3 \cdot RC$ time constant of the RC filter R322, C310) in order to trigger the ITRIP. This shall protect the PCB traces and the components in the high current path.

The microcontroller must provide the PWM signals (LIN1/2/3#, HIN1/2/3#) for the high-side and low-side switches. The PWM signals must be generated low-active.

The gate driver must be enabled via signal ENPOW.

A phase current measurement is provided via shunt resistors

- a) single shunt (10 mΩ) in the DC-link path and/or
- b) triple shunt (10 mΩ) in the low-side path

The resistance of the shunts limits the system behavior and may not fit to the low-ohmic power transistors. This is intended as the main purpose of this board is to proof SW algorithms and methods over a wide range.

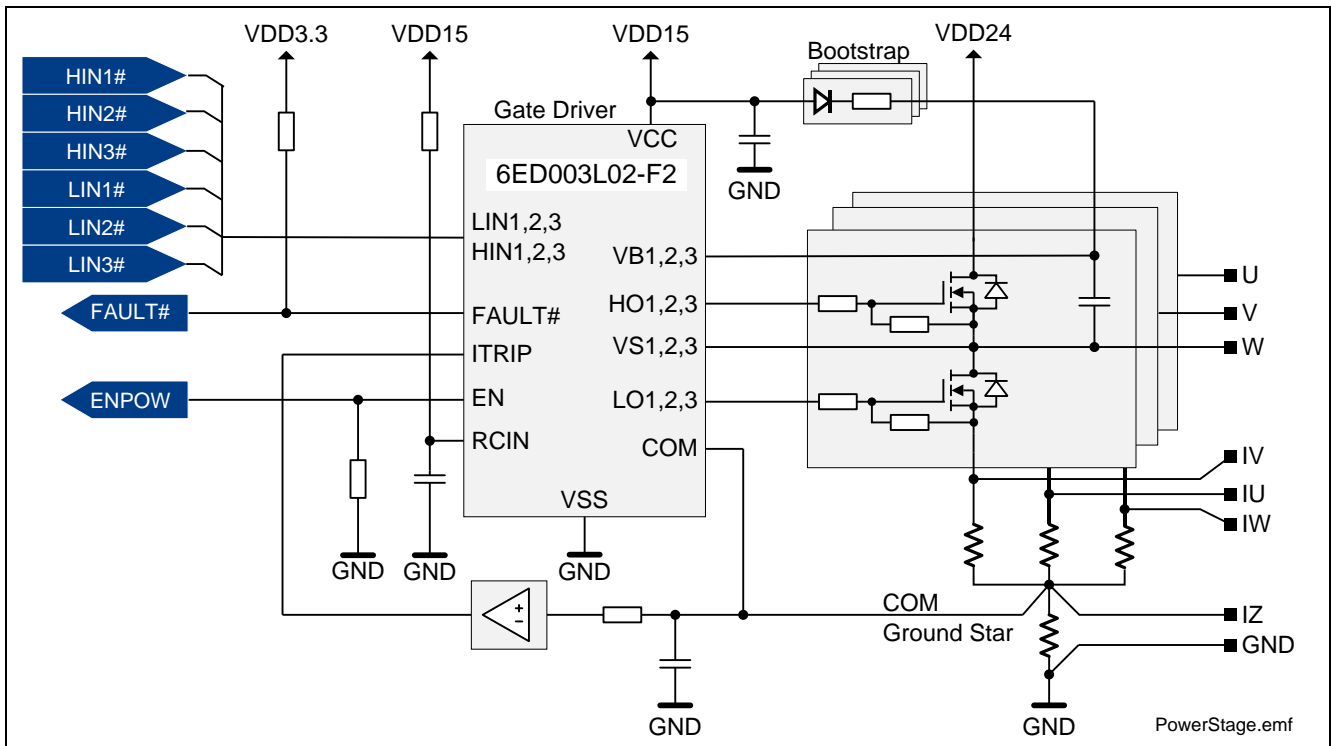


Figure 7 Block Diagram of the Gate Driver and the Power Stage

Table 3 shows the connection of the Gate Driver signals to the ACT satellite connector.

Table 3 Gate Driver signals connection to the ACT Satellite Connector

Pin No.	Signal Name	Description
25	FAULT#	this signal indicates over-current and under-voltage (low-active)
26	ENPOW	High level enables the power stage (high-active)
64	HIN1#	High-side logic input 1 (low-active)
66	LIN1#	Low-side logic input 1 (low-active)
68	HIN2#	High-side logic input 2 (low-active)
70	LIN2#	Low-side logic input 2 (low-active)
72	HIN3#	High-side logic input 3 (low-active)
74	LIN3#	Low-side logic input 3 (low-active)

2.4 Voltage and Current Measurements

The phase current measurement is illustrated on the left side of Figure 8; the right side shows the voltage divider for the voltage measurement.

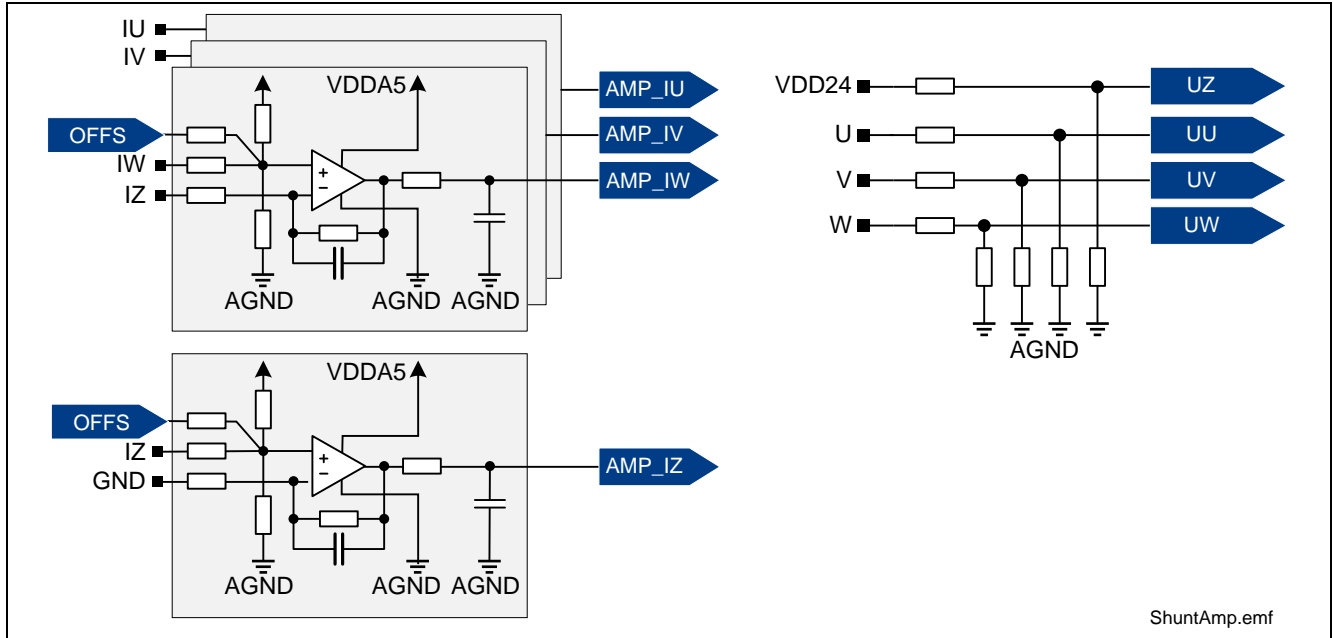


Figure 8 Measurement of Voltages and Currents

2.4.1 Phase Current Measurement

The current measurement can be done via a single shunt (signal IZ) in the DC-link path or via triple shunts (IU, IV, IW) in the emitter path. In both cases the measurement is dimensioned for the following requirements:

Motor power range up to 120W which leads to a nominal DC-link current of about 5 Ampere and a maximum phase peak current of about 20 Ampere. The phase current range is 75 mA to 20 A.

A shunt resistance of 10 mΩ leads to 0.75 mV voltage drop @ 75 mA and 200 mV voltage drop @ 20 A. This voltage is amplified by a non-inverting amplifier. The output of the operational amplifier (AMP_IU, AMP_IV, AMP_IW, AMP_IZ) is available at the ACT Satellite Connector and connected to ADC input channels of the XMC4000 microcontroller.

The gain of the operational amplifier is set to 21 ($G = 1 + (R1 / R2)$), which leads to an output voltage of 15.75 mV @ 75 mA and 4.20 V @ 20A.

The XMC4000 offers a DAC output which is used as DC offset generator for the OpAmps (signal OFFS). The DAC voltage must be adjusted to a voltage level of about 1.2 V in order to get 0 V at the output of the OpAmps when there is no current flow through the shunts. Alternatively the offset can be generated by a resistive voltage divider.

2.4.2 Phase Voltage Measurement

The phase voltage is directly measured using resistive dividers at the phases (signals UZ, UU, UV, and UW). The divider is dimensioned to divide the measured voltage UZ, UU, UV, UW by factor 10.21. The formula to calculate the phase voltage U_{PHx} from the measured voltage U_x is:

$$U_{PHx} = 10.21 * U_x$$

Table 4 summarizes all voltage signals and current signals available at the ACT satellite connector.

Table 4 Voltage and Current signals at the ACT Satellite Connector

Pin No.	Signal Name	Description
50	OFFS	Offset voltage input required for the shunt amplifier

Table 4 Voltage and Current signals at the ACT Satellite Connector

Pin No.	Signal Name	Description
53	AMP_IU	Amplified shunt voltage output representing the current of phase U
57	AMP_IV	Amplified shunt voltage output representing the current of phase V
49	AMP_IW	Amplified shunt voltage output representing the current of phase W
59	AMP_IZ	Amplified shunt voltage output representing the DC-link current
56	UU	Divided voltage output of phase U (divided by 10.21)
52	UV	Divided voltage output of phase V (divided by 10.21)
60	UW	Divided voltage output of phase W (divided by 10.21)
55, 58, 61	UZ	Divided DC-link output voltage (divided by 10.21)

2.5 Resolver Interface

For rotor position detection a resolver can be used. The three coils of the resolver must be connected to the connector X400 as shown in Figure 9.

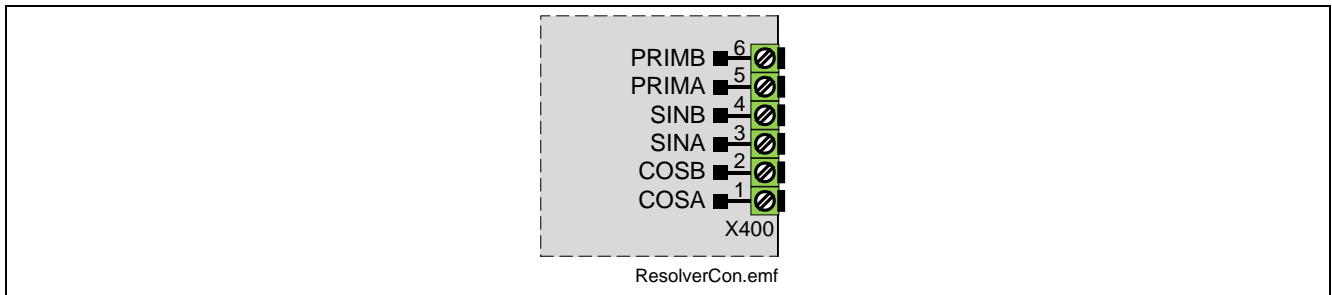


Figure 9 Connection Scheme of the Resolver Connector

The XMC4000 devices use an on-chip pattern generator for the excitation of the primary coil and a decimation filter to read the SIN/COS feedback measured by a delta-sigma modulator.

The primary coil excitation is done via the microcontroller signals PWMP/PWMN which is a digital data stream with a selectable clock rate in the MHz range. These signals are integrated, amplified and fed to the primary coil of the resolver as shown in Figure 10.

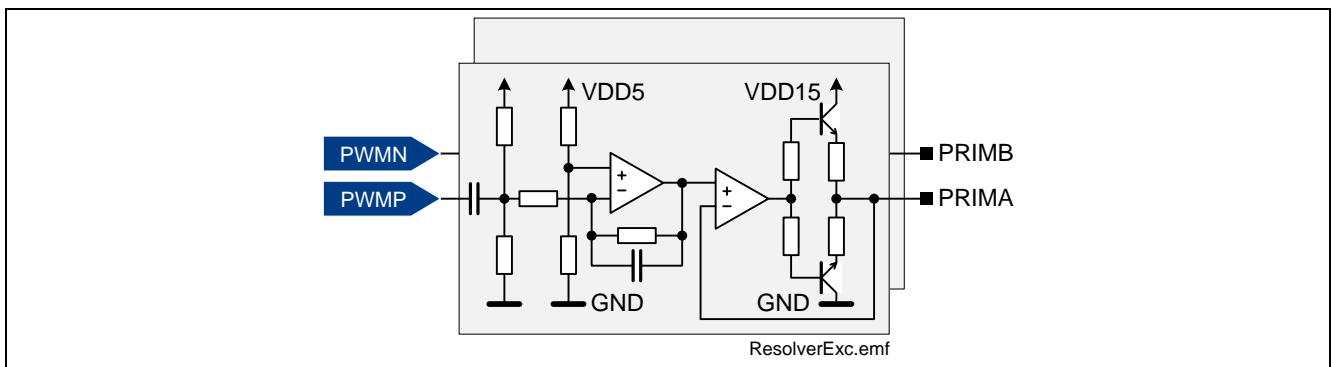


Figure 10 Resolver Excitation Circuit

The feedback signals (SINA/B and COSA/B) of the secondary coils are fed to a delta-sigma modulator ADS1205 which has an internal clock and generates the SIN/COS serial data stream on the signals MSIN/MCOS. It also provides the modulator clock MCLK. The circuit is shown in Figure 11.

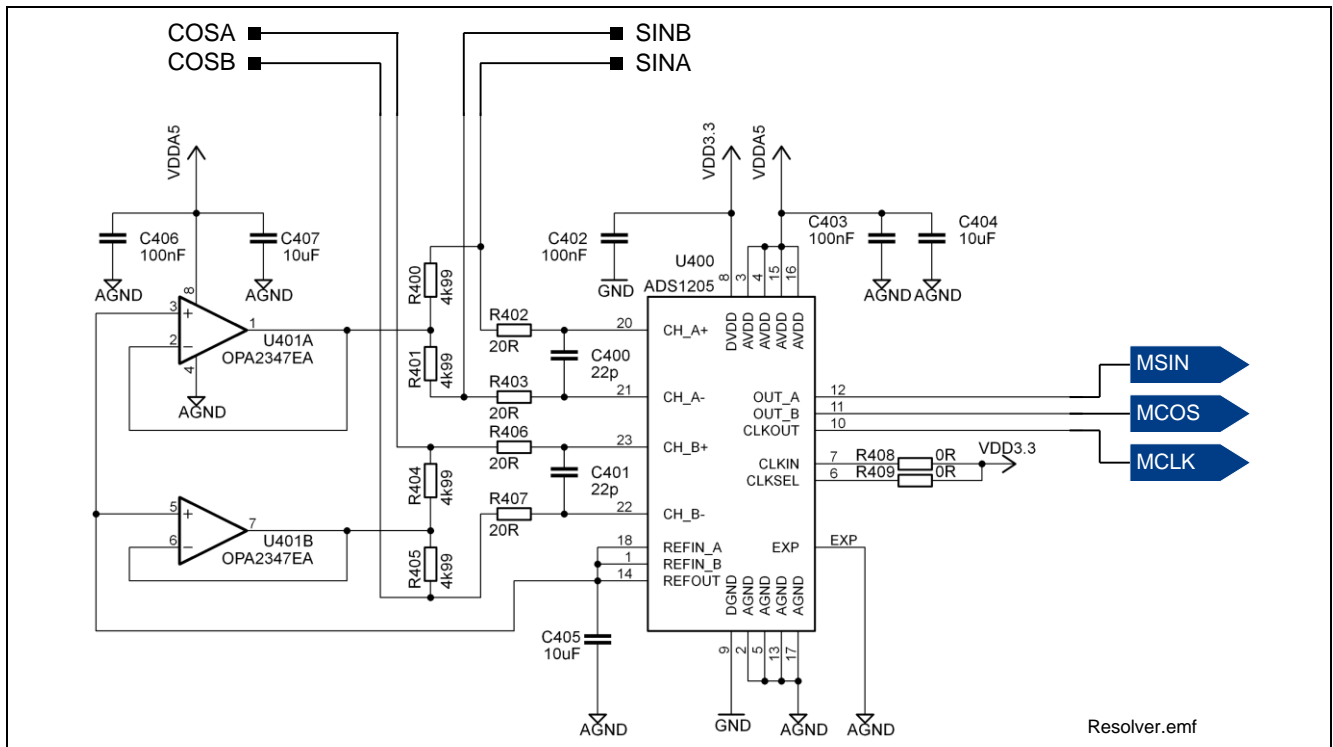


Figure 11 Resolver Modulator Circuit

Table 5 summarizes all signals of the resolver which are connected to the ACT satellite connector.

Table 5 Resolver signals at the ACT Satellite Connector

Pin No.	Signal Name	Description
9	PWMN	Excitation input signal (inverted)
11	PWMP	Excitation input signal
14	MCOS	COS signal output of the delta sigma modulator
16	MSIN	SIN signal output of the delta sigma modulator
15, 13	MCLK	Clock output of the delta sigma modulator

2.6 Encoder and Hall Interface

A quadrature encoder can be used for detecting the actual rotor position. There are single-ended and differential encoders, the board supports both types. For the differential types an encoder line receiver is required as the microcontroller needs single ended signals.

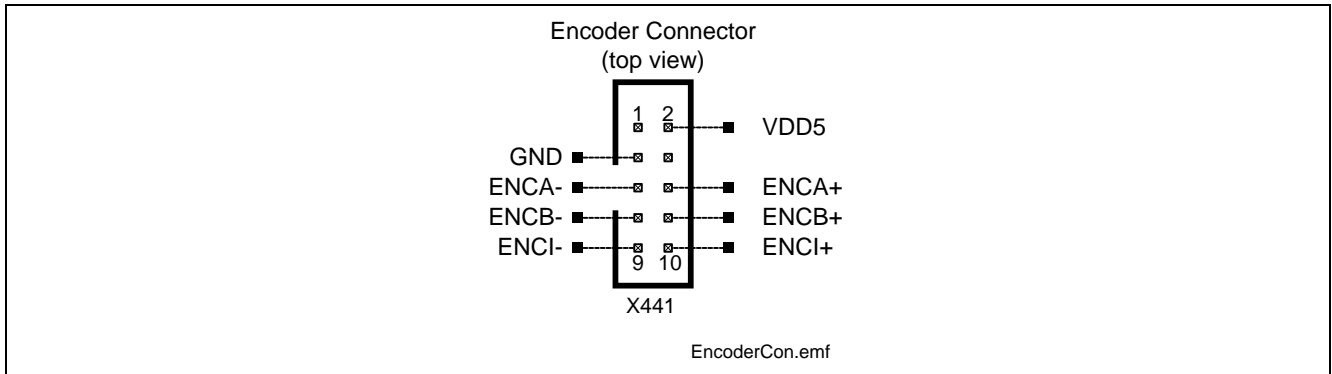


Figure 12 Encoder Connector for differential encoder signals

The differential signals from the encoder (ENCA+/-, ENCB+/-, ENCI+/-) must be connected to the 10-pin encoder connector X441 (Figure 13). The receiver must be enabled by the signal ENENC# (set to "0").

In case of using a single ended encoder or a hall sensor the signals must be applied to the connector X440 and the encoder line receiver must be disabled by setting the signal ENENC# to high level (default).

The parallel operation of both a differential encoder and a hall sensor is possible by adapting the resistor values shown in Figure 13. The pull-up resistors value must be changed to 4.7 k Ω , the serial resistors must be set to 680 Ω . This will ensure appropriate signal levels for the encoder signals ENCx in all use cases and limits the current to about 5 mA.

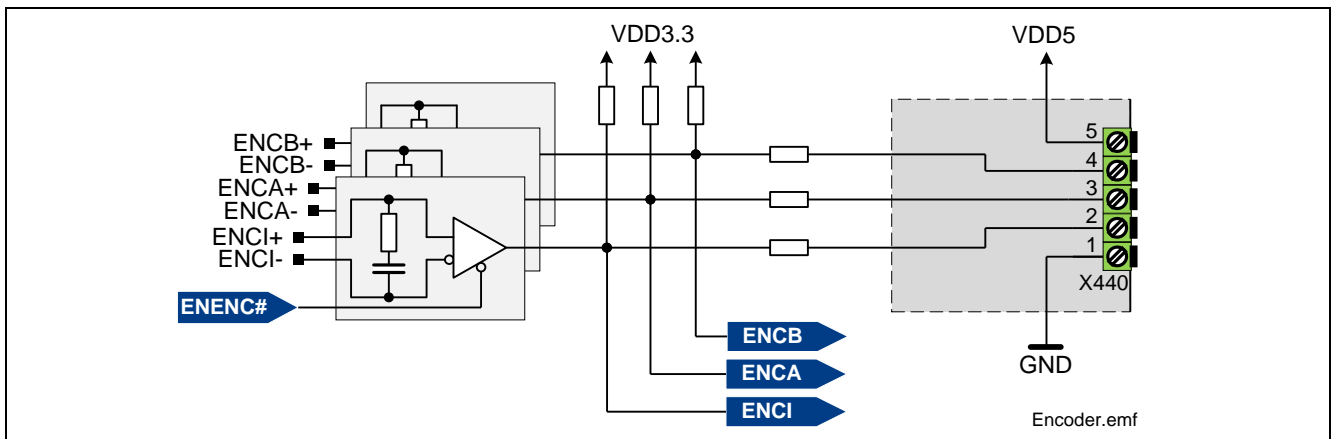


Figure 13 Encoder Line Receiver (differential signals) and hall interface

Figure 6 shows the connection of the encoder/hall signals available at the ACT satellite connector.

Table 6 Encoder / hall signals at the ACT Satellite Connector

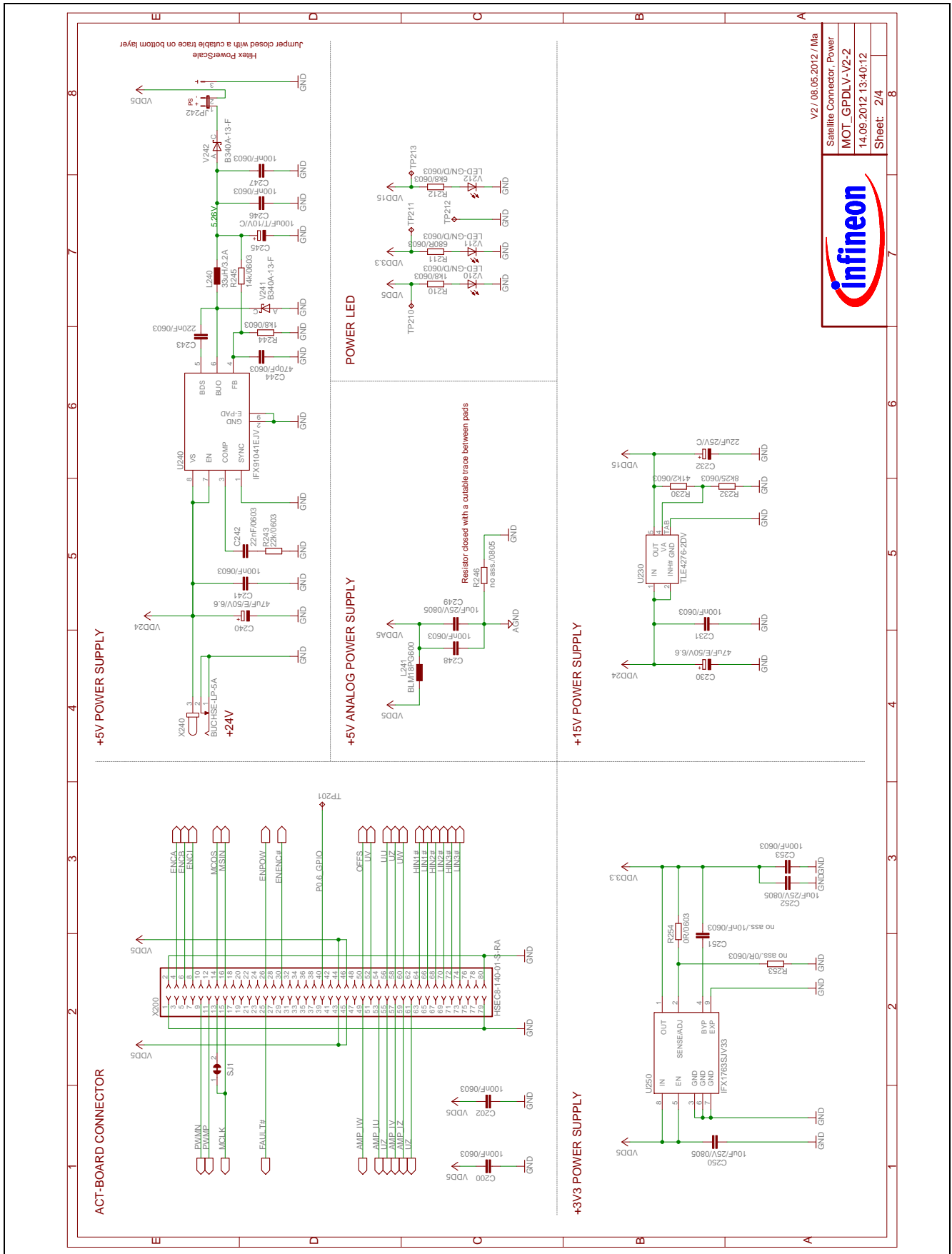
Pin No.	Signal Name	Description
30	ENCEN#	enable signal for the encoder line receiver (active low)
4	ENCA	Encoder channel A
6	ENCB	Encoder channel B
8	ENCI	Encoder channel I

3 Production Data

3.1 Schematics

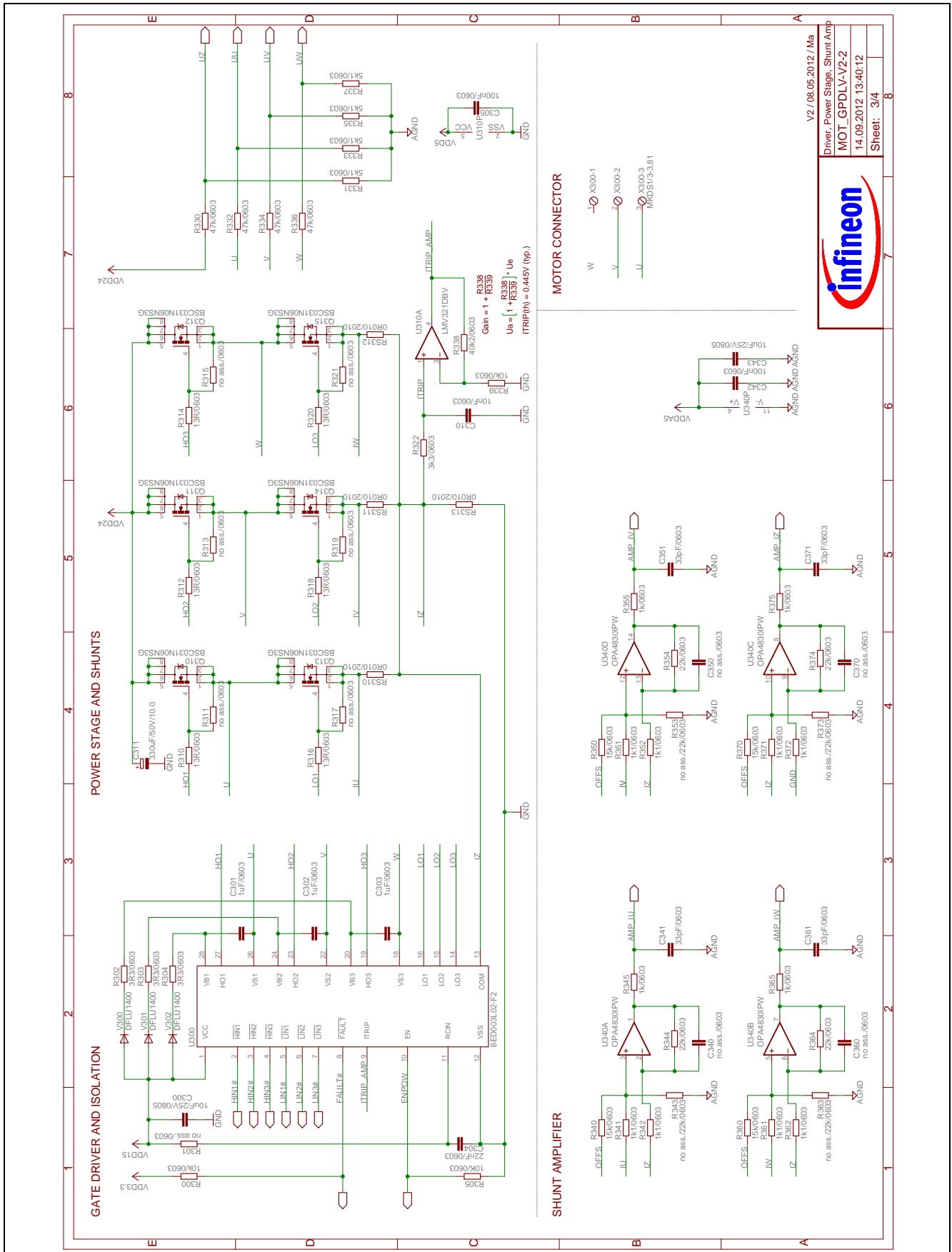
This chapter contains the schematics for the General Purpose Motor Drive Card (MOT_GPDLV-V2):

- Figure 14: Satellite Connector, Power Supply
- Figure 15: Gate Driver, Power Stage, Shunt Amplifier, Motor Connector
- Figure 16: Resolver, Encoder, Hall Connector



V2 / 08.05.2012 / Ma
Satellite Connector, Power
MOT_GPDLV-V2-2
14.09.2012 13:40:12
Sheet: 2/4

Figure 14 Satellite Connector, Power Supply



V2 / 08.05.2012 / Ma
Driver, Power Stage, Shunt Amp
MOT_GPDLV-V2-2
14.09.2012 13:40:12
Sheet: 3/4

Figure 15 Gate Driver, Power Stage, Shunt Amplifier, Motor Connector

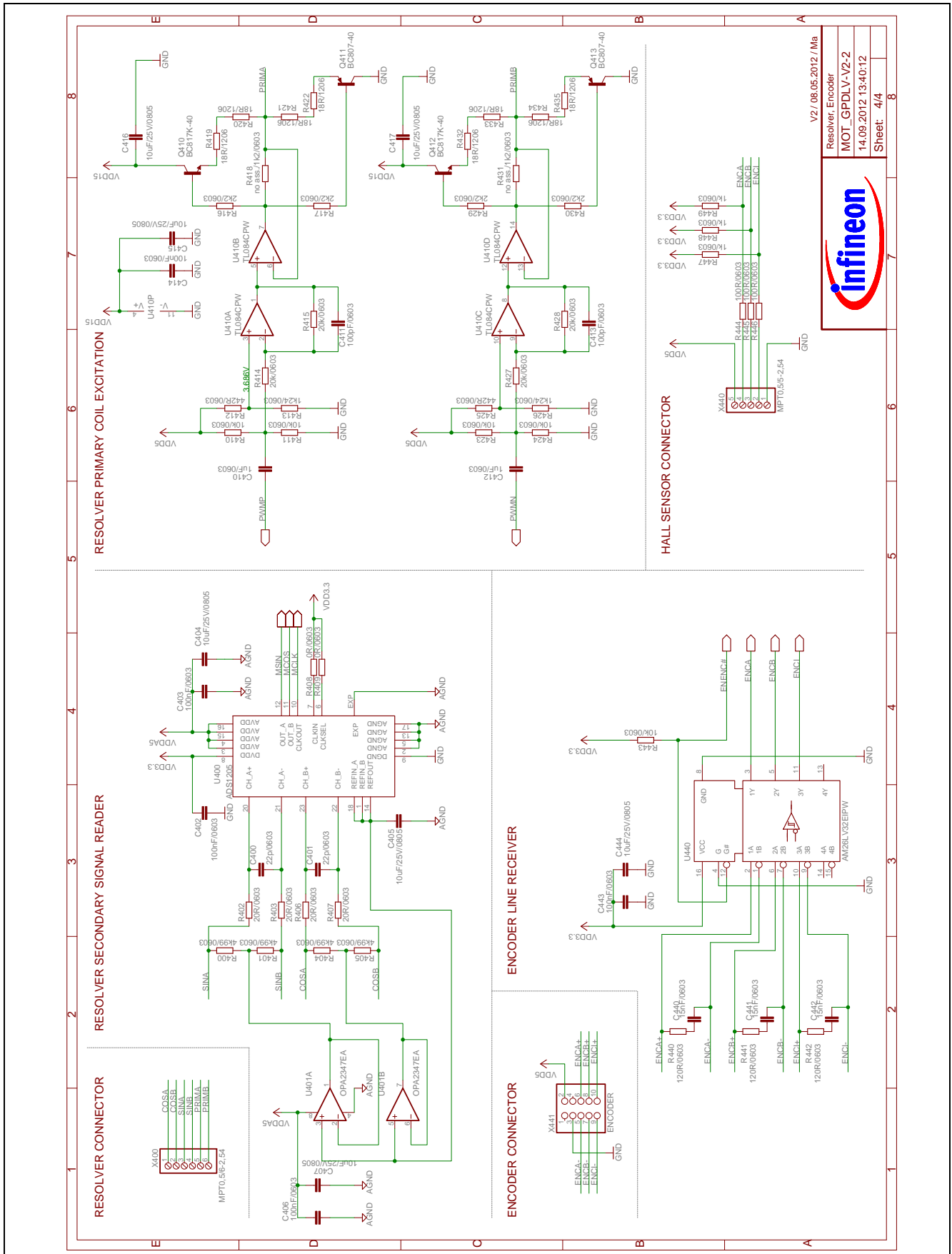


Figure 16 Resolver, Encoder, Hall Connector

3.2 Components Placement and Geometry

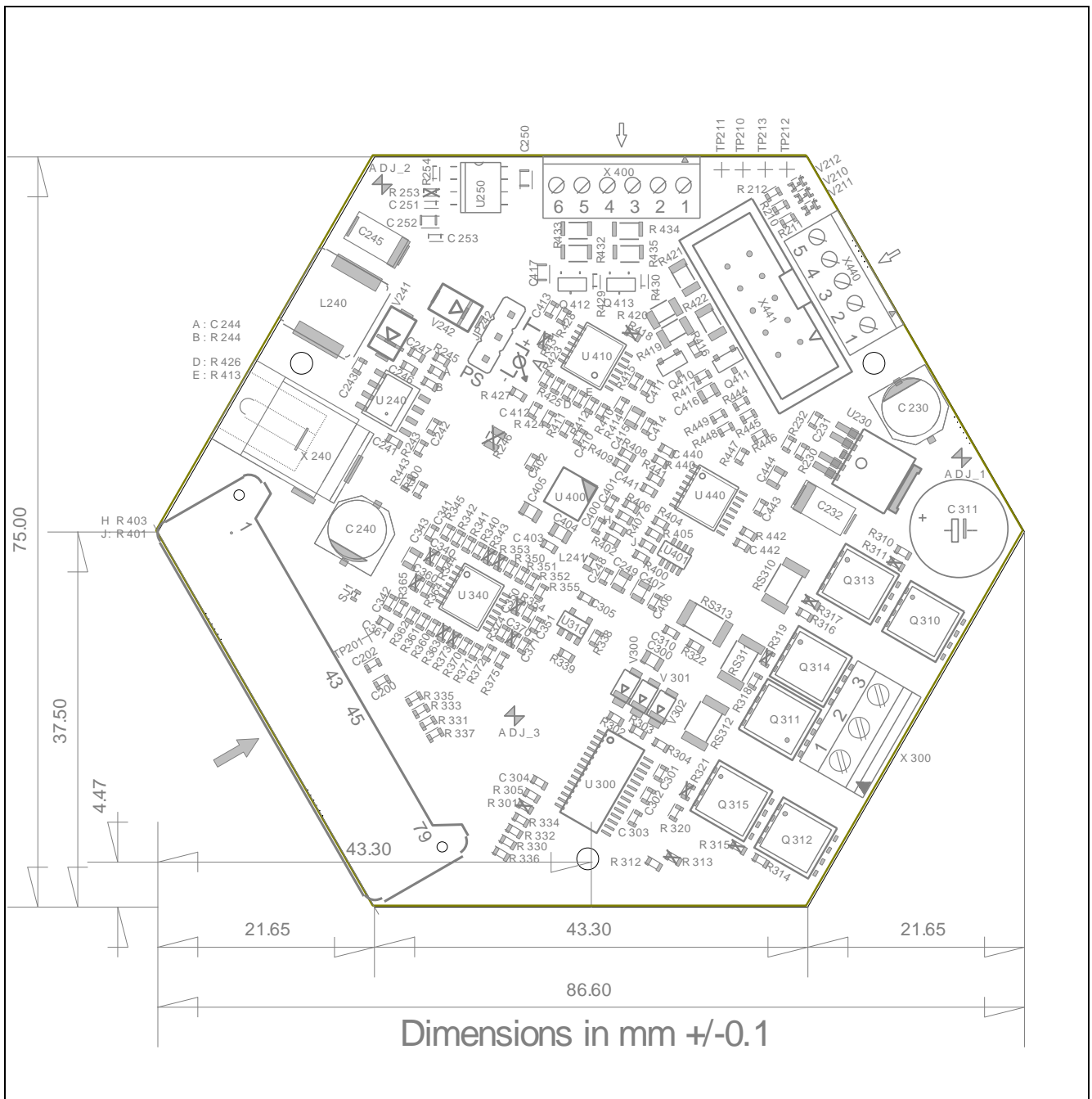


Figure 17 Components Placement and Geometry

3.3 List of Material

The list of material is valid for a certain assembly version for the General Purpose Motor Drive Card. This version is stated in the header of the Table 7. The assembly version number can be identified by the board identification code printed on the PCB. The last digit field "002" of the board identification codes "MOT_GPDLV-V2-002" is representing the assembly version. If there is no assembly version number printed on the PCB (white empty field) than the PCB has the assembly version number 1.

The only difference between both assembly version 1 and 2 is the value of the resistor R322. In version 1 it is 100 kΩ, whereas in assembly version 2 R322 is 3.3 kΩ.

Table 7 List of Material for General Purpose Motor Drive Card (MOT_GPDLV-V2-002)

Sl. No.	Qty	Value	Device	Reference Designator
1	3	0R/0603	Resistor	R254, R408, R409
2	4	0R010/2010	Shunt	RS310, RS311, RS312, RS313
3	7	1k/0603	Resistor	R345, R355, R365, R375, R447, R448, R449
4	8	1k1/0603	Resistor	R341, R342, R351, R352, R361, R362, R371, R372
5	2	1k8/0603	Resistor	R210, R244
6	2	1k24/0603	Resistor	R413, R426
7	5	1uF/0603	Capacitor	C301, C302, C303, C410, C412
8	4	2k2/0603	Resistor	R416, R417, R429, R430
9	3	3R3/0603	Resistor	R302, R303, R304
10	1	3k3/0603	Resistor	R322
11	4	4k99/0603	Resistor	R400, R401, R404, R405
12	4	5k1/0603	Resistor	R331, R333, R335, R337
13	1	6ED003L02-F2	Gate Driver 6ED003L02-F2	U300
14	1	6k8/0603	Resistor	R212
15	1	8k25/0603	Resistor	R232
16	8	10k/0603	Resistor	R300, R305, R339, R410, R411, R423, R424, R443
17	1	10nF/0603	Capacitor	C310
18	12	10uF/25V/0805	Capacitor	C249, C250, C252, C300, C343, C404, C405, C407, C415, C416, C417, C444
19	6	13R/0603	Resistor	R310, R312, R314, R316, R318, R320
20	1	14k/0603	Resistor	R245
21	4	15k/0603	Resistor	R340, R350, R360, R370
22	3	15nF/0603	Capacitor	C440, C441, C442
23	8	18R/1206	Resistor	R419, R420, R421, R422, R432, R433, R434, R435
24	4	20R/0603	Resistor	R402, R403, R406, R407
25	4	20k/0603	Resistor	R414, R415, R427, R428
26	5	22k/0603	Resistor	R243, R344, R354, R364, R374
27	2	22nF/0603	Capacitor	C242, C304
28	2	22p/0603	Capacitor	C400, C401
29	1	22uF/25V/C	Capacitor unipolar	C232
30	4	33pF/0603	Capacitor	C341, C351, C361, C371
31	1	33uH/3.2A	Inductor IHLP-3232DZ-11	L240

Table 7 List of Material for General Purpose Motor Drive Card (MOT_GPDLV-V2-002)

Sl. No.	Qty	Value	Device	Reference Designator
32	1	40k2/0603	Resistor	R338
33	1	41k2/0603	Resistor	R230
34	4	47k/0603	Resistor	R330, R332, R334, R336
35	2	47uF/E/50V/6.6	Capacitor unipolar	C230, C240
36	3	100R/0603	Resistor	R444, R445, R446
37	15	100nF/0603	Capacitor	C200, C202, C231, C241, C246, C247, C248, C253, C305, C342, C402, C403, C406, C414, C443
38	2	100pF/0603	Capacitor	C411, C413
39	1	100uF/T/10V/C	Capacitor unipolar	C245
40	3	120R/0603	Resistor	R440, R441, R442
41	1	220nF/0603	Capacitor	C243
42	1	330uF/50V/10.0	Capacitor unipolar	C311
43	2	442R/0603	Resistor	R412, R425
44	1	470pF/0603	Capacitor	C244
45	1	680R/0603	Resistor	R211
46	1	ADS1205	Delta-Sigma Modulator	U400
47	1	AM26LV32EIPW	Differential Line Receiver	U440
48	2	B340A-13-F	Schottky Diode	V241, V242
49	2	BC807-40	Transistor	Q411, Q413
50	2	BC817K-40	Transistor	Q410, Q412
51	1	BLM18PG600	Inductor	L241
52	6	BSC031N06NS3G	Infineon OptiMOS3 Power-Transistor	Q310, Q311, Q312, Q313, Q314, Q315
53	1	BUCHSE-LP-5A	Power Plug	X240
54	3	DFLU1400	Diode	V300, V301, V302
55	1	ENCODER	Connector	X441
56	3	FIDUCIAL	FIDUCIAL	ADJ_1, ADJ_2, ADJ_3
57	1	HSEC8-140-01-S-RA	SAMTEC 80-pin connetor	X200
58	1	IFX1763SJV33	Voltage Regulator	U250
59	1	IFX91041EJV	Voltage Regulator	U240
60	3	LED-GN/D/0603	LED green	V210, V211, V212
61	1	LMV321DBV	OpAmp	U310
62	1	MKDS1/3-3,81	PHOENIX Connector	X300
63	1	MPT0,5/5-2,54	PHOENIX Connector	X440
64	1	MPT0,5/6-2,54	PHOENIX Connector	X400
65	1	OPA2347EA	OpAmp	U401
66	1	OPA4830IPW	OpAmp	U340
67	1	TL084CPW	OpAmp	U410
68	1	TLE4276-2DV	Voltage Regulator	U230
69	1	no ass./0R/0603	Resistor	R253
70	2	no ass./1k2/0603	Resistor	R418, R431

Table 7 List of Material for General Purpose Motor Drive Card (MOT_GPDLV-V2-002)

Sl. No.	Qty	Value	Device	Reference Designator
71	1	no ass./10nF/0603	Capacitor	C251
72	4	no ass./22k/0603	Resistor	R343, R353, R363, R373
73	4	no ass./0603	Capacitor	C340, C350, C360, C370
74	7	no ass./0603	Resistor	R301, R311, R313, R315, R317, R319, R321
75	1	no ass./0805	Resistor	R246
76	1	3-pin header	PowerScale Connector	JP242
77	1	0402	Solder Jumper	SJ1
78	5	no assembly	SMD Pads	TP201, TP210, TP211, TP212, TP213

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