ISOLATING ANALOG SIGNALS USING THE Si86XX CMOS ISOLATOR FAMILY

1. Introduction

The ISOlinear reference design (Si86ISOLIN-KIT) provides galvanic isolation for analog signals over a frequency range of dc to 500 kHz. The circuits in this reference design can offer lower cost and better performance than analog isolation amplifiers and are useful for analog level translation, ground noise elimination, and safety isolation in applications, such as sensor interface circuits, motor/motion control systems, and isolated power systems. This application note describes three analog isolation circuits (see Table 1) with different cost/performance points from 9 to 12 bits of resolution.

Circuit operation is straightforward: incoming analog signals are digitized and transmitted across a digital isolation barrier, then restored to analog (see Figure 1). Isolation is provided by Silicon Labs' proprietary Si86xx CMOS isolators available in isolation ratings of 2.5 kVacRMS and 5 kVacRMS. These isolators offer industry-leading timing, power, EMI performance, reliability, and provide substantial advantages over alternative isolation technologies, such as optocouplers and transformers. For more information, visit www.silabs.com/isolation.

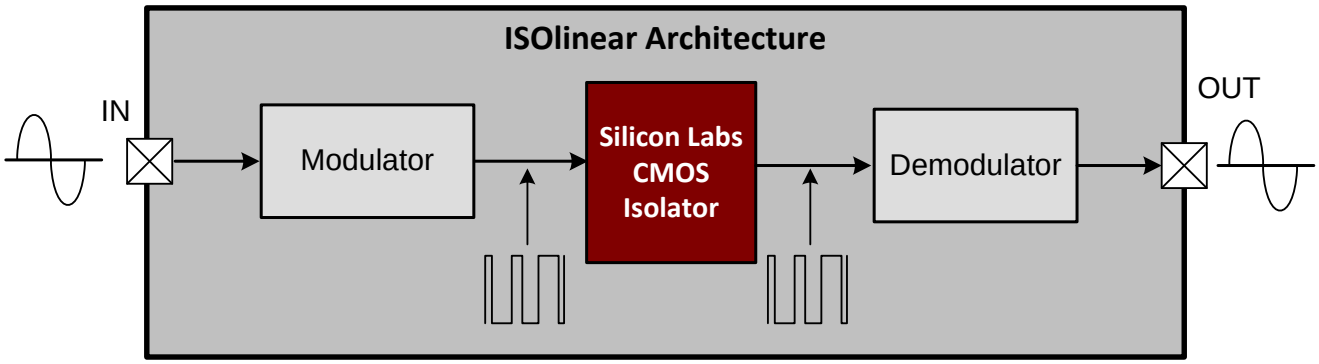

Figure 1. ISOlinear Design Architecture

Table 1. Circuit Performance

Circuit #	Resolution (Bits)	PWM frequency (MHz)	Bandwidth (kHz)	Output Ripple (mV)	Noise Density $\frac{\mu Vrms}{\sqrt{Hz}}$
1	12	1.12	100	10 mV	0.58
2	10	2	500	40 mV	1.10
3	9	2.25	250	10 mV	1.43

2. Design Considerations

This reference design uses a self-oscillating PWM modulator and fourth order filter demodulator circuits. Circuit performance is determined by the configuration of these two blocks as detailed in the following sections.

2.1. Noise and Ripple vs. Modulation Frequency

As shown in Table 1 and Figure 2, noise density is related to PWM modulation frequency where increasing modulator frequency results in higher noise density. The noise sources for all three circuits are a combination of thermal noise from both active and passive components and phase noise generated by the digital isolator.

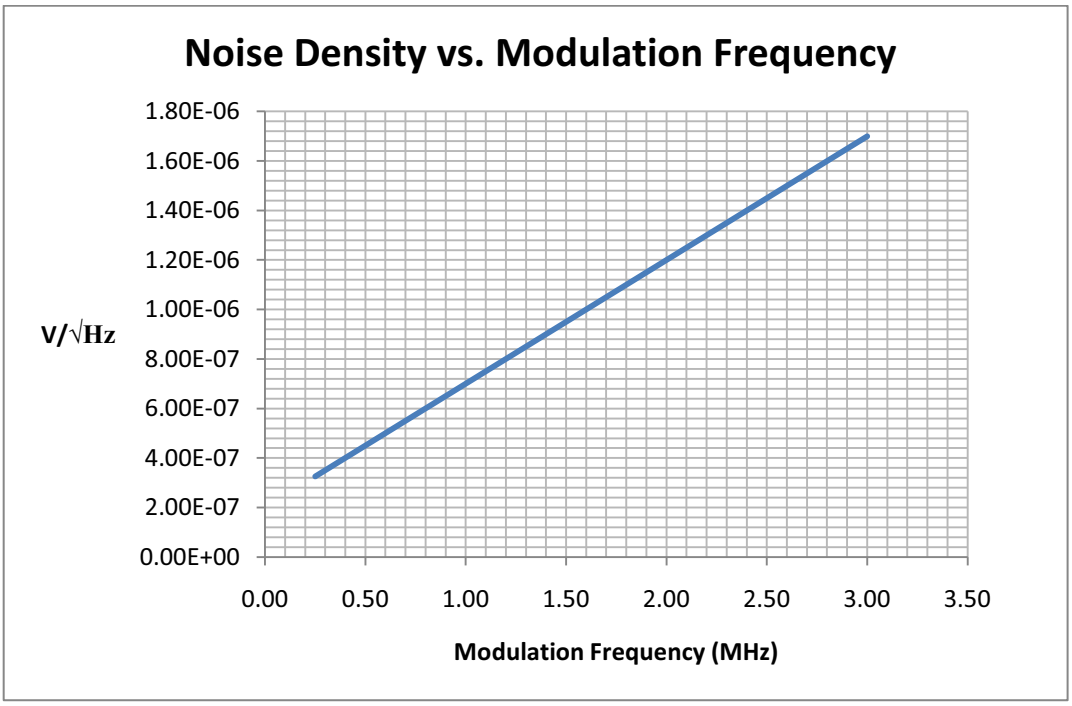

Figure 2. Trend Line Characterization (Noise Density vs. Modulation Frequency)

Therefore, it is important to optimize the PWM modulation frequency (F_{mod}) for the desired signal bandwidth. Too low an F_{mod} minimizes noise density but can increase output ripple (depending on the output filter design), and too high an F_{mod} reduces output ripple but increases noise density. Therefore, modulation frequency must be chosen for the compromise of noise density and output ripple.

2.2. Modulator Operation

This circuit is shown in the Si86xx isolinear reference design documentation. There are two circuit variations: One uses an individual op-amp and comparator, and the other uses a quad op-amp package in which the comparator function is implemented with an op-amp.

The self-oscillating modulator (see Figure 3) consists of an op-amp integrator and comparator with hysteresis. The comparator has an hysteresis voltage range determined by the values of R_F and R_{IN}. For a given comparator output state, the integrator output voltage ramps until the comparator's threshold is reached, at which time the comparator output changes state and the cycle repeats. The opamp used in this modulator design must have a slew rate >>$2F_{mod}$ and rail-to-rail outputs. The comparator must have a response time <10 ns.

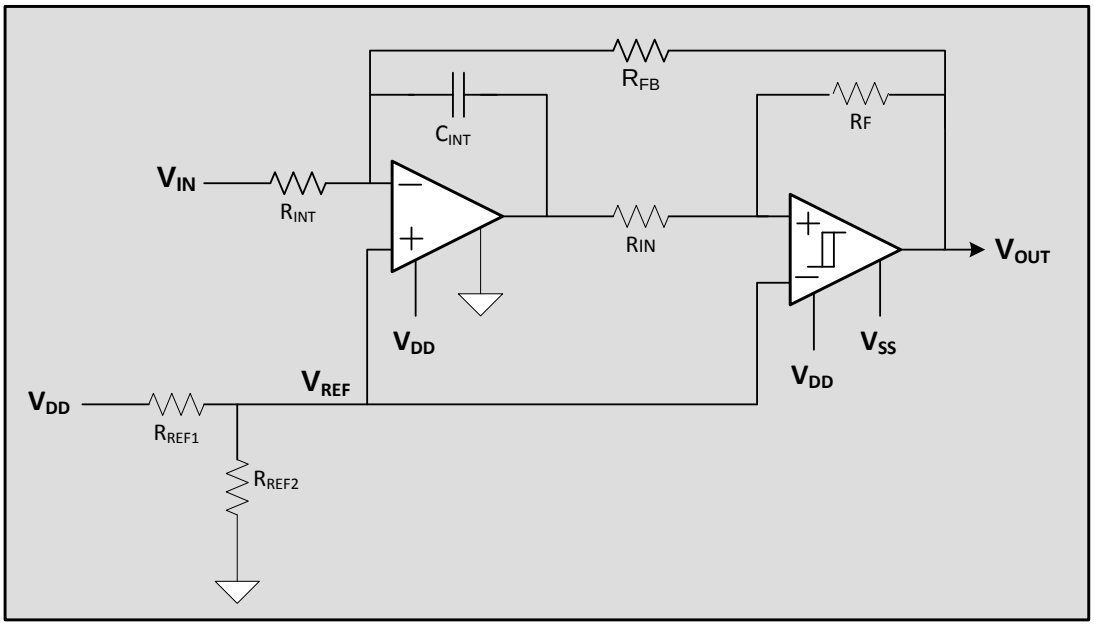

Figure 3. Self-Oscillating PWM Modulator

2.3. Determining Optimum Modulator Frequency

Modulator frequency selection starts with generating a noise budget for the application, then using Figure 2 to find the corresponding modulation frequency. For example, a maximum noise budget of 1.2 µV/√Hz requires a modulation frequency of 2.0 MHz. A good theoretical estimate of the circuit total noise and achievable signal-to-noise (SNR) can be made using the following equations:

$$\text{Noise (rms)} = \text{Noise Density}\left(\frac{V}{\sqrt{Hz}}\right) \times \sqrt{\text{Signal Bandwidth}}$$

Equation 1.

$$\text{SNR (dB)} = 20 \times \log_{10}\frac{\text{Signal (rms)}}{\text{Noise(rms)}}$$

Equation 2.

$$\text{Resolution (bits)} \sim \frac{\text{SNR (dB)}}{6}$$

Equation 3.

For example, the circuit total noise for a design having an input signal amplitude of 1 Vrms, a bandwidth of 100 kHz, and a modulation frequency of 2 MHz would be as follows:

$$\text{Noise density (for 2 MHz from Figure 2)} = \frac{1.2\ \mu\text{Vrms}}{\sqrt{Hz}}$$

$$\text{Noise (rms)} = 1.2 \times \sqrt{100e3} = 379.5\ \mu\text{Vrms}$$

$$\text{SNR(dB)} = 20\text{x}\log\left(\frac{1}{0.0003795}\right) = 68.4$$

$$\text{Resolution} = \left(\frac{68.4}{6}\right) = 11.4\ \text{bits}$$

Equation 4.

2.4. Setting Modulator Frequency

The values of C_{INT}, R_{INT}, R_{IN}, and R_F determine the modulator oscillator oscillation frequency and amplitude and are calculated using Equation 5.

$$\text{Modulation Frequency} = F_{mod} = \frac{1}{T} = \frac{1}{4R_{INT}C_{INT}R_{IN}} \times \frac{R_F}{R_{IN}}$$

Equation 5.

From the above derivation, C_{INT}, R_{INT}, and R_{IN}, R_F together determine the modulation frequency and the modulator's output amplitude. For example, in Equation 5, if R_F = 1.6 kΩ, R_{IN} = 1 kΩ, R_{INT} = 1 kΩ, and C_{INT} = 1 nF, F_{mod} would be 400 kHz. Table 2 shows measured typical SNR results for all three circuits as measured on the Silicon Labs ISOlinear reference design board (available at www.silabs.com/isolation).

Table 2. Circuit SNR vs. Bandwidth

	SNR(dB)				
Signal Bandwidth → Fsig	10 kHz	50 kHz	100 kHz	250 kHz	500 kHz
Circuit 1: 12 bits, Fmod = 1.12 MHz	81.8	74.8	71.8	67.8	64.8
Circuit 2: 10 bits, Fmod = 2.00 MHz	76	69	66	62	59.2
Circuit 3: 9 bits, Fmod = 2.25 MHz	67.8	60.8	57.8	53.8	50.8

2.5. Filter Optimization

Figure 4 shows the fourth-order output filter used in the Silicon Labs reference design board. It is based on Sallen-Key topology with Butterworth response and unity pass-band gain. Note that a lower-order filter can be used if the ripple requirements are relaxed.

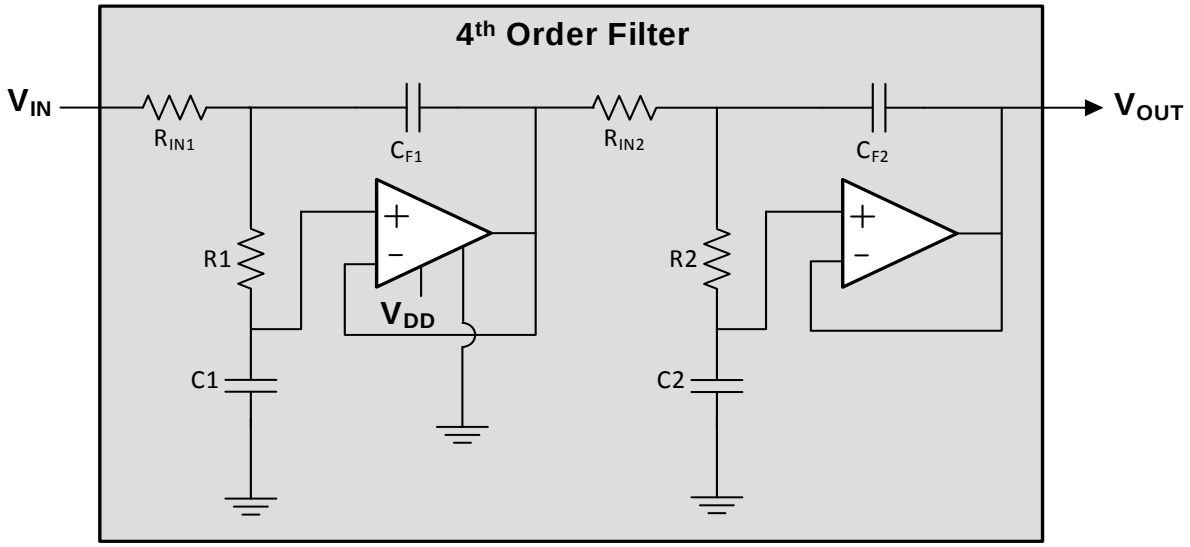

Figure 4. 4th Order Output Filter

A Butterworth filter is chosen for its maximally flat passband response and moderately steep roll-off above the cut-off frequency and is more than adequate for most linear isolator applications. While active filter design theory is beyond the scope of this application note, filter design can be simplified with the help of well-established look-up tables and by using a generic transfer function. For example, Table 3 shows the pole locations look-up table for Butterworth response for various orders.

Table 3. Butterworth Filter Pole Locations

Filter Order	Stages	Total Poles	Pole Locations
2	1	2	p1 = –0.7071 + j0.7071 p2 = –0.7071 – j0.7071
3	2	3	p1 = –0.5 + j0.8660 p2 = P0.5 – j0.8660 p3 = –1 + j0
4	2	4	p1 = –0.9239 + j0.3827 p2 = –0.9239 – j0.3827 p3 = –0.3827 +j0.9239 p4 = –0.3827 – j0.9239

The pole locations listed in Table 3 are the roots of the polynomial equations for corresponding filter order. The basic building block of all higher-order filters is the second-order filter shown in Figure 5.

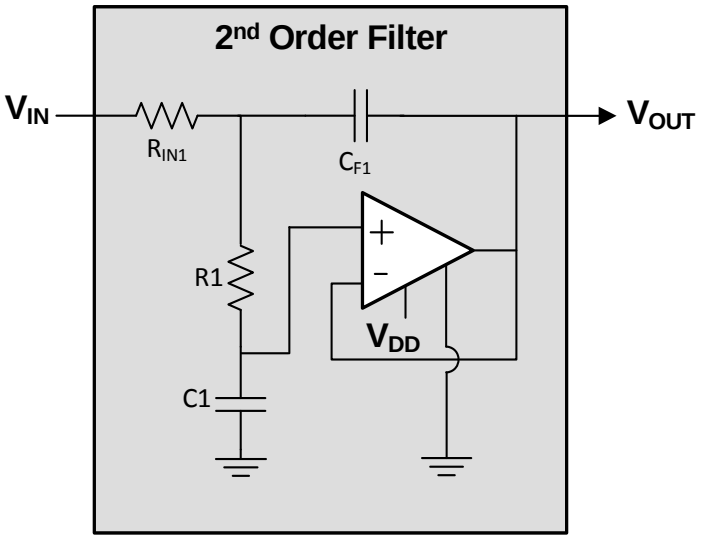

Figure 5. Basic 2nd Order Filter

The design process is as follows:

1. Convert the poles given in Table 3 into quadratic equation form as shown in Equation 6.

$$(s - p1)(s - p2) = s^2 - s(p1 + p2) + p1p2$$

Equation 6.

2. Equate the coefficients to the denominator of the second-order transfer function shown in Equation 7. (**Note**: use R1 = R_{IN1} = 1 for design simplification).

$$\frac{Vout(s)}{Vin(s)} = \frac{1}{s^2(C_{F1}C_1R_{IN1}R_1) + sC_1(R_{IN1} + R_1) + 1}$$

$$\text{Assuming } C_{F1}C_1R_{IN1}R_1 = 1;\ C(R_{IN} + R) = -(p1 + p2);\ 1 = p1p2$$

Equation 7.

3. Determine the values of C_{F1} and C_1.
4. Proportionally scale the values of R_{IN1}, R_1, C_{F1}, and C_1 to get standard component values.
5. Further scale down C_{F1} and C_1 by a factor of $2\pi F_{3dB}$ to achieve the desired pass band frequency.
6. Verify the pass band frequency using Equation 8.

$$F_{cutoff} = \frac{1}{2\pi\sqrt{R_{IN1}R_1C_{F1}C_1}}$$

Equation 8.

7. Repeat Steps 1 to 6 for the next stage component values using the next set of poles (p3 and p4 in case of fourth-order filter) and cascade them (Figure 4).
8. For an odd order filter, follow the pole location of the even order filter and scale the component values.

Example: use the above process to design a fourth-order Butterworth filter:

1. Substituting first stage filter pole locations p1 and p2 from the last row of Table 3 into Equation 6 and simplifying the equation:

$$s^2 + 1.8478s + 1$$

Equation 9.

Repeating the previous step for the second stage filter pole locations p3 and p4 (Table 3, last row) into Equation 6 and simplifying the equation:

$$s^2 + 0.7654s + 1$$

Equation 10.

2. Equating coefficients of Equation 9 for the first stage to that of Equation 7's denominator:

$$s2 + 1.8478s + 1 = s^2(C1C_{F1}R_{IN1}R1) + sC1(R_{IN1} + R1) + 1\ (stage1)$$
$$= C_{F1}C1R_{IN1}R1 = 1;C1(R_{IN1} + R1) = 1.8478$$

Equation 11.

Repeating the previous step, this time for the second-stage filter:

$$s2 + 0.7654s + 1 = s^2(C_{F2}C2R_{IN2}R2) + sC2(R_{IN2} + R2) + 1\ (stage2)$$
$$= C_{F2}C2R_{IN2}R2 = 1;\ C2(R_{IN2} + R2) = 0.7645$$

Equation 12.

3. Determining the values for C_{F1} and C1 by setting R_{IN1} = R1 = 1 Ω and R_{IN2} = R2 = 1 Ω:

For first stage:

$$C_{F1}C1R_{IN1}R1 = 1;\ C1\ (R_{IN1} + R1) = 1.8478$$

Setting R_{IN1} = R1 = 1Ω, we get

$$C_{F1}C1 = 1;\ 2C1 = 1.8478$$

Equation 13.

For second stage:

$$C_{F2}C2R_{IN2}R2 = 1;\ C2\ (R_{IN2} + R2) = 1.8478$$

Setting R_{IN2} = R2 = 1Ω, we get

$$C_{F2}C2 = 1;\ 2C2 = 1.8478$$

Equation 14.

4. Determining component values products calculated in Step 3:

$$R_{IN1} = R1 = 1\Omega;\ C1 = \frac{1.8478}{2} = 0.924\text{F};\ C_{F1} = \frac{1}{C1} = 1.08\text{F (stage 1)}$$

Equation 15.

$$R_{IN2} = R2 = 1\Omega;\ C2 = \frac{0.7654}{2} = 0.383\text{F};\ C_{F2} = \frac{1}{C2} = 2.61\text{F (stage 2)}$$

Equation 16.

5. Scaling Rs up by 1k and Cs down by 1k results in the following component values:

$$R_{IN1} = R1 = 1\text{k}\Omega;\ C_{F1} = 1.08\ \text{mF};\ C1 = 0.924\ \text{mF (stage 1)}$$

Equation 17.

$$R_{IN2} = R2 = 1\text{k}\Omega;\ C_{F2} = 2.61\ \text{mF};\ C2 = 0.383\ \text{mF (stage 2)}$$

Equation 18.

6. Setting the desired Fcutoff=100 kHz, we further scale down capacitors by 2 *100k results in the following values:

$$R_{IN1} = R1 = 1\text{k}\Omega;\ C_{F1} = 1.7\ \text{nF};\ C1 = 1.4\ \text{F (stage 1)}$$

Equation 19.

$$R_{IN2} = R2 = 1\text{k}\Omega;\ C_{F2} = 4.15\ \text{nF};\ C2 = 0.61\ \text{nF (stage 2)}$$

Equation 20.

7. Calculating the cutoff frequency using Equation 16:

$$F_{cutoff1} = \frac{1}{2\pi\sqrt{R_{IN1}R1C_{F1}C1}} = \frac{1}{2\pi\sqrt{1\ k\Omega \times 1\ k\Omega \times 1.7\ nF \times 1.4\ nF}} = 101\ kHz\ (stage\ 1)$$

Equation 21.

$$F_{cutoff2} = \frac{1}{2\pi\sqrt{R_{IN2}R2C_{F2}C2}} = \frac{1}{2\pi\sqrt{1\ k\Omega \times 1\ k\Omega \times 4.15\ nF \times 0.61\ nF}} = 100\ kHz\ (stage\ 2\ )$$

Equation 22.

8. Cascade the two stages for a 4th order filter with a pass band of ~100 kHz.

It is highly recommended that resistor values be limited to a range from 1 to 5 kΩ and that capacitor values be higher than 10 pF so that parasitic capacitive coupling does not influence the frequency response. For higher-order filter designs, repeat the above design process for each stage and cascade them. Note the opamps used in the filter must have a GBWP > 100 times F_{3dB} and a slew rate > 2 x π x Vout x F_{3dB}. The opamp common mode input range must be higher than the filter input peak voltage.

Other filter topologies can also be used (depending on the requirements of the end application) and are compared in Table 4. For example, selecting Chebyshev topology enables the use of a lower modulation frequency because of its steeper gain roll-off, which reduces output ripple and noise and improves SNR.

Table 4. Filter Selection

Filter Type	Advantages	Disadvantages
Butterworth	■ Maximally flat pass band response	■ Moderate gain roll-off in transition band ■ Slight overshoot to pulse response
Bessel	■ Minimal distortion and overshoot to pulse response ■ Flat pass band response	■ Slower gain roll-off in transition band
Chebyshev	■ Faster gain roll-off in transition band	■ Exhibits ripple in pass band response ■ Larger overshoot and distortion to pulse response

3. Reference Design Kit

The Silicon Labs ISOlinear reference design kit comes with an evaluation board, schematics, board layout, and bill-of-materials (BOM). This kit is available from Silicon Labs at www.silabs.com/isolation.

Table 5. Ordering Guide

Ordering Part Number	Description
Si86ISOLIN-KIT	High-performance analog isolation reference design using the Si86xx digital isolators

4. Summary

Isolinear reference design based on Si86xx isolators offers 5 kVrms analog isolation as an alternative to expensive analog isolation with the added benefits of user-flexibility, greater economy, and competitive performance. Proper selection of system parameters can further enhance performance and cost.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated Figure 4 on page 4.
- Updated Figure 5 on page 5.

Revision 0.2 to Revision 0.3

- Updated "2.2. Modulator Operation" on page 2.
- Updated Equation 1.
- "2.4. Setting Modulator Frequency" on page 4.
- Updated Table 3 on page 5.
  - Corrected 2nd pole location information for 3rd order filter.
- Corrected Equation 7 and Equation 8 on page 6.
- Corrected Equation 14 on page 7.

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