EFM8BB2

8-bit MCU Family with up to 16 kB of Flash

Memory

- Up to 16 kB flash
- 15 kB of flash organized in 512-byte sectors
- 1 kB of flash organized in 64-byte sectors
- Up to 2.25 kB RAM (2k + 256)

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers

12-Bit Analog-to-Digital Converter

- Up to 20 external input channels
- Up to 200 ksps 12-bit mode or 800 ksps 10-bit mode
- Internal VREF or external VREF supported

Clock Options

- High-frequency 48 MHz oscillator, ±2% accuracy over supply and temperature
- Low-current 24.5 MHz oscillator, ±2% accuracy over supply and temperature
- Low-current 80 kHz oscillator
- External CMOS input, up to 50 MHz.
- Flexible clock divider to generate frequencies at /1, /1.5, /2, /3, /4, /6, /8, ... /128 of selected clock.

Two Analog Comparators

- Programmable hysteresis and response time
- Internal adjustable reference
- Configurable as interrupt, wake, or reset source
- Low current

Supply Voltage:

- 2.2 to 5.25 V supported with 5V regulator option
- 2.2 to 3.6 V without 5V regulator

Temperature Range: –40 to +85 °C

High-Speed CIP-51 µC Core

- Efficient, pipelined instruction architecture
- Up to 50 MIPS operation
- Uses standard 8051 instruction set
- Expanded interrupt handler

Communication Peripherals

- Two UARTs
- SMBus™ master/slave
- High-speed (3.4 Mbps) I^2C slave
- SPI™

Timer/Counters and PWM

- 5 General-Purpose 16-bit Timer/Counters
- 16-bit Programmable Counter Array (PCA) with three channels of PWM, capture/compare, or frequency output capability, and hardware kill/safe state capability

General-Purpose I/O

- Up to 22 GPIO
- 5 V-Tolerant
- Crossbar-enabled

Additional Support Peripherals

- Independent watchdog timer clocked from LFO
- 16-bit CRC engine

Unique Identifier

- 32-bit unique key for each device

Package Options

- 20-pin QFN, 3 x 3 mm
- 24-pin QSOP
- 28-pin QFN, 5 x 5 mm

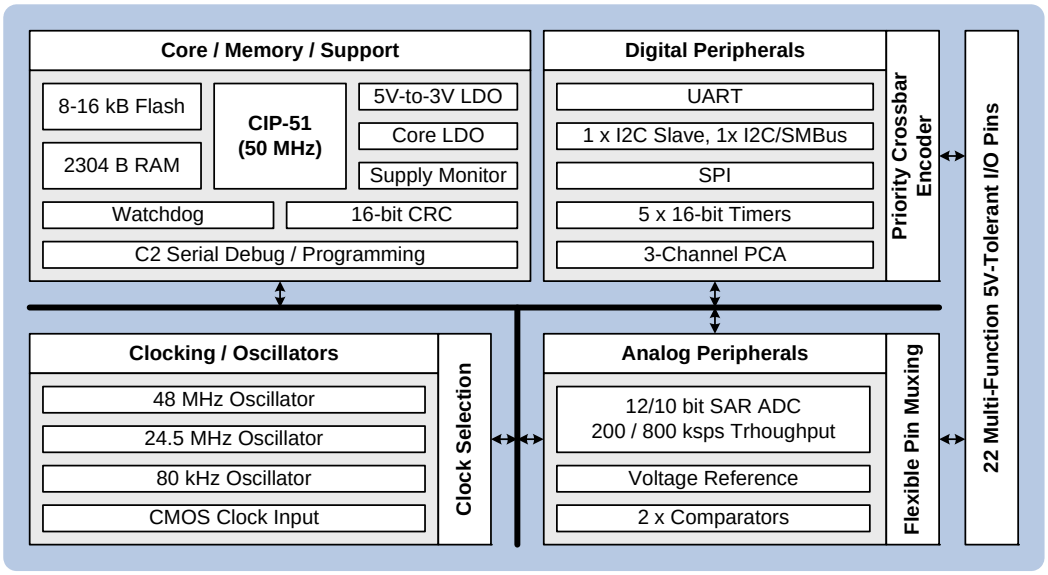

Table of Contents

1. Electrical Specifications

The specifications in this section are preliminary estimates for products in development, and will change after full silicon characterization. All of these estimates are based on design simulations and/or characterization of existing products with similar features, and are provided as guidance only.

1.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1, unless stated otherwise.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}		2.7	—	5.25	V
System Clock Frequency	f_{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C

Notes:
1. All voltages with respect to GND

Table 1.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode—Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 48 MHz[3]	—	11	TBD	mA
		F_{SYSCLK} = 24.5 MHz[3]	—	6.4	TBD	mA
		F_{SYSCLK} = 1 MHz[3]	—	450	TBD	µA
		F_{SYSCLK} = 80 kHz[4]	—	145	TBD	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 48 MHz[3]	—	5.5	TBD	mA
		F_{SYSCLK} = 24.5 MHz[3]	—	2.7	TBD	mA
		F_{SYSCLK} = 1 MHz[3]	—	210	TBD	µA
		F_{SYSCLK} = 80 kHz[4]	—	125	TBD	µA
Suspend Mode—Core halted and high frequency clocks stopped, Supply Monitor disabled.	I_{DD}	LFO Running	—	118	TBD	µA
		LFO Stopped	—	113	TBD	µA

Notes:
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
4. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
5. ADC0 always-on power excludes internal reference supply current.
6. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Snooze Mode—Core halted and high frequency clocks stopped. Regulator in low-power state, Supply Monitor disabled.	I_{DD}	LFO Running	—	17	TBD	µA
		LFO Stopped	—	12	TBD	µA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I_{DD}	Internal LDO ON	—	100	TBD	µA
		Internal LDO OFF	—	0.1	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	155	—	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 48 MHz, T_A = 25 °C	—	TBD	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	3.5	—	µA
ADC0 Always-on[5]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	845	1200	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	425	580	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	370	—	µA
		100 ksps, V_{DD} = 3.0 V	—	185	—	µA
		10 ksps, V_{DD} = 3.0 V	—	19	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	490	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	530	—	µA
		50 ksps, V_{DD} = 3.0 V	—	265	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA

Notes:

2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.

3. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.

4. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.

5. ADC0 always-on power excludes internal reference supply current.

6. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on[6]	I_{IREF}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPnMD = 11	—	0.5	—	µA
		CPnMD = 10	—	3	—	µA
		CPnMD = 01	—	10	—	µA
		CPnMD = 00	—	25	—	µA
Comparator Reference	I_{CPREF}		—	TBD	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Notes:

2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.

3. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.

4. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.

5. ADC0 always-on power excludes internal reference supply current.

6. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to $V_{DD} \geq 2.2$ V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
$\overline{RST}$ Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{SYSCLK} > 1$ MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 1.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1,2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1,2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming[3]	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the OSCICL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 1.5. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (48 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	45	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

Table 1.6. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

Table 1.7. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.		1.1		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB

***Note:** Absolute input pin voltage is limited by the V_{DD} supply.

Table 1.7. ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	–3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

***Note:** Absolute input pin voltage is limited by the V_{DD} supply.

Table 1.8. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	µA

Table 1.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	757	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	17	—	mV
Slope	M		—	2.85	—	mV/°C
Slope Error*	E_M		—	70	—	µV/°C
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

Table 1.10. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range[1]	V_{REGIN}		2.7	—	5.25	V
Output Voltage on VDD[2]	V_{REGOUT}	Output Current = 1 to 100 mA	3.1	3.3	3.6	V
Output Current[2]	I_{REGOUT}		—	—	100	mA

Notes:
1. Input range specified for regulation. When an external regulator is used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

Table 1.11. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPnMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CPnMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysteresis Mode 0 (CPnMD = 00)	HYS_{CP+}	CPnHYP = 00	—	0.4	—	mV
		CPnHYP = 01	—	8	—	mV
		CPnHYP = 10	—	16	—	mV
		CPnHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPnMD = 00)	HYS_{CP-}	CPnHYN = 00	—	-0.4	—	mV
		CPnHYN = 01	—	–8	—	mV
		CPnHYN = 10	—	–16	—	mV
		CPnHYN = 11	—	–32	—	mV
Positive Hysteresis Mode 1 (CPnMD = 01)	HYS_{CP+}	CPnHYP = 00	—	0.5	—	mV
		CPnHYP = 01	—	6	—	mV
		CPnHYP = 10	—	12	—	mV
		CPnHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPnMD = 01)	HYS_{CP-}	CPnHYN = 00	—	-0.5	—	mV
		CPnHYN = 01	—	–6	—	mV
		CPnHYN = 10	—	–12	—	mV
		CPnHYN = 11	—	–24	—	mV
Positive Hysteresis Mode 2 (CPnMD = 10)	HYS_{CP+}	CPnHYP = 00	—	0.7	—	mV
		CPnHYP = 01	—	4.5	—	mV
		CPnHYP = 10	—	9	—	mV
		CPnHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPnMD = 10)	HYS_{CP-}	CPnHYN = 00	—	-0.6	—	mV
		CPnHYN = 01	—	–4.5	—	mV
		CPnHYN = 10	—	–9	—	mV
		CPnHYN = 11	—	–18	—	mV

Table 1.11. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPnMD = 11)	HYS_{CP+}	CPnHYP = 00	—	1.5	—	mV
		CPnHYP = 01	—	4	—	mV
		CPnHYP = 10	—	8	—	mV
		CPnHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPnMD = 11)	HYS_{CP-}	CPnHYN = 00	—	-1.5	—	mV
		CPnHYN = 01	—	–4	—	mV
		CPnHYN = 10	—	–8	—	mV
		CPnHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N_{bits}			6		bits
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C

Table 1.12. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}		V_{DD} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND ≤ V_{IN} ≤ V_{DD}	–1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{DD}	I_{LK}	V_{DD} < V_{IN} < V_{DD}+2.0 V	0	5	150	µA

1.2. Thermal Conditions

Table 1.13. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	QFN-20 Packages	—	60	—	°C/W
		QFN-28 Packages	—	TBD	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

1.3. Absolute Maximum Ratings

Stresses above those listed under Table 1.14 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 1.14. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		GND–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND–0.3	5.8	V
Voltage on I/O pins or RSTb	V_{IN}	$V_{DD} \geq 3.3$ V	GND–0.3	5.8	V
		$V_{DD} < 3.3$ V	GND–0.3	V_{DD}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J		–40	105	°C

Notes:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. System Overview

The EFM8BB2 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 3.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- **Memory:**
  - 16 kB flash, including 1 kB of 64-byte sectors and 15 kB of 512-byte sectors.
  - 2304 bytes RAM (including 256 bytes standard 8051 RAM and 2048 bytes on-chip XRAM)
- **Power:**
  - 5 V-input LDO regulator
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- **I/O: Up to 22 total multifunction I/O pins:**
  - All pins 5 V tolerant under bias
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- **Clock Sources:**
  - Internal 48 MHz oscillator with accuracy of ±1.5%
  - Internal 24.5 MHz oscillator with ±2% accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
- **Timers/Counters and PWM:**
  - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare and frequency output modes
  - 5 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from low frequency oscillator
- **Communications and Digital Peripherals:**
  - 2 UARTs, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™ Master / Slave, up to 400 kbps
  - I^2C High-speed Slave, up to 3.4 Mbps
  - 16-bit CRC Unit, supporting automatic CRC of flash at 256-byte boundaries
- **Analog:**
  - 12-Bit Analog-to-Digital Converter (ADC)
  - 2 x Low-Current Comparators with Adjustable reference
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware.

The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 2.2 to 3.6 V operation (or up to 5.25 V with the 5V regulator option), and are available in 28-pin QFN, 20-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant. The device is specified over the -40 to +85 °C temperature range. See Table 3.1 for ordering information.

2.1. Power

2.1.1. LDOs

The EFM8BB2 devices include an internal regulator to regulate the supply voltage down the core operating voltage of 1.8 V. Additionally, on the EFM8BB22 devices, a 5V-to-3.3V regulator is available, capable of providing up to 100 mA to the system. The LDOs consume little power, but can be put into lower-current modes during snooze, or shut down completely in stop mode.

2.1.2. Voltage Supply Monitor (VMON0)

The EFM8BB2 devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware.

The supply monitor holds the device in reset if the main VDD supply drops below the VDD reset threshold.

2.1.3. Device Power Modes

The EFM8BB2 devices feature several low power modes in addition to normal operating mode, allowing the designer to save power when the core is not in use. All power modes are summarized in Table 2.1.

Table 2.1. EFM8BB2 Power Modes

Mode	Description	Mode Entrance	Mode Exit
Normal	Core and peripherals operating at full speed		
Idle	■ Core halted ■ Peripherals operate at full speed	Set IDLE bit in PCON	Any enabled interrupt or reset source
Suspend	■ Core halted and high-speed oscillators stopped ■ Select peripherals can act as a wake source ■ Regulators in normal bias current mode for fast wake	Switch to 24.5 MHz oscillator using CKCON and Set SUSPEND bit in PCON1	Any enabled wake or reset source
Snooze	■ Core halted and high-speed oscillators stopped ■ Select peripherals can act as a wake source ■ Regulators in low bias current mode to save power	Switch to 24.5 MHz oscillator using CKCON and Set SNOOZE bit in PCON1	Any enabled wake or reset source
Stop	■ All clocks stopped ■ Core LDO and (optionally) comparators still running ■ Pins retain state	Clear STOPCF in REG0MD and Set STOP bit in PCON	Any device reset

Table 2.1. EFM8BB2 Power Modes

Mode	Description	Mode Entrance	Mode Exit
Shutdown	■ All clocks stopped ■ Core LDO and all analog circuits shut down ■ Pins retain state	Set STOPCF in REG0MD and Set STOP bit in PCON	Device pin reset or power-on reset

In addition, the user may choose to lower the clock speed in Normal and Idle modes to save power when the CPU requirements allow for lower speed.

2.2. I/O

2.2.1. General Features

The EFM8BB2 ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes selectable per pin.
- Drive strength selectable per port.
- Port Match allows the device to recognize a change on a port pin value and wake from idle, suspend, or snooze mode or generate an interrupt.
- Internal pull-up resistors can be globally enabled or disabled.
- Two external interrupts provide unique interrupt vectors for monitoring time-critical events.
- Above-rail tolerance allows 5 V interface when device is powered.

2.2.2. Crossbar

The EFM8BB2 devices have a digital peripheral crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PnSKIP registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

2.3. Clocking

The EFM8BB2 devices have two internal oscillators and the option to use an external CMOS input at a pin as the system clock. A programmable divider allows the user to internally run the system clock at a slower rate than the selected oscillator if desired.

2.4. Counters/Timers and PWM

2.4.1. Programmable Counter Array (PCA0)

The EFM8BB2 devices include a three-channel, 16-bit Programmable Counter Array with the following features:

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Three independently-configurable channels.
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation).
- Output polarity control.
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Can accept hardware “kill” signal from comparator 0.

2.4.2. Timers (Timer 0, Timer 1, Timer 2,Timer 3, and Timer 4)

Timers include the following features:

- Timer 0 and Timer 1 are standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Timer 2, Timer 3 and Timer4 can each operate as 16-bit auto-reload or two independent 8-bit auto-reload timers, and include pin or LFO clock capture capabilities.
- Timer 3 and Timer 4 can be chained together to form a 32-bit timer.
- Timer 3 and Timer 4 can run autonomously from the LFO oscillator and Timer 4 may be used to wake the device from suspend or sleep modes.

2.4.3. Watchdog Timer (WDT0)

The watchdog timer includes a 16-bit timer with a programmable reset period. The registers are protected from inadvertent access by an independent lock and key interface.

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Runs from the low frequency oscillator.
- Lock-out feature to prevent any modification until a system reset.

2.5. Communications and other Digital Peripherals

2.5.1. Universal Asynchronous Receiver/Transmitters (UART0 and UART1)

The UARTs use two signals (TX and RX) and a predetermined fixed baud rate to provide asynchronous communications with other devices.

UART0 provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK / 2 (transmit) or SYSCLK / 8 (receive) generated by timer 1.
- 8- or 9-bit data.
- Automatic start and stop generation.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK / 2 (transmit) or SYSCLK / 8 (receive).
- 5, 6, 7, 8. or 9bit data.
- Automatic start and stop generation.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break detection.

2.5.2. Serial Peripheral Interface (SPI0)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI module includes the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to 12 Mbps in master or slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate (master).
- Programmable receive timeout (slave).
- Four byte FIFO on transmit and receive.
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

2.5.3. System Management Bus / I2C (SMBus0)

The SMBus interface is a two-wire, bi-directional serial bus compatible with both I2C and SMBus protocols. The two clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte-oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the system clock as a master or slave, which can be faster than allowed by the SMBus / I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus interface may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.

- Ability to inhibit all slave states.
- Programmable data setup/hold times.

2.5.4. High-Speed I2C Slave (I2C0)

The I2C Slave 0 interface is a 2-wire, bidirectional serial bus that is compatible with the I^2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. The interface also supports clock stretching for cases where the CPU may be temporarily prohibited from transmitting a byte or processing a received byte during an I^2C transaction. It can also operate in suspend and snooze modes without an active system clock and wake the CPU when a matching slave address is received.

It operates only as an I^2C slave device. The I2C0 peripheral provides control of the SCL (serial clock) synchronization, SDA (serial data), SCL Clock stretching, I^2C arbitration logic, and low power mode operation.

The I2C Slave 0 module includes the following features:

- High-speed (up to 3.4 Mbps), fast (400 kbps), and standard (up to 100 kbps) transfer speeds.
- Support for slave mode only.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Two byte FIFO on transmit and receive.
- Can operate in suspend or snooze mode without an active system clock and wake the CPU after receiving a matching slave address.

2.5.5. 16/32-bit CRC (CRC0)

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for four CCITT-16 polynomial.
- Byte-level bit reversal.
- Automatic CRC of flash contents on one or more 256-byte blocks.
- Initial seed selection of 0x0000 or 0xFFFF.

2.6. Analog Peripherals

2.6.1. 12-Bit Analog-to-Digital Converter (ADC0)

The ADC0 module on EFM8BB2 devices is a Successive Approximation Register (SAR) Analog to Digital Converter (ADC). The key features of the ADC module are:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.

2.6.2. Low Current Comparators (CMP0, CMP1)

The comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The Low Power Comparator module includes the following features:

- Multiple sources for the positive and negative inputs, including VDD, VREF, and I/O pins.
- Internal 6-bit reference voltage.
- Two outputs are available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- Provide “kill” signal to PCA module.
- Comparator 0 can be used to reset the device or wake from suspend and snooze modes.

2.7. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the $\overline{\text{RST}}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the Low Frequency Oscillator (LFO0) as its clock source. Program execution begins at location 0x0000.

2.8. On-Chip Debugging

The EFM8BB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3. Ordering Information

All EFM8BB2 family members have the following features:

- CIP-51 Core running up to 50 MHz
- Three Internal Oscillators (48 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 5 16-bit Timers
- 2 Analog Comparators
- 16-bit CRC Unit

In addition to these features, each part number in the EFM8BB2 family has a set of features that vary across the product line. The product selection guide in Table 3.1 shows the features available on each family member.

Table 3.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	5V-to-3.3V Regulator	Temperature Range	Package
EFM8BB22F16G-A-QFN28	16	2304	22	20	10	12	✓	✓	-40 to +85 C	QFN28
EFM8BB21F16G-A-QSOP24	16	2304	21	20	10	12	✓		-40 to +85 C	QSOP24
EFM8BB21F16G-A-QFN20	16	2304	16	15	10	7	✓		-40 to +85 C	QFN20

4. Pin Definitions

4.1. EFM8BB2xFxxG-A-QFN28 Pin Definitions

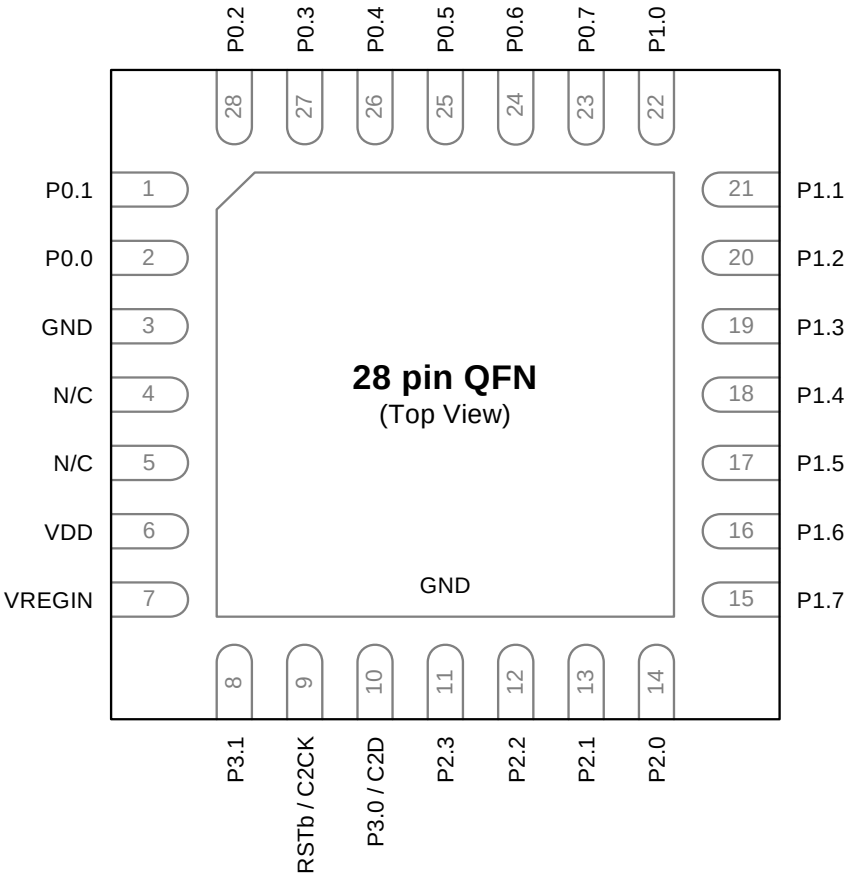

Figure 4.1. EFM8BB2xFxxG-A-QFN28 Pinout

Table 4.1. Pin Definitions for EFM8BB2xFxxG-A-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
3	GND	Ground			

Table 4.1. Pin Definitions for EFM8BB2xFxxG-A-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
4	N/C	No Connection			
5	N/C	No Connection			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	P3.1	Multifunction I/O			
9	$\overline{\text{RST}}$ / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
11	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.23 CP1P.12 CP1N.12
12	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.22 CP1P.11 CP1N.11
13	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.21 CP1P.10 CP1N.10
14	P2.0	Multifunction I/O	Yes	P2MAT.0	ADC0.20 CP1P.9 CP1N.9
15	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CP1P.7 CP1N.7
16	P1.6	Multifunction I/O	Yes	P1MAT.6 I2C0_SCL	ADC0.14 CP1P.6 CP1N.6
17	P1.5	Multifunction I/O	Yes	P1MAT.5 I2C0_SDA	ADC0.13 CP1P.5 CP1N.5

Table 4.1. Pin Definitions for EFM8BB2xFxxG-A-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
19	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CP1P.3 CP1N.3
20	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CP1P.2 CP1N.2
21	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1 CP0P.10 CP0N.10
22	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0 CP0P.9 CP0N.9
23	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7
24	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6
25	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CP0P.5 CP0N.5
26	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CP0P.4 CP0N.4

Table 4.1. Pin Definitions for EFM8BB2xFxxG-A-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
27	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
28	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
Center	GND	Ground			

4.2. EFM8BB2xFxxG-A-QSOP24 Pin Definitions

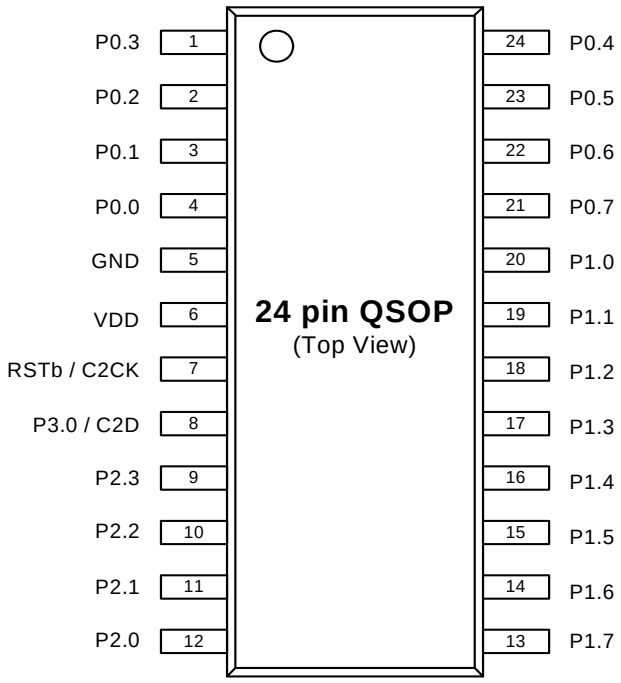

Figure 4.2. EFM8BB2xFxxG-A-QSOP24 Pinout

Table 4.2. Pin Definitions for EFM8BB2xFxxG-A-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
5	GND	Ground			

Table 4.2. Pin Definitions for EFM8BB2xFxxG-A-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	VDD	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.23 CP1P.12 CP1N.12
10	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.22 CP1P.11 CP1N.11
11	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.21 CP1P.10 CP1N.10
12	P2.0	Multifunction I/O	Yes	P2MAT.0	ADC0.20 CP1P.9 CP1N.9
13	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CP1P.7 CP1N.7
14	P1.6	Multifunction I/O	Yes	P1MAT.6 I2C0_SCL	ADC0.14 CP1P.6 CP1N.6
15	P1.5	Multifunction I/O	Yes	P1MAT.5 I2C0_SDA	ADC0.13 CP1P.5 CP1N.5
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
17	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CP1P.3 CP1N.3
18	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CP1P.2 CP1N.2

Table 4.2. Pin Definitions for EFM8BB2xFxxG-A-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1 CP0P.10 CP0N.10
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0 CP0P.9 CP0N.9
21	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7
22	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6
23	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CP0P.5 CP0N.5
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CP0P.4 CP0N.4

4.3. EFM8BB2xFxxG-A-QFN20 Pin Definitions

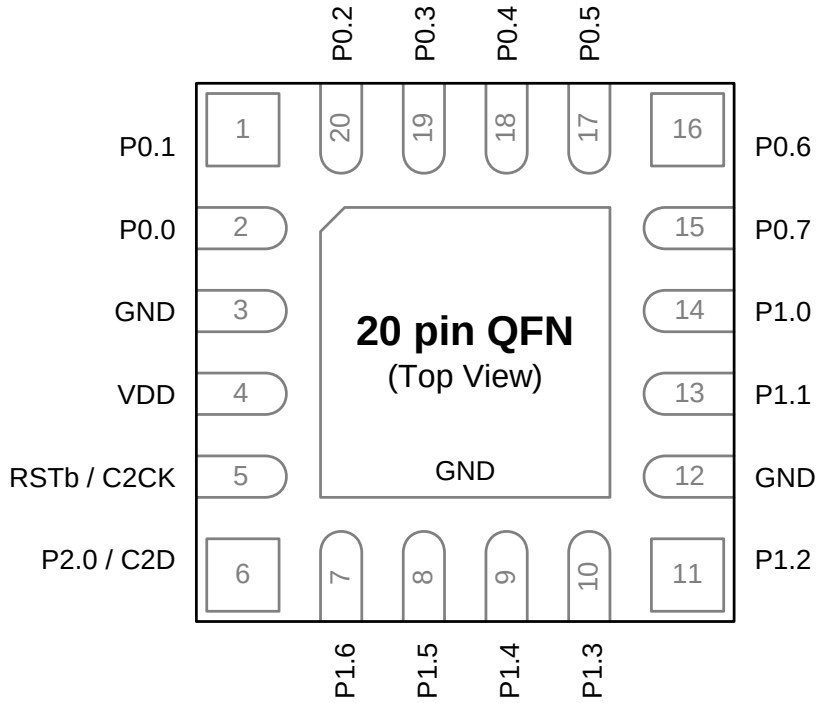

Figure 4.3. EFM8BB2xFxxG-A-QFN20 Pinout

Table 4.3. Pin Definitions for EFM8BB2xFxxG-A-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
3	GND	Ground			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Table 4.3. Pin Definitions for EFM8BB2xFxxG-A-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P2.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		
7	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CP1P.6 CP1N.6
8	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CP1P.5 CP1N.5
9	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
10	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SCL	ADC0.11 CP1P.3 CP1N.3
11	P1.2	Multifunction I/O	Yes	P1MAT.2 I2C0_SDA	ADC0.10 CP1P.2 CP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1 CP0P.10 CP0N.10
14	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0 CP0P.9 CP0N.9
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6

Table 4.3. Pin Definitions for EFM8BB2xFxxG-A-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CP0P.5 CP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CP0P.4 CP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
Center	GND	Ground			

5. QFN-28 Package Specifications

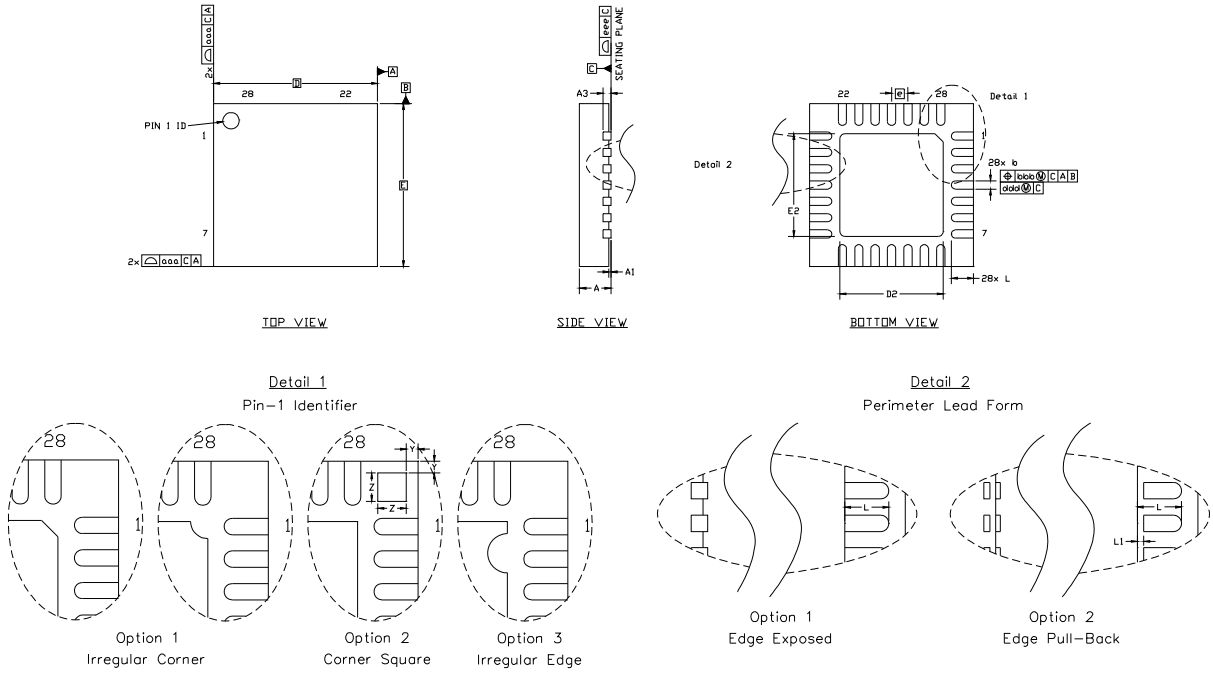

Figure 5.1. QFN-28 Package Drawing

Table 5.1. QFN-28 Package Dimensions

Dimension	Min	Typ	Max		Dimension	Min	Typ	Max
A	0.80	0.90	1.00		L	0.35	0.55	0.65
A1	0.00	0.02	0.05		L1	0.00	—	0.15
A3		0.25 REF			aaa		0.15	
b	0.18	0.23	0.30		bbb		0.10	
D		5.00 BSC.			ddd		0.05	
D2	2.90	3.15	3.35		eee		0.08	
e		0.50 BSC.			Z		0.44	
E		5.00 BSC.			Y		0.18	
E2	2.90	3.15	3.35					

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

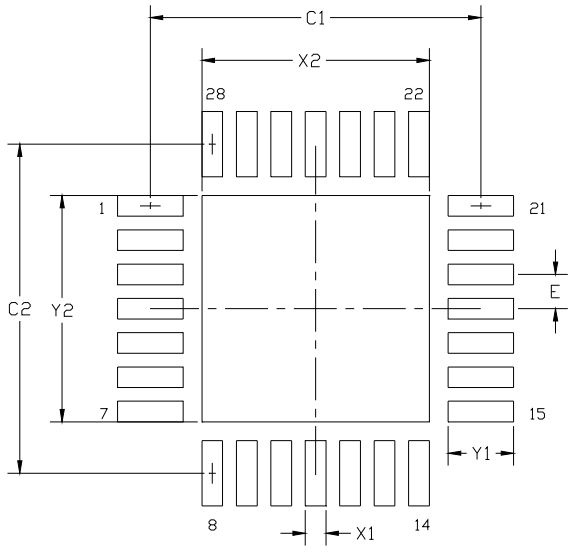

Figure 5.2. QFN-28 Recommended PCB Land Pattern

Table 5.2. QFN-28 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	
C2	4.80	
E	0.50 BSC	
X1	0.20	0.30

Dimension	Min	Max
X2	3.20	3.30
Y1	0.85	0.95
Y2	3.20	3.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 0.90 mm x 0.90 mm openings on a 1.10 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. QSOP-24 Package Specifications

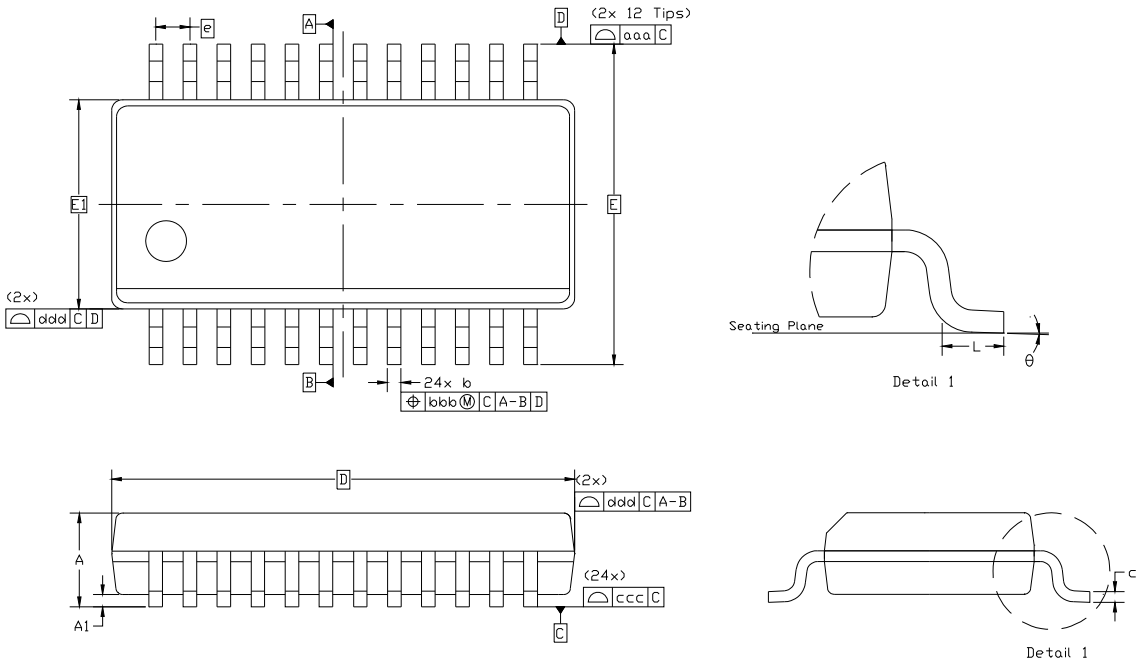

Figure 6.1. QSOP-24 Package Drawing

Table 6.1. QSOP-24 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		

Dimension	Min	Nom	Max
e	0.635 BSC		
L	0.40	—	1.27
θ	0º	—	8º
aaa	0.20		
bbb	0.18		
ccc	0.10		
ddd	0.10		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

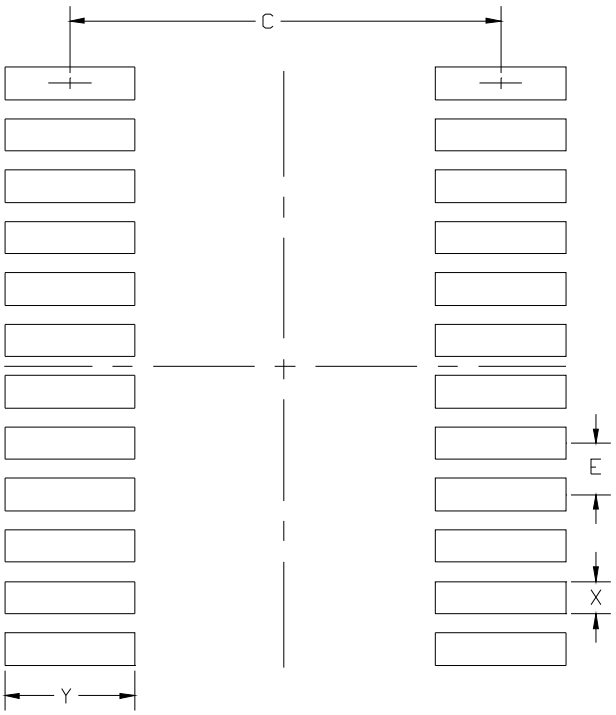

Figure 6.2. QSOP-24 PCB Land Pattern

Table 6.2. QSOP-24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. QFN-20 Package Specifications

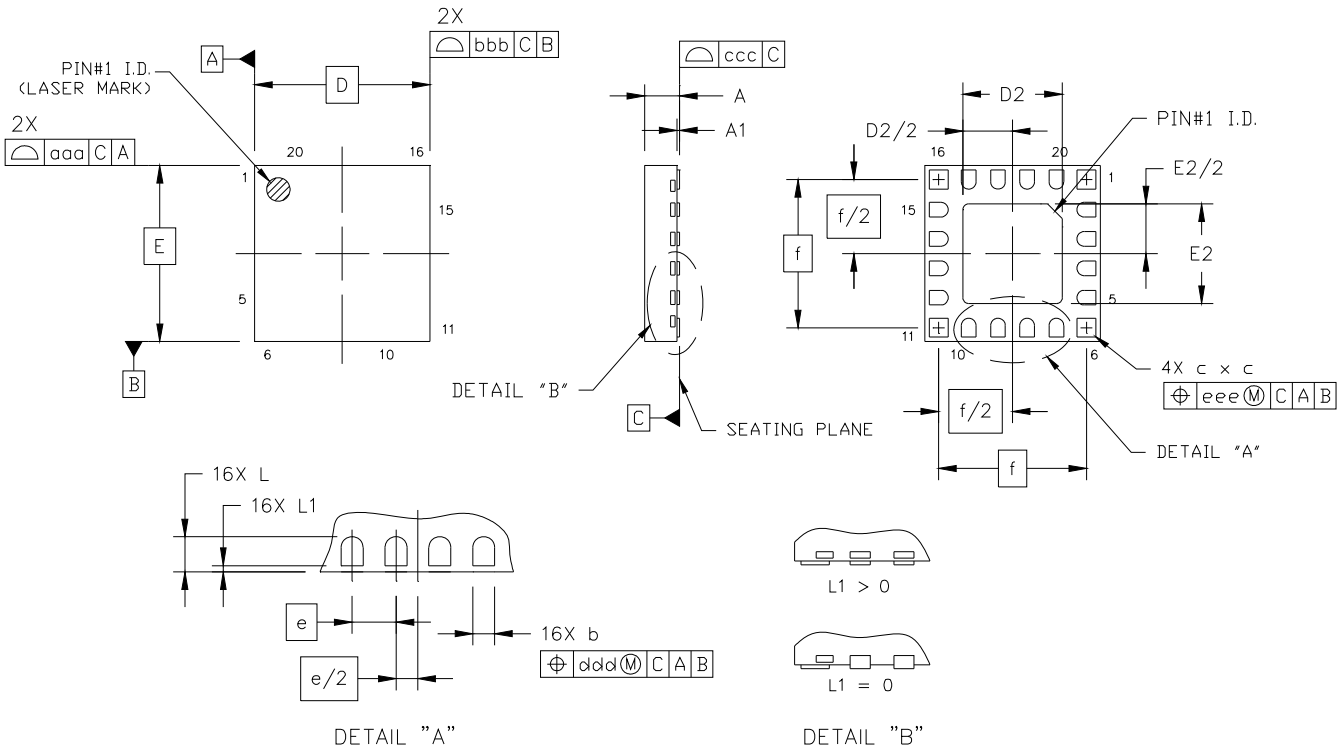

Figure 7.1. QFN-20 Package Drawing

Table 7.1. QFN-20 Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	1.70	1.8
e		0.50 BSC	
E		3.00 BSC	
E2	1.6	1.70	1.8

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.3	0.40	0.5
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:
1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

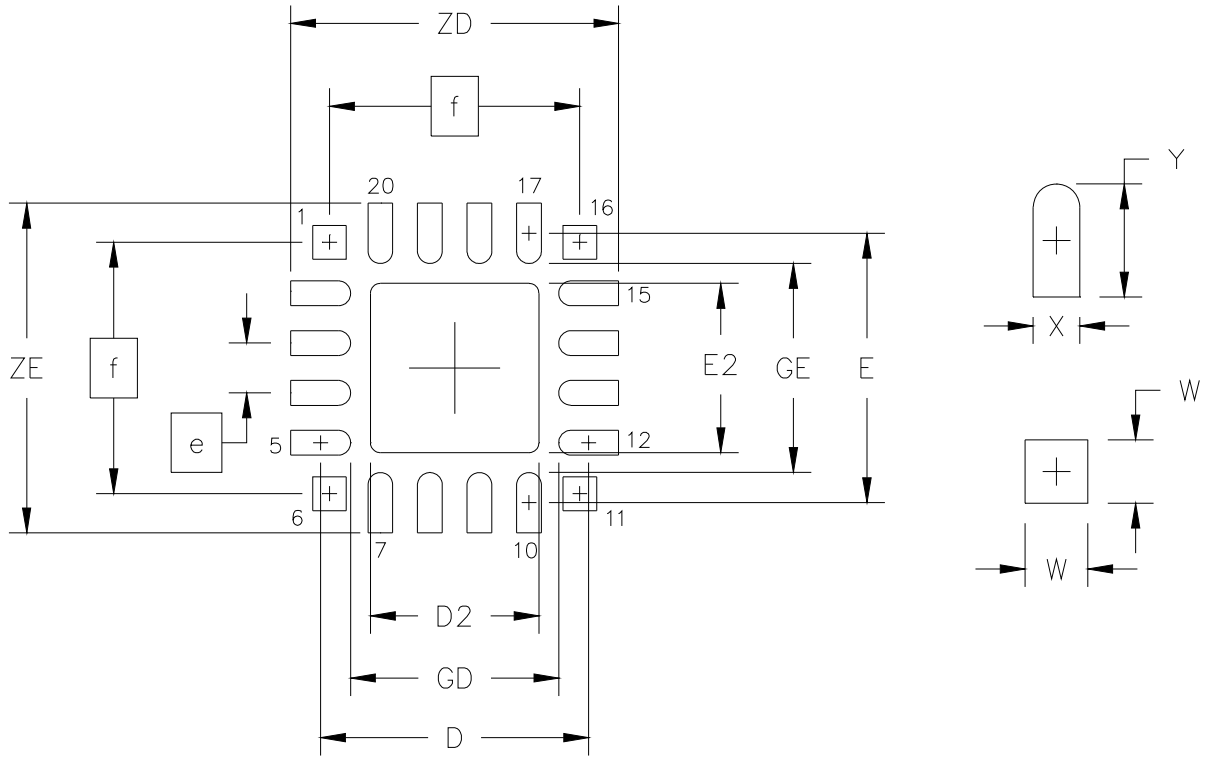

Figure 7.2. QFN-20 Landing Diagram

Table 7.2. QFN-20 Landing Diagram Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.