



Quick Start Guide

BSC9131RDB

QorIQ Qonverge BSC9131
Reference Design Board



freescale[™]
QorIQ Qonverge

Get to Know the BSC9131RDB

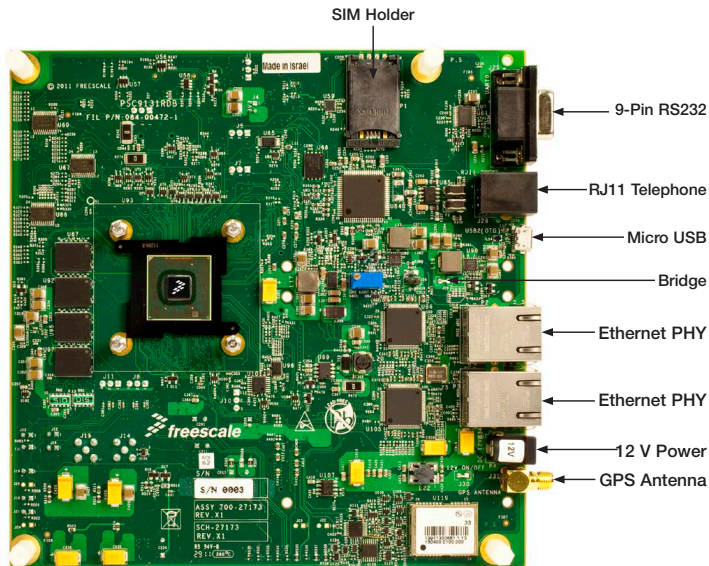


Figure 1: Front side of QorIQ Converge BSC9131RDB.

BSC9131RDB Overview

This quick start guide provides instruction on the various resources required to get started with the BSC9131RDB hardware kit. The BSC9131RDB includes a number of different connectivity and debugging options for the various internal systems of the device.

The BSC9131 device itself contains an e500 Power Architecture® core and an SC3850 StarCore DSP core. The complete system is controlled by the e500 core, which, by default, is set up to boot with u-boot and then run Linux with the user interfacing to u-boot/Linux via a terminal command prompt over the UART connector from the BSC9131RDB. Additional options of running code on the DSP will also be covered in this guide.

Step-by-Step Installation Instructions

In this quick start guide, you will learn how to set up the BSC9131RDB board.

1



Download Software and Tools

Get the installation software and documentation under **“Jump Start Your Design”** at freescale.com/BSC9131RDB.

2

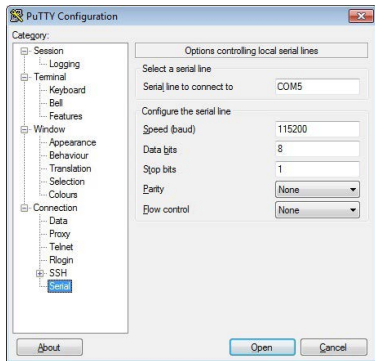
Check Hardware Kit Contents

Hardware Kit Inventory

1. BSC9131RDB board in enclosure (1)
2. Power supply kit (1)
 - a.) AC plug adapter
 - b.) Power cable
 - c.) 12 V, 5.5 A power supply unit
3. USB micro A male to USB A female cable (1)
4. Telephone RJ11 cable (1)
5. RS 232 serial cable DB9 male to USB A male (1)
6. Ethernet cable with RJ45 connectors (1)
7. RF spacer parts
 - a.) 16 mm spacer (8)
 - b.) Screws (16)
8. Active GPS antenna
9. Thumb drive

3 Attach RS232 Cable

In addition to the BSC9131RDB board, the user will also require a PC with a USB interface. Connect the UART (RS232) cable to connector J25 on the BSC9131RDB, and to the USB port on the user's PC.



4 Set Up Serial Connection in PC

1. In the user's PC, in HyperTerminal (standard with Windows XP), or if HyperTerminal is unavailable, PuTTY is another easy solution, configure a serial connection for the BSC9131RDB as 115200 (baudrate), 8 bits, no parity, 1 stop bit, no flow control. (See figure for PuTTY serial port configuration)
2. Enable the terminal software by "connecting" your connection in the serial software so it is up and is waiting for the BSC9131RDB u-boot prompt

5 Assemble and Connect Power Supply

1. Assemble the 12 V, 5.5 A power supply kit
2. Connect power supply to the 12 V connector (P4)
3. Plug the power cable into the wall outlet

6 Verify U-Boot Prompt

With the board powered and connected to the computer, and with HyperTerminal/ serial software running, we should see the u-boot screen, as shown in the picture. If the u-boot screen does not appear, press the power button on the front of the enclosure to initiate.

Press any key before the autoboot countdown reaches 0 in order to have access to the u-boot command prompt.

```

root@localhost:/home/fedora/rjns
NAND boot... WARNING: ECC not checked in SPL, check board cfg
U-Boot 2011.06 (Oct 20 2011 - 19:43:35)

CPU: PSC9131E, Version: 1.0, (0x86080010)
Core: E500, Version: 5.1, (0x80121251)
Clock Configuration:
CPU@1000 MHz,
CCB@400 MHz,
DDR@400 MHz (800 MT/s data rate) (Asynchronous), IFC@100 MHz
L1: D-cache 32 KB enabled
I-cache 32 KB enabled
Board: PSC9131RDB
I2C: ready
SPI: ready
DRAM: 580 MiB (DDR3, 32-bit, CL=6, ECC off)
L2: 256 KB enabled
NAND: 128 MiB

Bad block table found at page 65472, version 0x01
Bad block table found at page 65408, version 0x01
mand_bbt: ECC error while reading bad block table
mand_read_bbt: Bad block at 0x000006240000
In: serial
Out: serial
Err: serial
Net: eTSEC1 connected to Vitesse VSC641
eTSEC2 connected to Vitesse VSC641
eTSEC1, eTSEC2
Hit any key to stop autoboot: 9
>
105,0-1 24

```

7 Next Steps

At this point the BSC9131RDB has been verified as functional. The next section of this guide will discuss the available documentation for the BSC9131RDB user.

To continue on with u-boot, the SDK documentation introduced below will guide the reader on to the next logical steps in u-boot and Linux® configuration.

Other Supporting Documentation

This section will cover the various resources needed to get started with all components of the BSC9131RDB. The BSC9131RDB comes with a number of different connectivity and debugging options for the various internal systems of the device.

The BSC9131RDB

The BSC9131RDB has two main documents. As hardware setup is dependent on what software systems will be run on the RDB, these guides may be used as reference in addition to your specific software configuration guide.

The two documents for the RDB are:

- **Hardware Getting Started Guide (BSC9131RDB HGS_FINAL.pdf)**
Provides the user with a quick set of instructions for setting dip switches to default settings.
- **BSC9131RDB User Guide (BSC9131RDB_UG.pdf)**
Provides the user with a more in-depth set of information regarding the RDB.

The user can refer back to either document for hardware information if something is unclear in the following sections.

Other Supporting Documentation (continued)

Software Development Kit (SDK): U-Boot and Linux

The u-boot and Linux package is referred to as the WUSDK (SDK for short). RDBs come with some version of u-boot burned into the board's flash memory. All of the documentation for the SDK is provided with each SDK release. The document for getting started with u-boot and Linux (the SDK) is also included:

- **Using BSC9131RDB—A Step By Step Guide.doc**

Download the current WUSDK from the software tab on the BSC9131RDB web page and follow the step-by-step guide to get the SDK working on your board.

This guide also provides the basic dip switch settings for the RDB in order to verify various functionalities, instructions on how to update u-boot and Linux on the board and basic instructions for using various features. In addition to the SDK's getting started document, there is also a general reference manual for further specifics related to the SDK, titled **BSC913x_BSP_User_Guide.pdf**.

Inter-Processor Communication (IPC)

Once your RDB is up and running with the SDK, the next steps involve running code to prove that both the e500 and the DSP cores are working together. The most basic demo for this is the IPC demo. This demo shows the e500 and SC3850 cores sending messages to each other via the terminal screen. This is covered in the SDK documentation referenced in the previous section.

Software Debugging Tools for the BSC9131RDB

The above sections enable the user to verify that the e500 and SC3850 cores are functional and able to communicate with each other. The next step may be used to debug the user's own applications and software. The BSC9131 SoC has separate debugging tools for the e500 core and the SC3850 core. The e500 core can be debugged via GDB in Linux, or via CodeWarrior for PPC. The current intent is that programmers will debug via Linux, which is covered in the **SDK's BSC913x_BSP_User_Guide.pdf**.

For debugging the SC3850 core, programmers must use CodeWarrior for StarCore DSPs. Download CodeWarrior for StarCore (BSC913x) and CodeWarrior for PPC from **freescale.com** and use the following application note to get started with these debugger tools. The application note explaining the CodeWarrior debugger setup for BSC913x is

AN4384: Configuring the CodeWarrior Tools to Debug a BSC9131RDB Board

Follow this document to get up and running on the CodeWarrior tools for the BSC9131RDB.

Other Supporting Documentation (continued)

SmartDSP OS

Once the user has the basic flow of the SDK, IPC and debugging with CodeWarrior, the user may take advantage of the SmartDSP OS package, on which the SC3850 core operates. SmartDSP OS comes standard with the CodeWarrior for StarCore DSP tools suite, in the <CodeWarrior Install Folder>\SC\StarCore_Support\SmartDSP folder.

SmartDSP includes a number of demos on how to program SmartDSP to utilize various BSC9131 features. These demos are located in the following SmartDSP folder: SmartDSP\demos\starcore\BSC9x3x\. Each demo folder comes with a readme file explaining how to run the demo.

Two highlighted SmartDSP demos for the BSC9131 are the `aic_loopback` demo and the IPC demo. The user can run the IPC demo discussed in the SDK section of this document using the SmartDSP instructions instead of running via the Linux `dsp_bt` command command.

To demonstrate the AIC loopback demo, the user needs an RF card (the demo was created and tested using a Benetel RF card, sold separately from the RDB). Instructions for running the AIC loopback demo are included in the SDK documentation and the SmartDSP demo documentation. The user should read both sets of documentation for AIC programming, as Linux is used to initialize the AIC, while SmartDSP is used for runtime access of the AIC.

LTE Software

To get started with the LTE software stack on the BSC9131RDB, the user should request information and documentation from their Freescale sales representative or via the Freescale extranet website.

The **FSL_LTE_Small_Cell_Quick_Start_Guide** provides the initial steps for getting started with the Freescale LTE solution.

DSP Libraries

For more information on our DSP libraries, please see the application note (AN4207) and its corresponding example code download (AN4207SW).



Get Started

Download the installation software and documentation under **Jump Start Your Design** at **freescale.com/BSC9131RDB**.

Support

Visit **freescale.com/support** for a list of phone numbers within your region.

Warranty

Visit **freescale.com/warranty** for complete warranty information.

For more information about the QorIQ Qonverge families, visit **freescale.com/QorIQQonverge**

Freescale, the Freescale logo, QorIQ, QorIQ Qonverge and StarCore are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. QorIQ Qonverge is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. © 2013 Freescale Semiconductor, Inc.

