

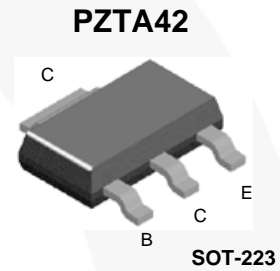
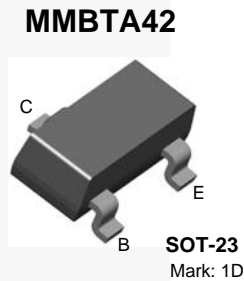
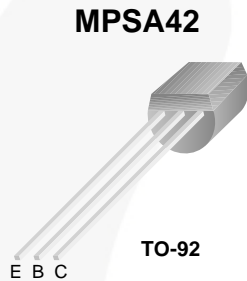


October 2014

MPSA42 / MMBTA42 / PZTA42 NPN High-Voltage Amplifier

Features

- This device is designed for application as a video output and other high-voltage applications.
- Sourced from process 48.



Ordering Information

Part Number	Top Mark	Package	Packing Method
MPSA42	MPSA42	TO-92 3L	Bulk
MMBTA42	1D	SOT-23 3L	Tape and Reel
PZTA42	A42	SOT-223 4L	Tape and Reel

Absolute Maximum Ratings^{(1), (2)}

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	300	V
V_{CBO}	Collector-Base Voltage	300	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current - Continuous	500	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Notes:

1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

MPSA42 / MMBTA42 / PZTA42 — NPN High-Voltage Amplifier

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Max.			Unit
		MPSA42	MMBTA42 ⁽³⁾	PZTA42 ⁽⁴⁾	
P_D	Total Device Dissipation	625	240	1000	mW
	Derate Above 25°C	5.00	1.92	8.00	mW/ $^\circ\text{C}$
$R_{\theta\text{JC}}$	Thermal Resistance, Junction-to-Case	83.3			$^\circ\text{C}/\text{W}$
$R_{\theta\text{JA}}$	Thermal Resistance, Junction-to-Ambient	200	515	125	$^\circ\text{C}/\text{W}$

Notes:

- Device is mounted on FR-4 PCB 1.6 inch x 1.6 inch x 0.06 inch.
- Device is mounted on FR-4 PCB 36 mm x 18 mm x 1.5 mm, mounting pad for the collector lead minimum 6 cm².

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
Off Characteristics					
$V_{(\text{BR})\text{CEO}}$	Collector-Emitter Breakdown Voltage ⁽⁵⁾	$I_C = 1.0 \text{ mA}, I_B = 0$	300		V
$V_{(\text{BR})\text{CBO}}$	Collector-Base Breakdown Voltage	$I_C = 100 \mu\text{A}, I_E = 0$	300		V
$V_{(\text{BR})\text{EBO}}$	Emitter-Base Breakdown Voltage	$I_E = 100 \mu\text{A}, I_C = 0$	6		V
I_{CBO}	Collector Cut-Off Current	$V_{\text{CB}} = 200 \text{ V}, I_E = 0$		0.1	μA
I_{EBO}	Emitter Cut-Off Current	$V_{\text{EB}} = 6 \text{ V}, I_C = 0$		0.1	μA
On Characteristics⁽⁵⁾					
h_{FE}	DC Current Gain	$V_{\text{CE}} = 10 \text{ V}, I_C = 1.0 \text{ mA}$	25		
		$V_{\text{CE}} = 10 \text{ V}, I_C = 10 \text{ mA}$	40		
		$V_{\text{CE}} = 10 \text{ V}, I_C = 30 \text{ mA}$	40		
$V_{\text{CE}(\text{sat})}$	Collector-Emitter Saturation Voltage	$I_C = 20 \text{ mA}, I_B = 2.0 \text{ mA}$		0.5	V
$V_{\text{BE}(\text{sat})}$	Base-Emitter Saturation Voltage	$I_C = 20 \text{ mA}, I_B = 2.0 \text{ mA}$		0.9	V
Small Signal Characteristics					
f_T	Current Gain - Bandwidth Product	$I_C = 10 \text{ mA}, V_{\text{CE}} = 20 \text{ V}, f = 100 \text{ MHz}$	50		MHz
C_{cb}	Collector-Base Capacitance	$V_{\text{CB}} = 20 \text{ V}, I_E = 0, f = 1.0 \text{ MHz}$		3.0	pF

Notes:

- Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Performance Characteristics

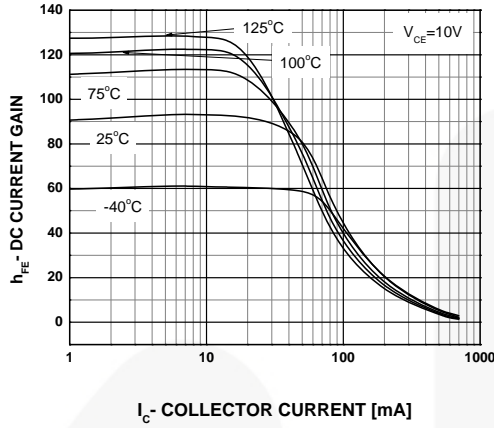


Figure 1. DC Current Gain vs. Collector Current

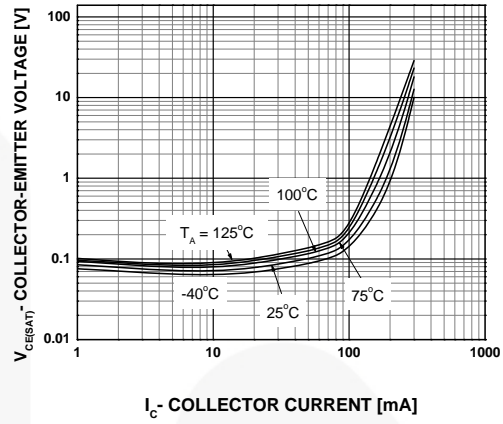


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

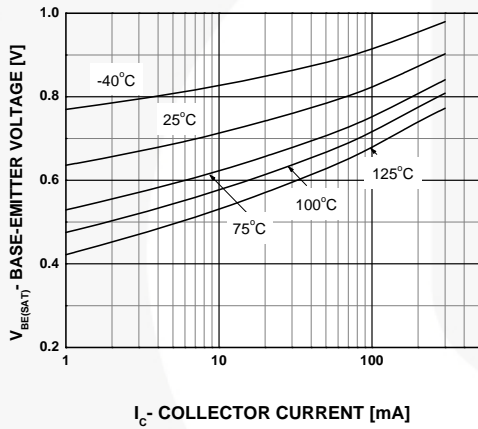


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

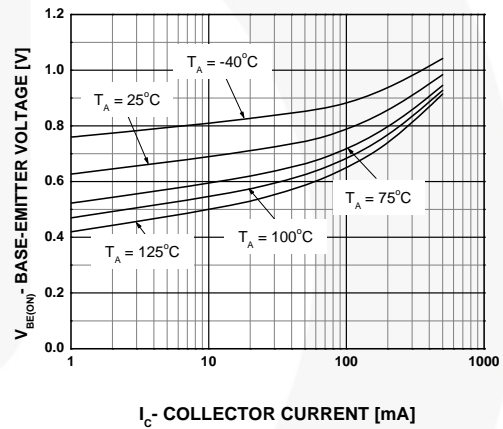


Figure 4. Base-Emitter On Voltage vs. Collector Current

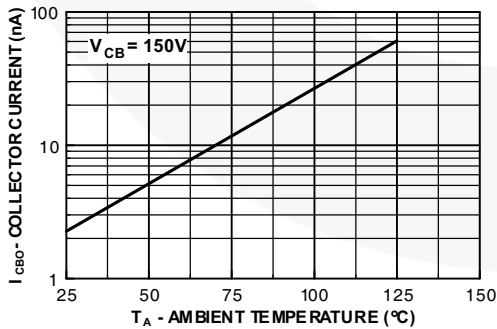


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

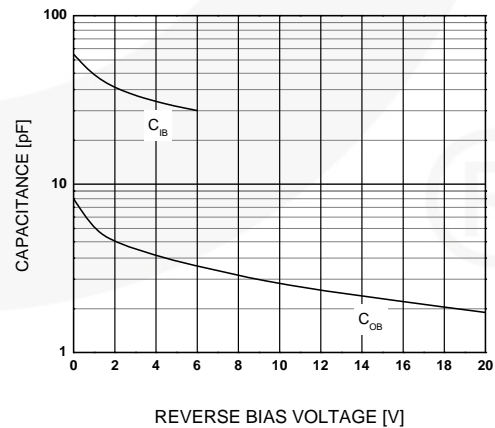


Figure 6. Collector-Base and Emitter-Base Capacitance vs. Reverse-Bias Voltage

Typical Performance Characteristics (Continued)

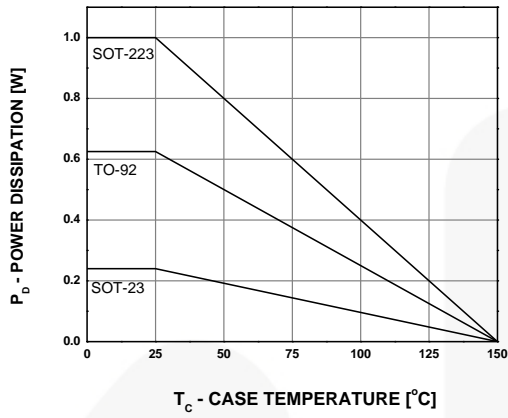
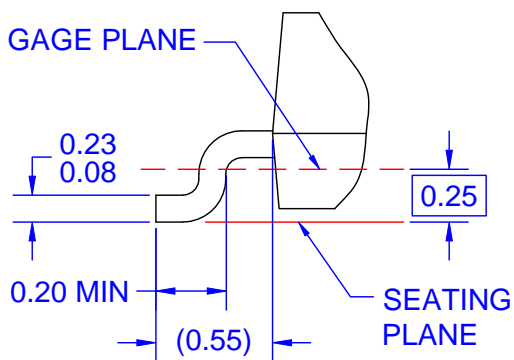
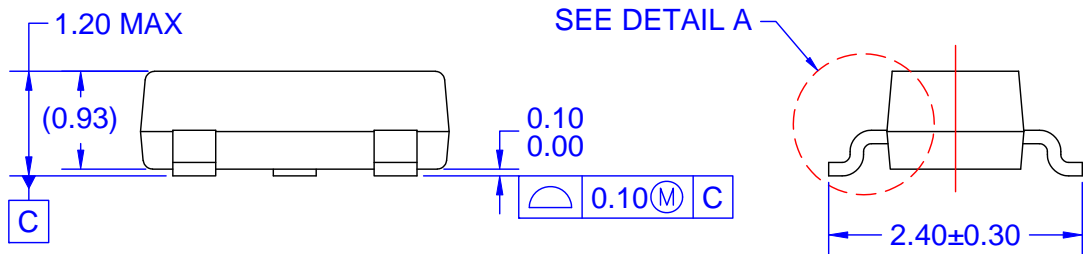
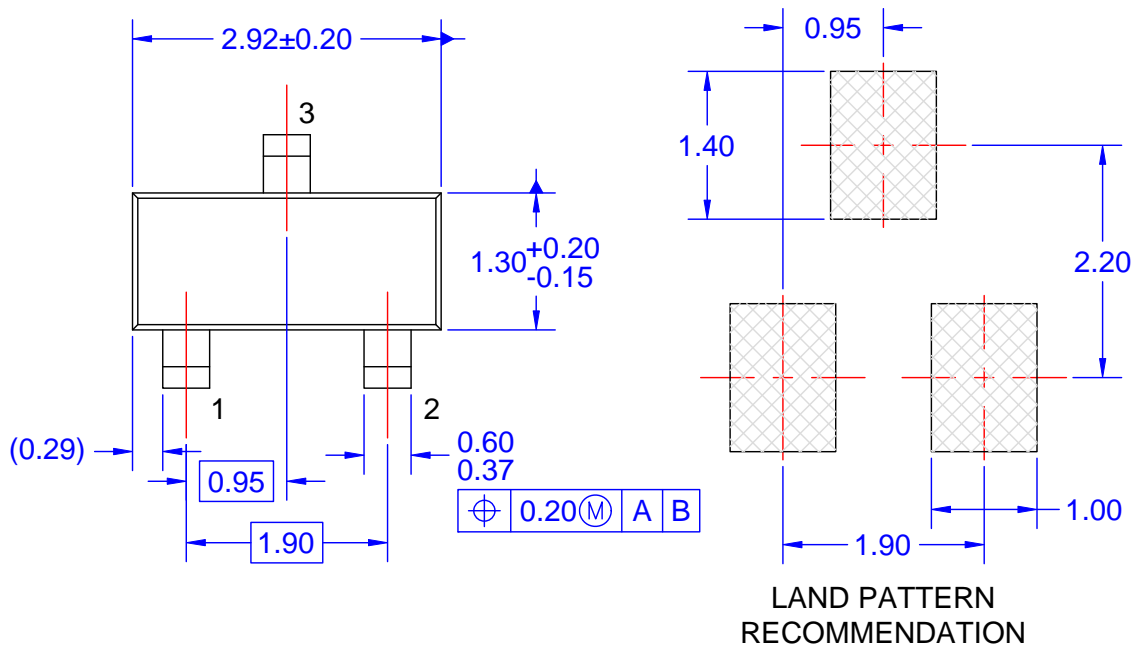


Figure 7. Power Dissipation vs. Ambient Temperature





DETAIL A
SCALE: 2X

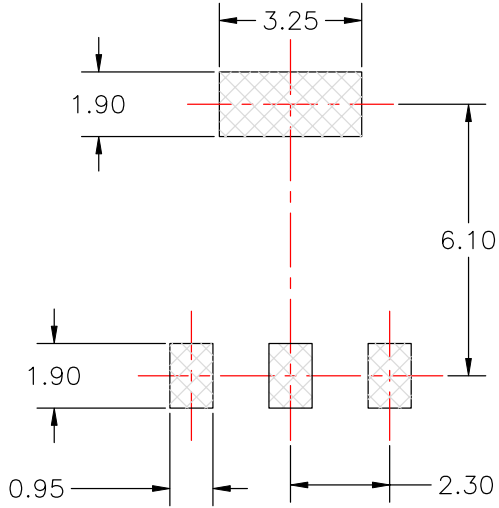
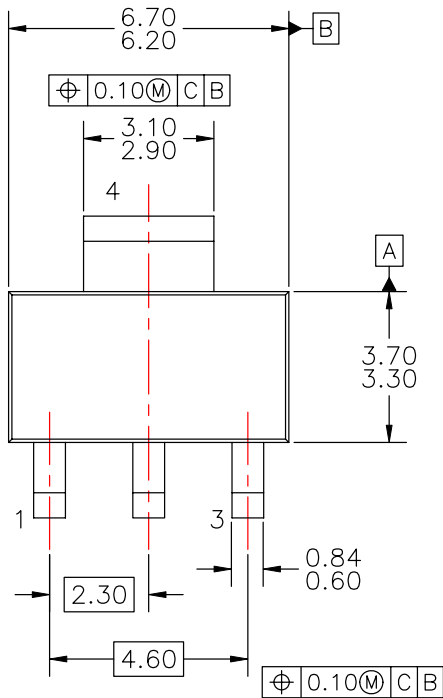
NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
- E) DRAWING FILE NAME: MA03DREV10

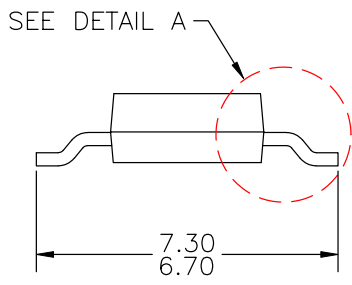
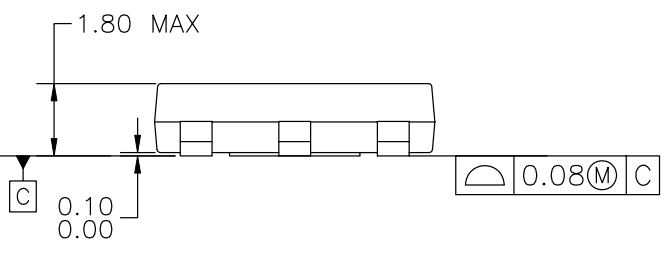
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APPROVED
July-14-2008

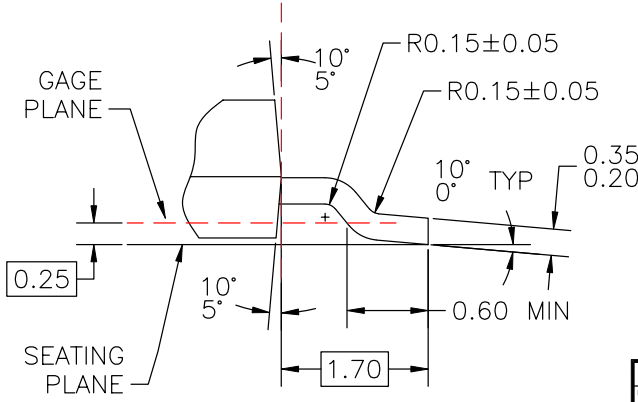
REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 ±0.03 TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.8 ±0.05 TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 ±0.03 TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 ±0.33 TO 3.30; CHG BODY LN FR 6.53 ±0.33 TO 6.30; CHG TOTAL PKG WID FR 6.94 ±0.33 TO 7.30; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
 - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - C) ALL DIMENSIONS ARE IN MILLIMETERS.
 - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - E) LANDPATTERN NAME: SOT230P700X180-4BN
 - F) DRAWING FILENAME: MKT-MA04AREV2



DETAIL A
SCALE: 2:1

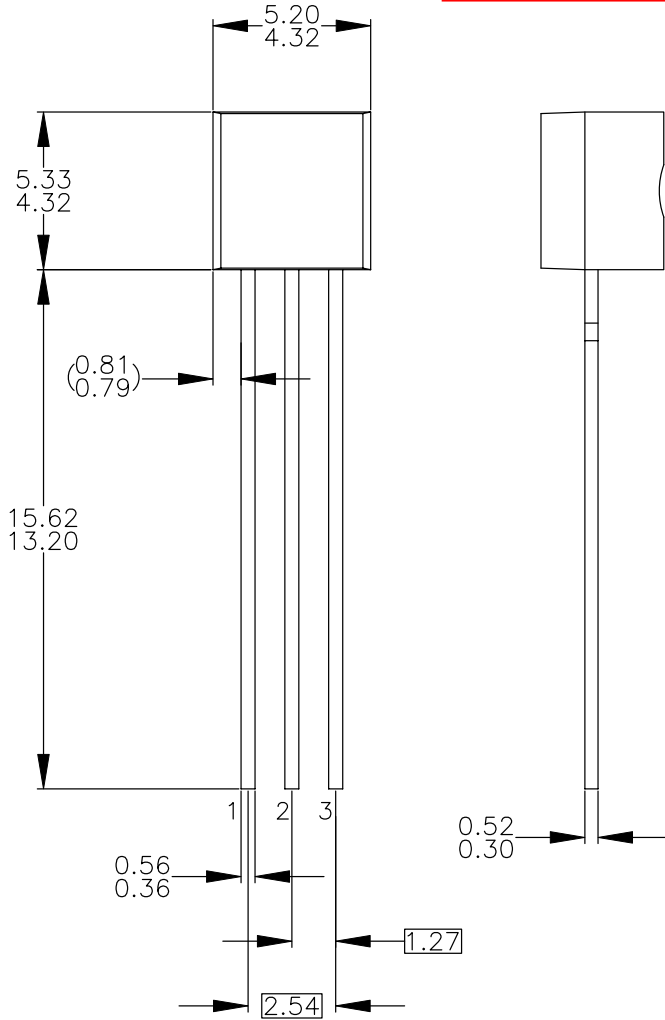
APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	26FEB2008	
CHECKED: L.Z. STA CRUZ		
APPROVED: M.R. GESTOLE		
G.S. BAJE		MOLDED PACKAGE SOT-223, 4 LEAD
		SCALE: 1:1
		SIZE: A3
		DRAWING NUMBER: MKT-MA04A
		REV: 2
		FORMERLY: N/A
		SHEET: 1 OF 1

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REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH(MM) TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14-1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32- 4.70 TO 4.32-4.83; CHG PKG HEIGHT DIM FR 4.32-4.70 TO 4.32-4.78; CHG LD THICK DIM FR 0.30- 0.48 TO 0.30-0.52; DAMBAR-PKG DIM FR 1.27-1.65 TO 0.90-1.65; LD LGH DIM FR 14.47-15.64 TO 14.47-15.62; PKG DIM: 1.02-1.52 TO 0.92-1.52, 3.81-4.45 TO 3.40-4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C. MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	4OCT1999	RCM/MRG
3	CHG LD LEN FR 1.81 TO 1.88 ; CHG MOLD BODY HT FR 1.33 TO 1.33 ; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO (0.81); CHG MOLD BODY WIDTH FR 1.33 TO 1.33 ; ADD PKG THICKNESS DIM "E"; CHG "S" DIM FR 2.13 TO 2.13 ; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M-1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP

APPROVED
 July-14-2008



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR	E - EMITTER	D - DRAIN
F - JFET	B - BASE	S - SOURCE
M - DMOS	C - COLLECTOR	G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

APPROVALS	DATE	<p>FAIRCHILD SEMICONDUCTOR™</p> <p>3LD, TO-92, MOLDED STD STRAIGHT LD (NO EOL CODE)</p>				
DRAWN: J.U. COMPARATIVO JR.	03APR2008		SCALE	SIZE	DRAWING NUMBER	REV
CHECKED: L. GALERA			1:1	N/A	MKT-ZA03D	3
APPROVED: M.R. GESTOLE			FORMERLY: N/A			SHEET : 1 OF 1
G.S. BAJE						



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I73