

## **ADS7043EVM-PDK**



This user's guide describes the characteristics, operation and use of the ADS7043-EVM performance demonstration kit (PDK). This kit is an evaluation platform for the ADS7043 low power, 12-bit pseudo-differential successive approximation register (SAR) analog-to-digital converters (ADCs) that support single-ended analog inputs.

This EVM eases the evaluation of the ADS7043 device with hardware and software for computer connectivity through universal serial bus (USB). This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

The following related documents are available through the Texas Instruments web site at <http://www.ti.com>.

**Table 1. Related Documentation**

Device	Literature Number
OPA316	<a href="#">SBOS703</a>
TPS79101	<a href="#">SLVS325</a>
REG71055	<a href="#">SBAS221</a>
TPS62080	<a href="#">SLVSAE8</a>
TPS3836K33	<a href="#">SGLS322</a>

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## 1 Overview

The ADS7043EVM-PDK is a platform for evaluation of the ADS7043 ADC. The evaluation kit combines the ADS7043EVM board with a Simple Capture Card controller board. This controller card consists of a TI Sitara embedded microcontroller (AM3352) and a field-programmable gate array (FPGA). It provides an interface from the EVM to the computer through a universal serial bus (USB) port. The included software communicates with the Simple Capture Card, and the controller card provides the power and digital signals used to communicate with the ADS7043EVM board. These demonstration kits include the ADS7043EVM board, the Simple Capture Card, a microSD memory card, and an A-to-micro-B USB cable.

### 1.1 ADS7043EVM Features

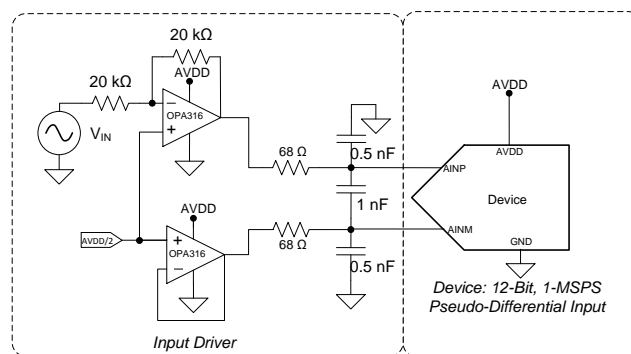
- Contains support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI)
- Onboard 5-V analog supply
- Onboard [OPA316](#) (10-MHz, low-power, low-noise, Rail-to-Rail Out (RRIO)) ADC input drivers

### 1.2 ADS7043EVM-PDK Features

- USB port for computer interface
- Easy-to-use evaluation software for Microsoft® Windows® XP, Windows 7, and Windows 8 operating systems
- Built-in analysis tools including scope, FFT, and histogram displays
- Data collection to text files supported

## 2 EVM Analog Interface

The ADS7043 is an extremely low-power, extremely small size ADC that supports single-channel ended analog inputs. The ADS7043EVM uses an OPA316 amplifier to drive the inputs of the ADC. The ADS7043EVM is designed for easy interfacing to multiple analog sources. SMA connector J3 (please refer to the schematics in [Section 7.3](#)) allows the EVM to have input signals connected through a coaxial cable. In addition, header connector P2 provides a convenient way to connect input signals. All analog inputs are buffered by the OPA316 amplifier in order to properly drive the ADS7043 ADC inputs.



**Figure 1. ADS7043EVM Analog Input Connections**

[Table 2](#) lists the analog interface connectors available. The ADS7043EVM accepts a signal of  $-AVDD / 2$  to  $AVDD / 2$  on J3 with common mode voltage of  $AVDD / 2$ . The AINM pin of the ADS7043 is set to  $AVDD / 2$  by OPA316 buffer (U1). Connecting an input signal greater than  $AVDD$  would cause the ADC output codes to saturate.

**Table 2. Analog Input Connections**

Reference Designator	Signal	Signal Description
J3	AINP	Positive input of the pseudo-differential signal provided at the SMA
J4	AINP	Alternate location to provide the pseudo-differential input signal

### 3 Power Supplies

The ADS7043 supports a wide range of operation on its analog supplies. The AVDD can operate from 1.8 V to 3.6 V. The DVDD operates from 1.65 V to 3.6 V, independent of the AVDD supply.

The analog portion of the ADS7043EVM-PDK operates from a 5-V supply. The ADS7043EVM-PDK is configured to use the onboard regulated analog 5-V supply that in turn generates an AVDD analog supply using the low-noise TPS79101 LDO. This supply is nominally set to 3.3 V at the factory, but this voltage maybe changed to any value within the valid range, by modifying the value of R15 as per [Table 3](#). In case any intermediate value needs to be set, the detailed formula to arrive at these values are available in the TPS79101 ([SGLS160](#)) datasheet.

**Table 3. AVDD Voltage Settings**

AVDD Voltage	R15	R19	C9
1.8 V	14.2 k $\Omega$	30.1 k $\Omega$	33 pF
2.0 V	19.1 k $\Omega$	30.1 k $\Omega$	27 pF
2.5 V	31.6 k $\Omega$	30.1 k $\Omega$	22 pF
3.0 V	43.7 k $\Omega$	30.1 k $\Omega$	15 pF
3.3 V (default)	51.1 k $\Omega$	30.1 k $\Omega$	15 pF
3.6 V	59.0 k $\Omega$	30.1 k $\Omega$	15 pF

By default, the OPA316 amplifier supplies, VDD\_OPA and VSS\_OPA, are tied to AVDD (supplied from the same LDO) and GND, respectively. DVDD\_ADC is set at 3.3 V from the controller. These three supplies may be externally supplied by making the modifications described in [Table 4](#).

**Table 4. Voltage Supply Options**

Supply	Supply Option	Source	Component	Setting
VDD_OPA	Onboard	AVDD LDO (U5)	R47	Assembled
	External	J7/pin1	R47	Disassembled
VSS_OPA	Onboard	GND	R48	Assembled
	External	J7/pin3	R48	Disassembled
DVDD_ADC	Onboard	3V3_SDCC supply from connector	R49	Assembled
	External	J9/pin1	R49	Disassembled

#### CAUTION

The external AVDD supply applied to external connector P3 must not exceed 3.6 V as this may damage the device. The external AVDD supply must be in the range of 1.8 V to 3.6 V for proper operation of the ADS7043EVM.

The digital portion of the ADS7043 ADC operates from a 3.3-V supply from the Simple Capture Card. The buffer U12 is included to ensure that the SDO can be driven to the controller with minimal distortion.

## 4 Digital Interface

The ADS7043 digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs) and FPGAs easy. The ADS7043EVM offers 50-Ω resistors between the SPI signals and edge connector J1 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these resistors slow down the signal edges in order to minimize signal overshoot.

The ADS7043EVM has clearly marked test points for all the SPI signals to allow observation of the interface signals using an oscilloscope.

## 5 ADS7043EVM-PDK Initial Setup

This section presents the steps required to set up the ADS7043EVM-PDK kit before operation.

### 5.1 Default Jumper Settings

A silkscreen plot detailing the default jumper settings is shown in [Figure 2](#).

[Table 5](#) explains the configuration for these jumpers.

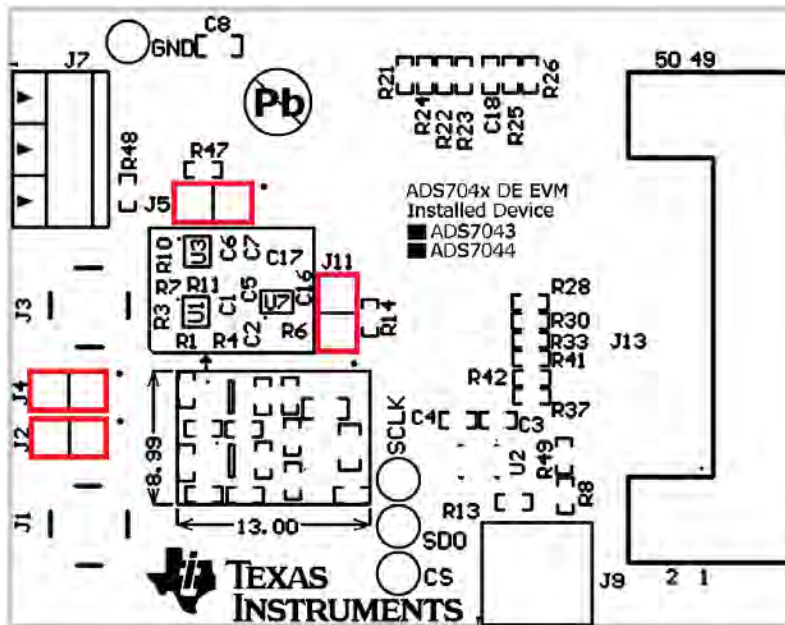


Figure 2. ADS7043EVM Default Jumper Settings

Table 5. Default Jumper Configurations

Reference Designator	Default Position	Description
J2	Open	Alternate location to provide the negative input of the differential signal
J4	Open	Unassembled, by default
J5	Closed	Point to insert an ammeter to measure VDD_ADC current, if required
J11	Closed	Point to insert an ammeter to measure VDD_OPA current, if required

## 5.2 Software Installation

This section presents the steps required to the install the software. [Section 6](#) explains how to operate the software to acquire data.

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**NOTE:** Ensure the microSD memory card included in the kit is installed in the microSD socket (P6) on the back of the Simple Capture Card as well as the microSD socket (J2) before connecting the EVM to the PC. Also ensure that the cards are not swapped or overwritten. If the contents of these cards are not available during boot up, Windows will not recognize the ADS7043EVM-PDK as a connected device.

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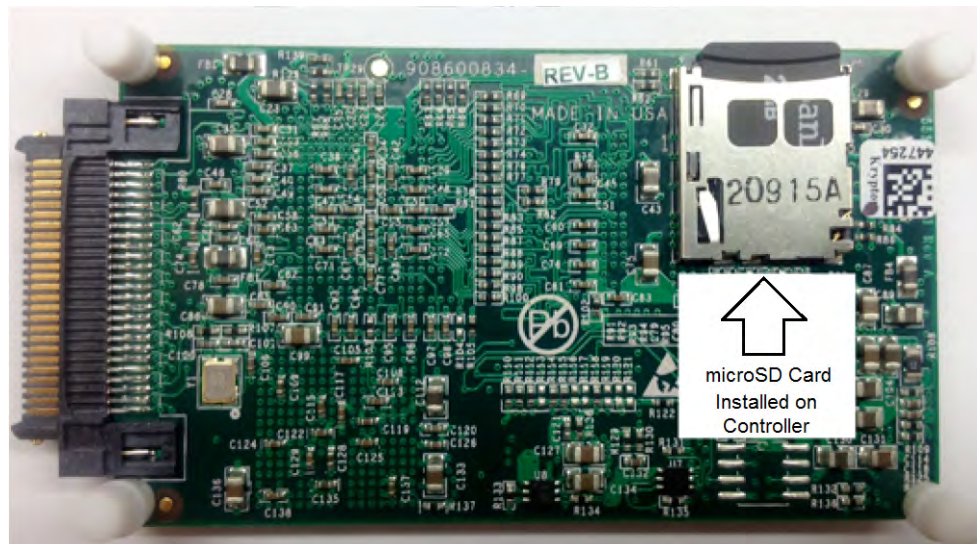
Complete the following steps to install the software:

- Step 1. Ensure that the microSD memory cards on both the Simple Capture Card and ADS7043 are installed.
- Step 2. Verify jumpers are in the factory-default positions and connect the hardware.
- Step 3. Locate, copy and install the ADS7043EVM software to the PC.
- Step 4. Complete the device driver installation.

Each of these steps is described in the following subsections.

### 5.2.1 Install the microSD Memory Cards on the Simple Capture Card Controller Board

As mentioned in the previous section, the ADS7043EVM-PDK includes two microSD memory cards. One is installed on the microSD socket (P6) at the back of the Simple Capture Card as shown in [Figure 3](#). The second microSD memory card is installed on the microSD socket (J2) at the back of the ADS7043EVM as shown in [Figure 4](#).



**Figure 3. Bottom View of Simple Capture Card with microSD Memory Card Installed**



**Figure 4. Bottom View of ADS7043EVM Board with microSD Memory Card Installed**

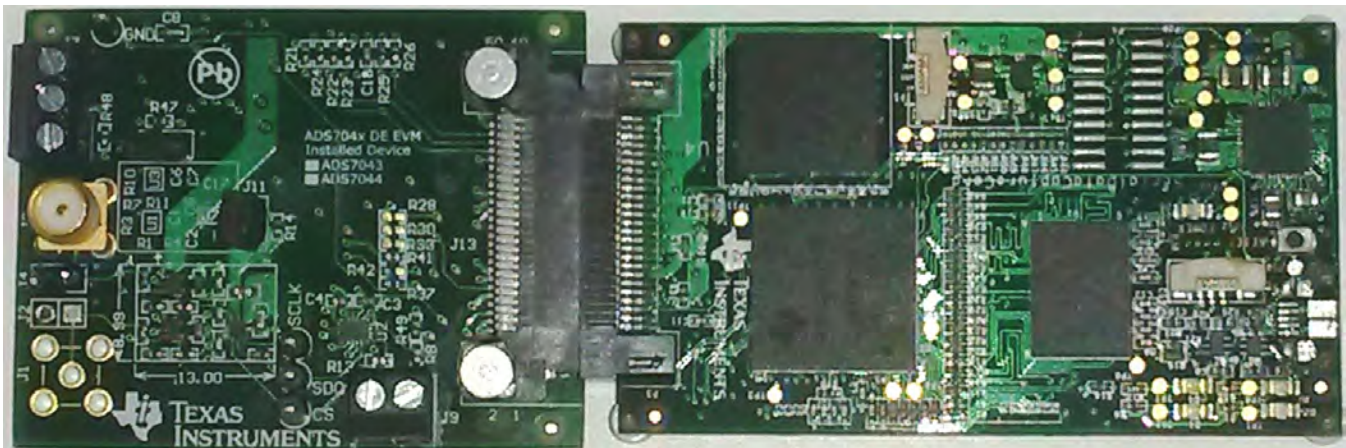
The microSD memory card is formatted at the factory with the necessary firmware files for the Simple Capture Card to boot properly. In addition to this the microSD card on the EVM contain Simple Capture Card firmware files (app and MLO files) and the ADS7043EVM-PDK software installation files inside the ADS7043 EVM V#.#.# folder. <V#.#.#> refers to the installation software version number, and increments with software installer releases.

### 5.2.2 Verify Jumpers are in the Factory-Default Position and Connect the Hardware

The ADS7043EVM-PDK includes both the ADS7043EVM and the Simple Capture Card; however, the boards are shipped unconnected.

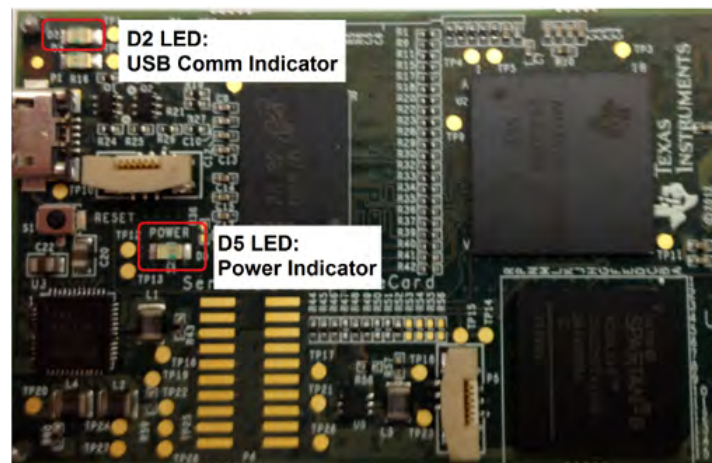
Follow these steps to verify that ADS7043EVM-PDK kit is configured and connected properly:

- Step 1. Verify the ADS7043EVM jumpers are configured as shown in [Figure 2](#).
- Step 2. Verify the microSD card is installed on the back of the Simple Capture Card, as shown in [Figure 3](#).
- Step 3. Verify the microSD card is installed on the back of the EVM board, as shown in [Figure 4](#).
- Step 4. Connect the ADS7043EVM board to the Simple Capture Card as [Figure 5](#) illustrates.



**Figure 5. Connecting ADS7043EVM Board to Simple Capture Card**

- Step 5. Connect the Simple Capture Card to the PC through the micro USB cable.
- Step 6. Verify that the LED D5 Power Good indicator is illuminated. Wait approximately ten seconds and verify that diode D2 blinks, indicating that USB communication with the host PC is functioning properly. [Figure 6](#) shows the location of the LED indicators in the Simple Capture Card.



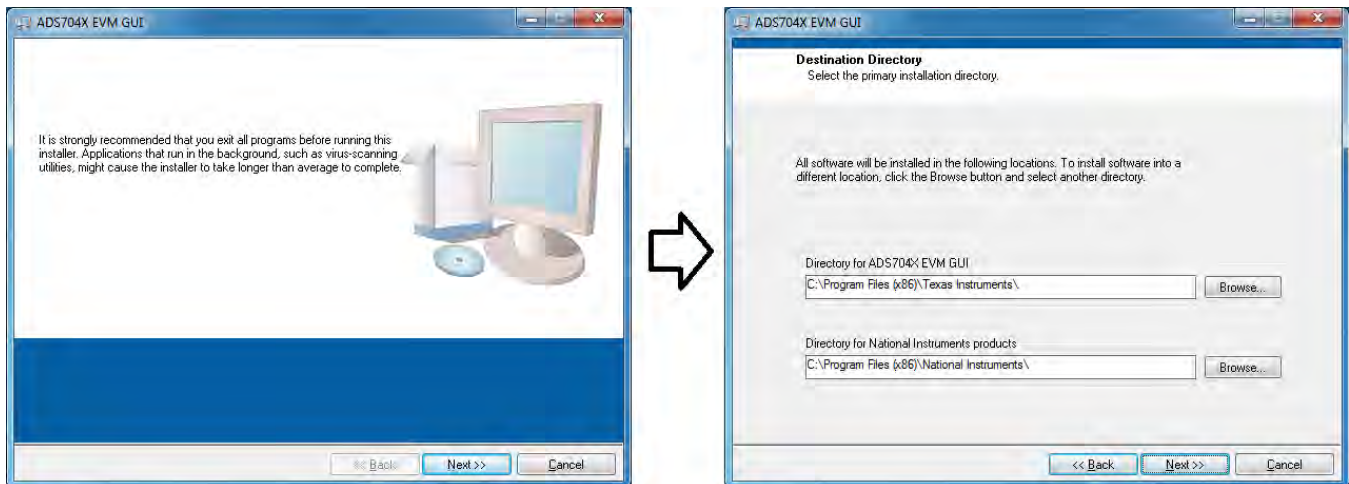
**Figure 6. LED Indicators on the Simple Capture Card**

### 5.2.3 Install the ADS7043EVM-PDK Software

The ADS7043 EVM V#.x.# software must be installed on the PC. This software supports the ADS7043-PDK. Administrator privileges are required to install the EVM software. The following steps list the directions to install the software:

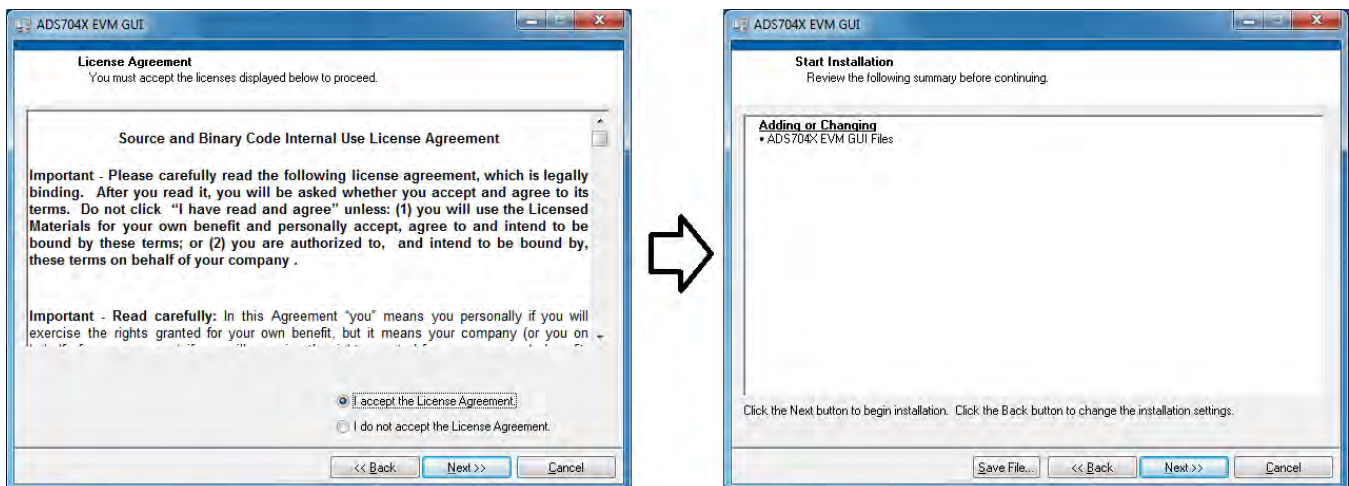
- Step 1. Open Windows Explorer and find the microSD memory card in the browser as a storage device.
- Step 2. Navigate to the `...\ADS7043 EVM Vx.x.x\Volume\` folder.
- Step 3. Run the installer by double-clicking the file `setup.exe`. This action installs the EVM GUI software and the required and device driver components.
- Step 4. After the installer begins, a welcome screen displays. Click *Next* to continue.
- Step 5. A prompt appears with the destination directory; select the default directory under: `...\Program Files(x86)\Texas Instruments\ADS7043evm\`.





**Figure 7. Welcome Screen and Destination Directory Screens**

- Step 6. One or more software license agreements appear. Select *I Accept the License Agreement* and click *Next*.
- Step 7. The *Start Installation* screen appears. Click *Next*.



**Figure 8. License Agreement and Start Installation Screens**

- Step 8. A progress bar appears; this step takes a few minutes.
- Step 9. The progress bar is followed by an *Installation Complete* notice.

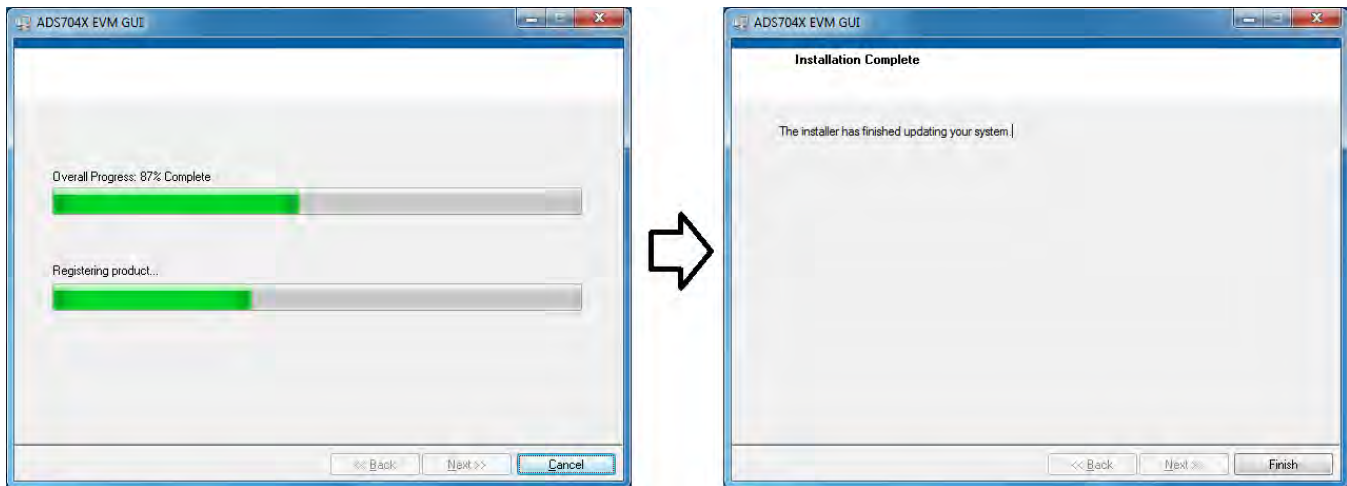


Figure 9. Progress Bar and Installation Complete Screens

### 5.2.4 Complete the Simple Capture Card Driver Installation

During installation of the Simple Capture Card driver, a prompt may appear with the Windows security message shown in Figure 10. Select *Install this driver software anyway* to install the driver required for proper operation of the software. The drivers contained within the installers are safe for installation to your system.

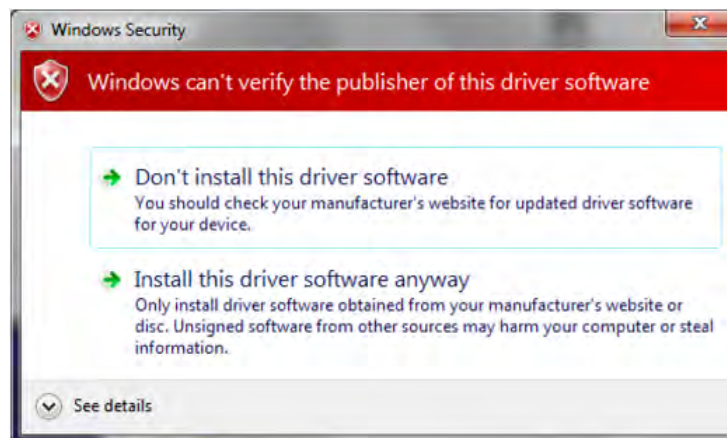


Figure 10. Windows 7 Driver Installation Warning

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**NOTE:** Driver installation prompts do not appear if the Simple Capture Card driver has been installed on your system previously.

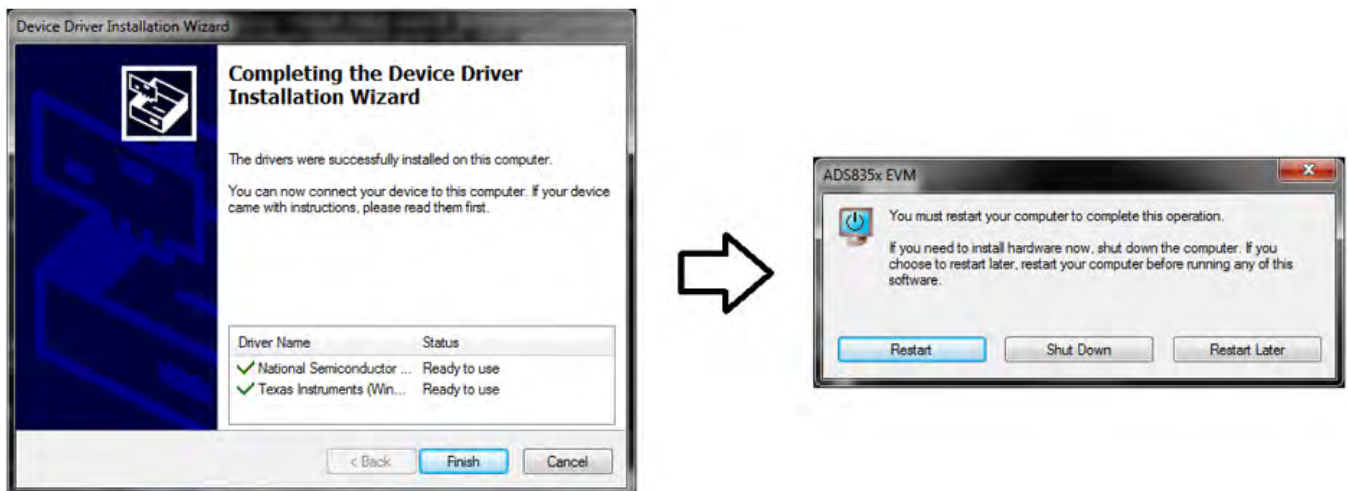
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The following steps describe how to install the Simple Capture Card driver:

- Step 1. Immediately after the ADS7043 EVM software installation is complete, prompts appear to install the Simple Capture Card driver, as shown in [Figure 11](#) and [Figure 12](#).
- Step 2. A computer restart may be required to finish the software installation. If prompted, restart the PC to complete the installation.



**Figure 11. Simple Capture Card Driver Installation**



**Figure 12. Simple Capture Card Driver Completion**

## 6 ADS7043EVM-PDK Kit Operation

This section describes how to use ADS7043EVM-PDK and the ADS7043EVM software to configure the EVM and acquire data.

### 6.1 About the SCC Controller Board

The SCC controller board provides the USB interface between the PC and the ADS7043. The controller board is designed around the AM335x processor, a USB 2.0 high-speed capability, 32-bit ARM core. The SCC controller board incorporates an onboard FPGA subsystem and 256MB of onboard DDR SRAM memory. The SCC controller board is not sold as a development board, and it is not available separately. TI cannot offer support for the SCC controller board except as part of this EVM kit.

### 6.2 Loading the ADS7043EVM Software

The ADS7043 EVM software provides the ability to capture and analyze data from the ADS7043.

To load the ADS7043 EVM software, follow these steps:

- Step 1. Make sure the EVM kit is configured and powered up as explained in [Section 5](#).
- Step 2. Start the ADS7043 EVM software. Go to Start → All Programs → Texas Instruments → ADS7043 EVM and click ADS7043 EVM to run the software.
- Step 3. Verify that the software detects the ADS7043. The GUI identifies the EVM hardware that is connected to the controller board and displays the *ADS7043EVM Front Page*. After the settings are loaded, *ADS7043EVM GUI* is displayed at the top of the GUI screen, which the device identified indicated at the right hand top corner as shown in [Figure 13](#).



Figure 13. GUI Display Prompt

### 6.3 Capturing Data with the ADS7043-PDK

Access the *Data Capture* page in the GUI to monitor data acquired by the ADS7043. This GUI page displays the acquired data versus time. To access the *Data Capture* page, hover the cursor over the blue arrow at the left center side of the GUI screen; a menu with different GUI pages appears. Click on the *Data Capture* option in the menu as shown in Figure 14.

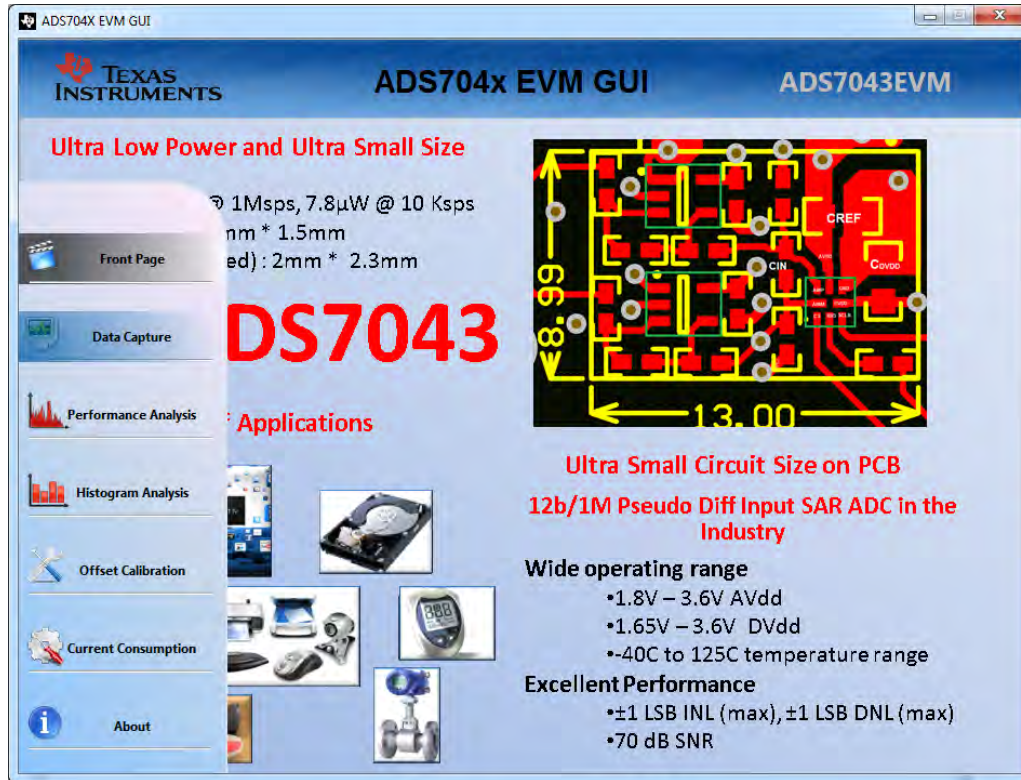


Figure 14. Open the Data Capture Page on the GUI

Figure 15 shows the *Data Capture* page of the EVM GUI. The device SCLK frequency and capture settings can be configured at the top right hand corner of the *Data Capture* page. Changes made to the configuration settings are executed on pressing the *Capture* button. The following list describes the different options available on the *Data Monitor* page.

- **SCLK:** This control sets the clock frequency used by the SPI interface to capture data. By configuring the SCLK frequency, the sampling rate of the ADS7043 is set. The ADS7043EVM-PDK software supports SCLK frequencies of 3.2 MHz to 16 MHz. In case the input in this field is beyond the capability of the device, it will be adjusted to the nearest value that can be supported.
- **Sampling Rate:** The upper limit of the sampling rate (displayed in ksp/s) is set based on the SCLK frequency selected. However, sampling rates lower than this displayed value may be set. The GUI supports these lower rates by increasing the CS high time between frames. Details of the interface protocol can be studied in the serial interface timing diagrams in the ADS7043 datasheet ([SBAS608](#)). In case the input to this field is beyond the capability calculated based on SCLK, it will be constrained to the maximum sampling rate possible at that SCLK frequency.
- **Sample Count:** This option is used to select the number of contiguous samples captured in a block. The drop-down menu can be used to select a data block in the range of 1024 samples to 1,048,576 samples per channel. The interface provides a drop-down list for values restricted to  $2n$ , where  $n$  is an integer.

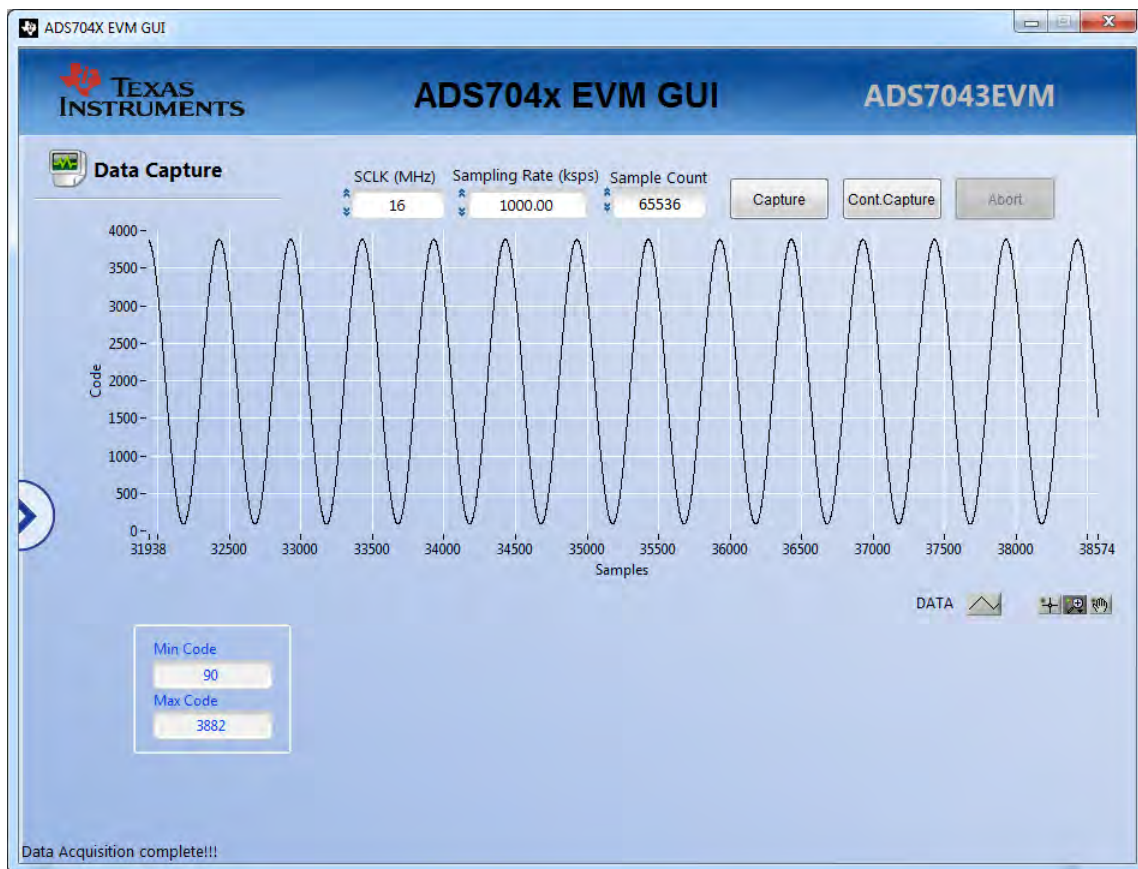


Figure 15. Data Capture Page

Once the ADC data is captured by the GUI using either of the *Capture* buttons, it is displayed on the graph area on this tab as shown in Figure 15. Once plotted, the graph can be zoomed into, panned, or resized by using the controls at the bottom of the graph area. The data captured may also be transferred to a file for further analysis by right clicking on the body of the graph and using the various options listed under *Export*.

## 6.4 FFT Analysis

The *Performance Analysis* page in the GUI performs the fast Fourier transform (FFT) of the captured data and displays the resulting frequency domain plot. This page also calculates key ADC dynamic performance parameters, such as signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and spurious-free dynamic range (SFDR). Figure 16 shows the FFT performance analysis display. The FFT calculated parameters are shown on the bottom right side of the display.

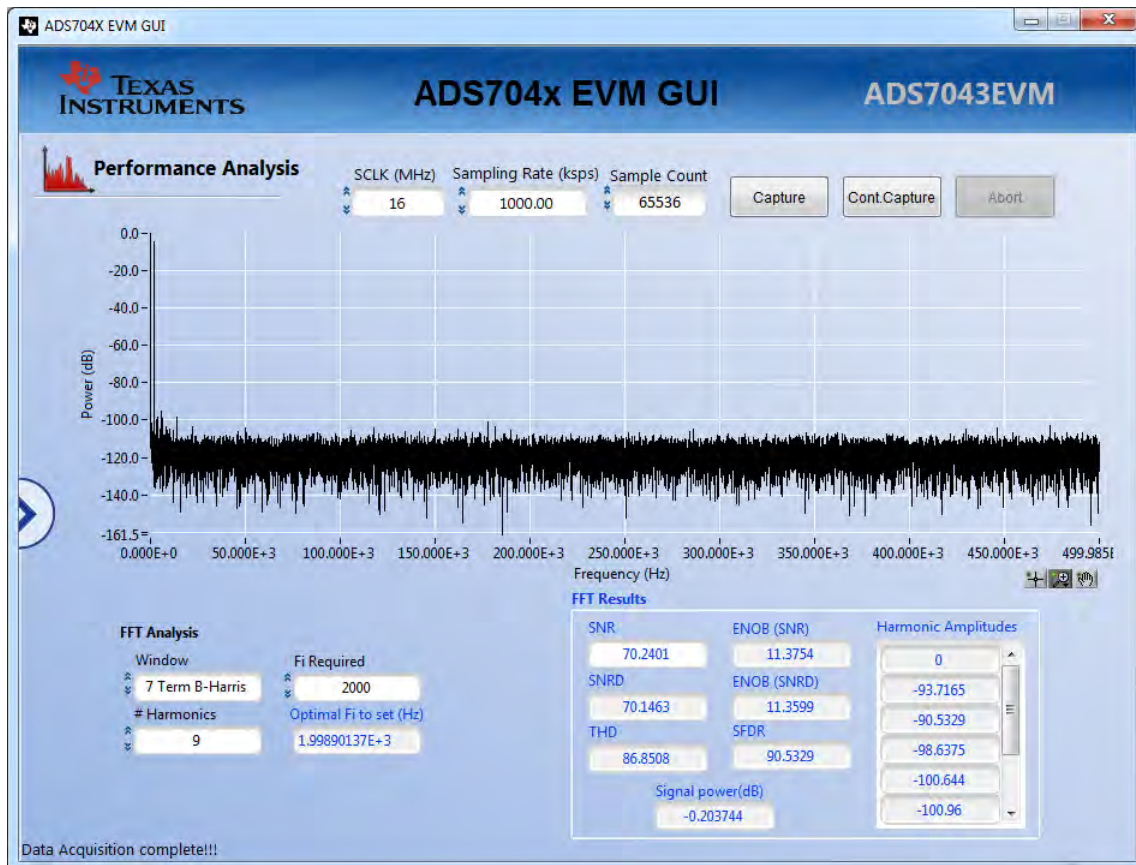


Figure 16. FFT Performance Analysis Page

### 6.4.1 FFT Analysis Settings and Controls

The SCLK, Sampling Rate and Sample Count fields are the same as described in Section 6.3.

**Fi Required:** Enter the frequency of the largest amplitude analog input signal here.

**Optimal Fi to set:** Adjust your input frequency from the signal source to this value computed by the GUI based on the *Fi Required* value entered. A minor difference from *Fi Required* will be seen here to enable a system to be coherent in nature.

**Window:** The window function is a mathematical function that reduces the signal to zero at the end points of the data block. In applications where coherent sampling cannot be achieved, a window-weighting function can be applied to the data to minimize spectral leakage. The following options are available:

- No windowing (no window weighting function applied; use for coherent data)
- Windowing. In this case the 7-Term Blackman-Harris window is applied by default. For a more thorough discussion of windowing, refer to [IEEE1241-2000](#).
- # Harmonics: This field sets the number of harmonics to be included in the calculations of the harmonic distortion. Any harmonic signal greater than this number is treated as noise in the performance calculations. The typical value used in this analysis is 9 as per the ADS7043 datasheet ([SBAS608](#)).

## 6.5 Histogram Analysis

Histogram testing is commonly used when characterizing ADCs. A histogram is merely a count of the number of times a code has occurred in a particular data set. The *Histogram Analysis* page of the GUI creates a histogram of the data of the acquired data set and displays it. Figure 17 shows the *Histogram Analysis* page of the GUI.

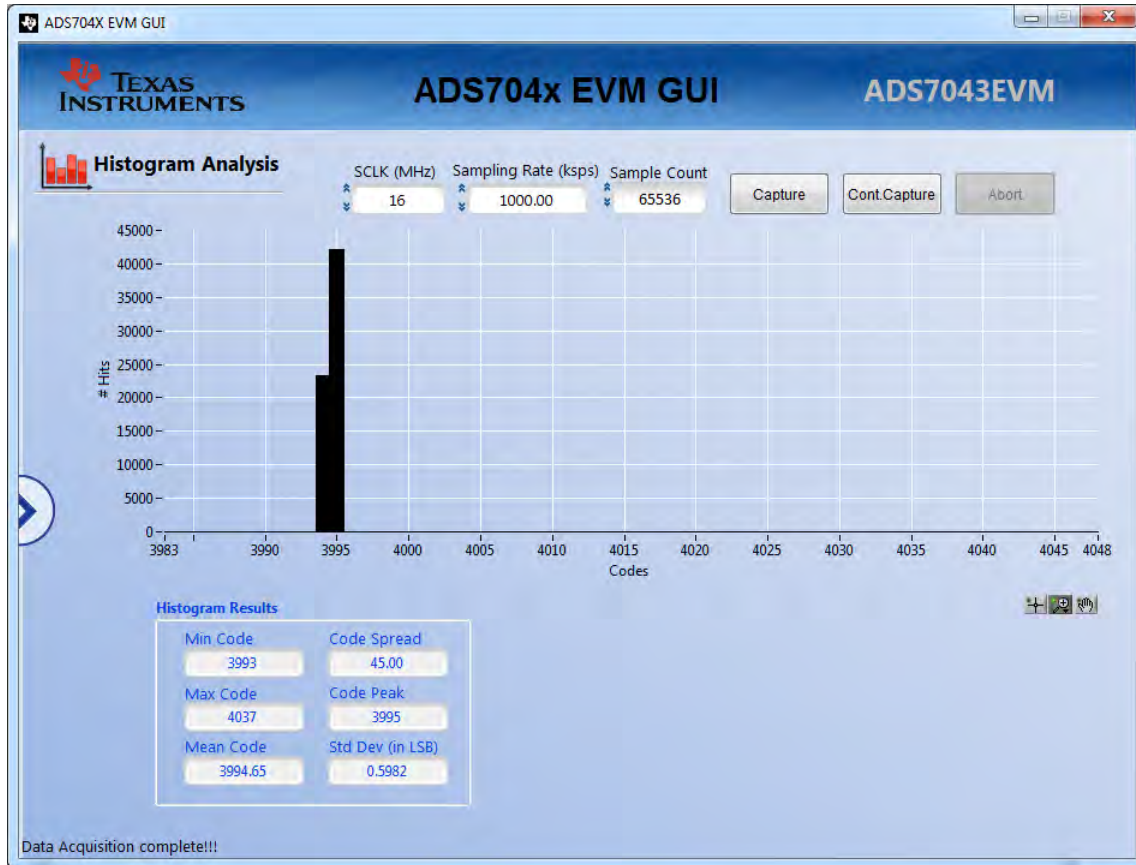


Figure 17. Histogram Analysis Page

The *Histogram Analysis* table shown in Figure 17 displays several parameters of the captured data set as described in the following list. Please note, all results displayed in this page are in LSBs.

- The *Min Code*, *Max Code*, and *Mean Code* indicators display the minimum, maximum and average value of the captured data set.
- The *Code Spread* column shows the peak-to-peak spread of the codes in the data set.
- The *Sigma* indicator displays standard deviation of the data set. This value is equivalent to the RMS noise of the signal when analyzing a dc data set.



## 6.6 Offset Calibration

The ADS7043 device has the ability to calibrate its internal offset. The offset calibration can be initiated by the user either on power-up or during normal operation. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage and connected to an internal reference. The result of the offset calibration is stored in an internal register. For subsequent conversions, the device adjusts the conversion results provided on the SDO output with the value stored in this internal register.

The ADS7043 GUI implements offset calibration as described in the *Offset Calibration During Normal Operation* section of ADS7043 datasheet ([SBAS608](#)). Figure 18 depicts the *Offset Calibration* page of the GUI.

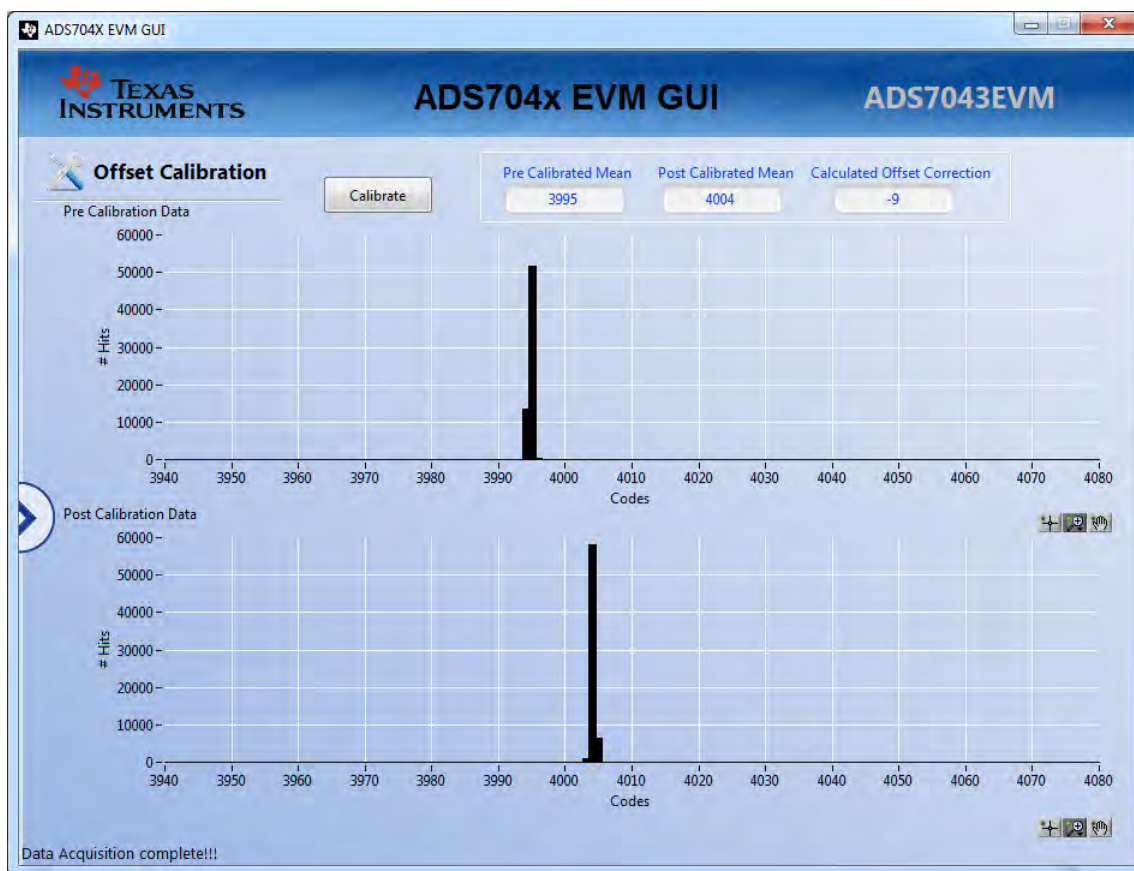


Figure 18. Offset Calibration Page

The Offset Calibration test is best conducted with a DC input at the Analog Input Terminal of the ADS7043EVM. Simply click the *Calibrate* button. The GUI first performs a histogram test for the device described in Section 6.5 and populates the first of the two graphs. The pre-calibrated Mean code is inserted in the indicator. Next, the calibration frame is sent to the ADS7043 device that enables the internal offset calibration logic. The GUI performs the histogram test for a second time and the second graph is populated and Post Calibrated Mean value computed. Finally, the difference between the first and second computed mean is populated in the Calculated Offset Correction indicator.

The computed offset for all subsequent attempts to calibrate the device will always yield a result of within the limits specified in the datasheet. This indicates that after the calibration is performed for the first time, the offset is actually being applied on all subsequent conversions. This computed offset will remain fixed, unless the device is reset or there is a significant change in operating temperature or analog supply voltage.

## 6.7 Estimated Current Consumption

The last tab in the GUI tabs menu opens up an *Estimated Current Consumption* tab as shown in Figure 19. This tab highlights the extremely low current and power consumption of the ADS7043 device and its scaling with sampling rate and AVDD voltage. This is computed based on characterization data collected across multiple devices at room temperature and it not based on data from the actual board connected to the GUI.

Set the desired Sampling rate and AVDD using the two dial in the right hand side of the page and observe the estimated current and power on the graph and the indicators on this page.

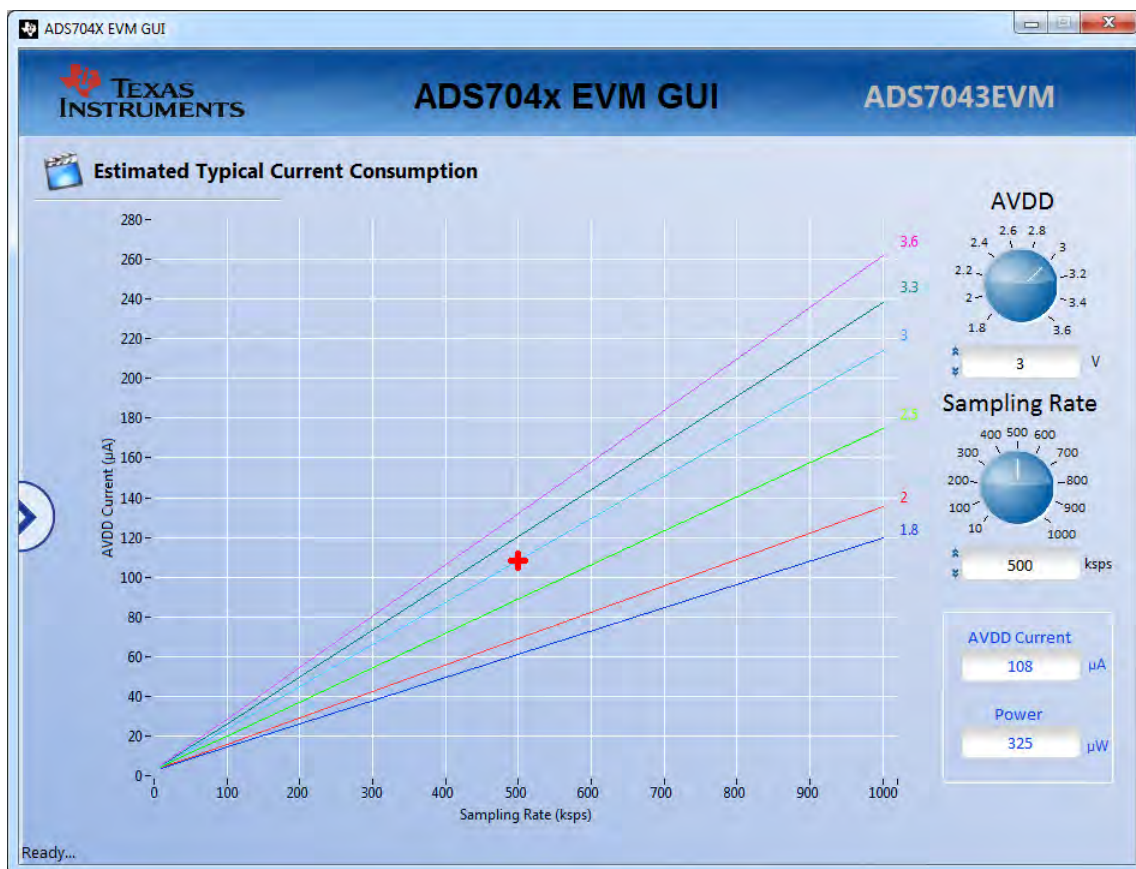


Figure 19. Estimated Current Consumption Page

## 6.8 Troubleshooting

Although the ADS7043EVM GUI rarely stops responding while the ADS7043EVM-PDK is connected, in case this does happen, unplug the USB cable from the EVM, unload the ADS7043EVM-PDK software, reconnect the ADS7043EVM-PDK to the PC and reload the ADS7043EVM software.

When initially setting up the EVM, the software detects the EVM hardware, and loads the appropriate hardware settings. If the EVM hardware is not detected, the GUI defaults to the *Capture Mode: Simulation* mode of operation using a preloaded captured data file for demonstration purposes.

## 7 Bill of Materials, PCB Layout, and Schematics

This section lists the bill of materials of the ADS7043EVM, shows the printed circuit board (PCB) layout for the ADS7043EVM. The schematics for the ADS7043EVM are appended to the end of this user's guide.

### 7.1 Bill of Materials

**NOTE:** All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant.

**Table 6. ADS7043EVM Bill of Materials**

Qty	Reference Designators	Description	Manufacturer	Part Number
8	C1, C3, C4, C6, C13, C18, C19, C20	CAP, CERM, 0.1uF, 50V, +/-10%, C0G/NP0, 0402	TDK	C1005X7R1H104K
2	C2, C7	CAP CER 1000PF 16V 5% NP0 0402	Samsung	CL05C102JO5NANC
1	C5	CAP, CERM, 2200pF, 50V, +/-5%, C0G/NP0, 0402	Kemet	C0402C222K4RACTU
2	C8, C12	CAP, CERM, 0.01uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E103KA01D
1	C9	CAP, CERM, 15pF, 16V, +/-2%, C0G/NP0, 0402	MuRata	GRM0222C1C150GD05
4	C10, C11, C16, C17	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	Taiyo Yuden	EMK107B7105KA-T
1	C14	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	MuRata	GRM21BR71A106KE51L
1	C15	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	AVX	06035C104KAT2A
4	CS, GND, SCLK, SDO	Test Point, Miniature, Black, TH	Keystone	5001
1	J1	Connector, TH, SMA	NI	NI
1	J3	Connector, TH, SMA	Emerson Network Power	142-0701-201
3	J4, J5, J11	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S
1	J2	Header, 100mil, 2x1, Gold, TH	NI	NI
1	J7	Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS
1	J9	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
1	J13	Receptacle, Micro High Speed Socket Strip, 0.8mm, 25x2, R/A, SMT	Samtec, Inc.	ERF8-025-01-L-D-RA-L-TR
1	J14	SD Memory Card Connector	Molex	502570-0893
3	R7, R9, R10	RES, 20.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040220K0FKED
1	R3	RES, 20.0k ohm, 1%, 0.063W, 0402	NI	NI
10	R2, R5, R28, R29, R30, R33, R38, R39, R40, R42	Resistor, Uninstalled	NI	NI
2	R4, R11	RES 30.0 OHM 1/16W 1% 0402 SMD	Vishay-Dale	CRCW040230R0FKED
7	R6, R8, R13, R31, R34, R35, R46	RES, 49.9 ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040249R9FKED
2	R12, R14	RES, 10.0, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210R0FKED
1	R15	RES, 51.1k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040251K1FKED
2	R17, R20	RES, 100k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW0402100KFKED
8	R1, R18, R36, R37, R41, R47, R48, R49	RES, 0 ohm, 5%, 0.063W, 0402	Yageo America	RC0402JR-070RL
1	R19	RES, 30.1k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040230K1FKED
7	R21, R22, R23, R24, R25, R26, R27	RES, 10.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040210K0FKED
2	U1, U3	IC, OPAMP GP 10MHZ RRO, SC-70	Texas Instruments	OPA316IDCK
1	U2	IC, 4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS, UQFN-16	TEXAS INSTRUMENTS	SN74AVC4T245RSVR
1	U4	NANOPOWER SUPERVISORY CIRCUITS, 2.93 V, DBV0005A	Texas Instruments	TPS3837K33QDBV
1	U5	Single Output High PSRR LDO, 100 mA, Adjustable 1.2 to 5.5 V Output, 2.7 to 5.5 V Input, 6-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS79101DBVR
1	U6	IC, 2K, Serial EEPROM	Atmel	AT24C02B
1	U7	IC, ULTRA-LOW POWER, 1-MSPS, SAR ADC, X2QFN-8	TEXAS INSTRUMENTS	ADS7043IRUG

## 7.2 PCB Layout

Figure 20 through Figure 23 show the PCB layouts for the ADS7043EVM.

**NOTE:** Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS7043EVM PCBs.

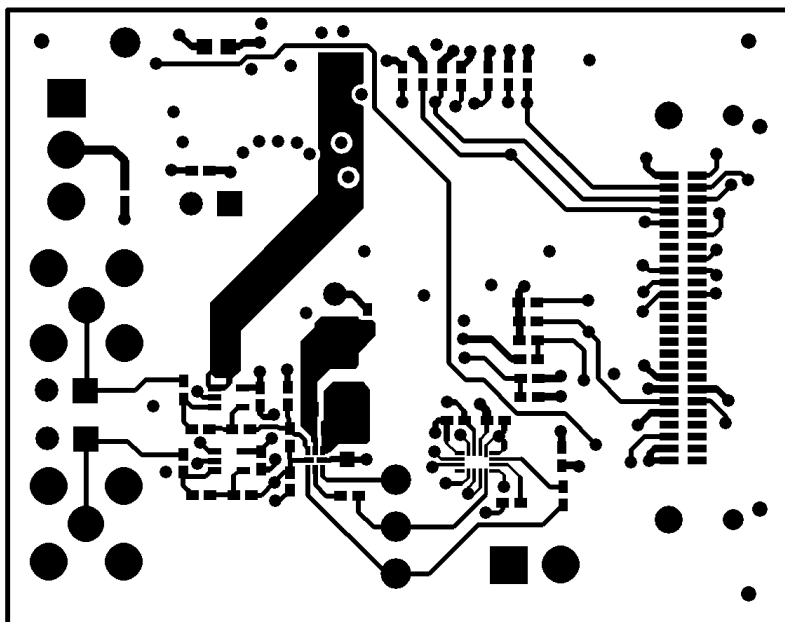


Figure 20. ADS7043EVM PCB: Top Layer (L1)

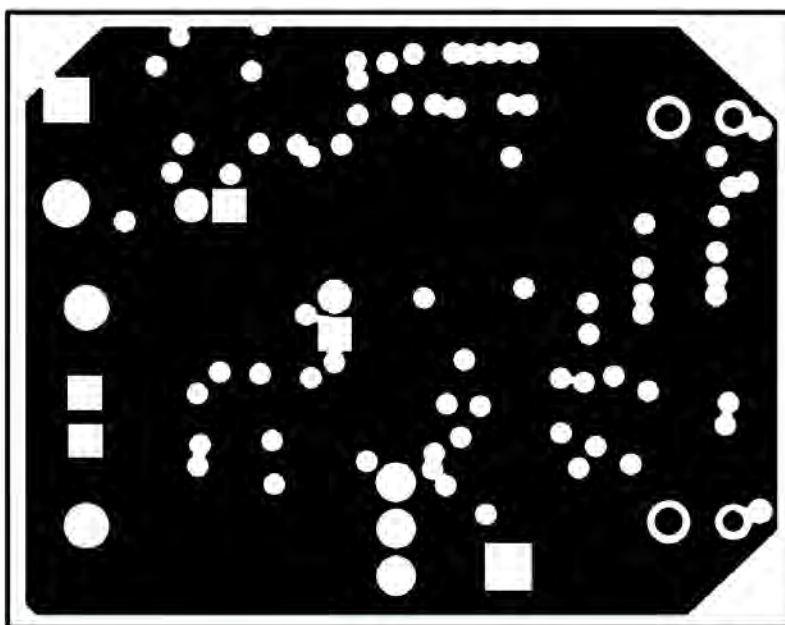


Figure 21. ADS7043EVM PCB: GND Layer (L2)

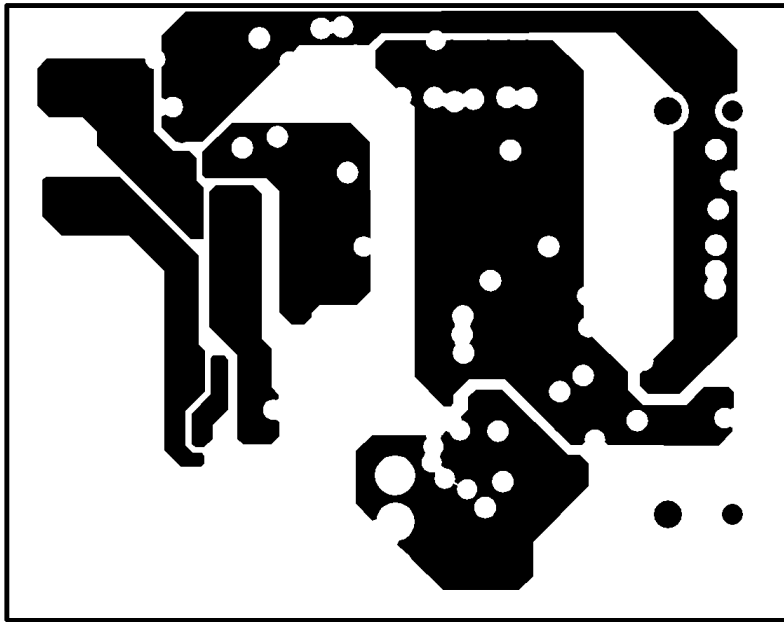


Figure 22. ADS7043EVM PCB: Power Layer (L3)

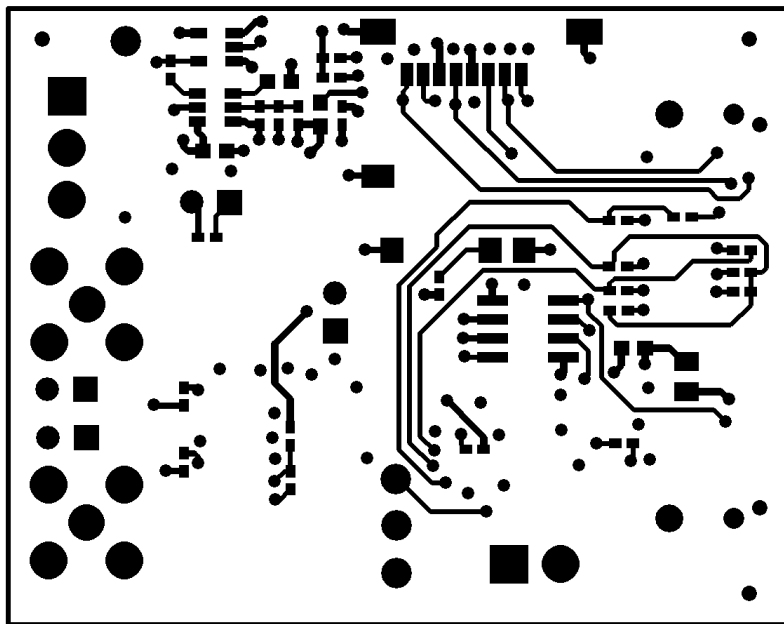
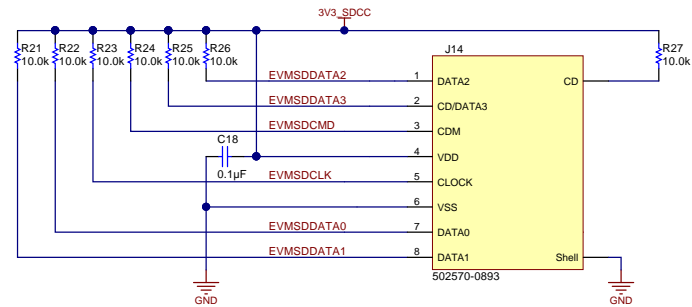
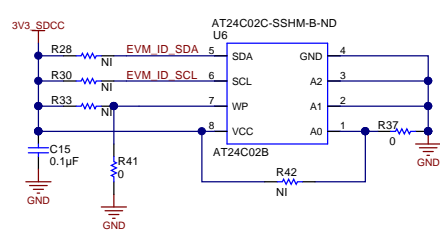
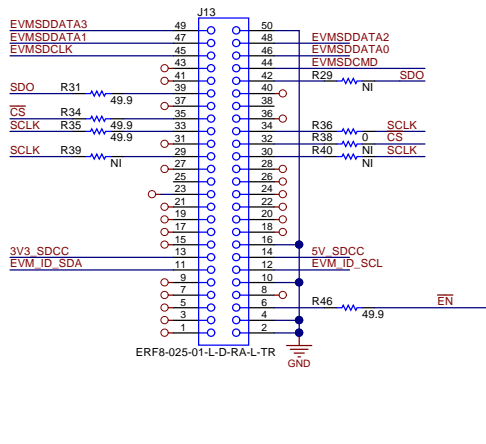
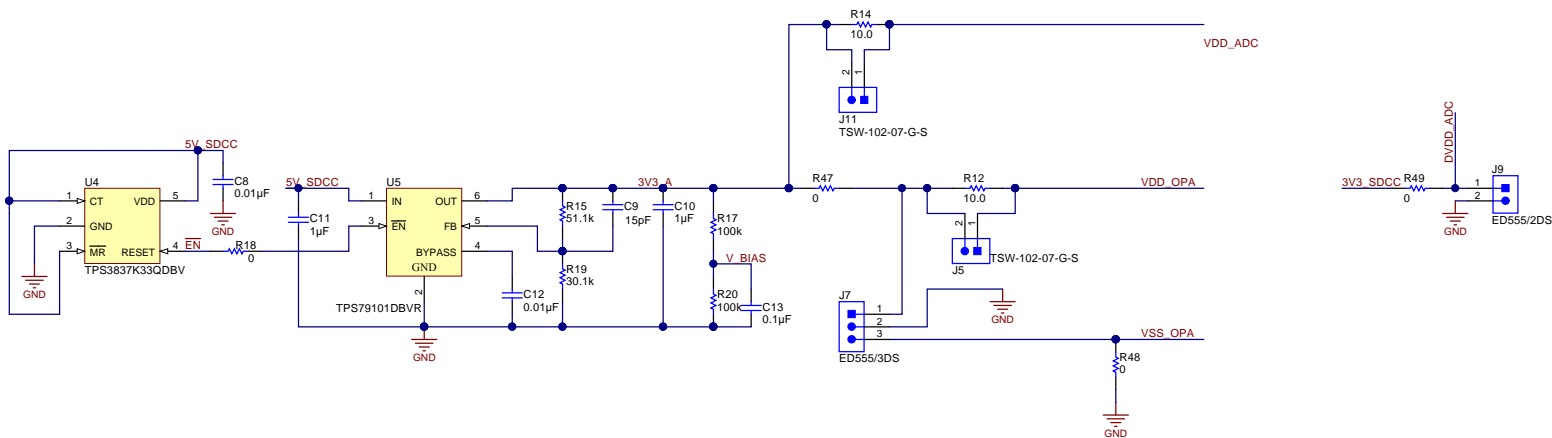
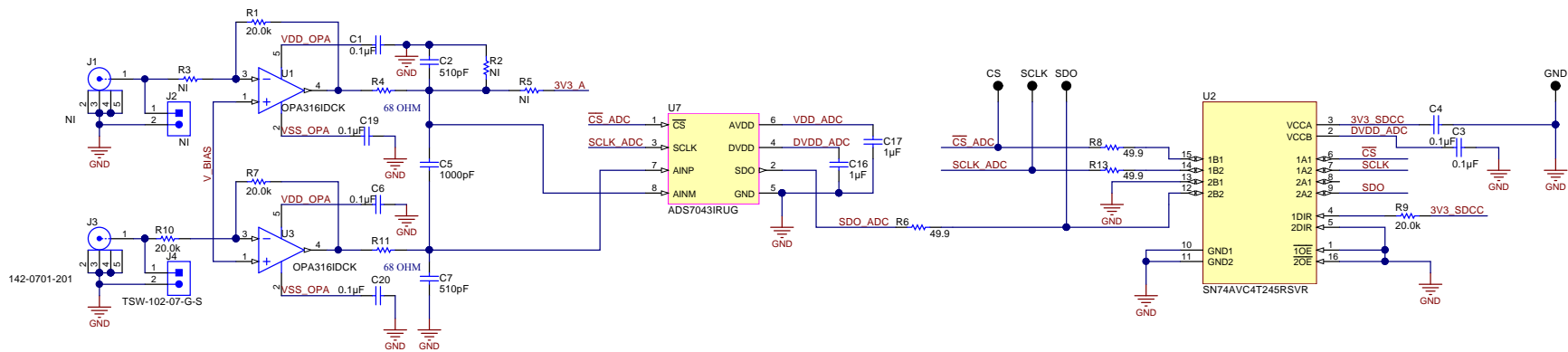


Figure 23. ADS7043EVM PCB: Bottom Layer (L4)

### **7.3 Schematics**

The schematics for the ADS7043EVM are appended to the end of this user's guide.



Title			ADS7043EVM		
Size	Number	Revision			
Date:	13-11-2014	Sheet of			
File:	D:\ADS704x EVM\ADS704x-DE-EVM.Sch	Drawn By:			

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    - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

### CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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## **FCC Interference Statement for Class B EVM devices**

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

#### **Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### **Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

#### **Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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