STM32F318C8 STM32F318K8

ARM®-based Cortex®-M4 32-bit MCU+FPU, 64 KB Flash, 16 KB SRAM, ADC, DAC, 3 COMP, Op-Amp, 1.8 V

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU (72 MHz max.), single-cycle multiplication and HW division, DSP instruction
- Memories
  - 64 Kbyte of Flash memory
  - 16 Kbyte of SRAM on data bus
- CRC calculation unit
- Power management
  - Supply: V_{DD} = 1.8 V ± 8%
    V_{DDA} voltage range = 1.65 V to 3.6 V
  - External POR pin
  - Low-power: Sleep, Stop
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 36 fast I/O ports, all mappable on external interrupt vectors, several 5 V-tolerant
- Interconnect matrix
- 7-channel DMA controller supporting timers, ADCs, SPIs, I^2Cs, USARTs and DAC
- 1 × ADC 0.20 µs (up to 11 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, single ended/differential mode, separate analog supply from 1.8 to 3.6 V
- Temperature sensor
- 1 x 12-bit DAC channel with analog supply from 2.4 to 3.6 V
- Three fast rail-to-rail analog comparators with analog supply from 1.8 to 3.6 V
- 1 x operational amplifier that can be used in PGA mode, all terminal accessible with analog supply from 2.4 to 3.6 V

UFQFPN32
(5 x 5 mm)

WLCSP49
(3.4 x 3.4 mm)

- Up to 17 capacitive sensing channels supporting touchkey, linear and rotary sensors
- Up to 9 timers
  - One 32-bit timer with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - One 16-bit 6-channel advanced-control timer, with up to 6 PWM channels, deadtime generation and emergency stop
  - Three 16-bit timers with IC/OC/OCN or PWM, deadtime gen. and emergency stop
  - One 16-bit basic timer to drive the DAC
  - 2 watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
- Calendar RTC with alarm, periodic wakeup from Stop
- Communication interfaces
  - Three I2Cs with 20 mA current sink to support Fast mode plus
  - Up to 3 USARTs, 1 with ISO 7816 I/F, autobaudrate detect and Dual clock domain
  - Up to two SPIs with multiplexed full duplex I2S
  - Infrared transmitter
- Serial wire debug (SWD), JTAG
- 96-bit unique ID

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F318x8 microcontrollers.

This datasheet should be read in conjunction with the STM32F301x6/8 and STM32F318x8 advanced ARM®-based 32-bit MCUs reference manual (RM0366). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from ARM website www.arm.com.

2 Description

The STM32F318x8 family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz and embedding a floating point unit (FPU). The family incorporates high-speed embedded memories (64 Kbyte of Flash memory, 16 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer a fast 12-bit ADC (5 Msps), three comparators, an operational amplifier, up to 17 capacitive sensing channels, one DAC channel, a low-power RTC, one general-purpose 32-bit timer, one timer dedicated to motor control, and up to three general-purpose 16-bit timers, and one timer to drive the DAC. They also feature standard and advanced communication interfaces: three I^2Cs, up to three USARTs, up to two SPIs with multiplexed full-duplex I2S, and an infrared transmitter.

The STM32F318x8 family operates in the –40 to +85°C and –40 to +105°C temperature ranges from at 1.8 V ± 8% power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F318x8 family offers devices in 32- and 49-pin packages.

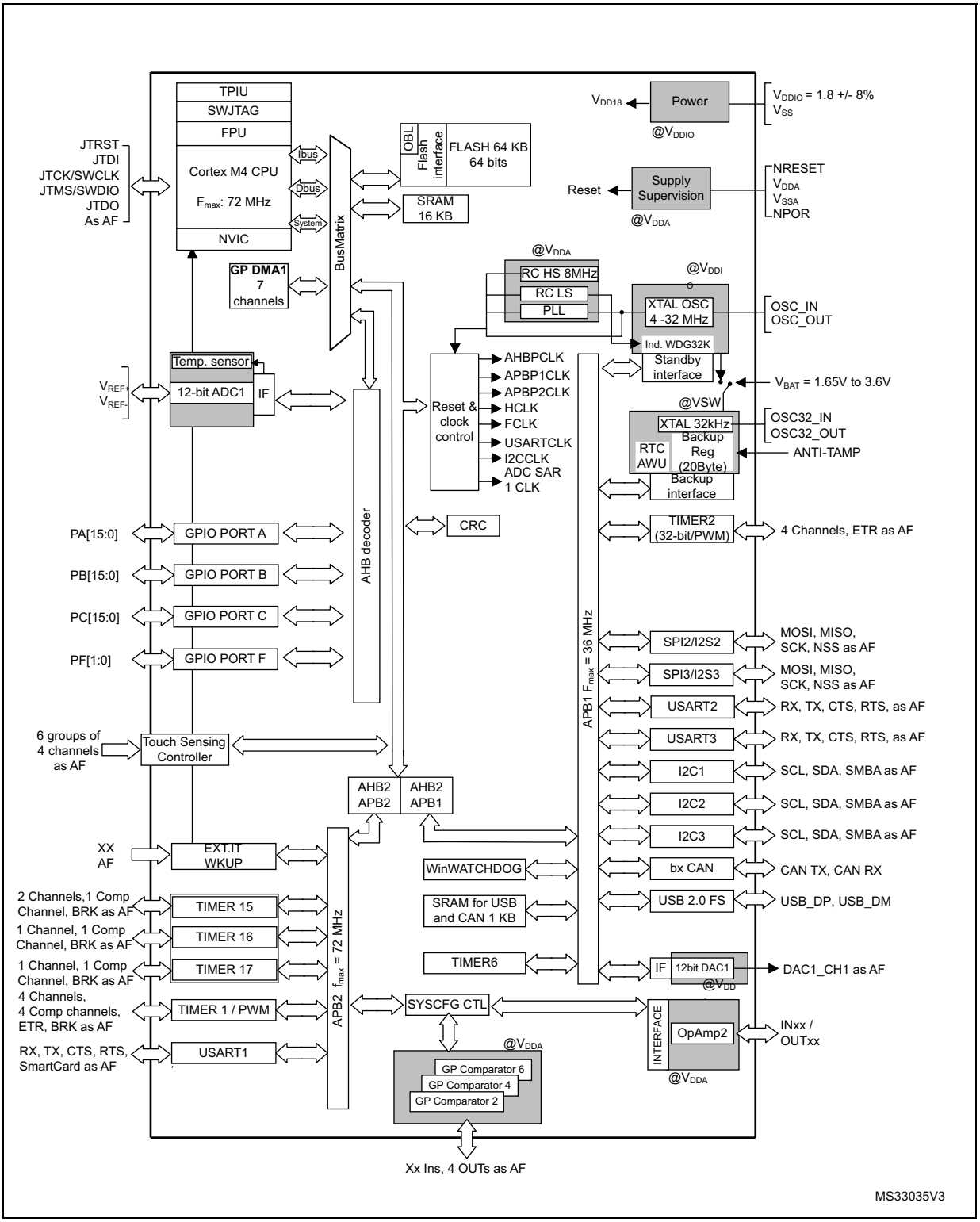
The set of included peripherals changes with the device chosen.

Table 1. STM32F318x8 device features and peripheral counts

Peripheral		STM32F318K8	STM32F318C8
Flash (Kbytes)		64	
SRAM (Kbytes)		16	
Timers	Advanced control	1 (16-bit)	
	General purpose	3 (16-bit) 1 (32 bit)	
	Basic	1	
	SysTick timer	1	
	Watchdog timers (independent, window)	2	
	PWM channels (all) (1)	16	18
	PWM channels (except complementary)	10	12
Comm. interfaces	SPI/I2S	2	
	I^2C	3	
	USART	2	3
GPIOs	Normal I/Os (TC, TTa)	9	19
	5-Volt tolerant I/Os (FT, FT1)	14	17
DMA channels		7	
Capacitive sensing channels		17	
12-bit ADC		1	
Number of ADC channels		8	11
12-bit DAC channels		1	
Analog comparator		2	3
Operational amplifier		1	
CPU frequency		72 MHz	
Operating voltage		V_{DD} = 1.8 V ± 8% V_{DDA} voltage range = 1.65 V to 3.6 V	
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C	
Packages		UFQFPN32	WLCSP49

1. This total number considers also the PWMs generated on the complementary output channels.

Figure 1. STM32F318x8 block diagram



3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU, embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single-precision FPU speeds up software development by using metalanguage development tools while avoiding saturation.

With its embedded ARM core, the STM32F318x8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F318x8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F318x8 devices feature 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

STM32F318x8 devices feature 16 Kbytes of embedded SRAM.

3.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10) or USART2 (PA2/Pa3) or I2C1 (PB6/PB7) or I2C3 (PA8, PB5).

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{SS}, V_{DD} = 1.8 V ± 8% V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 2* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.

Table 2. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC/COMP	1.8 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch which is guaranteed in the full range of V_{DD}) when V_{DD} is not present.

3.5.2 Power supply supervisor

The device power-on reset (POR) is controlled through the external NPOR pin. The device remains in reset state when NPOR pin is held low.

To guarantee a proper power-on reset, the NPOR pin must be held low when V_{DDA} is applied. Then, when V_{DD} is stable, the reset state can be exited by:

- either putting the NPOR pin in high impedance, NPOR pin has an internal pull up
- on forcing the pin to high level by connecting it to V_{DDA}.

3.5.3 Low-power modes

The STM32F318x8 supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, COMPx, I2C or USARTx.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop.

3.6 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 3. STM32F318x8 peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADC1 DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Compx	Comparator output blanking
COMPx	TIMx	Timer input: OCREF_CLR input, input capture
ADC1	TIM1	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx PVD GPIO	TIM1 TIM15, 16, 17	Timer break

Table 3. STM32F318x8 peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO	TIMx	External trigger, timer break
	ADC1 DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, please refer to the corresponding sections in the STM32F301x6/8 and STM32F318x8 *reference manual RM0366.*

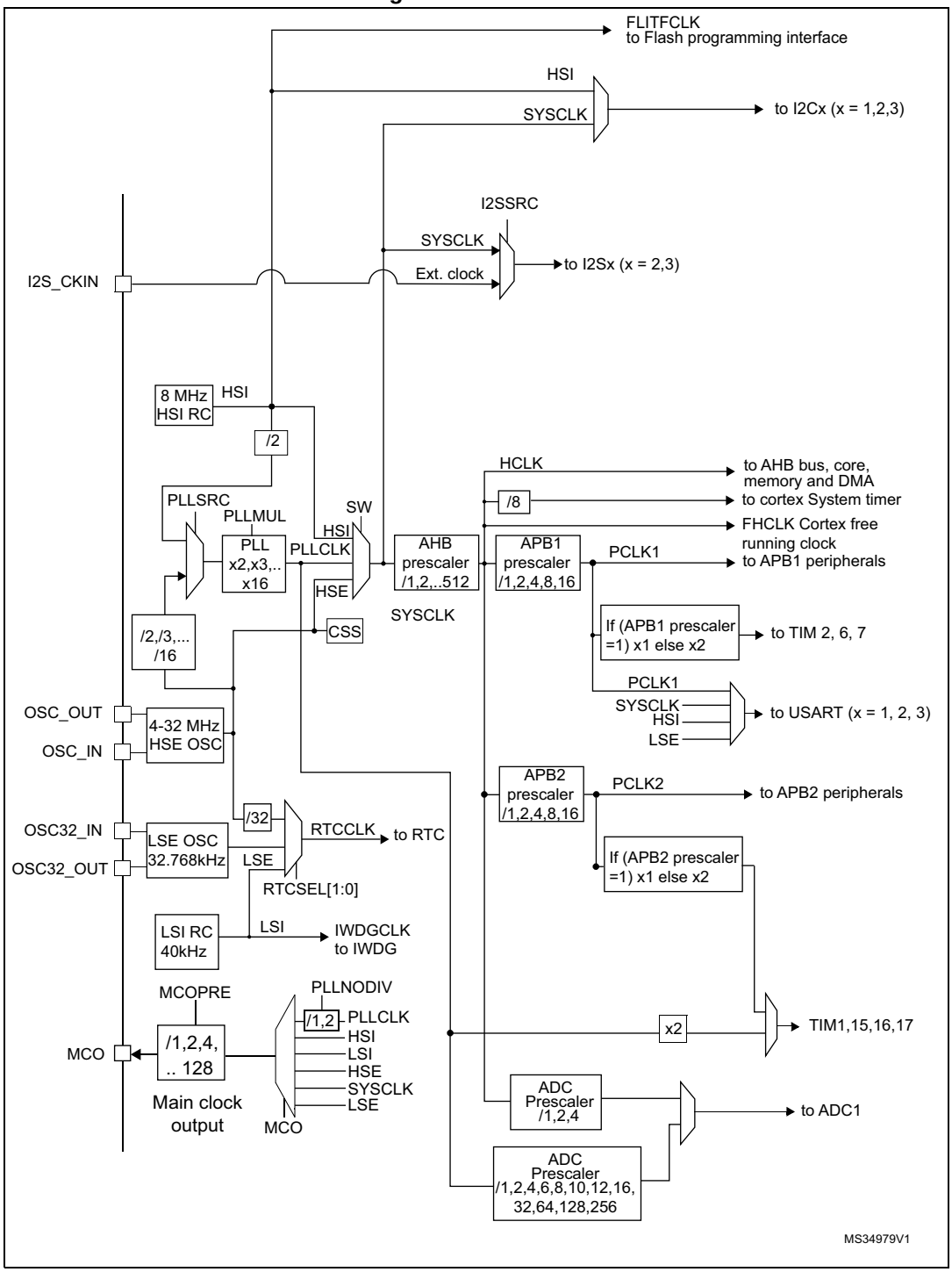
3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. To achieve audio class performance, an audio crystal can be used.

Figure 2. Clock tree



3.8 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.9 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, timers, DAC and ADC.

3.10 Interrupts and events

3.10.1 Nested vectored interrupt controller (NVIC)

The STM32F318x8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11 Fast analog-to-digital converter (ADC)

An analog-to-digital converter, with selectable resolution between 12 and 6 bit, is embedded in the STM32F318x8 family devices. The ADC has up to 11 external channels performing conversions in single-shot or scan modes. Channels can be configured to be either single-ended input or differential input. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available. The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.11.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.11.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC1_IN18 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.11.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.12 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

3.13 Operational amplifier (OPAMP)

The STM32F318x8 embeds one operational amplifier with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When the operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

3.14 Ultra-fast comparators (COMP)

The STM32F318x8 devices embed up to three ultra-fast rail-to-rail comparators which offer the features below:

- Programmable internal or external reference voltage
- Selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 22: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, and also generate interrupts and breaks for the timers.

3.15 Timers and watchdogs

The STM32F318x8 includes advanced control timer, up to general-purpose timers, basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
Advanced control	TIM1(1)	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
	TIM15(1)	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TIM16(1), TIM17(1)	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. TIM1/15/16/17 can be clocked from the PLL running at 144 MHz when the system clock source is the PLL and AHB or APB2 subsystem clocks are not divided by more than 2 cumulatively.

3.15.1 Advanced timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.15.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.15.2 General-purpose timers (TIM2, TIM15, TIM16, TIM17)

There are up to four synchronizable general-purpose timers embedded in the STM32F318x8 (see *Table 4* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

TIM2

TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

It features 4 independent channels for input capture/output compare, PWM or one-pulse mode output. It can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

It has independent DMA request generation and supports quadrature encoders.

TIM15, TIM16 and TIM 17

These three timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM15 has 2 channels and 1 complementary channel
- TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

3.15.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop mode. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.16 Real-time clock (RTC) and backup registers

The RTC and the 20 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the VBAT pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wake up from Stop mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop mode on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop mode on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.17 Inter-integrated circuit interfaces (I^2C)

The devices feature three I^2C bus interfaces which can operate in multimaster and slave mode. Each I2C interface can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

All I^2C interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 5. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2Cx (x=1,3) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 6* for the features available in I2C1, I2C2 and I2C3.

Table 6. STM32F318x8 I^2C implementation

I2C features(1)	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
SMBus	X	X	X
Wakeup from STOP	X	X	X

1. X = supported.

3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F318x8 devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbit/s.

All USARTs support hardware management of the CTS and RTS signals, multiprocessor communication mode, single-wire half-duplex communication mode and synchronous mode.

USART1 supports SmartCard mode, IrDA SIR ENDEC, LIN Master capability and autobaudrate detection.

All USART interfaces can be served by the DMA controller.

Refer to *Table 7* for the features available in all USARTs interfaces.

Table 7. USART features

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
SmartCard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	-	-
LIN mode	X	-	-
Dual clock domain and wakeup from Stop mode	X	-	-
Receiver timeout interrupt	X	-	-
Modbus communication	X	-	-
Auto baud rate detection	X	-	-
Driver Enable	X	X	X

1. X = supported.

3.19 Serial peripheral interfaces (SPI)/Inter-integrated sound interfaces (I2S)

Two SPI interfaces (SPI2 and SPI3) allow communication up to 18 Mbit/s in slave and master modes in full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master

mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 8* for the features available in SPI2 and SPI3.

Table 8. STM32F318x8 SPI/I2S implementation

SPI features[1]	SPI2	SPI3
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	X
TI mode	X	X

1. X = supported.

3.20 Touch sensing controller (TSC)

The STM32F318x8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 17 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (for example glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Table 9. Capacitive sensing GPIOs available on STM32F318x8 devices

Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0
	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
4	TSC_G4_IO1	PA9
	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA13
	TSC_G4_IO4	PA14
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
6	TSC_G6_IO1	PB11
	TSC_G6_IO2	PB12
	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14

Table 10. No. of capacitive sensing channels available on STM32F318x8 devices

Analog I/O group	Number of capacitive sensing channels	
	STM32F318C8	STM32F318K8
G1	3	3
G2	3	3
G3	2	1
G4	3	3
G5	3	3
G6	3	0
Number of capacitive sensing channels	17	13

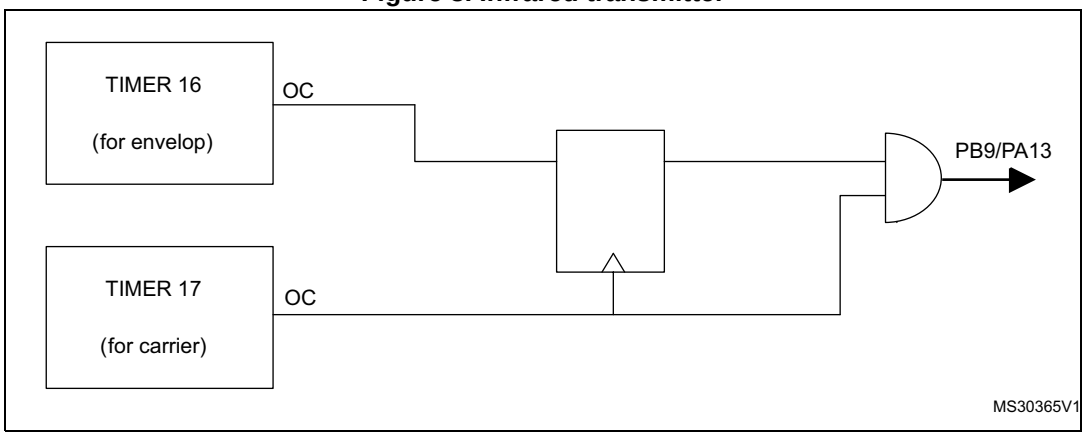
3.21 Infrared transmitter

The STM32F318x8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.22 Development support

3.22.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

4 Pinouts and pin description

Figure 4. STM32F318x8 UFQFPN32 pinout

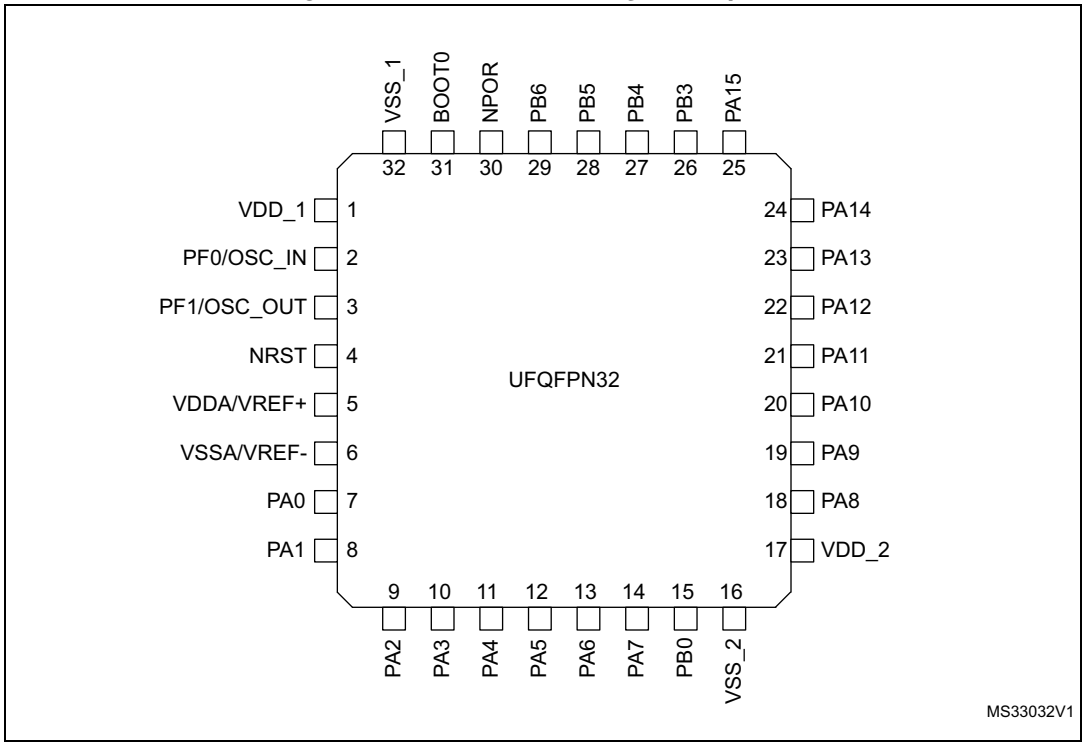


Figure 5. STM32F318x8 WLCSP49 ballout

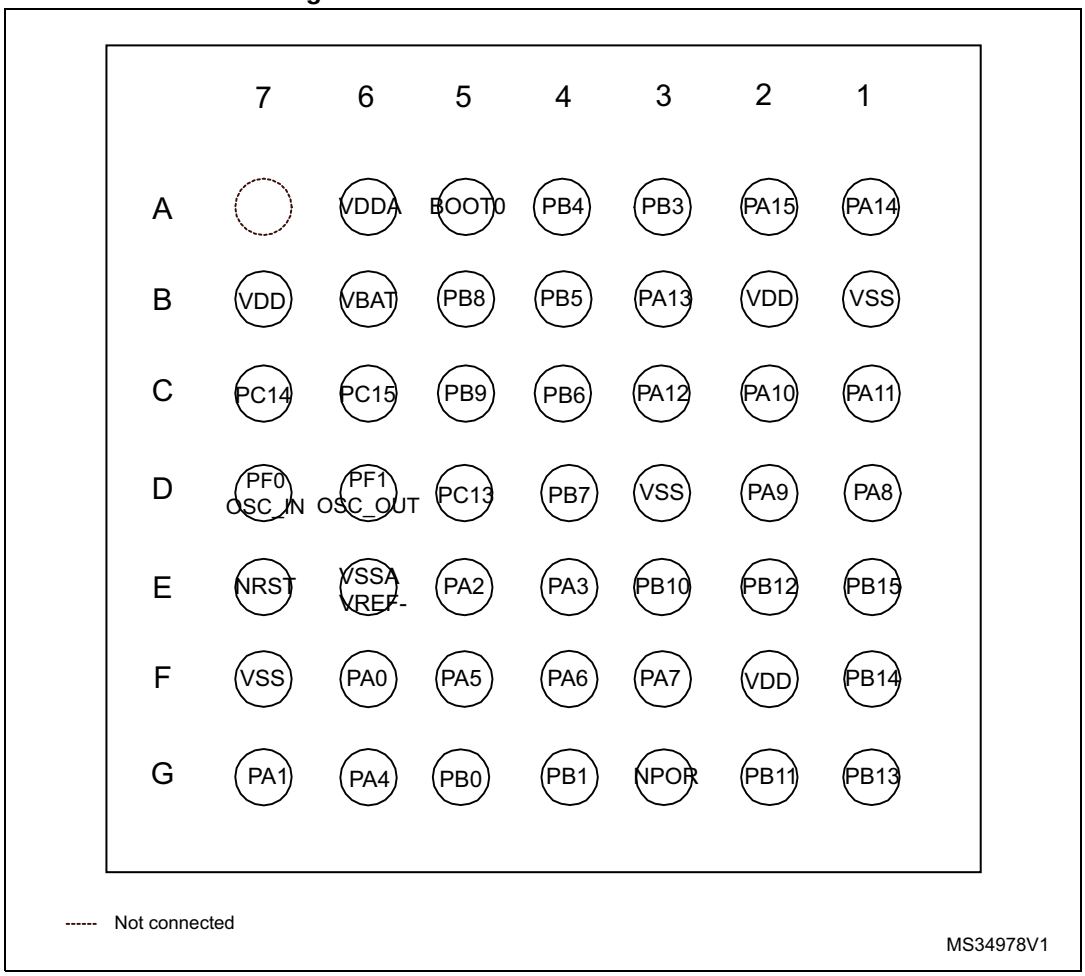


Table 11. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, I2C FM+ option
		TTa	3.3 V tolerant I/O directly connected to ADC1
		TT	3.3 V tolerant I/O
		TC	Standard 3.3V I/O
		POR	Dedicated to NPOR pin
		B	Dedicated BOOT0 pin
		RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. STM32F318x8 pin definitions

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49						
-	B6	VBAT	S	-		Backup power supply	
-	D5	PC13(1) TAMPER1 WKUP2 (PC13)	I/O	TC	(1)	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
-	C7	PC14(1) OSC32_IN (PC14)	I/O	TC	(1)	-	OSC32_IN
-	C6	PC15(1) OSC32_OUT (PC14)	I/O	TC	(1)	-	OSC32_OUT
2	D7	PF0 OSC_IN (PF0)	I/O	FTf		I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N	OSC_IN
3	D6	PF1 OSC_OUT (PF1)	O	FTf		I2C2_SCL, SPI2_SCK/I2S2_CK	OSC_OUT
4	E7	NRST	I/O	RST		Device reset input/internal reset output (active low)	
6	E6	VSSA/VREF-	S	-		Analog ground/Negative reference voltage	
5	A6	VDDA/VREF+	S	-		Analog power supply/Positive reference voltage	
7	F6	PA0 -TAMPER2-WKUP1	I/O	TTa		TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, EVENTOUT	ADC1_IN1, RTC_TAMP2, WKUP1

Table 12. STM32F318x8 pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49						
8	G7	PA1	I/O	TTa		RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC1_IN2
9	E5	PA2	I/O	TTa		TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3, COMP2_INM
10	E4	PA3	I/O	TTa		TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4
-	F7	VSS_4	S	-		-	-
-	F2	VDD_4	S	-		-	-
11	G6	PA4	I/O	TTa	(2)	TSC_G2_IO1, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN5, DAC1_OUT1, COMP2_INM, COMP4_INM, COMP6_INM
12	F5	PA5	I/O	TTa		TIM2_CH1/TIM2_ETR, TSC_G2_IO2, EVENTOUT	OPAMP2_VINM
13	F4	PA6	I/O	TTa	(2)	TIM16_CH1, TSC_G2_IO3, TIM1_BKIN, EVENTOUT	ADC1_IN10, OPAMP2_VOUT
14	F3	PA7	I/O	TTa		TIM17_CH1, TSC_G2_IO4, TIM1_CH1N, EVENTOUT	ADC1_IN15, COMP2_INP, OPAMP2_VINP

Table 12. STM32F318x8 pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49						
15	G5	PB0	I/O	TTa		TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	G4	PB1	I/O	TTa		TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC1_IN12
-	E3	PB10	I/O	TT		TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	-
-	G2	PB11	I/O	TTa		TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC1_IN14, COMP6_INP
16	D3	VSS_2	S	-		Digital ground	
17	B2	VDD_2	S	-		Digital power supply	
-	E2	PB12	I/O	TT		TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	-
-	G1	PB13	I/O	TTa		TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC1_IN13
-	F1	PB14	I/O	TTa		TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS_DE, EVENTOUT	OPAMP2_VINP

Table 12. STM32F318x8 pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49						
-	E1	PB15	I/O	TTa		RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	COMP6_INM
18	D1	PA8	I/O	FT		MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, EVENTOUT	-
19	D2	PA9	I/O	FTf		I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT	-
20	C2	PA10	I/O	FTf		TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, EVENTOUT	-
21	C1	PA11	I/O	FT		SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, TIM1_CH4, TIM1_BKIN2, EVENTOUT	-
22	C3	PA12	I/O	FT		TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, TIM1_ETR, EVENTOUT	-
23	B3	PA13	I/O	FT		SWDIO, TIM16_CH1N, TSC_G4_IO3, IR-OUT, USART3_CTS, EVENTOUT	-

Table 12. STM32F318x8 pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49						
-	B1	VSS_3	S	-		Digital ground	
-	B2	VDD_3	S	-		Digital power supply	
24	A1	PA14	I/O	FTf		SWCLK-JTCK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT	-
25	A2	PA15	I/O	FTf		JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI3_NSS/I2S3_WS, USART2_RX, TIM1_BKIN, EVENTOUT	-
26	A3	PB3	I/O	FT		JTDO-TRACESWO, TIM2_CH2, TSC_G5_IO1, SPI3_SCK/I2S3_CK, USART2_TX, EVENTOUT	-
27	A4	PB4	I/O	FT		JTRST, TIM16_CH1, TSC_G5_IO2, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT	-
28	B4	PB5	I/O	FT		TIM16_BKIN, I2C1_SMBAI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT	-
29	C4	PB6	I/O	FTf		TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, EVENTOUT	-

Table 12. STM32F318x8 pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49						
-	D4	PB7	I/O	FTf		TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, EVENTOUT	-
30	G3	NPOR	I	POR		Device power-on reset input	
31	A5	BOOT0	I	B		Boot memory selection	
-	B5	PB8	I/O	FTf		TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX TIM1_BKIN, EVENTOUT	-
-	C5	PB9	I/O	FTf		TIM17_CH1, I2C1_SDA, IR-OUT, USART3_TX, COMP2_OUT, EVENTOUT	-
32	D3	VSS_1	S	-		Digital ground	
"1"	B7	VDD_1	S	-		Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:

   - The speed should not exceed 2 MHz with a maximum load of 30 pF

   - These GPIOs must not be used as current sources (e.g. to drive an LED).

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0366 reference manual.

2. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 13. Alternate functions for Port A

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			EVENT
PA0	-	TIM2_CH1/ TIM2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	-	-	-	-	-	-		EVENT OUT
PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS_DE	-	-	-	-	-	-	-	EVENT OUT
PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENT OUT
PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	-	-	-	-	-	-	EVENT OUT
PA4	-	-	-	TSC_G2_IO1	-	-	SPI3_NSS/ I2S3_WS	USART2_CK	-	-	-	-	-	-	-	EVENT OUT
PA5	-	TIM2_CH1/ TIM2_ETR	-	TSC_G2_IO2	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PA6	-	TIM16_CH1	-	TSC_G2_IO3	-	-	TIM1_BKIN	-	-	-	-	-	-	-	-	EVENT OUT
PA7	-	TIM17_CH1	-	TSC_G2_IO4	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENT OUT
PA8	MCO	-	-	I2C3_SCL	I2C2_SMBAL	I2S2_MCK	TIM1_CH1	USART1_CK	-	-	-	-	-	-	-	EVENT OUT

Table 13. Alternate functions for Port A (continued)

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			EVENT
PA9	-	-	I2C3_SMBAL	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	-	-	TIM2_CH3	-	-	-	-	EVENT OUT
PA10	-	TIM17_BKIN		TSC_G4_IO2	I2C2_SDA	SPI2_MISO/I2S2ext_SD	TIM1_CH3	USART1_RX	COMP6_OUT		TIM2_CH4	-	-	-	-	EVENT OUT
PA11	-	-	-	-	-	SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS	-	-	-	TIM1_CH4	TIM1_BKIN2	-	-	EVENT OUT
PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	-	-	TIM1_ETR	-	-	-	EVENT OUT
PA13	SWDAT-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR-OUT	-	USART3_CTS	-	-	-	-	-	-	-	EVENT OUT
PA14	SWCLK-JTCK		-	TSC_G4_IO4	I2C1_SDA	-	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	-	EVENT OUT
PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	TSC_SYNC	I2C1_SCL	-	SPI3_NSS/ I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	-	EVENT OUT

Table 14. Alternate functions for Port B

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16/TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/TIM16/TIM17	SPI2/I2S2/SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/Infrared	USART1/USART2/USART3/GPCOMP6	I2C3/GPCOMP2/GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			EVENT
PB0	-	-	-	TSC_G3_IO2	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	EVENT OUT
PB1	-	-	-	TSC_G3_IO3	-	-	TIM1_CH3N	-	COMP4_OUT	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACESWO	TIM2_CH2	-	TSC_G5_IO1	-	-	SPI3_SCK/I2S3_CK	USART2_TX	-	-	-	-	-	-	-	EVENT OUT
PB4	JTRST	TIM16_CH1	-	TSC_G5_IO2	-	-	SPI3_MISO/I2S3_SD	USART2_RX	-	-	TIM17_BKIN	-	-	-	-	EVENT OUT
PB5	-	TIM16_BKIN	-		I2C1_SMBAI	-	SPI3_MOSI/I2S3ext_SD	USART2_CK	I2C3_SDA	-	TIM17_CH1	-	-	-	-	EVENT OUT
PB6	-	TIM16_CH1N	-	TSC_G5_IO3	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	-	EVENT OUT
PB7	-	TIM17_CH1N	-	TSC_G5_IO4	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	-	-	EVENT OUT
PB8	-	TIM16_CH1	-	TSC_SYNC	I2C1_SCL	-	-	USART3_RX	-	-	-	-	TIM1_BKIN	-	-	EVENT OUT
PB9	-	TIM17_CH1	-		I2C1_SDA	-	IR-OUT	USART3_TX	COMP2_OUT	-	-	-	-	-	-	EVENT OUT
PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	-	-	EVENT OUT

Table 14. Alternate functions for Port B (continued)

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			EVENT
PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	-	-	EVENT OUT
PB12	-	-	-	TSC_G6_IO2	I2C2_SMBAL	SPI2_NSS/I2S2_WS	TIM1_BKIN	USART3_CK	-	-	-	-	-	-	-	EVENT OUT
PB13	-	-	-	TSC_G6_IO3	-	SPI2_SCK/ I2S2_CK	TIM1_CH1N	USART3_CTS	-	-	-	-	-	-	-	EVENT OUT
PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	SPI2_MISO/I2S2ext_SD	TIM1_CH2N	USART3_RTS_DE	-	-	-	-	-	-	-	EVENT OUT
PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	SPI2_MOSI/ I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 15. Alternate functions for Port F

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2/ TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/ Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/USART2/USART3/ GPCOMP6
PF0	-	-	-	-	I2C2_SDA	SPI2_NSS/ I2S2_WS	TIM1_CH3N	-
PF1	-	-	-	-	I2C2_SCL	SPI2_SCK/ I2S2_CK	-	-

5 Memory mapping

Figure 6. STM32F318x8 memory mapping

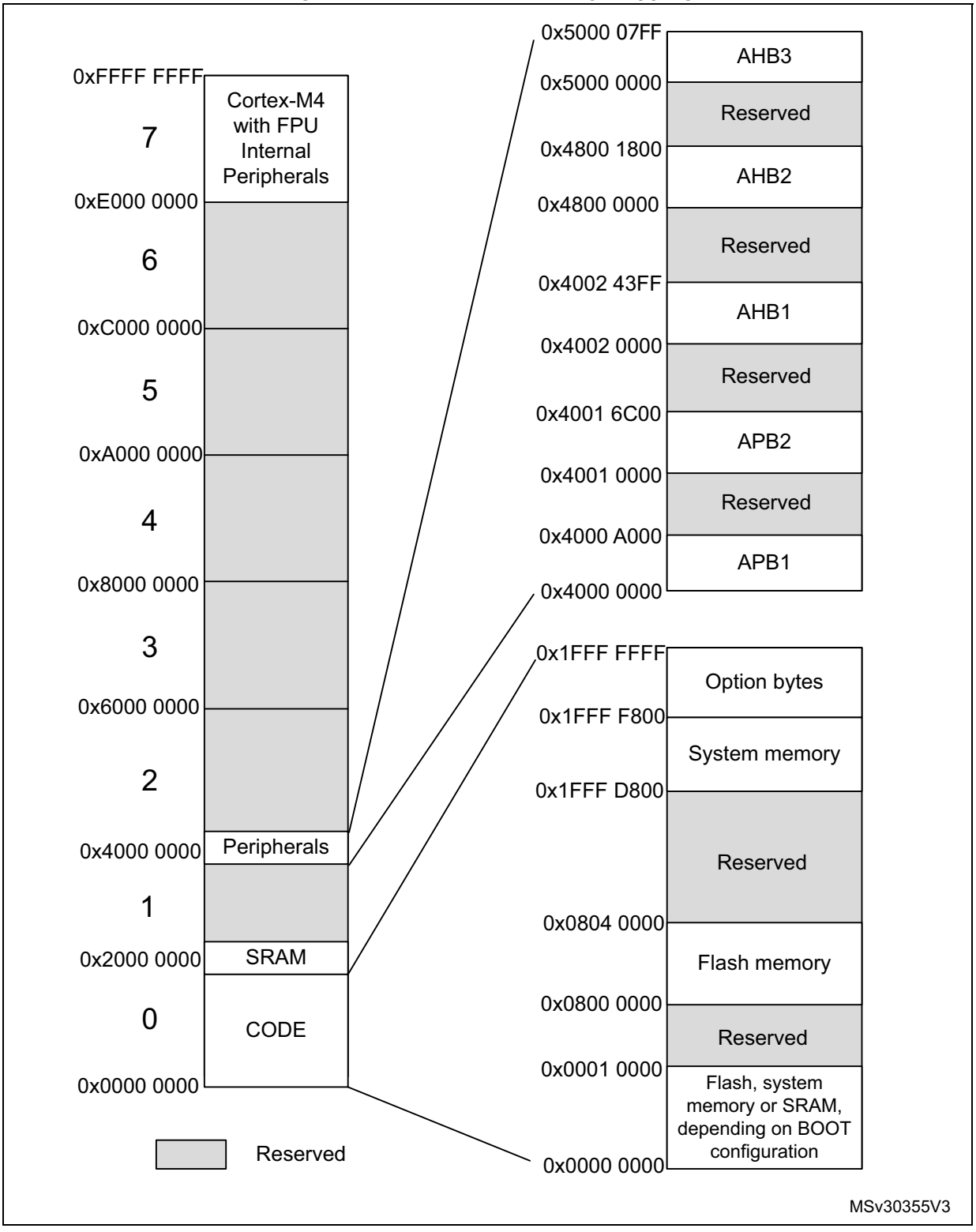


Table 16. STM32F318x8 peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 K	Reserved
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0400 - 0x4002 0FFF	3 K	Reserved
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3000 - 0x4001 37FF	2 K	Reserved
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	8 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
	0x4000 9C00 - 0x4000 FFFF	25 K	Reserved

Table 16. STM32F318x8 peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 7C00 - 0x4000 9BFF	8 K	Reserved
	0x4000 7800 - 0x4000 7BFF	1 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC1
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 5C00 - 0x4000 6FFF	5 K	Reserved
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 4C00 - 0x4000 53FF	2 K	Reserved
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1400 - 0x4000 27FF	5 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0400 - 0x4000 0FFF	3 K	Reserved
	0x4000 0000 - 0x4000 03FF	1 K	TIM2
	0x2000 4000 - 3FFF FFFF	~512 M	Reserved
	0x2000 0000 - 0x2000 3FFF	16 K	SRAM
	0x1FFF F800 - 0x1FFF FFFF	2 K	Option bytes
	0x1FFF D800 - 0x1FFF F7FF	8 K	System memory
	0x0801 0000 - 0x1FFF D7FF	~384 M	Reserved
	0x0800 0000 - 0x0800 FFFF	64 K	Main Flash memory
	0x0001 0000 - 0x07FF FFFF	~128 M	Reserved
	0x0000 000 - 0x0000 FFFF	64 K	Main Flash memory, system memory or SRAM depending on BOOT configuration

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V,V_{DDA}= 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

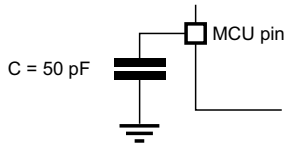
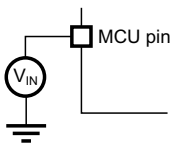
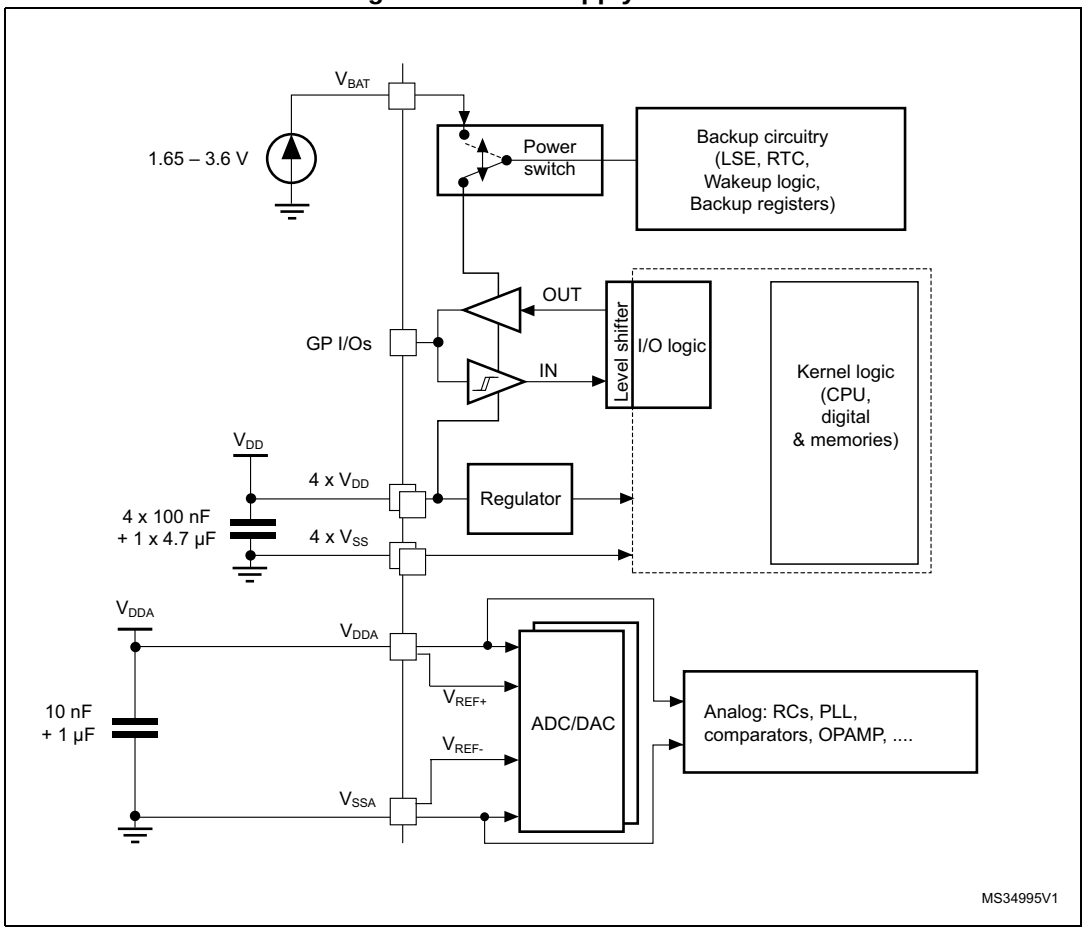


Figure 8. Pin input voltage



6.1.6 Power supply scheme

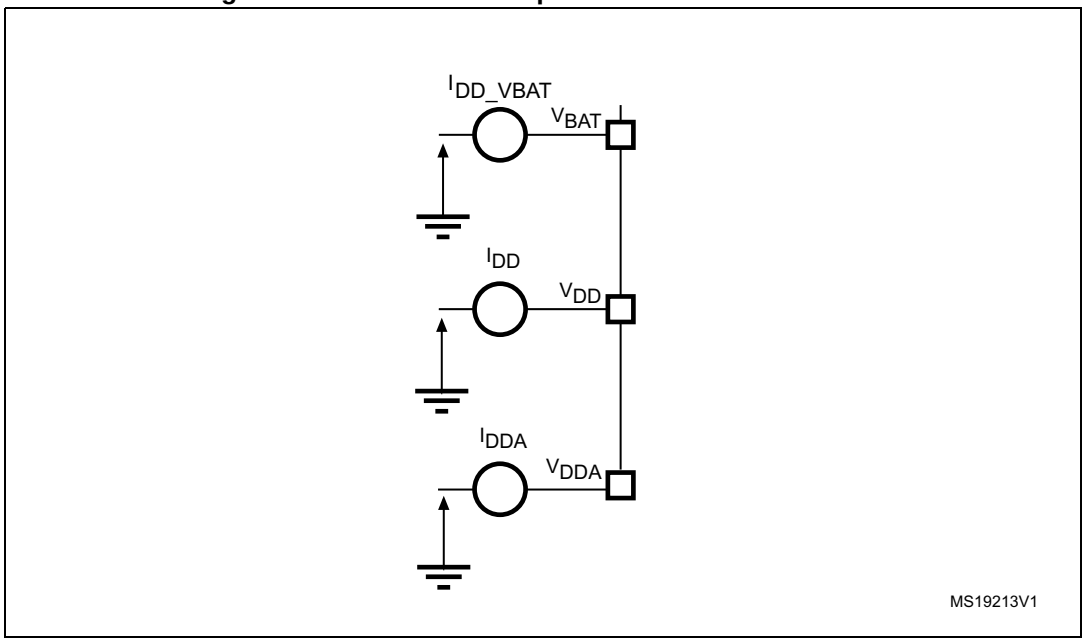
Figure 9. Power supply scheme



Caution: Each power supply pair (for example V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 17: Voltage characteristics*, *Table 18: Current characteristics*, and *Table 19: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DD} and V_{BAT})	-0.3	1.95	V
V_{DDA}–V_{SS}	External main supply voltage	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DD} + 4.0	V
	Input voltage on TTa and TT pins	V_{SS} – 0.3	4.0	
	Input voltage on POR pin	V_{SS} – 0.3	V_{DDA} + 4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		V

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{IN} maximum must always be respected. Refer to *Table 18: Current characteristics* for the maximum allowed injected current values.

Table 18. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	130	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	-130	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	+/-5	
	Injected current on TTa pins(5)	+/-5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	+/-25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 17: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 61*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 20. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	1.65	1.95	V
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	1.65	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
	Analog operating voltage		1.8	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	–0.3	V_{DD}+0.3	V
		TT I/O(1)	-0.3	3.6	
		TTa I/O pins and POR pin	–0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	–0.3	5.2	
		BOOT0	0	5.2	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	WLCSP49	-	408	mW
		UFQFPN32	-	540	mW
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}. See *Table 72: Package thermal characteristics*.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}. See *Table 72: Package thermal characteristics*

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 21* are derived from tests performed under the ambient temperature condition summarized in *Table 20*.

Table 21. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reference voltage

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 22. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24 (1)	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 1.8 V ±10 mV	-	-	10(2)	mV
T_{Coeff}	Temperature coefficient	-	-	-	100 (2)	ppm/°C
T_{REFINT_RDY} (3)	Internal reference voltage temporization	-	1.5	2.5	4.5	ms

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. Guaranteed by design, not tested in production. Latency between the time when pin NPOR is set to 1 by the application and the time when $V_{REFINTRDYF}$ is set to 1 by the hardware.

Table 23. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: The total current consumption is the sum of I_{DD} and I_{DDA}.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When f_{HCLK} > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 24* to *Table 30* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 24. Typical and maximum current consumption from VDD supply at VDD = 1.8V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25°C	85°C	105°C		25°C	85°C	105°C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	43.8	47.6	48.9	52.0	24.7	26.3	26.9	28.1	mA
			64 MHz	39.3	42.6	43.7	46.2	22.1	23.6	24.1	25.0	
			48 MHz	30.0	32.3	33.2	34.8	16.9	18.0	18.4	19.0	
			32 MHz	20.5	21.8	22.5	23.4	11.6	12.3	12.6	12.9	
			24 MHz	15.7	16.6	17.2	17.7	8.9	9.4	9.7	10.0	
			8 MHz	5.3	5.6	5.8	6.4	3.11	3.24	3.45	3.59	
			1 MHz	0.99	1.13	1.19	1.36	0.71	0.84	0.88	1.03	
		Internal clock (HSI)	64 MHz	36.2	39.0	39.8	41.8	21.9	23.3	23.7	24.5	
			48 MHz	27.7	29.7	30.4	31.6	16.7	17.8	18.1	18.6	
			32 MHz	19.0	20.3	20.7	21.4	11.5	12.2	12.3	12.6	
			24 MHz	14.6	15.5	15.9	16.3	6.0	6.4	6.5	6.7	
			8 MHz	5.2	5.5	5.7	5.8	3.09	3.31	3.38	3.51	

Table 24. Typical and maximum current consumption from VDD supply at VDD = 1.8V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25°C	85°C	105°C		25°C	85°C	105°C	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	43.4	47.2(2)	48.5	51.3(2)	24.3	26.0(2)	26.5	27.6(2)	mA
			64 MHz	38.9	42.0	43.2	45.6	21.6	23.1	23.7	24.5	
			48 MHz	29.4	31.6	32.6	34.1	16.6	17.6	18.1	18.7	
			32 MHz	20.0	21.3	22.0	22.8	11.1	11.8	12.1	12.4	
			24 MHz	15.1	16.2	16.6	17.1	8.4	8.9	9.2	9.4	
			8 MHz	4.95	5.31	5.52	5.69	2.73	2.95	3.10	3.24	
			1 MHz	0.60	0.73	0.83	0.99	0.33	0.40	0.52	0.69	
		Internal clock (HSI)	64 MHz	35.6	38.3	39.1	41.0	21.3	22.8	23.2	23.9	
			48 MHz	27.1	29.0	29.6	30.8	16.1	17.2	17.4	17.9	
			32 MHz	18.4	19.6	20.0	20.7	10.8	11.6	11.8	12.0	
			24 MHz	13.9	14.8	15.2	15.6	5.4	5.8	6.0	6.1	
			8 MHz	4.69	5.02	5.19	5.34	2.60	2.81	2.92	3.05	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	29.1	31.2(2)	32.4	33.9(2)	5.9	6.3(2)	6.6	6.8(2)	
			64 MHz	26.0	27.9	28.8	30.1	5.3	5.6	5.9	6.1	
			48 MHz	16.5	17.6	18.3	19.0	3.37	3.63	3.83	3.98	
			32 MHz	13.3	14.2	14.7	15.2	2.74	2.94	3.10	3.26	
			24 MHz	10.1	10.7	11.2	11.5	2.12	2.30	2.42	2.56	
			8 MHz	3.28	3.54	3.76	3.93	0.66	0.77	0.88	1.05	
			1 MHz	0.40	0.50	0.61	0.78	0.09	0.14	0.27	0.41	
		Internal clock (HSI)	64 MHz	22.6	24.2	24.9	25.9	4.89	5.21	5.41	5.58	mA
			48 MHz	17.2	18.4	18.9	19.5	3.70	3.96	4.12	4.27	
			32 MHz	11.7	12.4	12.8	13.2	2.49	2.66	2.81	2.96	
			24 MHz	8.9	9.4	9.7	10.0	1.28	1.46	1.59	1.68	
			8 MHz	3.02	3.26	3.42	3.58	0.53	0.64	0.74	0.91	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 25. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	72 MHz	225	248(3)	261	266(3)	248	270(3)	290	296(3)	µA
			64 MHz	198	221	234	239	219	241	258	263	
			48 MHz	149	169	178	182	163	182	196	200	
			32 MHz	102	120	128	131	112	131	139	142	
			24 MHz	79	96	101	104	87	104	110	112	
			8 MHz	3.1	4.1	4.1	5.1	3.1	4.1	4.1	5.1	
			1 MHz	3.1	4.1	4.1	5.1	3.1	4.1	4.1	5.1	
		HSI clock	64 MHz	263	287	301	306	292	317	333	339	
			48 MHz	214	236	248	252	237	260	272	277	
			32 MHz	167	187	196	199	185	206	216	219	
			24 MHz	144	164	171	173	161	179	188	191	
			8 MHz	67	81	85	86	77	91	93	95	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based on characterization results and tested in production with code executing from RAM.

Table 26. Typical and maximum V_{DD} consumption in Stop mode

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}= 1.8 V V_{DDA} = 3.3 V)	Max			Unit
			1.8 V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD}	Supply current in Stop mode	All oscillators off	3.11	7.3	160	359	µA

Table 27. Typical and maximum V_{DDA} consumption in Stop mode

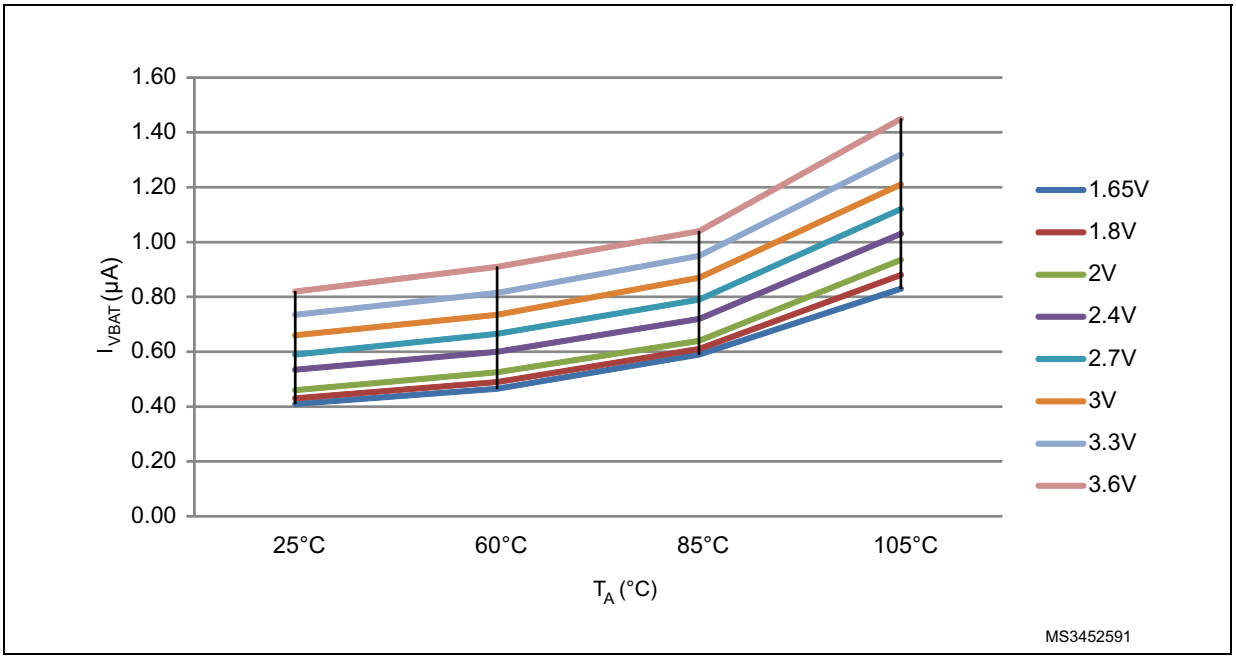
Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD} = 1.8 V)							Max			Unit
			1.8 V	2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DDA}	Supply current in Stop mode	All oscillators off	0.70	0.71	0.73	0.76	0.81	0.87	0.94	1.6	2.1	2.7	µA

Table 28. Typical and maximum current consumption from V_{BAT} supply

Symbol	Para meter	Conditions (1)	Typ.@V_{BAT}								Max. @V_{BAT}= 3.6V(2) T_A (°C)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	25	85	105	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; “Xtal mode” lower driving capability; LSEDRV[1:0] = '00'	0.41	0.43	0.46	0.54	0.59	0.66	0.74	0.82	-	-	-	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.65	0.68	0.73	0.80	0.87	0.95	1.03	1.14	-	-	-	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

Figure 11. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ‘00’)



Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = 1.8 V, V_{DDA} = 3.3 V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 29. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	42.6	24.0	mA
			64 MHz	38.2	21.6	
			48 MHz	29.1	16.5	
			32 MHz	19.9	11.3	
			24 MHz	15.2	8.6	
			16 MHz	10.2	5.9	
			8 MHz	5.2	3.08	
			4 MHz	2.97	1.79	
			2 MHz	1.76	1.13	
			1 MHz	1.16	0.80	
			500 kHz	0.86	0.63	
			125 kHz	0.63	0.50	
I_{DDA} (1)	Supply current in Run mode from V_{DDA} supply		72 MHz	237.3		µA
			64 MHz	208.7		
			48 MHz	154.6		
			32 MHz	105.1		
			24 MHz	81.3		
			16 MHz	57.7		
			8 MHz	0.87		
			4 MHz	0.87		
			2 MHz	0.87		
			1 MHz	0.87		
			500 kHz	0.87		
			125 kHz	0.87		

1. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 30. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	27.5	5.6	mA
			64 MHz	24.5	5.0	
			48 MHz	18.5	3.82	
			32 MHz	12.5	2.62	
			24 MHz	9.4	2.02	
			16 MHz	6.3	1.42	
			8 MHz	3.08	0.65	
			4 MHz	1.93	0.55	
			2 MHz	1.24	0.48	
			1 MHz	0.90	0.44	
			500 kHz	0.73	0.42	
			125 kHz	0.59	0.41	
I_{DDA} (1)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	237.3		µA
			64 MHz	208.7		
			48 MHz	154.6		
			32 MHz	105.1		
			24 MHz	81.3		
			16 MHz	57.7		
			8 MHz	0.87		
			4 MHz	0.87		
			2 MHz	0.87		
			1 MHz	0.87		
			500 kHz	0.87		
			125 kHz	0.87		

1. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 48: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 32: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 31. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 1.8 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.10	mA
			4 MHz	0.17	
			8 MHz	0.40	
			18 MHz	0.78	
			36 MHz	1.51	
			48 MHz	2.06	
		V_{DD} = 1.8 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.14	
			4 MHz	0.25	
			8 MHz	0.57	
			18 MHz	1.16	
			36 MHz	2.45	
			48 MHz	3.03	
		V_{DD} = 1.8 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.19	
			4 MHz	0.36	
			8 MHz	0.75	
			18 MHz	1.59	
			36 MHz	3.25	
		V_{DD} = 1.8 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.23	
			4 MHz	0.45	
			8 MHz	0.94	
			18 MHz	1.97	
			36 MHz	3.62	
		V_{DD} = 1.8 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.28	
			4 MHz	0.55	
			8 MHz	1.15	
			18 MHz	2.42	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and V_{DD} = 1.8 V, V_{DDA} = 3.3 V.

Table 32. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	11.3	µA/MHz
DMA1	6.7	
CRC	2.0	
GPIOA	8.5	
GPIOB	8.3	
GPIOC	8.6	
GPIOD	1.5	
GPIOF	1.0	
TSC	4.7	
ADC1	15.9	
APB2-Bridge (3)	2.7	
SYSCFG	3.2	
TIM1	27.6	
USART1	21.0	
TIM15	14.3	
TIM16	10.1	
TIM17	10.4	
APB1-Bridge (3)	5.8	
TIM2	40.7	
TIM6	7.4	
WWDG	4.6	
SPI2	35.2	
SPI3	34.2	
USART2	13.9	
USART3	13.1	
I2C1	9.4	
I2C2	9.4	
PWR	4.5	
DAC	8.3	
I2C3	10.5	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU or DMA1).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.5 Wakeup time from low-power mode

The wakeup times given in *Table 33* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 33. Low-power mode wakeup timings

Symbol	Parameter	Typ @ V_{DD} = 1.8 V, V_{DDA} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	3.9	4.5	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	6.0	-	CPU clock cycles
t_{WUPOR}	Wakeup from Power Off mode	72.8	103	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

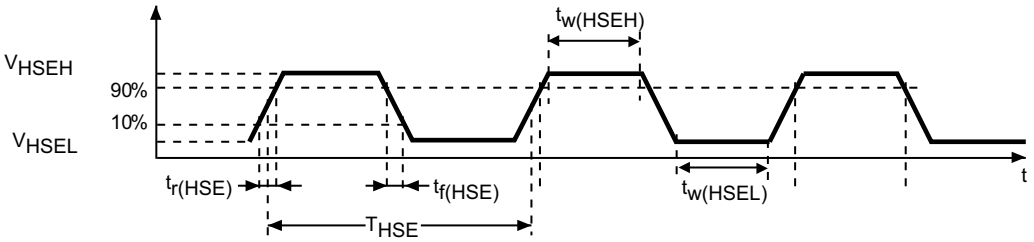
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 34. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

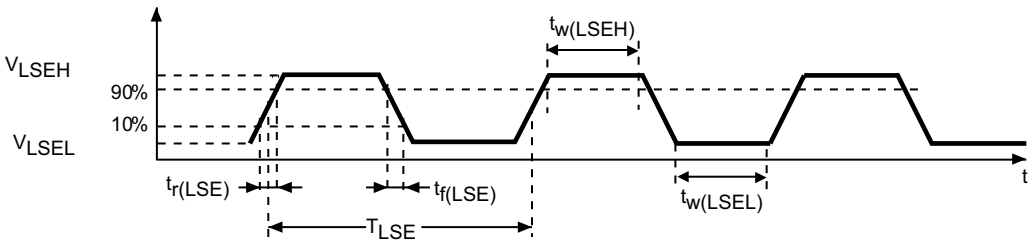
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 13*

Table 35. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 13. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 36*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 36. HSE oscillator characteristics

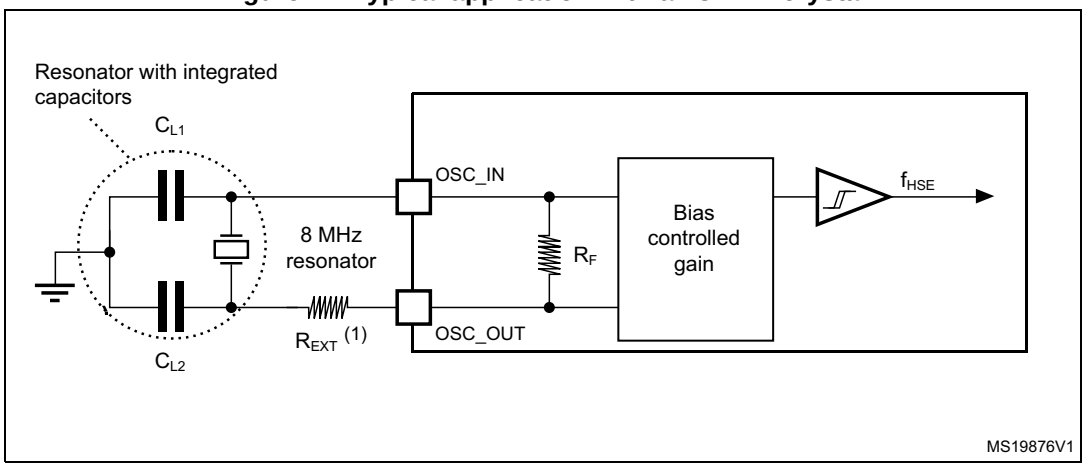
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}=3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL= 5 pF@32 MHz	-	0.8	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

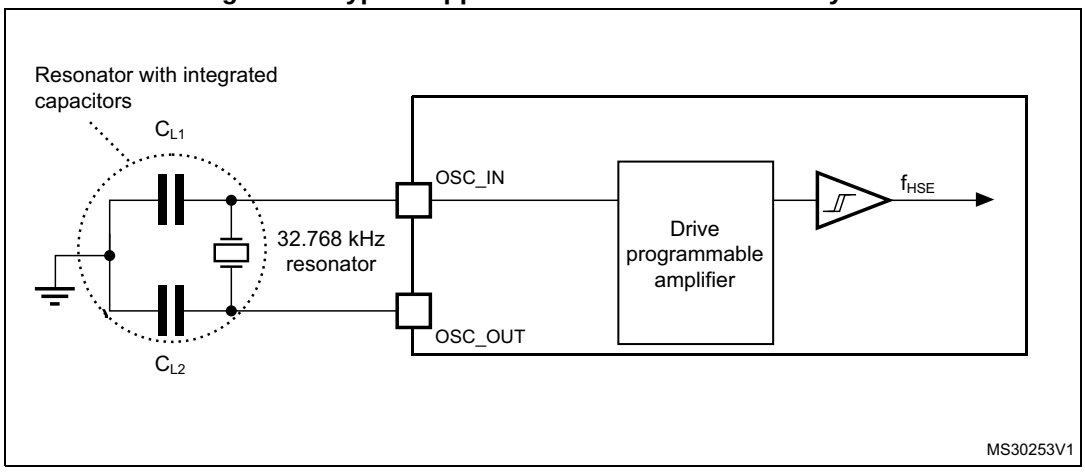
Table 37. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=01 medium low driving capability	-	-	1	
		LSEDRV[1:0]=10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=01 medium low driving capability	8	-	-	
		LSEDRV[1:0]=10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20*.

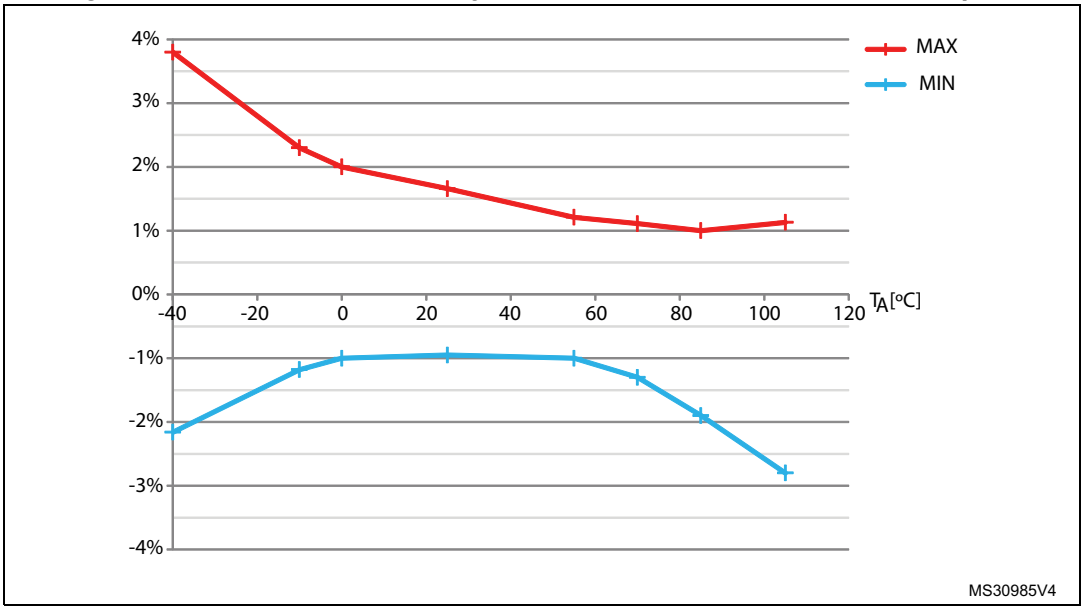
High-speed internal (HSI) RC oscillator

Table 38. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 16. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 39. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.8 PLL characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 40. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 41. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 1.8 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 1.8 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 1.8 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	10	
			130 MHz to 1GHz	25	
			SAE EMI Level	4	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	WLCSP49	C3	250	V
			UFQFPN32	C4	500	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	2 level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 47*

Table 47. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PC0 pin (TTa pin)	-0	+5	
	Injected current PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA6, PA7, PC4, PB0, PB10, PB11, PB13 with induced leakage current on other pins from this group less than -100 µA or more than +100 µA	-5	+5	
	Injected current on any other TT, FT, FTf and NPOR pins	-5	NA	
	Injected current on all other TC, TTa and RESET pins	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant.

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TTa and TT I/O	-	-	0.3 V_{DD} + 0.07 (1)	V
		FT and FTf I/O	-	-	0.475 V_{DD} -0.2 (1)	
		NPOR I/O input low-level voltage	-	-	0.475 V_{DDA} -0.2	
		BOOT0 I/O	-	-	0.3 V_{DD} – 0.3 (1)	
		All I/Os except BOOT0	-	-	0.3 V_{DD} (2)	
V_{IH}	High level input voltage	TTa and TT I/O	0.445 V_{DD}+0.398 (1)	-	-	V
		FT and FTf I/O	0.5 V_{DD}+0.2 (1)	-	-	
		NPOR I/O input high-level voltage	0.5 V_{DDA}+0.2	-	-	
		BOOT0	0.2 V_{DD}+0.95 (1)	-	-	
		All I/Os except BOOT0	0.7 V_{DD} (2)	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 (1)	-	mV
		FT, FTf I/O and NPOR pin	-	100 (1)	-	
		BOOT0	-	300 (1)	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
		POR $V_{DDA} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ

Table 48. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation
2. Tested in production.
3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 47: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 17* and *Figure 18* for standard I/Os.

Figure 17. TC and TTa I/O input characteristics

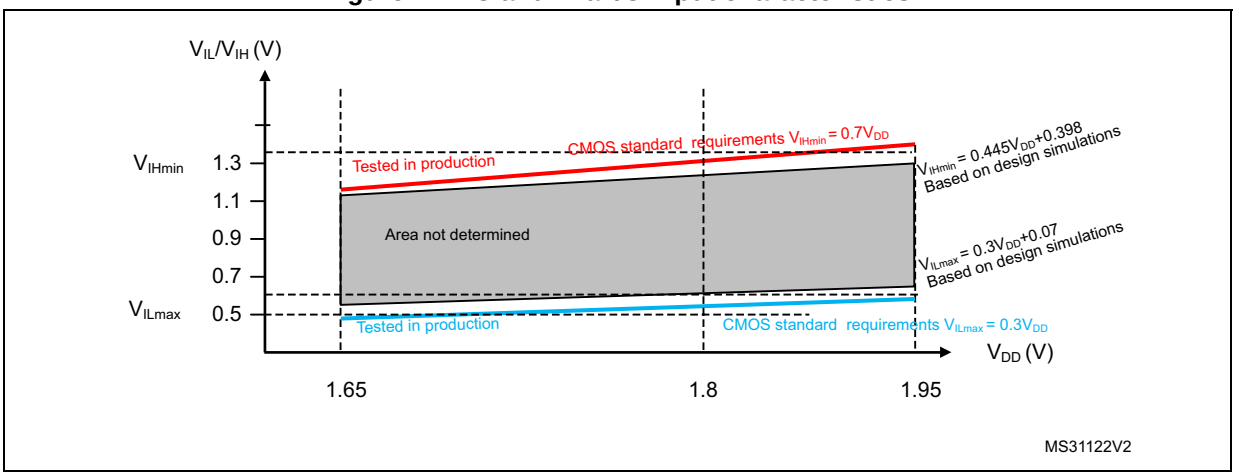
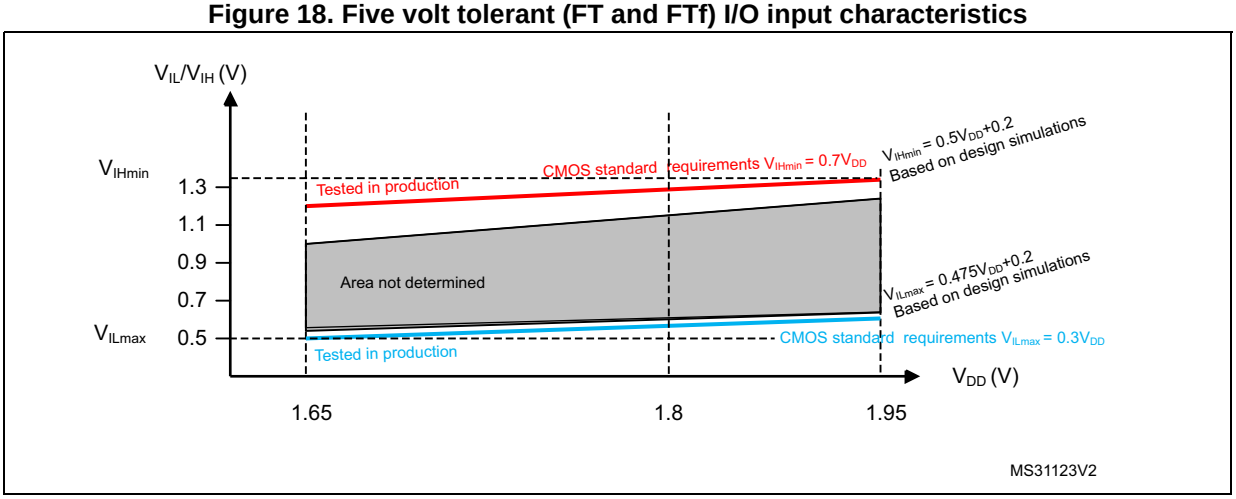


Figure 18. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 49. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V < V_{DD} < 1.95 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin	I_{IO} = -4 mA 1.65 V < V_{DD} < 1.95 V	V_{DD}–0.4	-	
V_{OLFM+}(1)(3)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +10 mA V_{DD} = 1.65 V to 1.95 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 18* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 18* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
3. Guaranteed by design, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 50*, respectively.

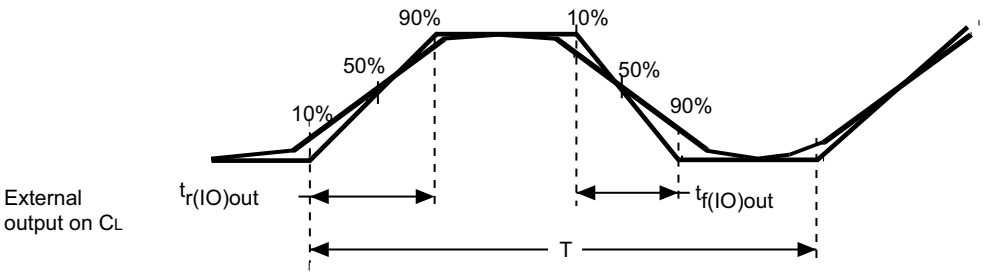
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 50. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	1	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	4(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	62.5(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	0.5(3)(4)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	16(4)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	44(3)(4)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-‘	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0366 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 19*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F318C8 STM32F318K8 reference manual RM0366 for a description of FM+ I/O mode configuration.

Figure 19. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by C_L (see note 1).

MS34942V1

1. See *Table 50: I/O AC characteristics*.

6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 48*).

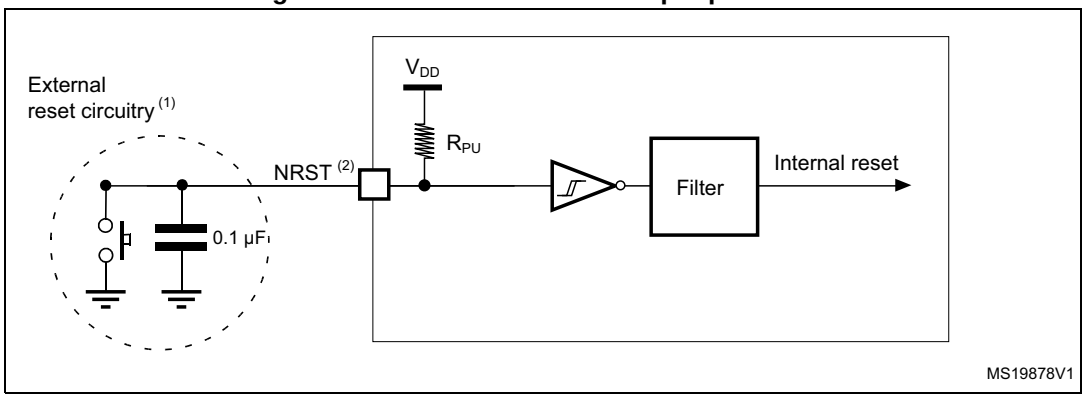
Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}+0.07$(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}+0.398$(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	700(1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 51*. Otherwise the reset will not be taken into account by the device.

6.3.15 NPOR pin characteristics

The NPOR pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, Rpu (see *Table 52*) connected to V_{DDA} supply.

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature and V_{DDA} supply voltage conditions summarized in *Table 20*.

Table 52. NPOR pin characteristics

Symbol(1)	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$	NPOR Input low level voltage	-	-	-	0.475 V_{DDA} - 0.2	V
$V_{IH(NPOR)}$	NPOR Input low level voltage	-	0.5 V_{DDA} +0.2	-	-	
$V_{hys(NPOR)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.16 Timer characteristics

The parameters given in *Table 53* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 53. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIMxCLK}$ = 144 MHz, x = 1, 15,16, 17	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIMxCLK}$ = 144 MHz, x= 1/15/16/17	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIMxCLK}$ = 144 MHz, x= 1/15/16/17	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Table 54. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 55. WWDG min-max timeout value @72 MHz (PCLK)(1)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.17 Communications interfaces

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 56. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 57* for SPI or in *Table 58* for I^{2}S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^{2}S).

Table 57. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	18	MHz
		Slave mode	-	-	18	
		Slave mode transmitter/full duplex	-	-	13(2)	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	0	-	-	
		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	2.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	8	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	14	
$t_{v(SO)}$	Data output valid time	Slave mode	-	23	38	
$t_{v(MO)}$		Master mode	-	1.5	4	
$t_{h(SO)}$	Data output hold time	Slave mode	9.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.
2. 2.Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

Figure 21. SPI timing diagram - slave mode and CPHA = 0

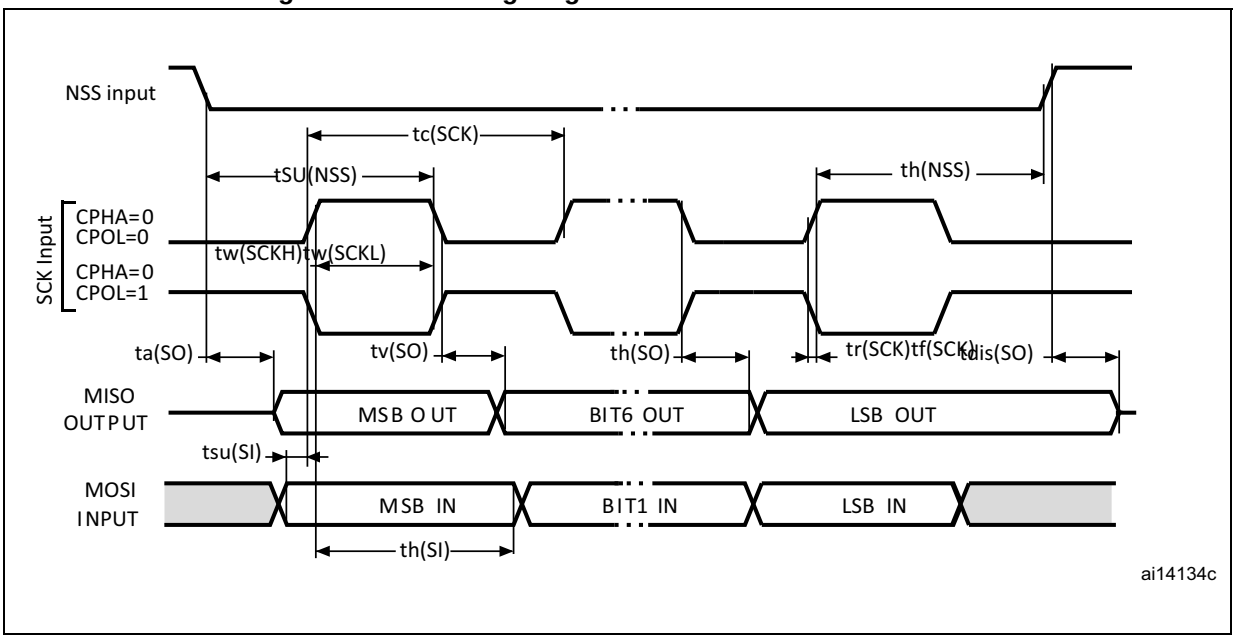
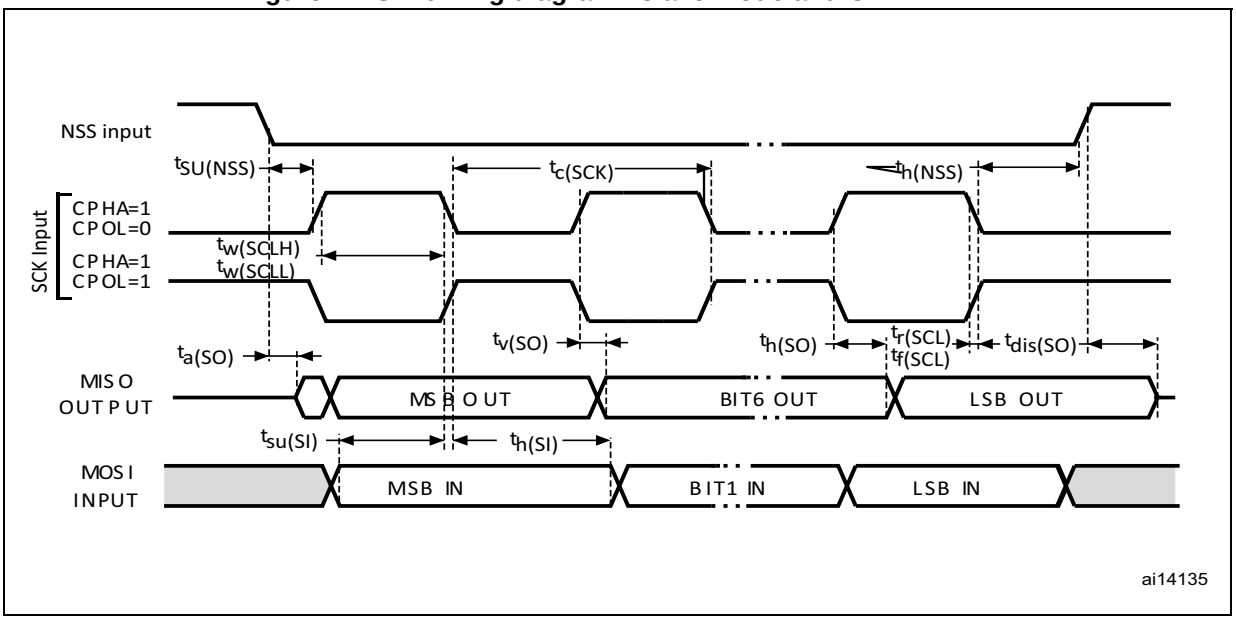
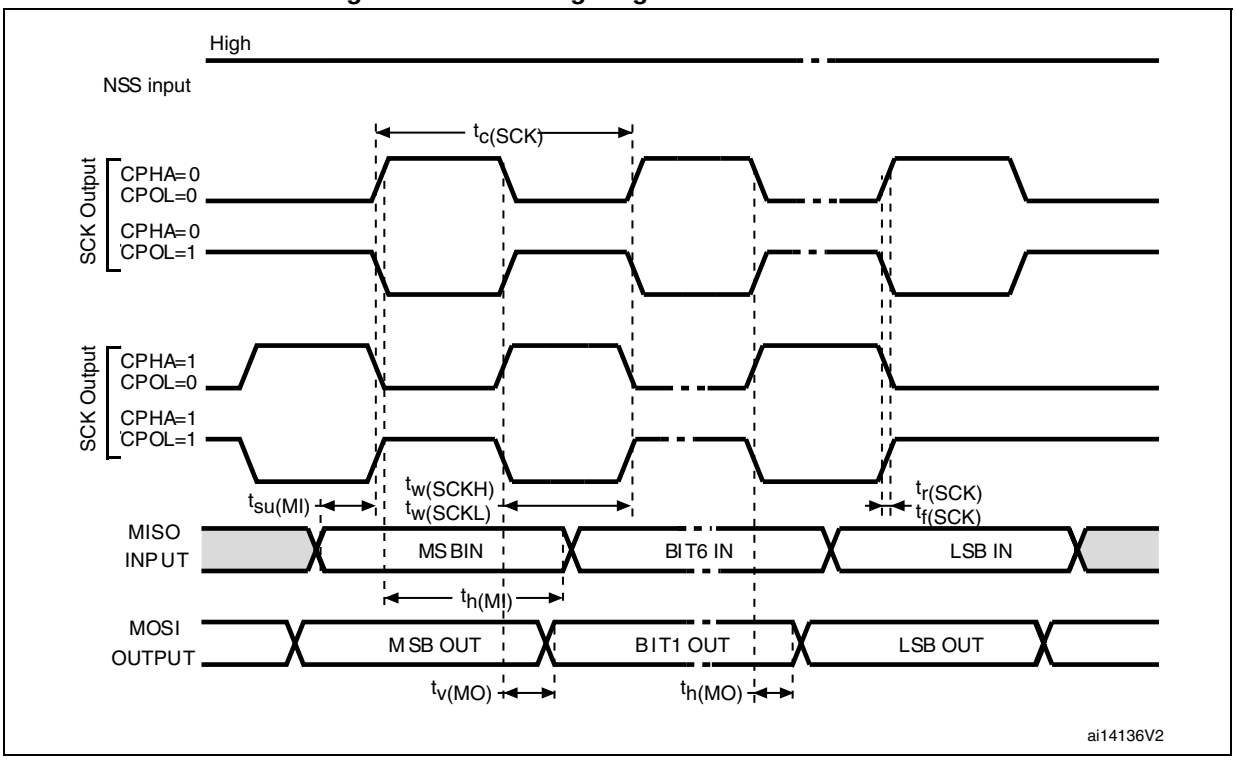


Figure 22. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 23. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 58. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%

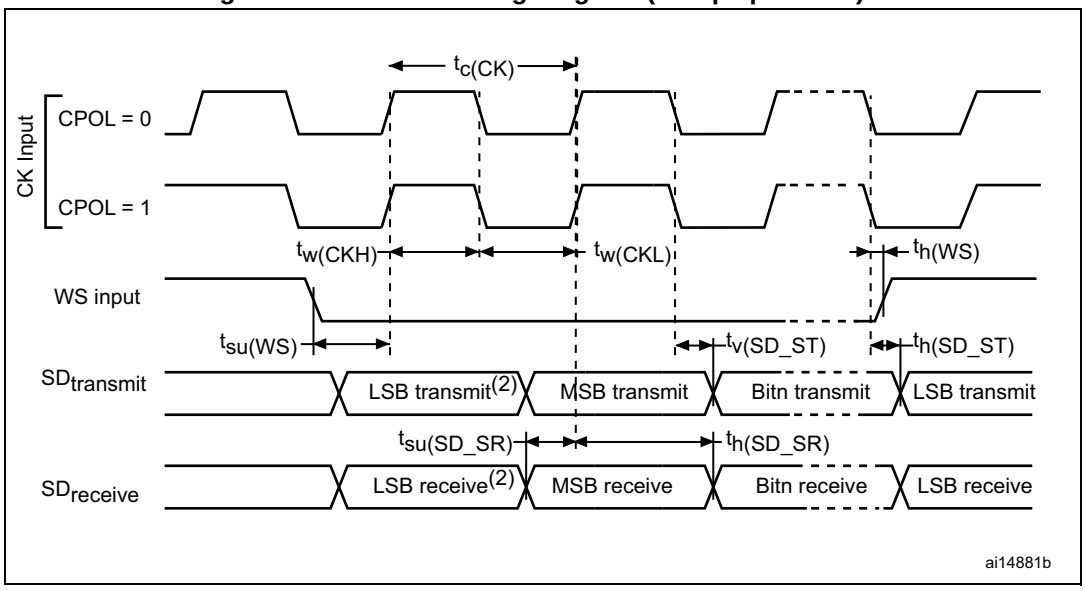
Table 58. I2S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	20	ns
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	0	-	
$t_{h(WS)}$	WS hold time	Slave mode	4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	8	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	50	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	22	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1	-	

1. Data based on characterization results, not tested in production.
2. 256xFs maximum is 36 MHz (APB1 Maximum frequency)

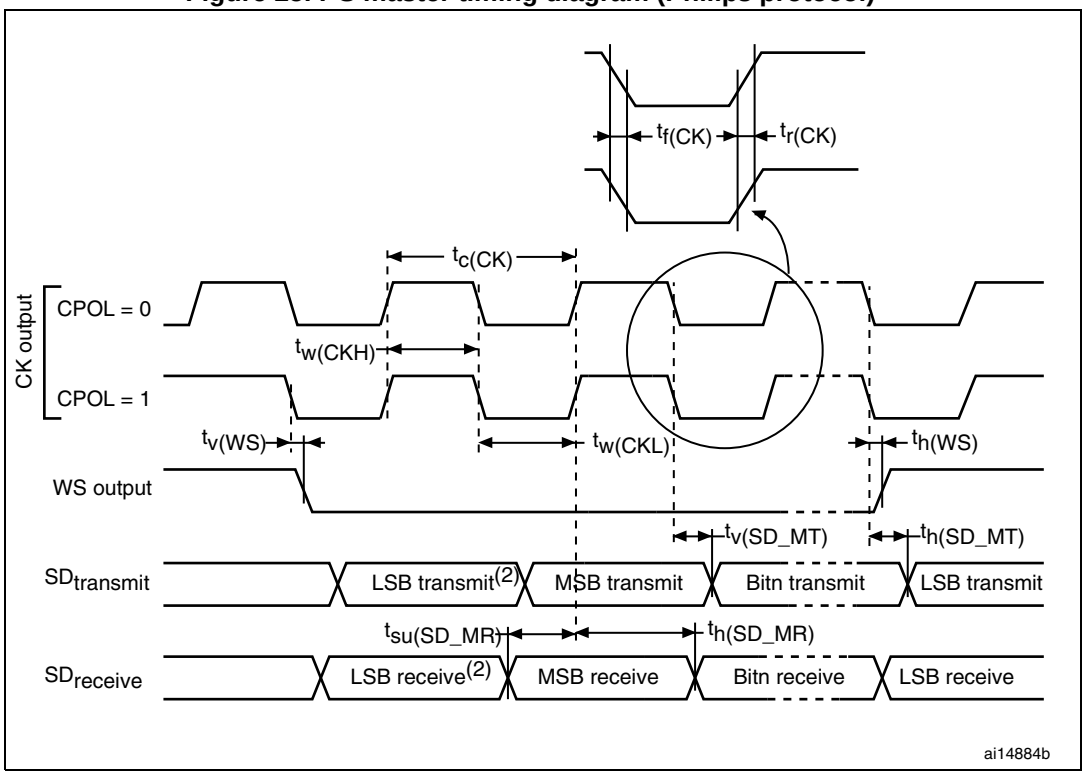
*Note: Refer to RM0366 Reference Manual I2S Section for more details about the sampling frequency (Fs), fMCK, fCK, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max (I2SDIV+ODD)/(2*I2SDIV+ODD) and Fs max supported for each mode/condition.*

Figure 24. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 25. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 59* to *Table 61* are guaranteed by design, with conditions summarized in *Table 20*.

Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	1.8	-	3.6	V
I_{DDA}	ADC current consumption (see *Figure 26*)	Single-ended mode, 5 MSPS	-	1011.3	1172.0	µA
		Single-ended mode, 1 MSPS	-	214.7	322.3	
		Single-ended mode, 200 KSPS	-	54.7	81.1	
		Differential mode, 5 MSPS	-	1061.5	1243.6	
		Differential mode, 1 MSPS	-	246.6	337.6	
		Differential mode, 200 KSPS	-	56.4	83.0	
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$

Table 59. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	$1/f_{ADC}$
TADCVREG_STUP(1)	ADC Voltage Regulator Start-up time	-	-	-	10	µs
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

1. Data guaranteed by design.

Figure 26 illustrates the ADC current consumption as per the clock frequency in single-ended and differential modes.

Figure 26. ADC typical current consumption in single-ended and differential modes

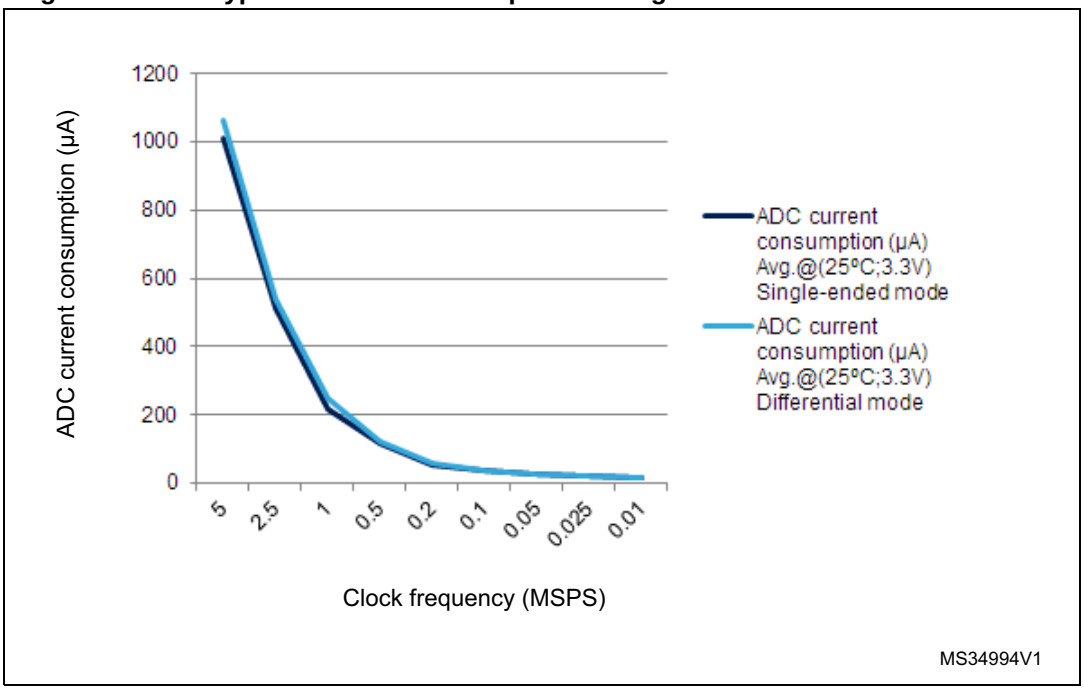


Table 60. Maximum ADC R_{AIN} (1)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channel on PA6.

3. Channel available on PA6.

Table 61. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V_{DDA} = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±4	±4.5	LSB
				Slow channel 4.8 Ms	-	±5.5	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±2	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±5	±5.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±2	±3	
			Differential	Fast channel 5.1 Ms	-	±1.5	±1.5	
				Slow channel 4.8 Ms	-	±1.5	±2	
ENOB (4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.8	10.8	-	bit
				Slow channel 4.8 Ms	10.8	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.2	11.3	-	
SINAD (4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 61. ADC accuracy - limited test conditions(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a –0.5dB Full Scale 50kHz sine wave input signal.

Table 62. ADC accuracy (1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 1.8 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	

Table 62. ADC accuracy (1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 1.8 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a –0.5dB Full Scale 50kHz sine wave input signal.

Table 63. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.13: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 27. ADC accuracy characteristics

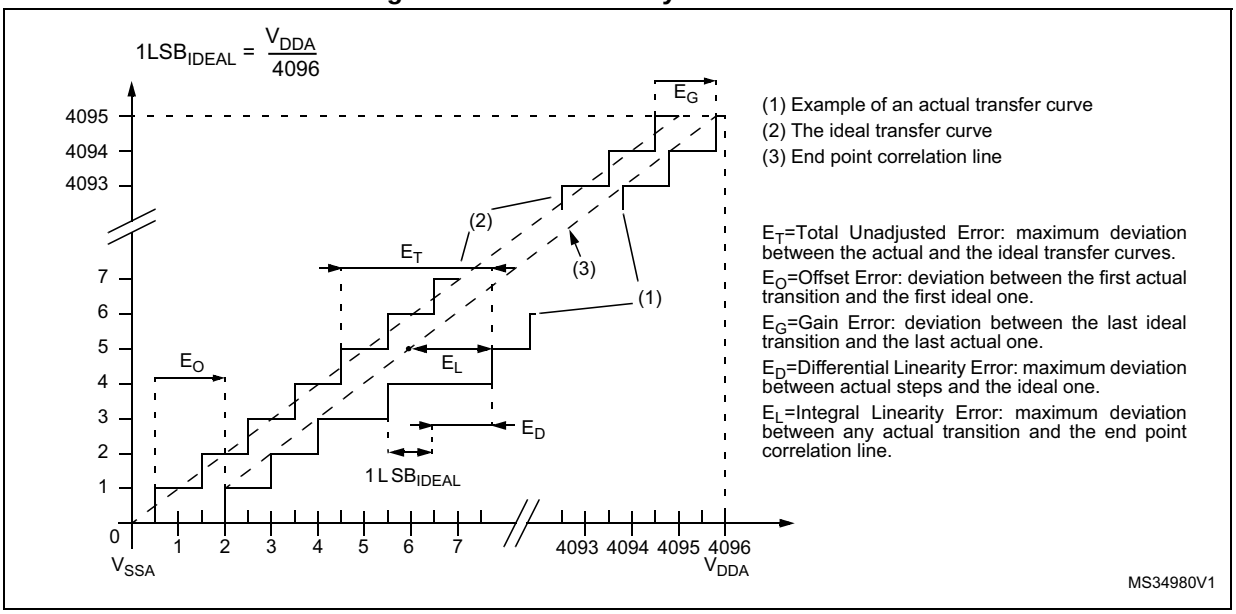
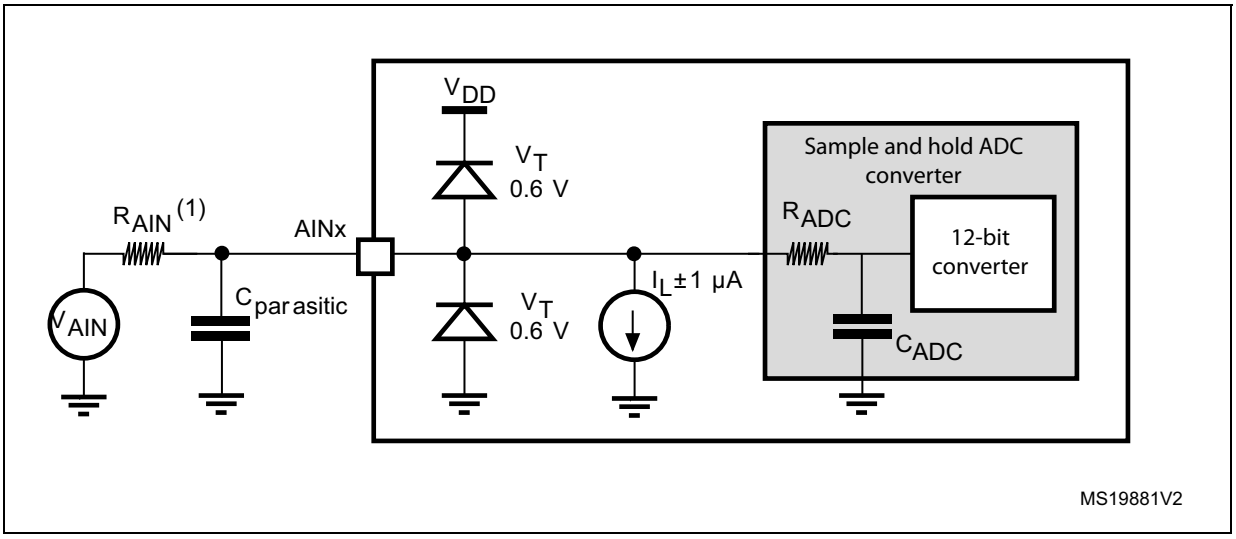


Figure 28. Typical connection diagram using the ADC



1. Refer to *Table 59* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.19 DAC electrical specifications

Table 64. DAC characteristics

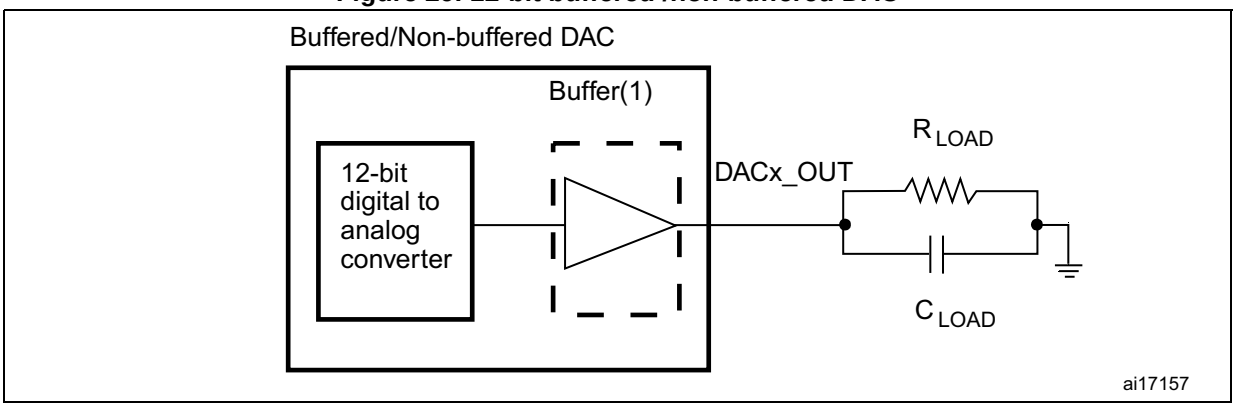
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	DAC output buffer ON	2.4	-	3.6	V
R_{LOAD} (1)	Resistive load	DAC output buffer ON	5	-	-	kΩ
R_O (1)	Output impedance	DAC output buffer ON	-	-	15	kΩ
C_{LOAD} (1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT} (1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	-	0.5	V_{DDA} - 1LSB	mV
I_{DDA} (3)	DAC DC current consumption in quiescent mode (2)	With no load, middle code (0x800) on the input.	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA
DNL (3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	±0.5	LSB
		Given for a 12-bit input code	-	-	±2	LSB
INL (3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset (3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V	-	-	±12	LSB
Gain error (3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$ (3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ	-	3	4	µs
Update rate (3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ	-	-	1	MS/s

Table 64. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	$C_{LOAD} = 50$ pF, No $R_{LOAD} \geq 5$ kΩ,	-	–67	–40	dB

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 29. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.20 Comparator characteristics

Table 65. Comparator characteristics(1)

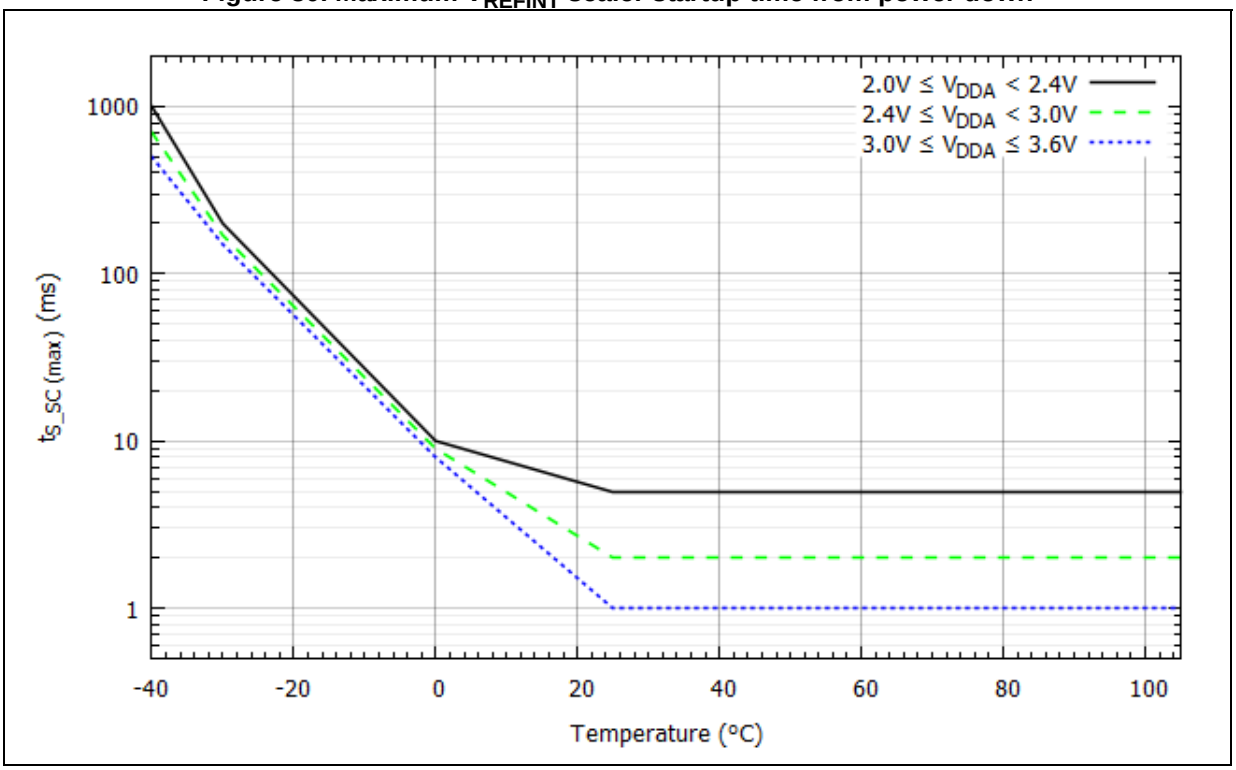
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	V_{REFINT} scaler not in use	1.8	-	3.6	V
		V_{REFINT} scaler in use	2	-	3.6	
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	V
V_{BG}	Scaler input voltage	-	-	$V_{REFINIT}$	-	
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	V_{REFINT} scaler activation after device power on	-	-	1(2)	s
		Next activations	-	-	0.2	ms
t_{START}	Comparator startup time	$V_{DDA} \geq 2.7$ V	-	-	4	µs
		$V_{DDA} < 2.7$ V	-	-	10	

Table 65. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_D	Propagation delay for 200 mV step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	25	28	ns
		$V_{DDA} < 2.7$ V	-	28	30	
	Propagation delay for full range step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	32	35	
		$V_{DDA} < 2.7$ V	-	35	40	
V_{OFFSET}	Comparator offset error	$V_{DDA} \geq 2.7$ V	-	±5	±10	mV
		$V_{DDA} < 2.7$ V	-	-	±25	
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
$I_{DD(COMP)}$	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.
2. For more details and conditions, see *Figure 30: Maximum VREFINT scaler startup time from power down*.

Figure 30. Maximum V_{REFINT} scaler startup time from power down



6.3.21 Operational amplifier characteristics

Table 66. Operational amplifier characteristics(1)

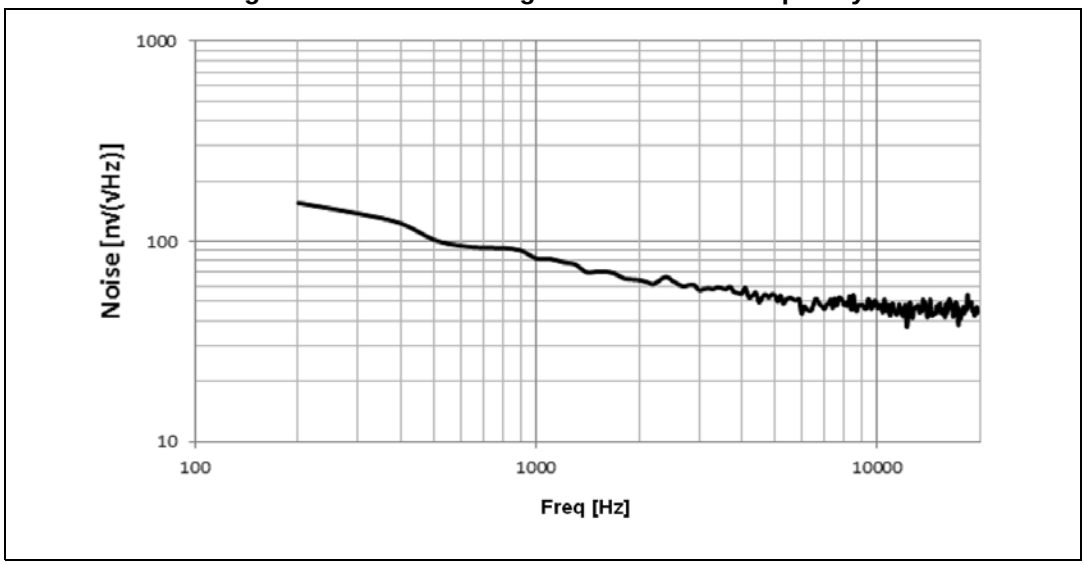
Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage		R_{load} = min, Input at V_{DDA}.	-	-	100	mV
			R_{load} = 20K, Input at V_{DDA}.	-	-	20	
VOL_{SAT}	Low saturation voltage		Rload = min, input at 0V	-	-	100	
			Rload = 20K, input at 0V.	-	-	20	
φm	Phase margin		-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.		$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ, Follower configuration	-	2.8	5	µs
$t_{S\_OPAM\_VOUT}$	ADC sampling time when reading the OPAMP output			400	-	-	ns

Table 66. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	
			-	8	-	
			-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode (2)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	%
I_{bias}	OPAMP input bias current	-	-	-	±0.2(3)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.
2. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
3. Mostly TTa I/O leakage, when used in analog mode.

Figure 31. OPAMP Voltage Noise versus Frequency



6.3.22 Temperature sensor characteristics

Table 67. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 68. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

6.3.23 V_{BAT} monitoring characteristics

Table 69. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

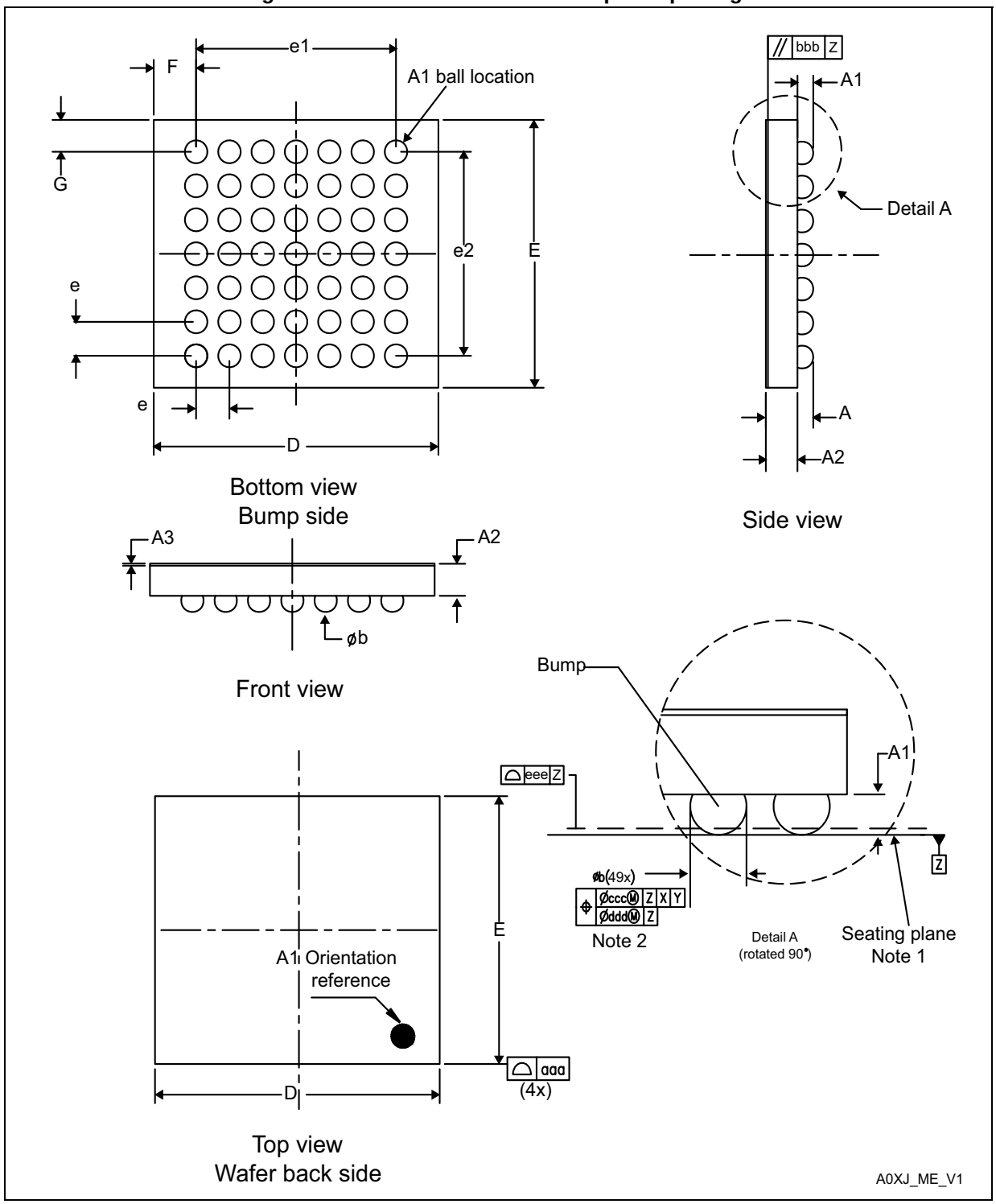
1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 32. WLCSP49 wafer level chip size package



1. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
2. Bump position designation per JESD 95-1, SPP-010.

Table 70. WLCSP49 wafer level chip size package mechanical data(1)

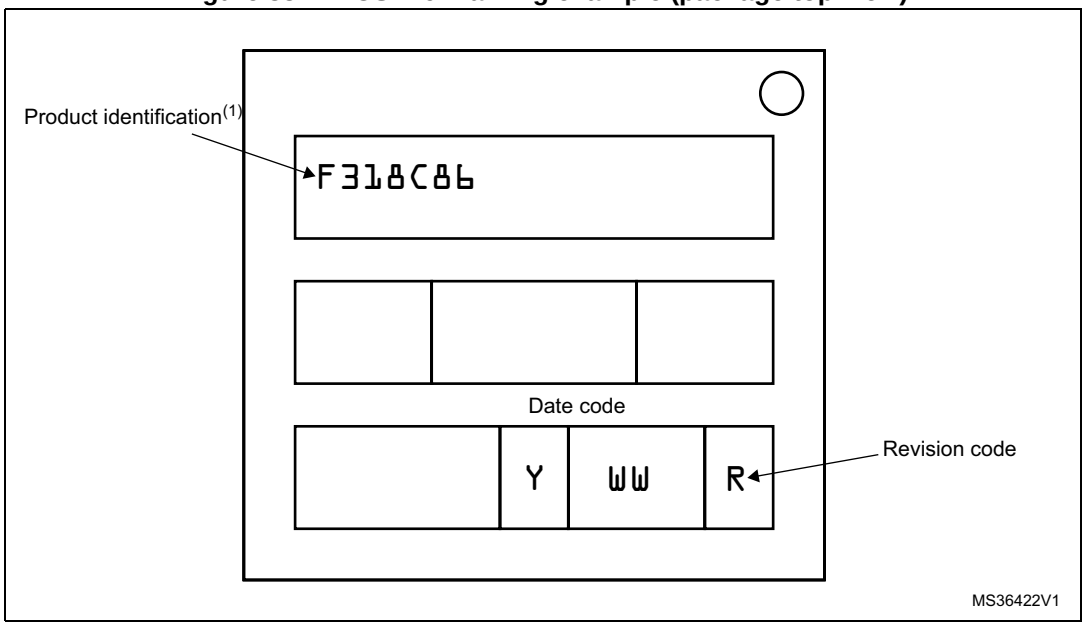
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(2)	-	0.025	-	-	0.0010	-
b(3)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.382	3.417	3.452	0.1331	0.1345	0.1359
E	3.116	3.151	3.186	0.1227	0.1241	0.1254
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.508	-	-	0.200	-
G	-	0.375	-	-	0.148	-
aaa	-	0.100	-	-	1.9291	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-
N	Number of pins					
	49					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Device marking

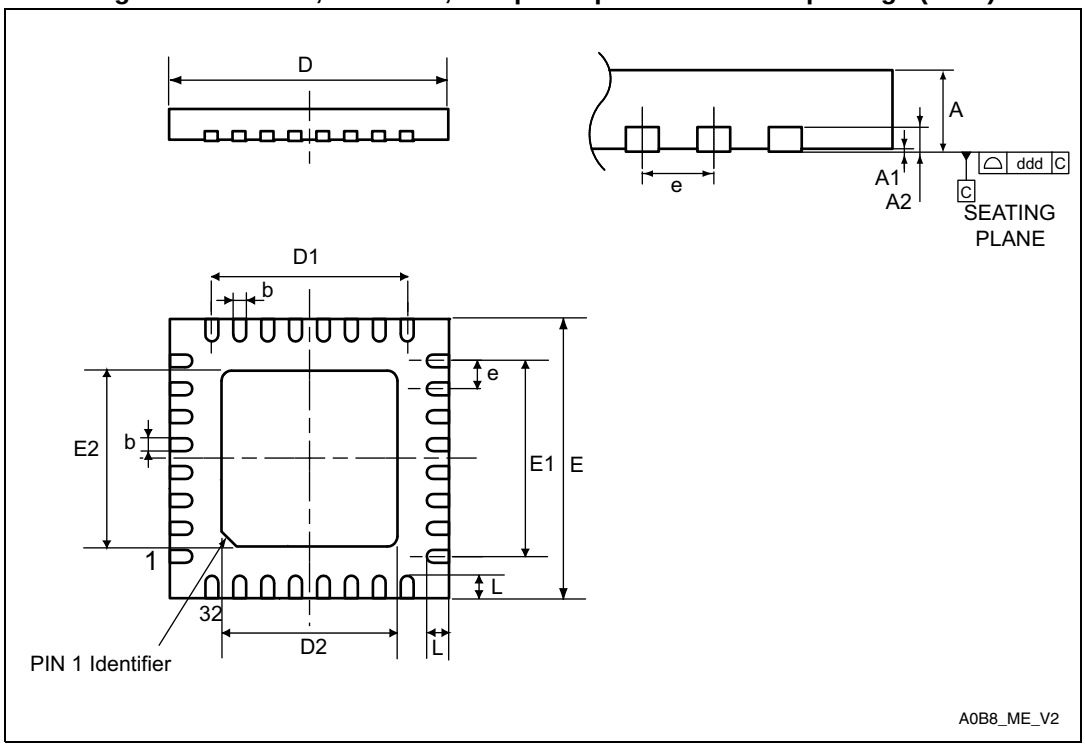
The following figure shows the marking for the WLCSP49 package.

Figure 33. WLCSP49 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 34. 32-lead, ultra thin, fine pitch quad flat no-lead package (5 x 5)



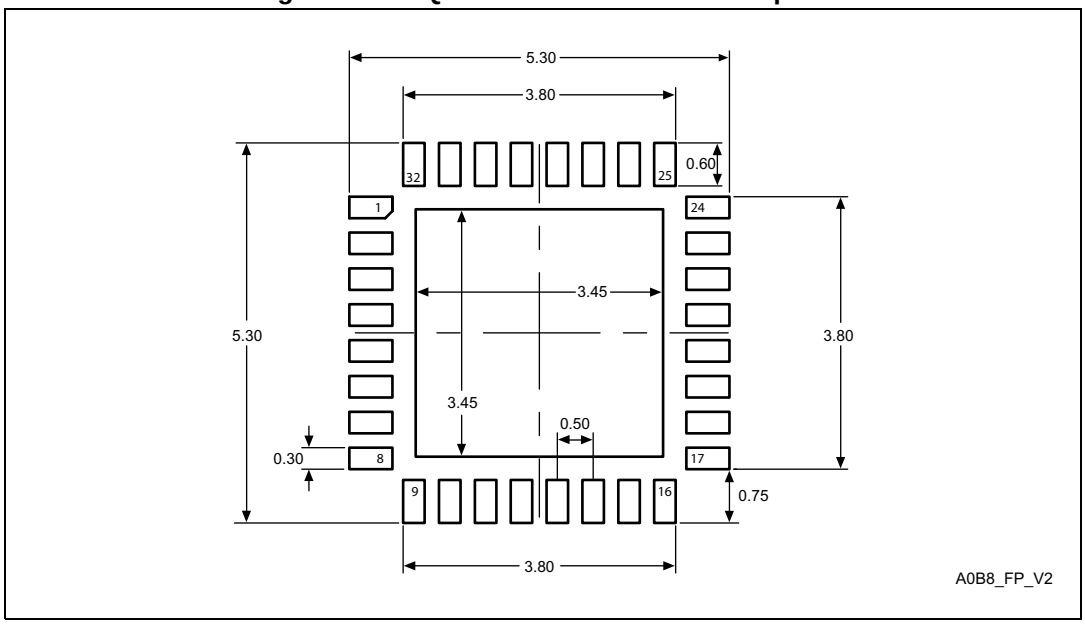
1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the UFQFPN package. This pad is not internally connected to the VSS or VDD power pads. It is recommended to connect it to VSS.
3. All leads/pads should also be soldered to the PCB to improve the lead solder joint life.

Table 71. 32-lead, ultra thin, fine pitch quad flat no-lead package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.500	0.600	0.0217	0.0197	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
A3	0.200	-	-	0.0079	-	-
b	0.250	0.180	0.300	0.0098	0.0071	0.0118
D	5.000	4.850	5.150	0.1969	0.1909	0.2028
D2	3.450	3.200	3.700	0.1358	0.1260	0.1457
E	5.000	4.850	5.150	0.1969	0.1909	0.2028
E2	3.450	3.200	3.700	0.1358	0.1260	0.1457
e	0.500	-	-	0.0197	-	-
L	0.400	0.300	0.500	0.0157	0.0118	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. UFQFPN32 recommended footprint

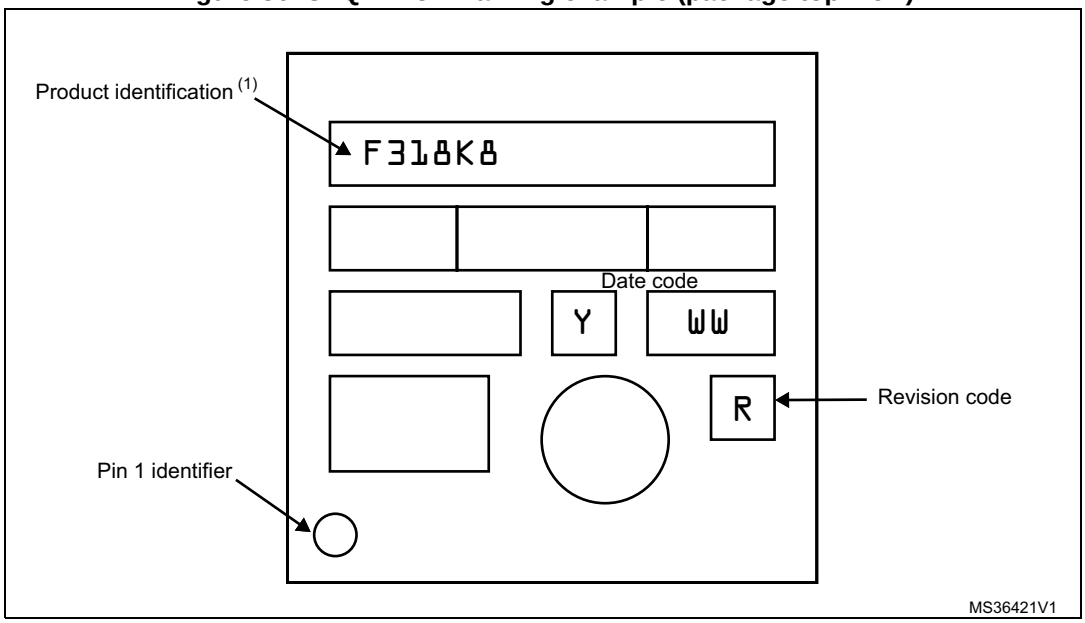


1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking

The following figure shows the marking for the UFQFPN32 package.

Figure 36. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 20: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 72. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** WCSP49 - 3.4 x 3.4 mm	49	°C/W
	Thermal resistance junction-ambient UFQPFN32 - 5 x 5 mm	37	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F318C8 STM32F318K8 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 175 + 61.6 = 236.6 mW

Thus: P_{Dmax} = 236.6 mW

Using the values obtained in *Table 72* T_{Jmax} is calculated as follows:

– For WLCSP49, 49°C/W

T_{Jmax} = 82 °C + (49°C/W x 236.6 mW) = 82°C + 11.6°C = 93.6°C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 70 + 28.8 = 98.8 mW

Thus: P_{Dmax} = 98.8 mW

Using the values obtained in *Table 72* T_{Jmax} is calculated as follows:

– For WLCSP49, 49°C/W

T_{Jmax} = 115 °C + (49°C/W x 98.8 mW) = 115°C + 4.8°C = 119.8°C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

8 Part numbering

Table 73. Ordering information scheme

Example: STM32 F 318 K 8 T 6 xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

318 = STM32F318xx, 1.65 to 1.94 V operating voltage

Pin count

K = 32 pins

C = 49 pins

Flash memory size

8 = 64 Kbytes of Flash memory

Package

Y= WLCSP

U= UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

9 Revision history

Table 74. Document revision history

Date	Revision	Changes
27-May-2014	1	Initial release.
10-Jun-2014	2	Added the number of comparators in the document title. Updated the position of VSSA/VREF- pin in WLCSP49 package in *Table 12: STM32F318x8 pin definitions*. Added the maximum value for wake up time from stop mode in *Table 33: Low-power mode wakeup timings*.
02-Dec-2014	3	Applied the following changes: – updated the comparator analog supply range in *Features*, – added “Interconnect matrix” in *Features*, – added some information related to timers in *Table 1: STM32F318x8 device features and peripheral counts* – updated *Section 3.5.1: Power supply schemes* and added *Table 2: External analog supply values for analog peripherals*, – added the last footnote to *Table 12: STM32F318x8 pin definitions*, – updated *Table 38: HSI oscillator characteristics* and *Figure 16: HSI oscillator accuracy characterization results for soldered parts*, – updated V_{DDA} min value in *Table 65: Comparator characteristics*, – updated *Table 27: Typical and maximum VDDA consumption in Stop mode*, – updated *Table 33: Low-power mode wakeup timings*, – updated UFQFPN32 and WLCSP49 marking in *Chapter 7: Package characteristics*.
09-Feb-2015	4	Updated: – the order of columns in *Table 25: Typical and maximum current consumption from the VDDA supply*, – *Table 36: HSE oscillator characteristics*, – *Table 41: Flash memory characteristics*, – *Table 52: NPOR pin characteristics*, – *Table 65: Comparator characteristics*. Added: – *Figure 30: Maximum VREFINT scaler startup time from power down*.