



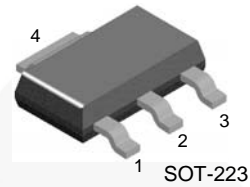
November 2014

# BSP52

## NPN Darlington Transistor

### Description

This device is designed for applications requiring extremely high-current gain at collector currents to 500 mA. Sourced from process 03.



1. Base 2,4. Collector 3. Emitter

### Ordering Information

Part Number	Marking	Package	Packing Method
BSP52	BSP52	SOT-223 4L	Tape and Reel

### Absolute Maximum Ratings<sup>(1),(2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-Emitter Voltage	80	V
$V_{CBO}$	Collector-Base Voltage	90	V
$V_{EBO}$	Emitter-Base Voltage	5	V
$I_C$	Collector Current - Continuous	800	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Notes:

1. These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

**Thermal Characteristics<sup>(3)</sup>**

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Max.	Unit
$P_D$	Total Device Dissipation	1000	mW
	Derate Above $25^\circ\text{C}$	8.0	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	125	$^\circ\text{C}/\text{W}$

**Note:**

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

**Electrical Characteristics**

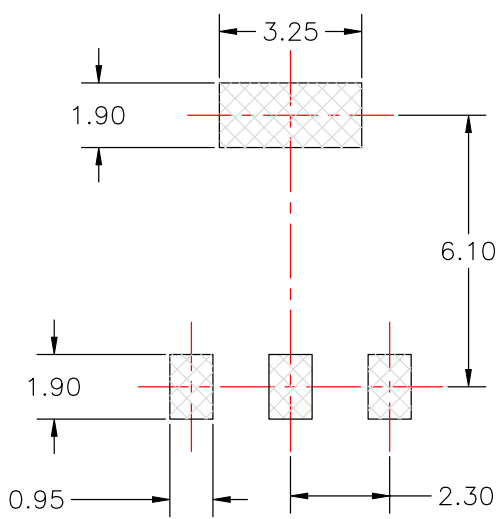
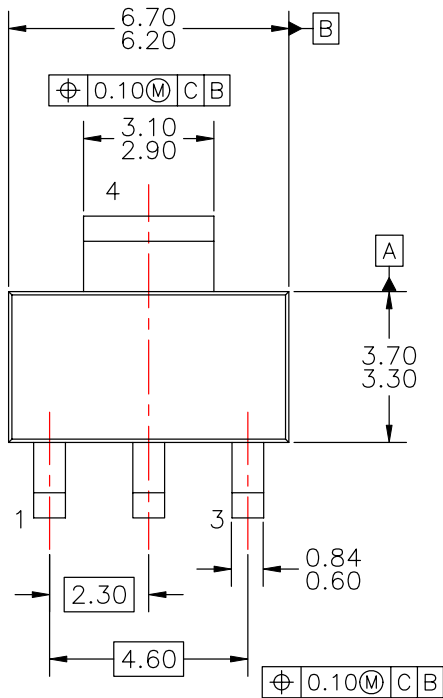
Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100 \mu\text{A}$ , $I_E = 0$	90			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10 \mu\text{A}$ , $I_C = 0$	5			V
$I_{CES}$	Collector Cut-Off Current	$V_{CE} = 80 \text{ V}$ , $V_{BE} = 0$			10	$\mu\text{A}$
$I_{EBO}$	Emitter Cut-Off Current	$V_{EB} = 4.0 \text{ V}$ , $I_C = 0$			10	$\mu\text{A}$
$h_{FE}$	DC Current Gain	$I_C = 150 \text{ mA}$ , $V_{CE} = 10 \text{ V}$	1000			
		$I_C = 500 \text{ mA}$ , $V_{CE} = 10 \text{ V}$	2000			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 500 \text{ mA}$ , $I_B = 0.5 \text{ mA}$			1.3	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 500 \text{ mA}$ , $I_B = 0.5 \text{ mA}$			1.9	V

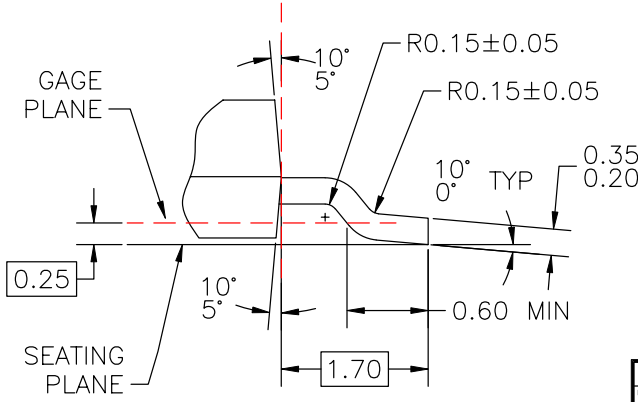
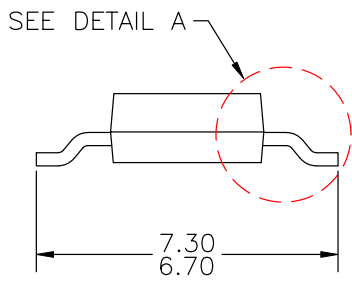
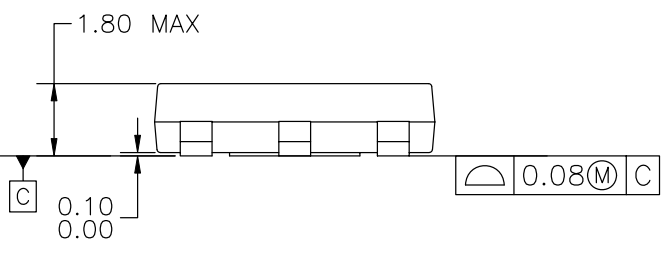
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**APPROVED**  
July-14-2008

REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 <del>±0.03</del> TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.8 <del>±0.05</del> TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 <del>±0.03</del> TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 <del>±0.33</del> TO 3.30; CHG BODY LN FR 6.53 <del>±0.33</del> TO 6.30; CHG TOTAL PKG WID FR 6.94 <del>±0.33</del> TO 7.30; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



LAND PATTERN RECOMMENDATION



DETAIL A  
SCALE: 2:1






- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
  - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - C) ALL DIMENSIONS ARE IN MILLIMETERS.
  - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
  - E) LANDPATTERN NAME: SOT230P700X180-4BN
  - F) DRAWING FILENAME: MKT-MA04AREV2

APPROVALS	DATE	<b>FAIRCHILD</b> SEMICONDUCTOR™
DRN: J.U. COMPARATIVO JR.	26FEB2008	
CHEK: L.Z. STA CRUZ		
APPROV: M.R. GESTOLE		
G.S. BAJE		<b>MOLDED PACKAGE</b> <b>SOT-223, 4 LEAD</b>
PROJECTION 	SCALE: 1:1	SIZE: A3
INCH (MM)	FORMERLY: N/A	DRAWING NUMBER: MKT-MA04A
		REV: 2
		SHEET: 1 OF 1



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I73