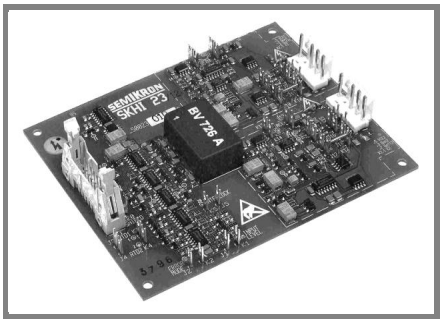
SKHI 23/12 (R) ...



SEMIDRIVER™

Medium Power Double IGBT Driver

SKHI 23/12 (R)

Features

- SKHI 23/12 drives all SEMIKRON IGBTs with V_{CES} up to 1200 V (V_{CE}-monitoring adjusted from factory for 1200 V-IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drivers
- CMOS / TTL (HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / ouput signal (LOW or HIGH logic)
- Driver interlock top / bottom
- Internal isolated power supply

Typical Applications

- High frequency SMPS
- Half and Full bridges
- Three phase motor inverters
- High power UPS

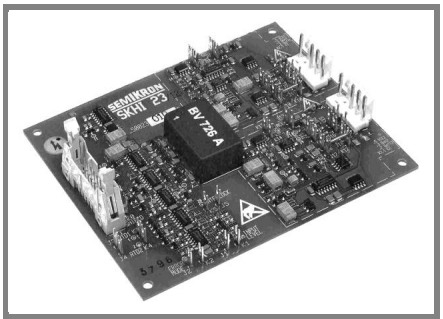
1) This current value is a function of the output load condition
2) Operating fsw = 0 Hz
3) This value does not consider t_{on} of IGBT and t_{MIN} adjusted by R_{CE} and C_{CE}; see also fig. 14
4) Matched to be used with IGBTs < 100 A; for higher currents, see table 4
5) With R_{CE} = 18 kΩ, C_{CE} = 330 pF; see fig. 6
6) Factory adjusted; other values see table 3

Absolute Maximum Ratings T_a = 25 °C, unless otherwise specified

Symbol	Conditions	Values	Units
V_S	Supply voltage primary	18	V
V_{iH}	Input signal voltage (HIGH) (for 15 V and 5 V input level)	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	± 8	A
$Iout_{AV}$	Output average current	± 50	mA
V_{CE}	Collector emitter voltage sense	1200	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
$V_{isol\ IO}$	Isolation test volt. IN-OUT (2 sec. AC)	2500	V
$R_{Gon\ min}$	minimal R_{Gon}	2,7	Ω
$R_{Goff\ min}$	minimal R_{Goff}	2,7	Ω
$Q_{out/pulse}$	charge per pulse	4,8	µC
T_{op}	Operating temperature	- 25 ... + 85	°C
T_{stg}	Storage temperature	- 25 ... + 85	°C

Characteristics T_a = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_S	Supply current (max.)		0,32[1)]		A
I_{SO}[2)]	Supply current primary side (standby)		0,12		A
V_{iT+}	Input threshold voltage (HIGH) min.				
	15 V input level	12,5			V
	for 5 V input level	2,4			V
V_{iT-}	Input threshold voltage (LOW) max.				
	for 15 V input level			3,6	V
	for 5 V input level			0,50	V
$V_{G(on)}$	Turn-on output gate voltage		+ 15		V
$V_{G(off)}$	Turn-off output gate voltage		- 8		V
f	Maximum operating frequency		see fig. 15		
$td(on)_{IO}$	Input-output turn-on propagation time		1,4		µs
$td(off)_{IO}$	Input-output turn-off propagation time		1,4		µs
$t_{d(err)}$	Error input-output propagation time		1,0[3)]		µs
t_{TD}	Dead time		10[6)]		µs
V_{CEstat}	Reference voltage for V_{CE} monitoring		5,2[5)]		V
R_{Gon}	Internal gate resistor for ON signal		22[4)]		Ω
R_{Goff}	Internal gate resistor for OFF signal		22[4)]		Ω
C_{ps}	Primary to secondary capacitance		12		pF



SEMIDRIVER™

Medium Power Double IGBT Driver

SKHI 23/17 (R)

Features

- SKHI 23/17 drives all SEMIKRON IGBTs with V_{CES} up to 1700 V (V_{CE}-monitoring adjusted from factory for 1700 V-IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drivers
- CMOS / TTL (HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / ouput signal (LOW or HIGH logic)
- Driver interlock top / bottom
- Internal isolated power supply

Typical Applications

- High frequency SMPS
- Half and Full bridges
- Three phase motor inverters
- High power UPS

1) This current value is a function of the output load condition
2) Operating fsw = 0 Hz
3) This value does not consider t_{on} of IGBT and t_{MIN} adjusted by R_{CE} and C_{CE}; see also fig. 14
4) Matched to be used with IGBTs < 100 A; for higher currents, see table 4
5) With R_{CE} = 36 kΩ, C_{CE} = 470 pF; see fig. 6
6) Factory adjusted; other values see table 3

Absolute Maximum Ratings T_a = 25 °C, unless otherwise specified

Symbol	Conditions	Values	Units
V_S	Supply voltage primary	18	V
V_{iH}	Input signal voltage (HIGH) (for 15 V and 5 V input level)	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	± 8	A
$Iout_{AV}$	Output average current	± 50	mA
V_{CE}	Collector emitter voltage sense	1700	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
$V_{isol\ IO}$	Isolation test volt. IN-OUT (2 sec. AC)	4000	V
$R_{Gon\ min}$	minimal R_{Gon}	2,7	Ω
$R_{Goff\ min}$	minimal R_{Goff}	2,7	Ω
$Q_{out/pulse}$	charge per pulse	4,8	µC
T_{op}	Operating temperature	- 25 ... + 85	°C
T_{stg}	Storage temperature	- 25 ... + 85	°C

Characteristics T_a = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_S	Supply current (max.)		0,32[1)]		A
I_{SO}[2)]	Supply current primary side (standby)		0,12		A
V_{iT+}	Input threshold voltage (HIGH) min.				
	15 V input level	12,5			V
	for 5 V input level	2,4			V
V_{iT-}	Input threshold voltage (LOW) max.				
	for 15 V input level			3,6	V
	for 5 V input level			0,50	V
$V_{G(on)}$	Turn-on output gate voltage		+ 15		V
$V_{G(off)}$	Turn-off output gate voltage		- 8		V
f	Maximum operating frequency		see fig. 15		
$td(on)_{IO}$	Input-output turn-on propagation time		1,4		µs
$td(off)_{IO}$	Input-output turn-off propagation time		1,4		µs
$t_{d(err)}$	Error input-output propagation time		1,0[3)]		µs
t_{TD}	Dead time		10[6)]		µs
V_{CEstat}	Reference voltage for V_{CE} monitoring		6,3[5)]		V
R_{Gon}	Internal gate resistor for ON signal		22[4)]		Ω
R_{Goff}	Internal gate resistor for OFF signal		22[4)]		Ω
C_{ps}	Primary to secondary capacitance		12		pF

Block diagramm SKHI 23

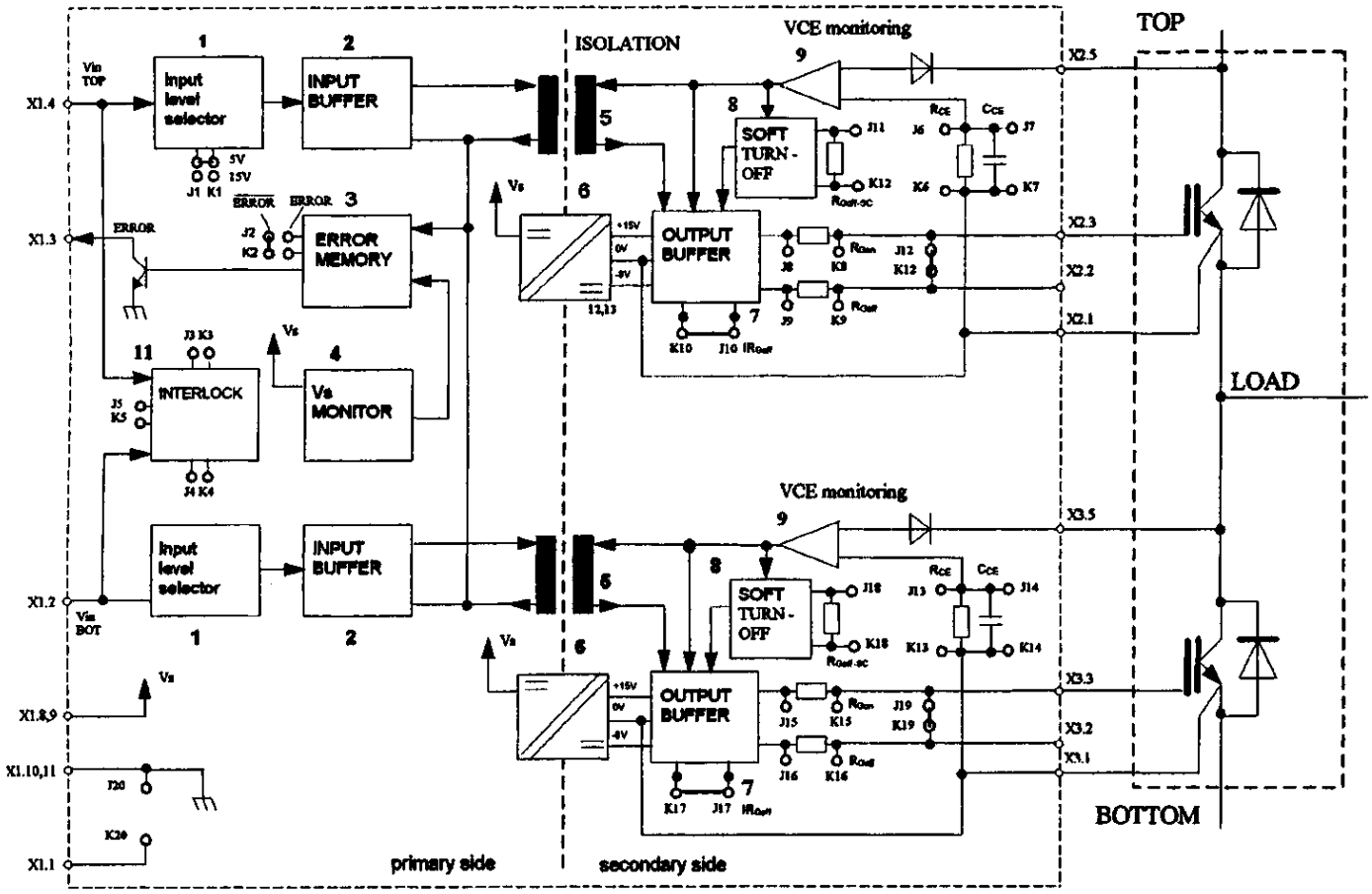
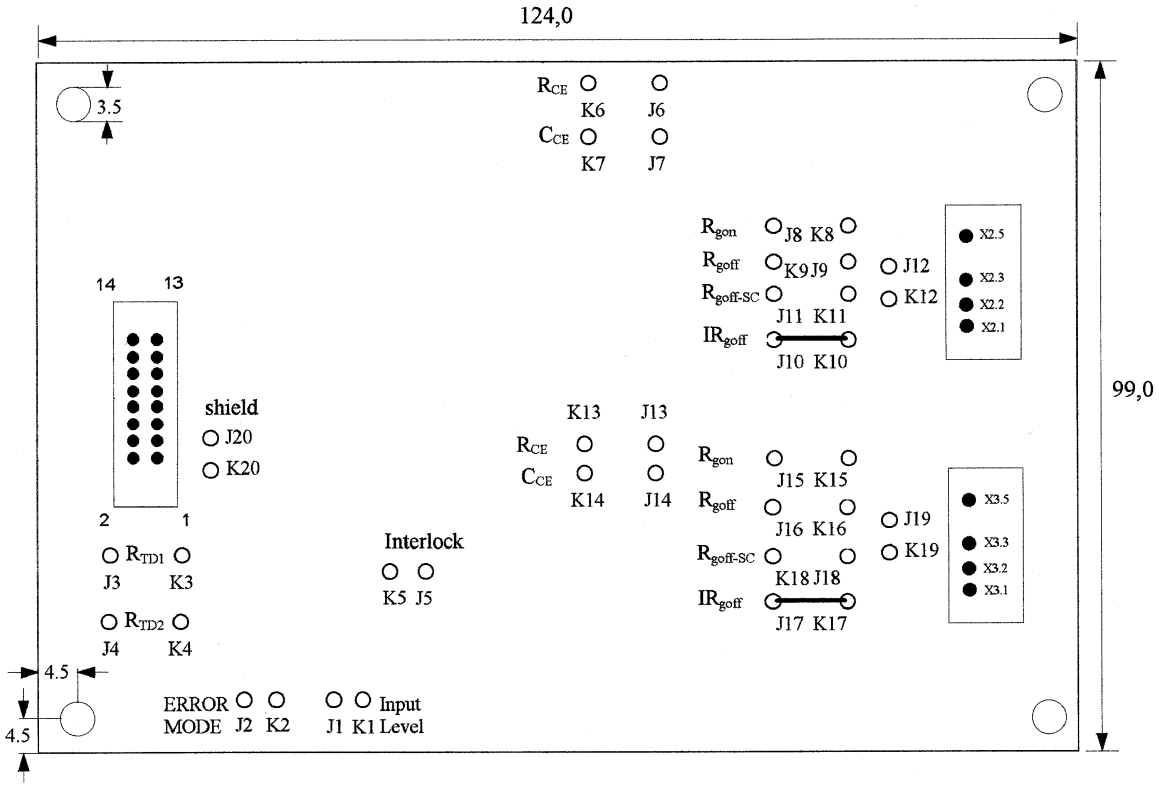


Fig. 1 The numbers refer to the description on page B14 – 45, section B.



Input connector = 14 pin flat cable according to DIN 41651
Output connector = MOLEX 41791 Series (mates with 41695 crimp terminals 7258)

Fig. 2 Dimensions (in mm) and connections of the SKHI 23

SEMIDRIVER™ SKHI 23/12
SEMIDRIVER™ SKHI 23/17

Medium Power Double IGBT Driver

Overview

The new intelligent double IGBT driver, SKHI 23 respectively SKHI 23/17 is a standard driver for all power IGBTs in the market.

SKHI 23/12 drives all IGBTs with V_{CE} up to 1200 V. SKHI 23/17 drives all IGBTs with V_{CE} up to 1700 V. To protect the driver against moisture and dust it is coated with varnish. The adaption of the drivers to the application has been improved by using pins to changing several parameters and functions. The connections to the IGBTs can be made by using only one MOLEX connector with 12 pins or by using 2 separate connectors with 5 pins for each IGBT.

The high power outputs capability was designed to switch high current double or single modules (or paralleled IGBTs). The output buffers have been improved to make it possible to switch up to 200 A IGBT modules at frequencies up to 20 kHz.

A new function has been added to the short circuit protection circuitry (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overshoot enabling the use of higher DC-bus voltages. This means an increase in the final output power.

Integrated DC/DC converters with high galvanic isolation (4 kV) ensures that the user is protected from the high voltage (secondary side).

The power supply for the driver may be the same as used in the control board (0/+15 V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75 kV/µs).

The driver input stages are connected directly to the control board output and due to different control board operating voltages, the input circuit includes a user voltage level selector (+15 V or +5 V). In the following only the designation SKHI 23 is used. This is valid for both driver versions. Any unique features will be marked as SKHI 23/12 (V_{CE} = 1200 V) or SKHI 23/17 (V_{CE} = 1700 V) respectively.

A. Features and Configuration of the Driver

a) A short description is given below. For detailed information, please refer to section B. The following is valid for both channels (TOP and BOTTOM) unless specified.

b) The SKHI 23 has an INPUT LEVEL SELECTOR circuit for two different levels. It is preset for CMOS (15 V) level, but can be changed by the user to HCMOS (5 V) level by solder bridging between pins J1 and K1. For long input cables, we do not recommend the 5 V level due to possible disturbances emitted by the power side.

c) An INTERLOCK circuit prevents the two IGBTs of the half bridge to switch-on at the same time, and a “deadtime” can be adjusted by putting additional resistors between pins J3 and K3 (R_{TD1}) and pins J4 and K4 (R_{TD2}). Therefore it will be possible to reduce the deadtimet t_{TD} (see also table 3).
The interlocking may also be inhibit by solder bridging between pins J5 and K5 to obtain two independent drivers.

d) The ERROR MEMORY blocks the transmission of all turn-on signals to the IGBT if either a short circuit or malfunction of Vs is detected, a signal is sent to the external control board through an open collector transistor. It is preset to “high-logic” but can be set to “low-logic” (ERROR).

e) The V_s MONITOR ensures that V_s actual is not below 13 V.

f) With a FERRITE TRANSFORMER the information between primary and secondary may flow in both directions and high levels of dv/dt and isolation are obtained.

g) A high frequency DC/DC CONVERTER avoids the requirement of external isolated power supplies to obtain the necessary gate voltage. An isolated ferrite transformer in half-bridge configuration supplies the necessary power to the gate of the IGBT. With this feature, we can use the same power supply used in the external control circuit, even if we are using more than one SKHI 23, e.g. in three-phase configurations.

h) Short circuit protection is provided by measuring the collector-emitter voltage with a V_{CE} MONITORING circuit. An additional circuit detects the short circuit after a delay (adjusted with R_{CE} (this value can only be reduced) and C_{CE} (this value can only be increased) and decreases the turn off speed (adjusted by $R_{goff\text{-}SC}$) of the IGBT. SOFT TURN-OFF under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster turn off during normal operation.

i) The OUTPUT BUFFER is responsible for providing the correct current to the gate of the IGBT. If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT) the equivalent value of R_{gon} and the R_{goff} must be matched to the optimum value. This can be done by putting additional parallel resistors R_{gon}, R_{goff} with those already on the board. If only one IGBT is to be used, (instead of paralleled IGBTs) only one cable could be connected between driver and gate by solder bridging between the pins J12 and K12 (TOP) as well as between J19 and K19 (Bottom).

j) Fig. 1 shows a simplified block diagram of the SKHI 23 driver. Some preliminary remarks will help the understanding:

- Stabilised +15 V must be present between pins X1.8,9 (V_s) and X1.10,11 (⊥); an input signal (ON or OFF command to the IGBTs) from the control system is supplied to pins X1.2 and X1.4 (V_{in}) where HIGH=ON and LOW=OFF. The pin X1.1 can be used as a shield for the input signals.
- Pin X2.5 on TOP (and X3.5 on BOT) at secondary side is normally connected to the collector of the IGBTs to monitor V_{CE}, but for initial tests without connecting the IGBT it must be connected to pin X2.1 on TOP (and X3.1 on BOT) to avoid ERROR signal and enable the output signals to be measured.
- The RESET is performed when both input V_{in} signals are zero (TOP = BOT = LOW).
- To monitor the ERROR signal in “high-logic”, a pull-up resistor must be provided between pin X1.3 and $V_{s.}$
- Table 1 (see page B 14–46) shows the factory adjustment and the different possible adjustments of the pins.

B. Description of the Circuit Block Diagram (Fig. 1)

The circuit in Fig. 1 shows the input on the left and output on the right (primary/secondary).

1. Input level circuit

This circuit was designed to accept two different CMOS logic voltage levels. The standard level is +15 V (factory adjusted) intended for noisy environments or when long connections (l > 50 cm) between the external control circuit and SKHI 23 are used, where noise immunity must be considerate. For lower power, and short connections between control and driver, the TTL-HCMOS level (+5 V) can be selected by solder bridging between J1 and K1, specially useful for signals coming from uP based controllers.

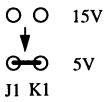


Fig.3 Selecting J1, K1 for 5 V level (TTL-HCMOS)

When connecting the SKHI 23 to a control board using short connections no special attention needs to be taken (Fig. 4a).

Otherwise, if the length is 50 cm or more (we suggest to limit the cable length to about 1 meter), some care must be taken. The TTL level should be avoided and CMOS/ 15 V is to be used instead; flat cable must have the pairs of conductors twisted or be shielded to reduce EMI/RFI susceptibility (Fig. 4b). If a shielded cable is used, it can be connected to pinX1.1 and coupled to 0 V through a capacitor, resistor or by solder bridging between pins J20 and K20.

As the input impedance of the INPUT LEVEL SELECTOR circuit is very high, an internal pull-down resistor keeps the IGBT in OFF state in case the V_{in} connection is interrupted or left non connected.

The following overview is showing the input treshold voltages

V_{IT+} (High)	min	typ	max
15 V	9,5 V	11,0 V	12,5 V
5 V	1,8 V	2,0 V	2,4 V

V_{IT-} (Low)	min	typ	max
15 V	3,6 V	4,2 V	4,8 V
5 V	1,8 V	0,65 V	0,8 V

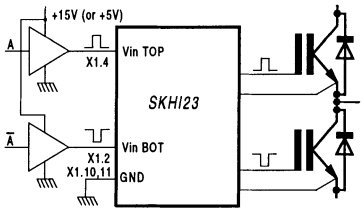


Fig. 4a Connecting the SKHI 23 with short cables

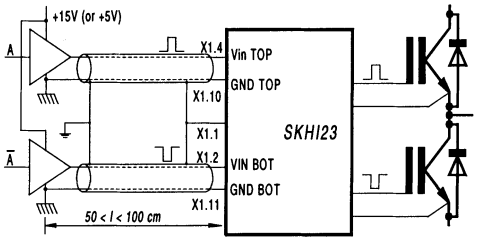


Fig. 4b Connecting the SKHI 23 with long cables

2. Input buffer

This circuit enables and improves the input signal V_{in} to be transferred to the pulse transformer and also prevents spurious signals being transmitted to the secondary side.

3. Error memory and RESET signal

The ERROR memory is triggered only by following events:

- short circuit of IGBTs
- V_s-undervoltage

In case of short circuit, the V_{CE} monitor sends a trigger signal (fault signal) through the pulse transformer to a FLIP-FLOP on the primary side giving the information to an open-collector transistor (pin X1.3), which may be connected to the external control circuit as ERROR message in “high-logic” (or “low-logic” if pins J2 and K2 are bridged). If V_s power supply falls below 13 V for more than 0,5 ms, the FLIP-FLOP is set and pin X1.3 is activated. For “high-logic” (factory preset), an external R_C must be connected, preferably in the control main board. In this way the connection between main board and driver is also monitored.

Function	pin description	adjustment by factory		possibilities of functions
input level selector	J1 / K1	not bridged ⇒15V CMOS		soldering bridged ⇒5V HCMOS
error - logic	J2 / K2	not bridged ⇒HIGH-aktiv		soldering bridged ⇒LOW-aktiv
interlock time	J3 / K3 (TOP R_{TD1}) J4 / K4 (BOT R_{TD2})	not equiped ⇒max. t_{TD} = 10 µs		adjustment according table 3
interlock of TOP and BOTTOM	J5 / K5	not bridged ⇒interlock activ		soldering bridged ⇒no interlock
$R_{CE\ TOP}$	J6 / K6	**SKHI 23/12** not equiped ⇒ R_{CE}= 18 kΩ	**SKHI 23/17** not equiped ⇒ R_{CE}= 36 kΩ	adjustment according tab. 4a/b
$C_{CE\ TOP}$	J7 / K7	**SKHI 23/12** not equiped ⇒ C_{CE}= 330 pF	**SKHI 23/17** not equiped ⇒ C_{CE}= 470 pF	adjustment according tab. 4a/b
$R_{gon\ TOP}$	J8 / K8	**SKHI 23/12** not equiped ⇒ R_{gon}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{gon}= 22 Ω	adjustment according tab. 4a/b
$R_{goff\ TOP}$	J9 / K9	**SKHI 23/12** not equiped ⇒ R_{goff}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{goff}= 22 Ω	adjustment according tab. 4a/b
$IR_{goff\ TOP}$	J10 / K10	equiped with IR_{goff}= 0 Ω		adjustment according tab. 4a/b
$R_{goffSC\ TOP}$	J11 / K11	equiped with ⇒R_{goffSC}= 22 Ω		
TOP: one IGBT/ paralleled IGBTs	J12 / K12	not bridged ⇒2 cables to gates		soldering bridged ⇒1 cable to gate
$R_{CE\ BOT}$	J13 / K13	**SKHI 23/12** not equiped ⇒ R_{CE}= 18 kΩ	**SKHI 23/17** not equiped ⇒ R_{CE}= 36 kΩ	adjustment according tab. 4a/b
$C_{CE\ BOT}$	J14 / K14	**SKHI 23/12** not equiped ⇒ C_{CE}= 330 pF	**SKHI 23/17** not equiped ⇒ C_{CE}= 470 pF	adjustment according tab. 4a/b
$R_{gon\ BOT}$	J15 / K15	**SKHI 23/12** not equiped ⇒ R_{gon}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{gon}= 22 Ω	adjustment according tab. 4a/b
$R_{goff\ BOT}$	J16 / K16	**SKHI 23/12** not equiped ⇒ R_{goff}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{goff}= 22 Ω	adjustment according tab. 4a/b
$IR_{goff\ BOT}$	J17 / K17	equiped with IR_{goff}= 0 Ω		adjustment according tab. 4a/b
$R_{goffSC\ BOT}$	J18 / K18	equiped with ⇒R_{goffSC}= 22 Ω		
BOT: one IGBT/ paralleled IGBTs	J19 / K19	not bridged ⇒2 cables to gates		soldering bridged ⇒1 cable to gate
shield	J20 / K20	not bridged ⇒no screening		soldering bridged ⇒screening to GND

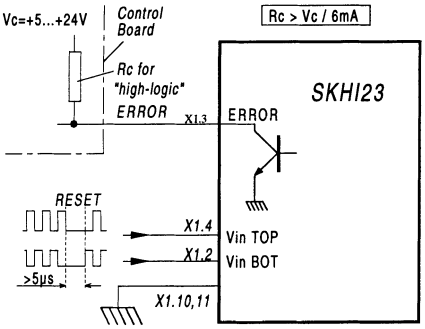


Fig. 5 Driver status information ERROR, and RESET

If “low-logic” version ERROR is used (pins J2 and K2 are bridged), an internal pull-up resistor (internally connected to V_S) is provided, and the ERROR signal from more SKHI23s can be connected together to perform an wired-or-circuit.

The ERROR signal may be disabled either by delivering zero to both signal inputs (RESET = active = $V_{in\text{-}TOP}$ = $V_{in\text{-}BOT}$ = 0) or by switching the power supply (V_S) off. The “RESET” signal width must be more than 5 µs long (see Fig. 5).

FAULT	RESET	ERROR[1)]	switching on of IGBT
no	no active	0	possible
no	active	0	not possible
yes	no active	1	not possible
yes	active	0	not possible

1) default logic (HIGH); for LOW logic the signals are complementary

Table 2 ERROR signal truth table

The open-collector transistor (pin X1.3) may be connected through a pull-up resistor to an extemal (internal V_S for the “low-logic” version) voltage supply +5 V...+24 V, limiting the current to I_{sink} 6 mA.

4. Power supply (V_s) monitor

The supply voltage V_S is monitored. If it falls below 13 V an ERROR signal is generated and the turn-on pulses for the IGBTs gate are blocked.

5. Pulse transformer

It transmits the turn-on and turn-off signals to the driver’s secondary side. In the reverse direction the ERROR signal from the V_{CE} monitoring is transmitted via the same transformer. The isolation is 4 kV_{AC}.

6. DC/DC converter

In the primary side of the converter, a half-bridge inverter transfers the necessary energy from V_S to the secondary of a ferrite transformer. In the secondary side, a full bridge and filters convert the high frequency signal coming from the primary to DC levels (+15V/- 8V) that are stabilised by a voltage regulator circuit.

7. Output buffer

The output buffer is supplied by the +15V/- 8V from the DC/DC converter and amplifies the control signal received from the pulse transformer. If the operation proceeds normally (no fault), the signal is transmitted to the gate of an IGBT through R_{gon} and R_{goff}. The output stage has a MOSFET pair which is able to source/sink up to 8 A peak current to/from the gate improving the turn-on/off time of the IGBT. Additionally, we can select I_{Rgoff} (see Fig. 2) either to discharge the gate capacitance with a voltage source (standard) or with a current source, specially design for the 1700 V IGBT series (it speeds up the turn-off time of the IGBT). The present factory setting is voltage source (I_{Rgoff} = 0Ω). and to change to current source I_{Rgoff}, must be adjusted, while R_{goff} = 0.

8. Soft turn-off

In case of short-circuit, a further circuit (SOFT TURN-OFF) increases the resistance in series with R_{goff} and turns-off the IGBT at a lower speed. This produces a smaller voltage spike (due LSTRAY ’ di/dt) above the DC link by reducing the di/dt value. Because in short-circuit conditions the Homogeneous IGBT’s peak current increases up to 8 times the nominal current (up to 10 times with Epitaxial IGBT structures), and some stray inductance is ever present in power circuits, it must fall to zero in a longer time than at normal operation. This “soft turn-off time” can be reduced by connecting a parallel resistor R_{goff}-SC (see Fig. 2) with those already on the printed circuit board.

9. V_{CE} monitoring

This circuit is responsible for short-circuit sensing. Due to the direct measurement of V_{CEstat} on the IGBT’s collector, it blocks the output buffer (through the soft turn-off circuit) in case of short-circuit and sends a signal to the ERROR memory on the primary side. The recognition of which V_{CE} level must be considered as a short circuit event, is adjusted by R_{CE} and C_{CE} (see Fig. 2), and it depends of the IGBT used. For the drivers SKHI23/12 typical values R_{CE} =18 kΩ and C_{CE} =330 pF for SKHI 10 are delivered from factory (Fig. 6, curve 2). Using SKHI 10/17 the driver will be delivered with R_{CE} = 36 kΩ and C_{CE} = 470 pF from factory.

The V_{CEref} is not static but a dynamic reference which has an exponential shape starting at about 15 V and decreases to V_{CEstat} (determinated by R_{CE}), with a time constant τ (controlled by C_{CE}).

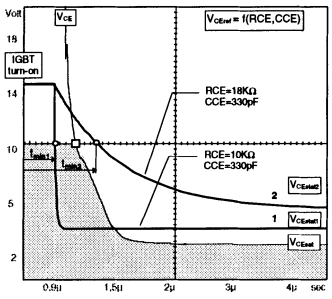


Fig. 6 V_{CEref} waveform with parameters R_{CE}, C_{CE}

Adjustements for SKHI 23/12

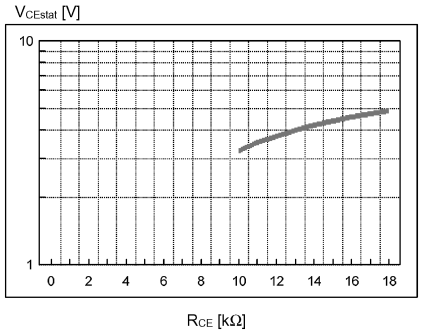


Fig. 7a V_{CEstat} as function of R_{CE}

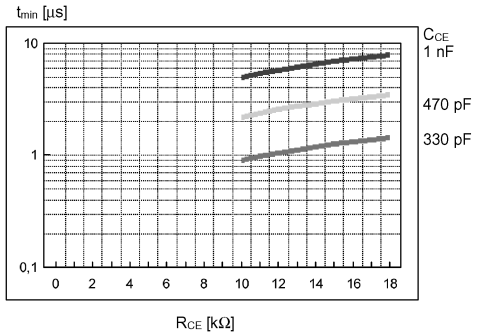


Fig. 7b t_{min} as function of R_{CE} and C_{CE}

Adjustements for SKHI 23/17

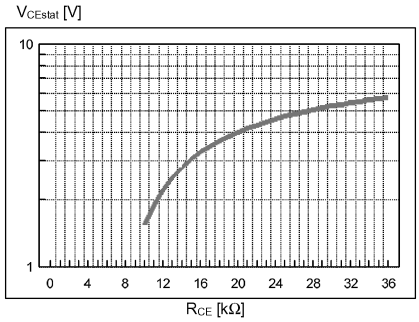


Fig. 7c V_{CEstat} as function of R_{CE}

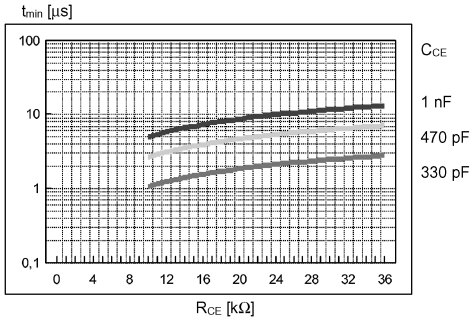


Fig. 7d t_{min} as function of R_{CE} and C_{CE}

The V_{CEstat} must be adjusted to remain above V_{CEsat} in normal operation (the IGBT is already in full saturation).

To avoid a false failure indication when the IGBT just starts to conduct (V_{CEsat} value is still too high) some decay time must be provided for the V_{CEref}. As the V_{CE} signal is internally limited at 10 V, the decay time of V_{CEref} must reach this level after V_{CE} or a failure indication will occur (see Fig.6, curve 1). A t_{min} is defined as function of V_{CEstat} and τ to find out the best choice for R_{CE} and V_{CE} (see Fig.6, curve 2). The time the IGBT come to the 10 V (represented by a "□" in Fig. 6) depends on the IGBT itself and R_{gon} used.

The R_{CE} and C_{CE} values can be found from Fig. 7a and 7b for SKHI 23/12 and from Fig. 7c and 7d for SKHI 23/17 by taking the V_{CEstat} and t_{min} as input values with following remarks:

- R_{CE} > 10KΩ
- C_{CE} < 2,7nF

Attention!: If this function is not used, for example during the experimental phase, the V_{CE} MONITORING must be connected with the EMITTER output to avoid possible fault indication and consequent gate signal blocking.

10. R_{gon}, R_{goff}

These two resistors are responsible for the switching speed of each IGBT. As an IGBT has input capacitance (varying during the switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of resistance is difficult to predict, because it depends on many parameters, as follows:

- DC-link voltage
- stray inductance of the circuit
- switching frequency
- type of IGBT

The driver is delivered with two R_g resistors (22 Ω) on the board. This value can be reduced to use the driver with bigger modules or higher frequencies, by putting additional resistors in parallel.

The outputs G_{on} and G_{off} were previewed to connect the driver with more than one IGBT (paralleling). In that case we need both signals ON/OFF separately to connect additional extremal resistors R_{gon} and R_{goff} for each IGBT. If only one IGBT is to be used, we suggest connecting both outputs together by solder bridging between pins J12 and K12 and respectiveley pins J19 and K19 to save on external connection. We also suggest using two restistors for R_{gon} and two resistors for R_{goff} when using low values of resistance, due the high current peak (up to 8 A) which could damage a single resistor.

11. Interlock

The interlock circuit prevents the IGBT turning on before the gate charge of the other IGBT is completely discharged. It should be set to delay time longer than the turn-off time of the IGBT. From the factory: t_{TD} = 10 µs. By putting additional resistors onto the pins J3/K3 ($R_{TD\ TOP}$) and onto the pins J4/K4 ($R_{TD\ BOT}$) the interlock time t_{TD} can be reduced (see table 3).

$R_{TD1} = R_{TD2}$	interlock time t_{TD}
10 kΩ	0,9 µs
22 kΩ	1,8 µs
33 kΩ	2,5 µs
47 kΩ	3,2 µs
68 kΩ	4,0 µs
100 kΩ	5,0 µs
330 kΩ	7,7 µs
not equiped (adjustement by factory)	10 µs

It have to be considered: $R_{TD1} = R_{TD2}$ 10 kΩ
Table 3 adjustement of interlock time

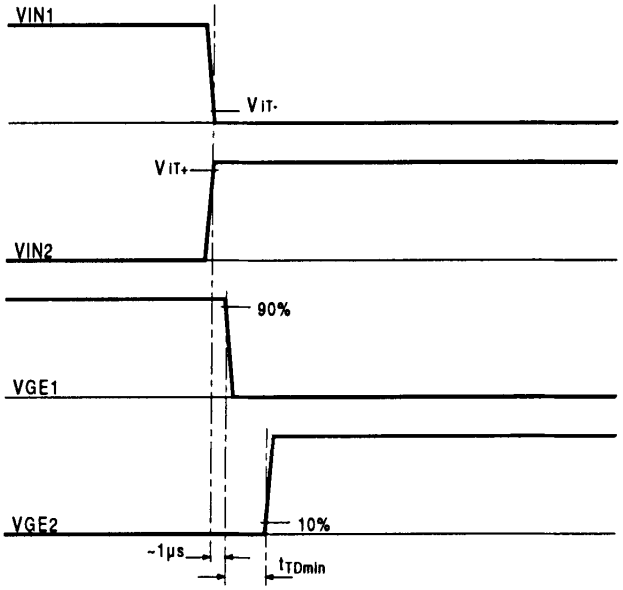


Fig. 8 Interlock function time diagram

C. Operating Procedure

1. One dual IGBT connection

To realize the correct switching and short-circuit monitoring of one IGBT-module some additional components must be used (Fig. 9).

Typical component values: *)

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kW	I_{rgoff} Ω
SKM 75GB123D	22	22	330	18	0
SKM 100GB123D	15	15	330	18	0
SKM 145GB123D	12	12	330	18	0
SKM 150GB123D	12	12	330	18	0
SKM 200GB123D	10	10	330	18	0
SKM 300GB123D	8,2	8,2	330	18	0

Table 4a 1200V IGBT@ DC-link< 700V

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kW	I_{rgoff} Ω
SKM 75GB123D	15	15	470	36	0
SKM 100GB123D	12	12	470	36	0
SKM 150GB123D	10	10	470	36	0
SKM 200GB123D	8,2	8,2	470	36	0
SKM 300GB123D	6,8	6,8	470	36	0

Table 4b 1700V IGBT@ DC-link< 1000V

*) Only starting values, for final optimization.

The adjustment of R_{goffSC} (factory adjusted R_{goffSC} = 22 Ω) should be done observing the overvoltages at the module in case of short circuit. When having a low inductive DC-link the module can be switched off faster.

The shown values should be considered as standard values for a mechanical/electrical assembly, with acceptable stray inductance level, using only one IGBT per SKHI 23 driver. The final optimised value can be found only by measuring.

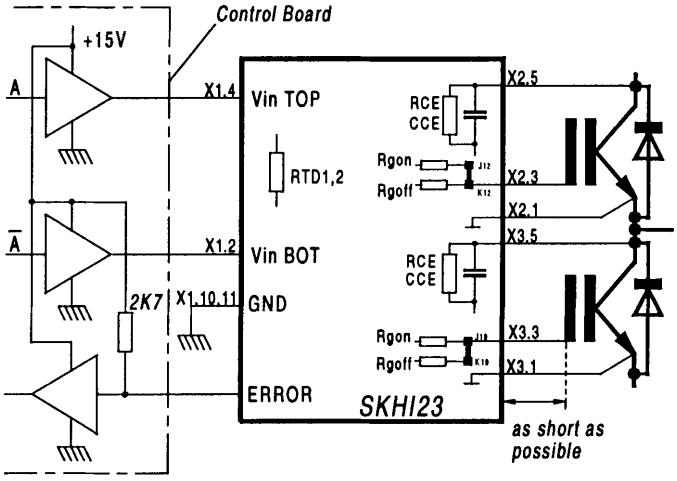


Fig. 9 Preferred dual IGBT-module standard circuit

2. Paralleling IGBTs

The parallel connection is recommended only by using IGBTs with homogeneous structure (IGHT), that have a positive temperature coefficient resulting in a perfect current sharing without any external auxiliary element. Care must be considered to reach an optimized circuit and to obtain the total performance of the IGBT (Fig. 10). The IGBTs must have independent values of R_{gon} and R_{goff}, and an auxiliary emitter resistor R_e as well as an auxiliary collector resistor R_c must also be used. The external resistors R_{gonx}, R_{goffx}, R_{ex} and R_{cx} should be mounted on an additional circuit board near the paralleled modules, and the R_{gon}/R_{goff} should be changed to zero ohms.

The R_{ex} has a value of 0,5 Ω and its function is to avoid the main current to circulate by the auxiliary ermitter what could make the ermitter voltage against ground unbalanced.

The R_{cx} assumes a value of 47 Ω and its function is to create an average of V_{CEsat} in case of short circuit for V_{CE}-monitoring.

The mechanical assembly of the power circuit must be symmetrical and low inductive.

The maximum recommended gate charge is 4,8 µC.

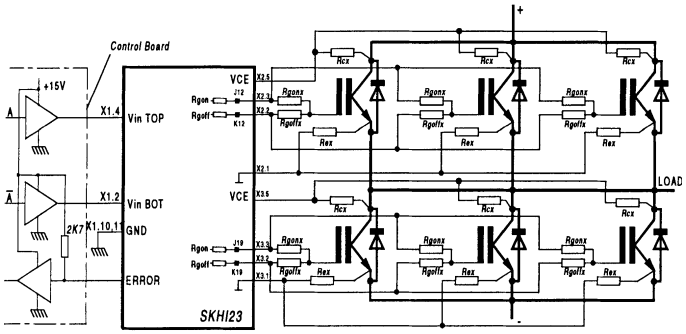


Fig. 10 Preferred circuit for paralleld dual IGBT-modules

D. Signal Waveforms

The following signal waveforms were measured under the conditions below:

- V_S = 15 V
- T_{amb} = 25 °C
- load = SKM75GB120D
- R_{CE} = 18 kΩ
- C_{CE} = 330 pF
- U_{DC} = 600 V
- I_C = 100 A

All results are typical values if not otherwise specified.

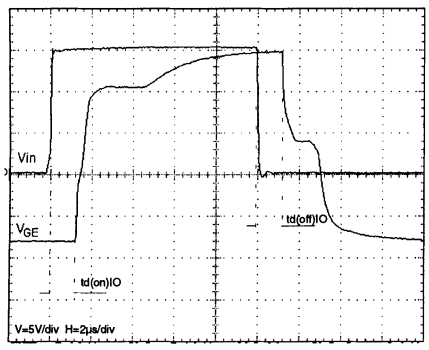


Fig. 11 Input and output voltage propagation time

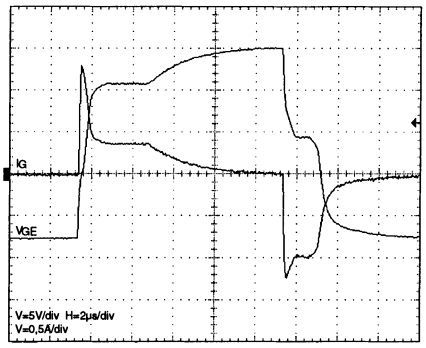


Fig. 12 Output voltage V_{GE} and output current (I_G)

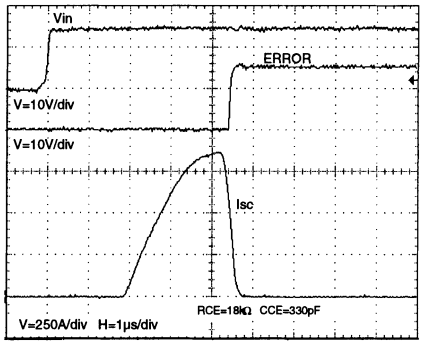


Fig.13 Short circuit and ERROR propagation time worste case (V_{IN} with SC already present)

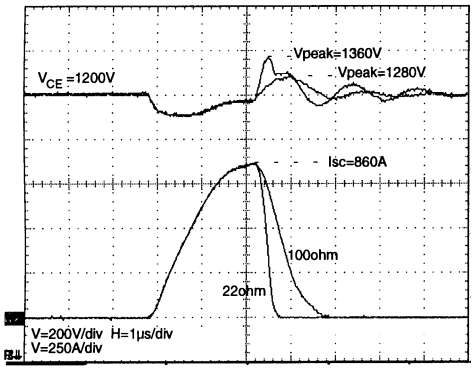


Fig.14 Effect of $R_{goff\text{-}SC}$ in short - circuit

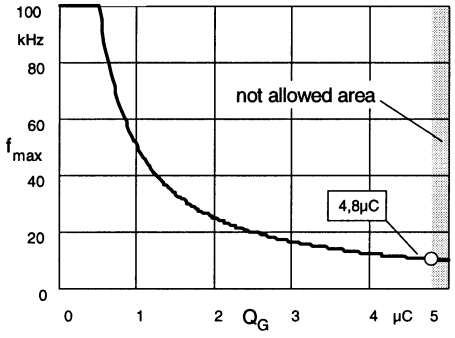


Fig. 15 Maximum operating frequency x gate charge

The limit frequency of SKHI 23 depends on the gate charge connected in its output pins.

If small IGBT modules are used, the frequency could theoretically reach 100 kHz. For bigger modules or even paralleled modules, the maximum frequency must be determinate (Fig. 15). Q_G is the total equivalent gate charge connected to the output of the driver. The maximum allowed value is limited (about 4,8 µC).

E. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than (V_S + 0,3 V) or under - 0,3 V may destroy these inputs.

Therefore the following safety requirements are to be observed:

- To make sure that the control signals do not see overvoltages exceeding the above values.
- Protection against static discharges during handling. As long as the hybrid driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded. The same safety requirements apply to the IGBTs.

2. The connecting leads between the driver and the power module must be as short as possible, and should be twisted.

3. Any parasitic inductance should be minimized. Overvoltages may be damped by C or RCD snubber networks between the main terminals [3] = C1 (+) and [2] = E2 (-) of the power module.

4. When first operating a newly developed circuit, low collector voltage and load current should be used in the beginning. These values should be increased gradually, observing the turn-off behavior of the free-wheeling diodes and the turn-off voltage spikes across the IGBT by means of an oscilloscope. Also the case temperature of the power module should be monitored. When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.

5. It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.

For further details ask SEMIKRON