



FDD8445

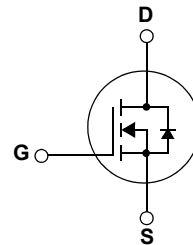
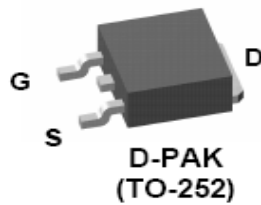
N-Channel PowerTrench® MOSFET 40V, 50A, 8.7mΩ

Features

- $R_{DS(ON)} = 6.7 \text{ m}\Omega$ (Typ), $V_{GS} = 10\text{V}$, $I_D = 50\text{A}$
- $Q_{g(10)} = 45\text{nC}$ (Typ), $V_{GS} = 10\text{V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- RoHS Compliant

Applications

- Powertrain Management
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems



Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS}=10\text{V}$) (Note 1)	70	A
	Continuous ($V_{GS}=10\text{V}$, with $R_{\theta JA} = 52^\circ\text{C/W}$)	15.2	A
	Pulsed	Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	144	mJ
P_D	Power Dissipation	79	W
	Derate above 25°C	0.53	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, lin^2 copper pad area	52	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8445	FDD8445	TO-252AA	13"	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	2.8	4	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 50\text{A}, V_{GS} = 10\text{V}$	-	6.7	8.7	m Ω
		$I_D = 50\text{A}, V_{GS} = 10\text{V},$ $T_J = 175^\circ\text{C}$	-	12.5	16.3	

Dynamic Characteristics

C _{ISS}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	3040	4050	pF
C _{OSS}	Output Capacitance			-	295	390	pF
C _{RSS}	Reverse Transfer Capacitance			-	178	270	pF
R _G	Gate Resistance	f = 1MHz		-	1.7	-	Ω
Q _{g(TOT)}	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 20V, I _D = 50A	-	45	59	nC
Q _{g(5)}	Total Gate Charge at 5V	V _{GS} = 0 to 5V		-	17	22	nC
Q _{g(TH)}	Threshold Gate Charge	V _{GS} = 0 to 2V		-	5.8	7.6	nC
Q _{gs}	Gate to Source Gate Charge			-	12.5	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau			-	9.5	-	nC
Q _{gd}	Gate to Drain “Miller” Charge			-	10.5	-	nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Switching Characteristics

$t_{(on)}$	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 50\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 2\Omega$	-	-	138	ns
$t_{d(on)}$	Turn-On Delay Time		-	10	-	ns
t_r	Turn-On Rise Time		-	82	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	-	ns
t_f	Turn-Off Fall Time		-	9.6	-	ns
t_{off}	Turn-Off Time		-	-	53	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD}=50\text{A}$	-	-	1.25	V
		$I_{SD}=25\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_F = 50\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$	-	-	39	ns
Q_{rr}	Reverse Recovery Charge	$I_F = 50\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$	-	-	38	nC

Notes:

1: Maximum package current capability is 50A.

2: Starting $T_J = 25^\circ\text{C}$, $L=0.18\text{mH}$, $I_{AS}=40\text{A}$.

Typical Characteristics

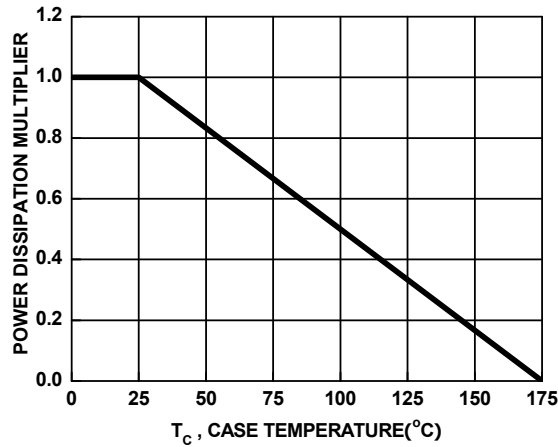


Figure 1. Normalized Power Dissipation vs Case Temperature

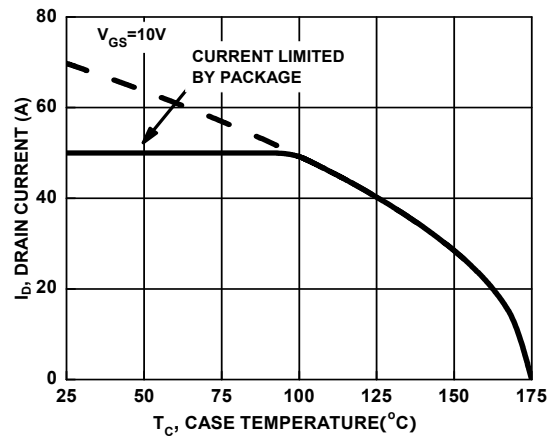


Figure 2. Maximum Continuous Drain Current vs Case Temperature

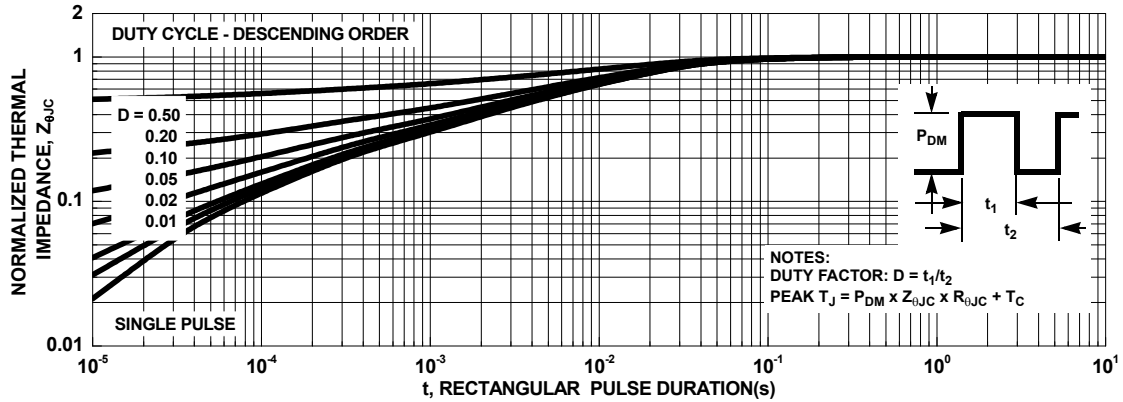


Figure 3. Normalized Maximum Transient Thermal Impedance

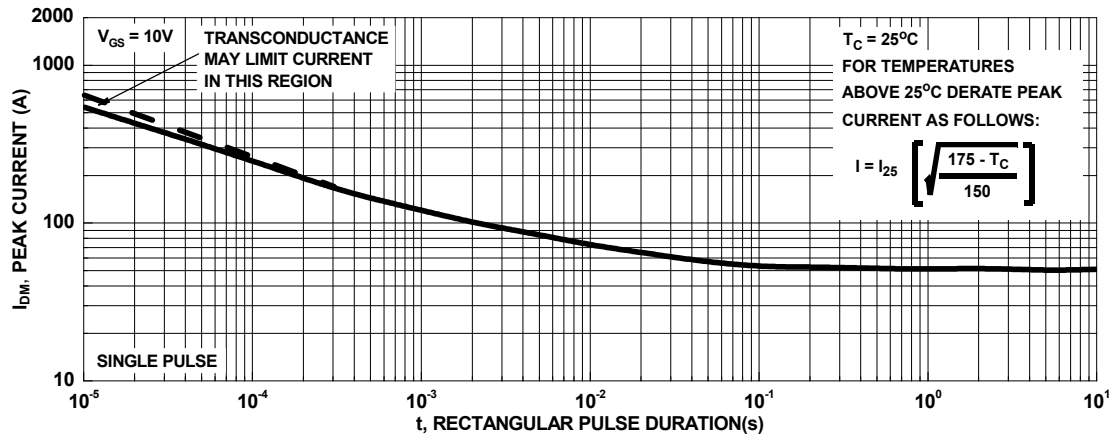


Figure 4. Peak Current Capability

Typical Characteristics

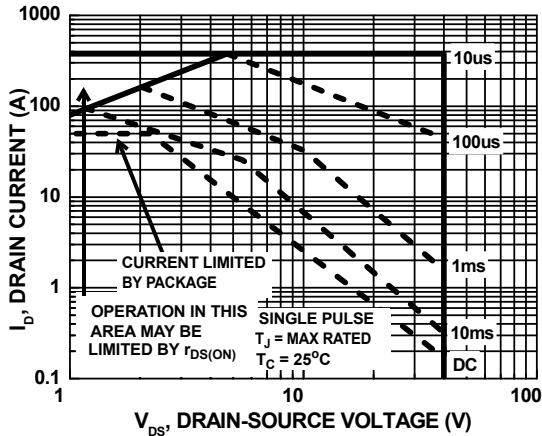
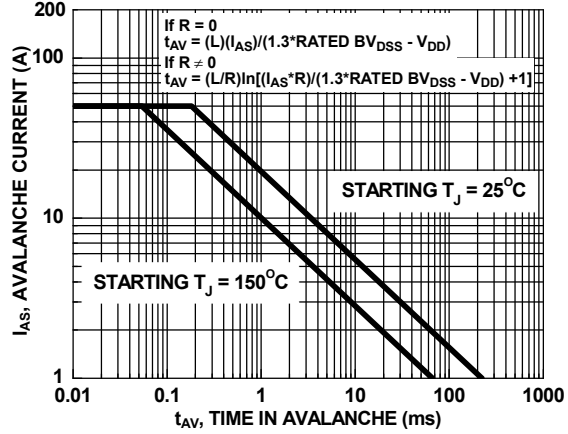


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

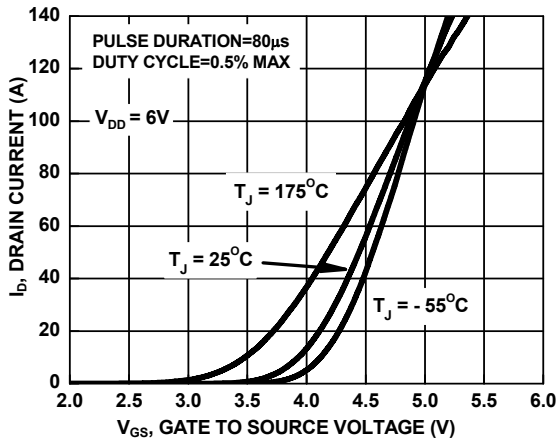


Figure 7. Transfer Characteristics

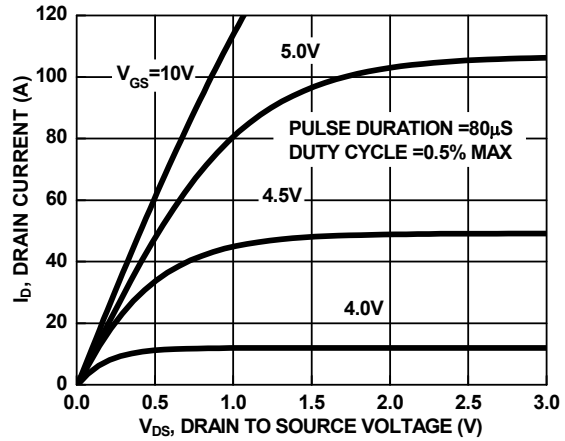


Figure 8. Saturation Characteristics

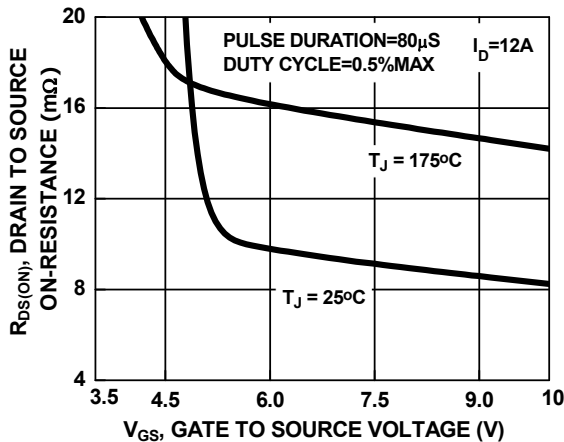


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

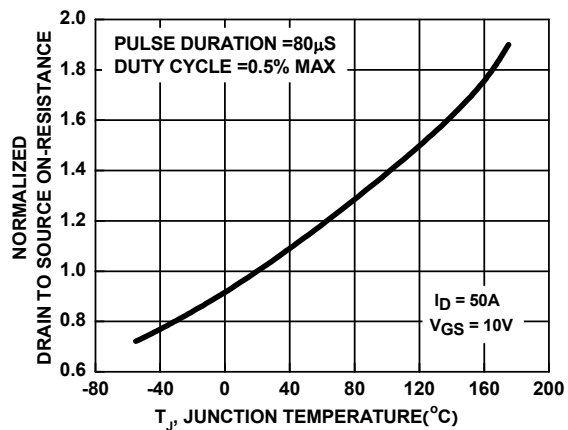


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

Typical Characteristics

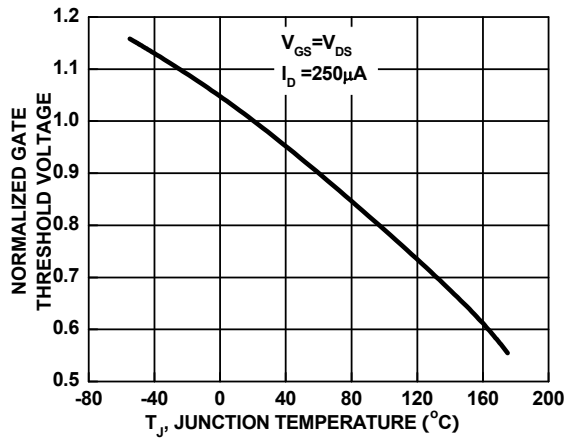


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

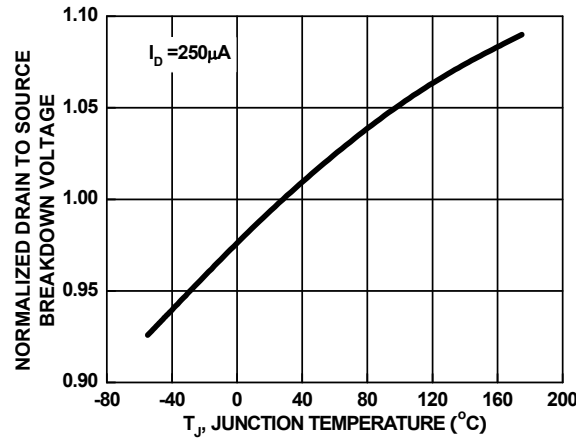


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

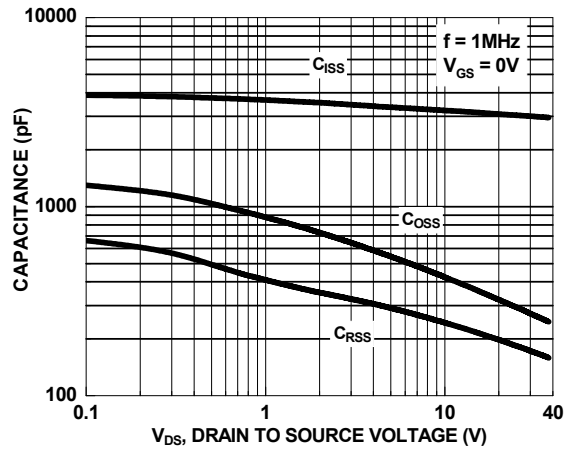


Figure 13. Capacitance vs Drain to Source Voltage

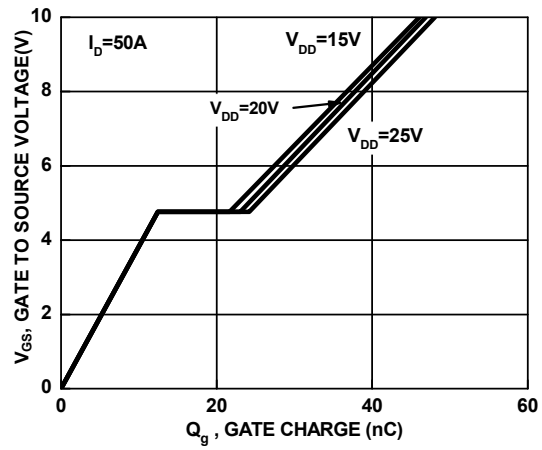
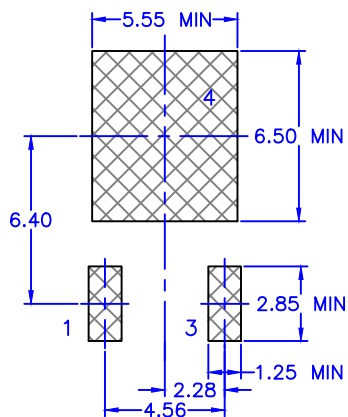
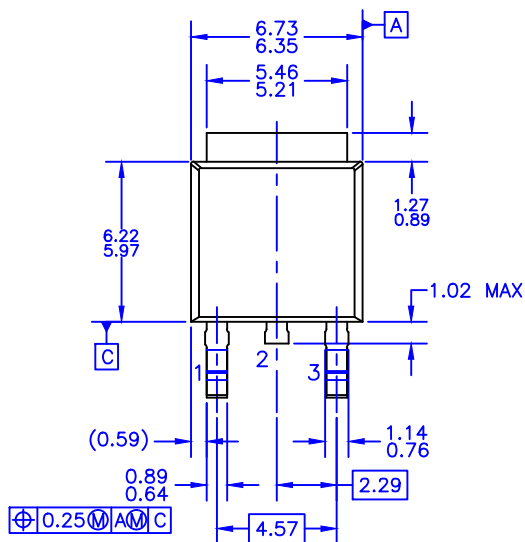
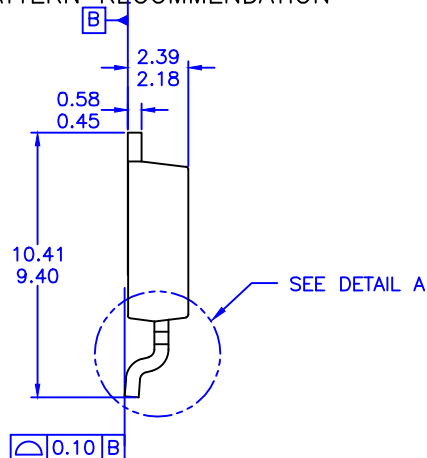
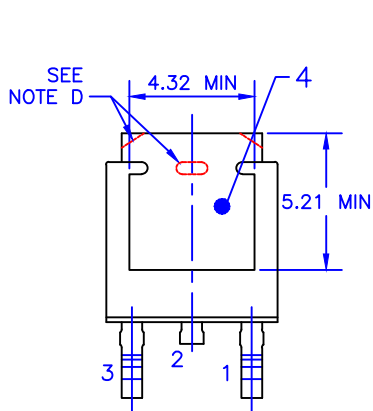


Figure 14. Gate Charge vs Gate to Source Voltage

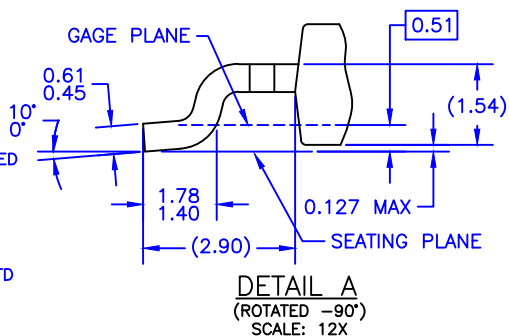


LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- DRAWING NUMBER AND REVISION: MKT-TO252A03REV9.
- FAIRCHILD SEMICONDUCTOR.



DETAIL A
(ROTATED -90°)
SCALE: 12X



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