

# Autonomous Audio Headset Switch with Reduced GND Switch $R_{ON}$ and FM Capability

Check for Samples: [TS3A226E](#)

## FEATURES

- Ground FET Switches (60mΩ typical)
- Autonomous Detection of Headset Types: 3-Poles or 4-Poles (with MIC on SLEEVE or RING2)
- Microphone Line Switches
- Supports FM Signal Transmission Through the Ground FETs
- Reduction of Click/Pop Noise
- VDD Range: 2.6 V – 4.7 V
- THD (Mic): 0.002% Typical
- Low Current Consumption: 6.5-μA Typical
- ±8kV Contract Discharge (IEC 61000-4-2) ESD Performance on SLEEVE and RING2 Pins

## APPLICATIONS

- Mobile Phones / Tablet PCs
- Notebook/Ultrabook Computers

## DESCRIPTION

The TS3A226E is an audio headset switch that detects 3- or 4-pole 3.5mm accessories. For a 4-pole accessory with a microphone, the TS3A226E also detects the MIC location and routes the microphone and ground signals automatically. The ground signal is routed through a pair of low-impedance ground FETs (60mΩ typical), resulting minimal impact on audio cross-talk performance. The autonomous detection feature allows end users to plug in accessories with different audio pole configurations into the mobile device and have them operate properly with no added software control and complexity. The ground FETs of the device are designed to allow FM signal pass-through, making it possible to use the ground line of the headset as an FM antenna in mobile audio application.

The TS3A226E is packaged within a 1.2mm × 1.2mm WCSP package, making it suitable for use in mobile application.

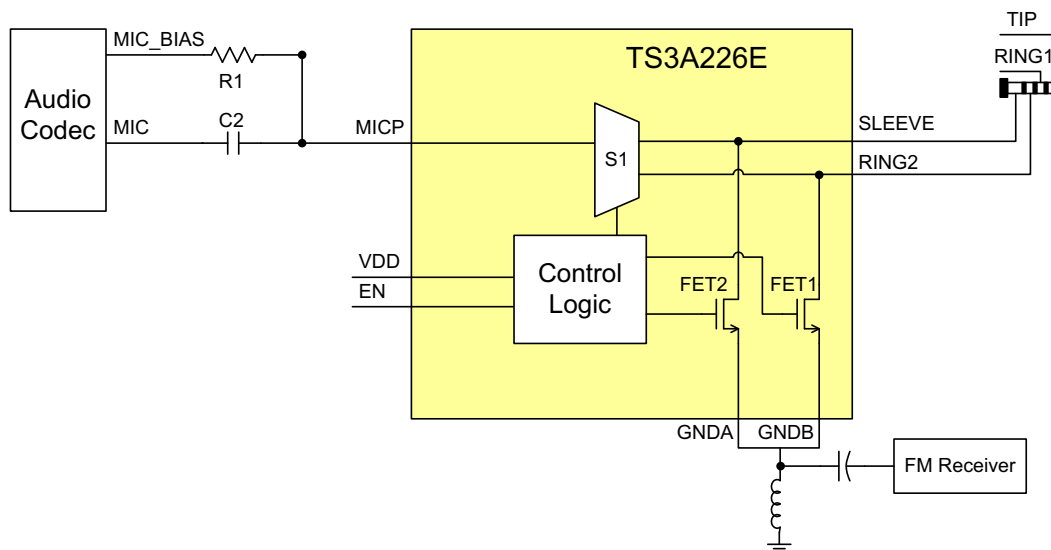


Figure 1. Typical Application Diagram

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>(1)(2)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | YFF- WCSP                 | Tape and reel | TS3A226EYFFR          | YP226E           |

- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TS3A226E

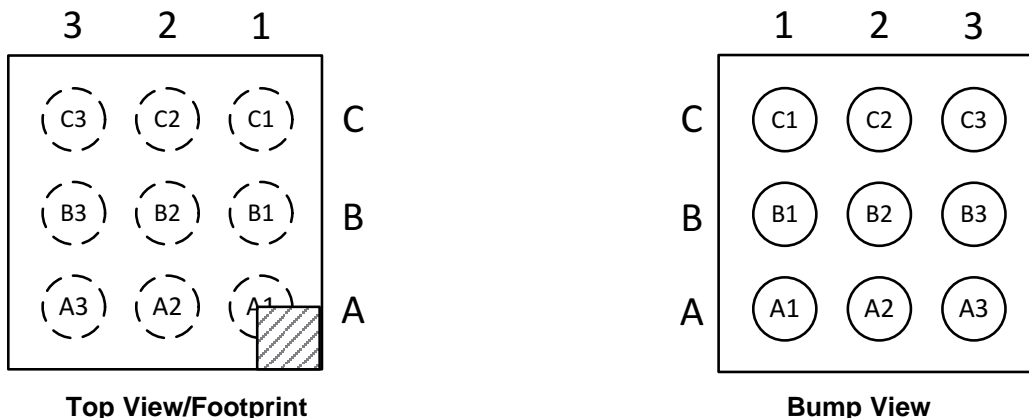
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## PACKAGE; YFF-WCSP



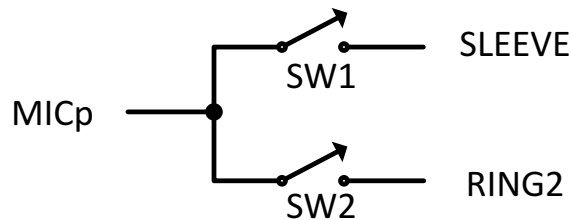
Die Size: 1.2mm x1.2mm  
 Bump Size: 0.25mm  
 Bump Pitch: 0.4mm

TS3A226E Pin Mapping (Top View)

|   |        |      |      |
|---|--------|------|------|
|   | 3      | 2    | 1    |
| C | GND    | TIP  | EN   |
| B | SLEEVE | GNDA | MICp |
| A | RING2  | GNDB | VDD  |

### PIN FUNCTIONS

| NUMBER | PIN    |        | DESCRIPTION  |
|--------|--------|--------|--|
|        | NAME   | TYPE   |  |
| A1     | VDD    | Supply | Power supply for the chip.   |
| A2     | GNDB   | Ground | FET2 ground reference.   |
| A3     | RING2  | I/O    | Connected to the RING2 segment of the jack. The pin will be routed automatically by TS3A226E to either MICp or GNDB depending on the type of accessory.    |
| B1     | MICp   | I/O    | Microphone signal connection to codec. Microphone bias should be fed into this pin.  |
| B2     | GNDA   | Ground | FET1 ground reference.   |
| B3     | SLEEVE | I/O    | Connected to the SLEEVE segment of the jack. The pin will be routed automatically by TS3A226E to either MICp or GNDA depending on the type of accessory.   |
| C1     | EN     | Input  | A rising edge triggers the detection sequence. This pin can be connected to the headset jack to allow automatic pull-up to supply after headset insertion. |
| C2     | TIP    | I/O    | Connected to the TIP segment of the headphone jack.  |
| C3     | GND    | Ground | Chip ground reference.   |

**S1 MUX DETAIL**

**Figure 2. S1 Mux Detail**
**FUNCTIONAL TABLES: INTERNAL SWITCHES**

| EN | Accessory Type                  | Accessory Configuration  | SW1    | SW2    | FET1   | FET2   |
|----|---------------------------------|--|--------|--------|--------|--------|
| 0  | N/A                             | —  | High Z | High Z | High Z | High Z |
| 1  | TRS 3-pole Headphone or Speaker | TIP = Audio Left<br>Ring = Audio Right<br>Sleeve = <b>Ground</b>                               | High Z | High Z | On     | On     |
| 1  | TRRS 4-pole Headphone           | TIP = Audio Left<br>Ring1 = Audio Right<br>Ring2 = <b>Ground</b><br>Sleeve = <b>Microphone</b> | On     | High Z | High Z | On     |
| 1  | TRRS 4-pole Headphone           | TIP = Audio Left<br>Ring1 = Audio Right<br>Ring2 = <b>Microphone</b><br>Sleeve = <b>Ground</b> | High Z | On     | On     | High Z |
| 1  | N/A                             | —  | High Z | High Z | High Z | High Z |

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                      |  | VALUE                        | UNIT |
|----------------------|--|------------------------------|------|
| V <sub>I</sub>       | Voltage range on VDD <sup>(2)</sup>                          | -0.3 to 5                    | V    |
|                      | Voltage range on EN, MICP, RING2, SLEEVE, TIP <sup>(2)</sup> | -0.3 to V <sub>DD</sub> +0.5 | V    |
| T <sub>A</sub>       | Operating ambient temperature range <sup>(3)</sup>           | -40 to 85                    | °C   |
| T <sub>J (MAX)</sub> | Maximum operating junction temperature                       | 125                          | °C   |
| T <sub>stg</sub>     | Storage temperature range                                    | -65 to 150                   | °C   |
| ESD rating           | Machine model (JESD 22 A115)                                 | 100                          | V    |
|                      | Charge device model (JESD 22 C101)                           | 500                          | V    |
|                      | Human body model (JESD 22 A114)                              | 2                            | kV   |
|                      | Contact discharge on RING2, SLEEVE, TIP (IEC 61000-4-2)      | 8                            | kV   |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> - (θ<sub>JA</sub> × P<sub>D(max)</sub>)

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**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

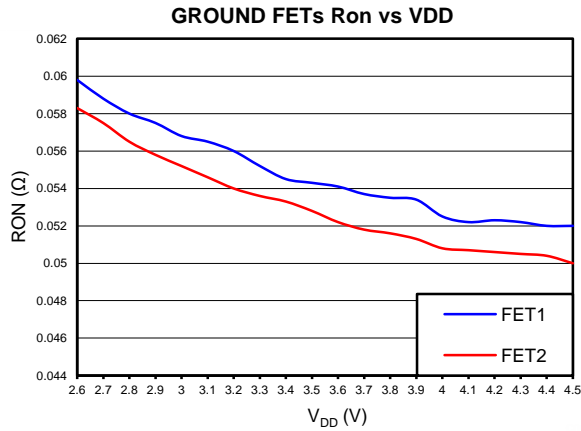
|                 |   | MIN                     | MAX             | UNIT            |   |
|-----------------|---|-------------------------|-----------------|-----------------|---|
| V <sub>DD</sub> | Supply voltage range                                      | 2.6                     | 4.5             | V               |   |
| V <sub>IO</sub> | Input/Output voltage range (EN, MICP, RING2, SLEEVE, TIP) | 0                       | V <sub>DD</sub> | V               |   |
| V <sub>IH</sub> | Input Logic High for EN                                   | V <sub>DD</sub> = 2.6 V | 1.16            | V <sub>DD</sub> | V |
|                 |   | V <sub>DD</sub> = 3.3 V | 1.24            | V <sub>DD</sub> |   |
|                 |   | V <sub>DD</sub> = 4.5 V | 1.48            | V <sub>DD</sub> |   |
| V <sub>IL</sub> | Input Logic Low for EN                                    | V <sub>DD</sub> = 2.6 V | 0               | 0.19            | V |
|                 |   | V <sub>DD</sub> = 3.3 V | 0               | 0.3             |   |
|                 |   | V <sub>DD</sub> = 4.5 V | 0               | 0.5             |   |
| T <sub>A</sub>  | Operating temperature range                               | -40                     | 85              | °C              |   |

**KEY ELECTRICAL CHARACTERISTICS**

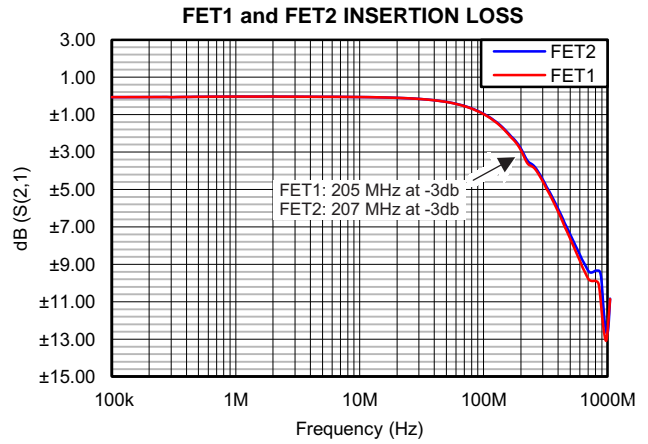
Unless otherwise noted the specification applies over the V<sub>DD</sub> range and operating junction temperature  $-40^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ . Typical values are for V<sub>DD</sub> = 3.3V and T<sub>J</sub> = 25°C.

| PARAMETER                             | TEST CONDITIONS                               | MIN  | TYP | MAX    | UNIT |     |
|---------------------------------------|---|--|-----|--------|------|-----|
| V <sub>DD</sub>                       | Input Voltage Range                           | 2.6  | 3.3 | 4.5    | V    |     |
| I <sub>DD</sub>                       | Quiescent Current                             | V <sub>DD</sub> = 4.5 V, V <sub>MICP</sub> = 1.8 V to V <sub>DD</sub>                        |     | 6.5    | 14   | μA  |
| <b>SWITCH RESISTANCE</b>              |   |  |     |        |      |     |
| R <sub>F1</sub>                       | FET1 On Resistance                            | V <sub>DD</sub> = 2.6 V, V <sub>GND</sub> = 0 V, I <sub>GND</sub> = 10 mA                    |     | 60     | 85   | mΩ  |
| R <sub>F2</sub>                       | FET2 On Resistance                            |  |     | 60     | 85   |     |
| R <sub>SW1</sub>                      | SW1 On Resistance                             | V <sub>DD</sub> = 2.6 V, V <sub>SLEEVE/RING2</sub> = 0 V to 2.6 V, I <sub>MIC</sub> = ±10 mA |     | 10.5   |      | Ω   |
| R <sub>SW2</sub>                      | SW2 On Resistance                             |  |     | 10.5   |      |     |
| <b>SWITCH LEAKAGE CURRENT</b>         |   |  |     |        |      |     |
| I <sub>OFF-0.1</sub>                  | FET1 and FET2 off leakage                     | V <sub>IN</sub> = 0 V to 2.6 V, V <sub>OUT</sub> = 0 V, V <sub>DD</sub> = 4.5 V              |     | 1      |      | μA  |
| I <sub>OFF-10</sub>                   | SW1, SW2 off leakage                          |  |     | 1      |      |     |
| I <sub>ON-10</sub>                    | SW1, SW2 on leakage                           |  |     | 1      |      |     |
| <b>SWITCH DYNAMIC CHARACTERISTICS</b> |   |  |     |        |      |     |
| BW <sub>F1</sub>                      | FET1 Bandwidth                                | V = 60 mV <sub>PP</sub> , I <sub>bias</sub> = 10 mA  |     | 160    | 200  | MHz |
| BW <sub>F2</sub>                      | FET2 Bandwidth                                |  |     | 160    | 200  |     |
| PSR <sub>217</sub>                    | Power Supply Rejection, R <sub>L</sub> = 50 Ω | V = 200 mV <sub>PP</sub> , f = 217 Hz  |     | -110   |      | dB  |
| PSR <sub>1k</sub>                     |   | V = 200 mV <sub>PP</sub> , f = 1 kHz   |     | -100   |      |     |
| PSR <sub>20k</sub>                    |   | V = 200 mV <sub>PP</sub> , f = 20 kHz  |     | -85    |      |     |
| ISO <sub>S1</sub>                     | SLEEVE or RING2 to MICP Isolation             | V = 200 mV <sub>PP</sub> , f = 20 kHz, R <sub>L</sub> = 50 Ω                                 |     | -80    |      | dB  |
| SEP <sub>S1</sub>                     | SLEEVE to RING2 Separation                    | V = 200 mV <sub>PP</sub> , f = 20 kHz, R <sub>L</sub> = 50 Ω (see Figure 5)                  |     | -80    |      | dB  |
| THD <sub>10</sub>                     | Total Harmonic Distortion                     | V = 10 mV <sub>PP</sub> , f = 20-20 kHz, R <sub>S</sub> = 600 Ω                              |     | 0.01%  |      |     |
| THD <sub>200</sub>                    |   | V = 200 mV <sub>PP</sub> , f = 20-20 kHz, R <sub>S</sub> = 600 Ω                             |     | 0.002% |      |     |

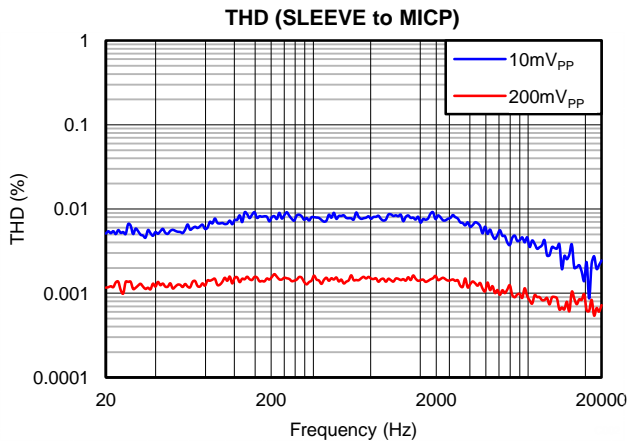
**TYPICAL CHARACTERISTICS**



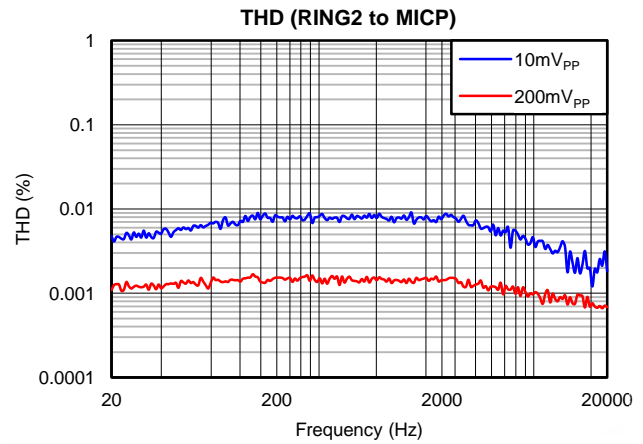
**Figure 3.**



**Figure 4.**



**Figure 5.**



**Figure 6.**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|-------------------------|---------|
| TS3A226EYFFR     | OBSOLETE      | DSBGA        | YFF                | 9    |                | TBD             | Call TI                 | Call TI              | -40 to 85    | YP2<br>26E              |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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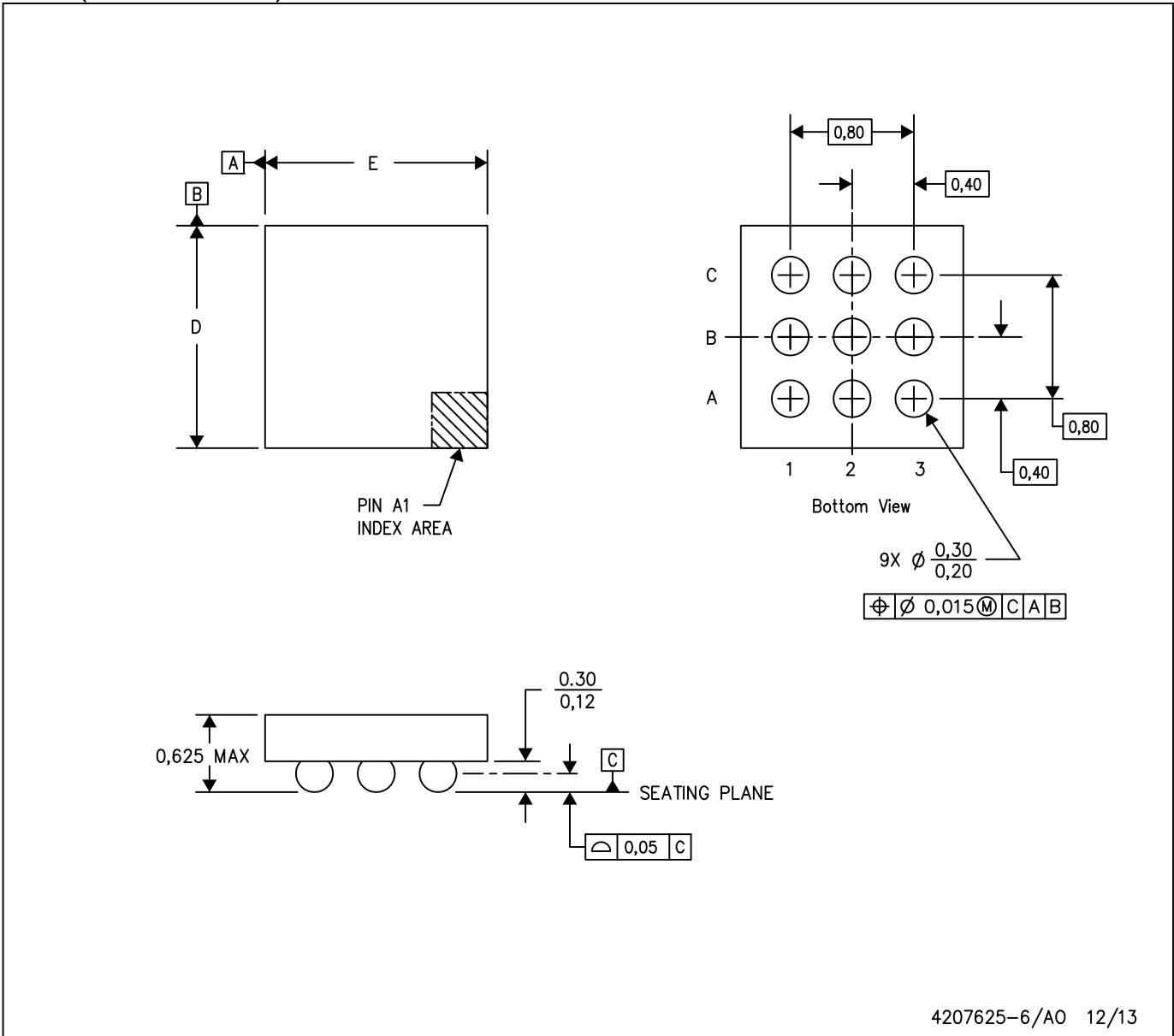
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# MECHANICAL DATA

YFF (S-XBGA-N9)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.  
 C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



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|                               |  |
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