MICROCHIP

PIC16F630/676

Data Sheet

14-Pin FLASH-Based 8-Bit

CMOS Microcontrollers

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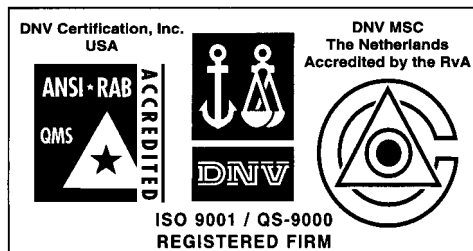
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PIC16F630/676

14-Pin FLASH-Based 8-Bit CMOS Microcontroller

High Performance RISC CPU:

- Only 35 instructions to learn
  - All single cycle instructions except branches
- Operating speed:
  - DC - 20 MHz oscillator/clock input
  - DC - 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect, and Relative Addressing modes

Special Microcontroller Features:

- Internal and external oscillator options
  - Precision Internal 4 MHz oscillator factory calibrated to ±1%
  - External Oscillator support for crystals and resonators
  - 5 μs wake-up from SLEEP, 3.0V, typical
- Power saving SLEEP mode
- Wide operating voltage range - 2.0V to 5.5V
- Industrial and Extended temperature range
- Low power Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Detect (BOD)
- Watchdog Timer (WDT) with independent oscillator for reliable operation
- Multiplexed $\overline{\text{MCLR}}$/Input-pin
- Interrupt-on-pin change
- Individual programmable weak pull-ups
- Programmable code protection
- High Endurance FLASH/EEPROM Cell
  - 100,000 write FLASH endurance
  - 1,000,000 write EEPROM endurance
  - FLASH/Data EEPROM Retention: > 40 years

Low Power Features:

- Standby Current:
  - 1 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current
  - 300 nA @ 2.0V, typical
- Timer1 oscillator current:
  - 4 μA @ 32 kHz, 2.0V, typical

Peripheral Features:

- 12 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
  - One analog comparator
  - Programmable on-chip comparator voltage reference (CV$_{REF}$) module
  - Programmable input multiplexing from device inputs
  - Comparator output is externally accessible
- Analog-to-Digital Converter module (PIC16F676):
  - 10-bit resolution
  - Programmable 8-channel input
  - Voltage reference input
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- In-Circuit Serial Programming™ (ICSP™) via two pins

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit
	FLASH (words)	SRAM (bytes)	EEPROM (bytes)				
PIC16F630	1024	64	128	12		1	1/1
PIC16F676	1024	64	128	12	8	1	1/1

PIC16F630/676

Pin Diagrams

14-pin PDIP, SOIC, TSSOP

PIC16F630

Pin	Signal
1	VDD
2	RA5/T1CKI/OSC1/CLKIN
3	RA4/T1G/OSC2/CLKOUT
4	RA3/MCLR/VPP
5	RC5
6	RC4
7	RC3
14	VSS
13	RA0/CIN+/ICSPDAT
12	RA1/CIN-/ICSPCLK
11	RA2/COUT/T0CKI/INT
10	RC0
9	RC1
8	RC2

PIC16F676

Pin	Signal
1	VDD
2	RA5/T1CKI/OSC1/CLKIN
3	RA4/T1G/OSC2/AN3/CLKOUT
4	RA3/MCLR/VPP
5	RC5
6	RC4
7	RC3/AN7
14	VSS
13	RA0/AN0/CIN+/ICSPDAT
12	RA1/AN1/CIN-/VREF/ICSPCLK
11	RA2/AN2/COUT/T0CKI/INT
10	RC0/AN4
9	RC1/AN5
8	RC2/AN6

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NOTES:

PIC16F630/676

TABLE 1-1: PIC16F630/676 PINOUT DESCRIPTION

| Name	Function	Input Type	Output Type	Description
RA0/AN0/CIN+/ICSPDAT	RA0	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and Interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	CIN+	AN		Comparator input
	ICSPDAT	TTL	CMOS	Serial Programming Data I/O
RA1/AN1/CIN-/VREF/ ICSPCLK	RA1	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and Interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	CIN-	AN	—	Comparator input
	VREF	AN	—	External Voltage reference
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/COUT/T0CKI/INT	RA2	ST	CMOS	Bi-directional I/O w/ programmable pull-up and Interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	COUT	—	CMOS	Comparator output
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	Input port with Interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear
	VPP	HV	—	Programming voltage
RA4/$\overline{\text{T1G}}$/AN3/OSC2/ CLKOUT	RA4	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and Interrupt-on-change
	$\overline{\text{T1G}}$	ST	—	Timer1 gate
	AN3	AN3	—	A/D Channel 3 input
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	F$_{OSC}$/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and Interrupt-on-change
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RC0/AN4	RC0	TTL	CMOS	Bi-directional I/O
	AN4	AN4	—	A/D Channel 4 input
RC1/AN5	RC1	TTL	CMOS	Bi-directional I/O
	AN5	AN5	—	A/D Channel 5 input
RC2/AN6	RC2	TTL	CMOS	Bi-directional I/O
	AN6	AN6	—	A/D Channel 6 input
RC3/AN7	RC3	TTL	CMOS	Bi-directional I/O
	AN7	AN7	—	A/D Channel 7 input
RC4	RC4	TTL	CMOS	Bi-directional I/O
RC5	RC5	TTL	CMOS	Bi-directional I/O
VSS	VSS	Power	—	Ground reference
VDD	VDD	Power	—	Positive supply

Legend: Shade = PIC16F676 only
TTL = TTL input buffer
ST = Schmitt Trigger input buffer

2.0   MEMORY ORGANIZATION

2.1   Program Memory Organization

The PIC16F630/676 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h - 03FFh) for the PIC16F630/676 devices is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 1K x 14 space. The RESET vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1:   PROGRAM MEMORY MAP AND STACK FOR THE PIC16F630/676
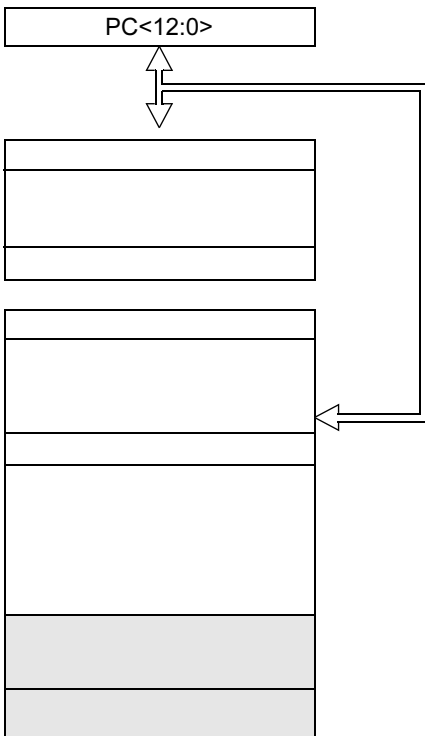
2.2   Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose registers and the Special Function registers. The Special Function registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

• RP0 = 0 Bank 0 is selected
• RP0 = 1 Bank 1 is selected

2.2.1   GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC16F630/676 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4).
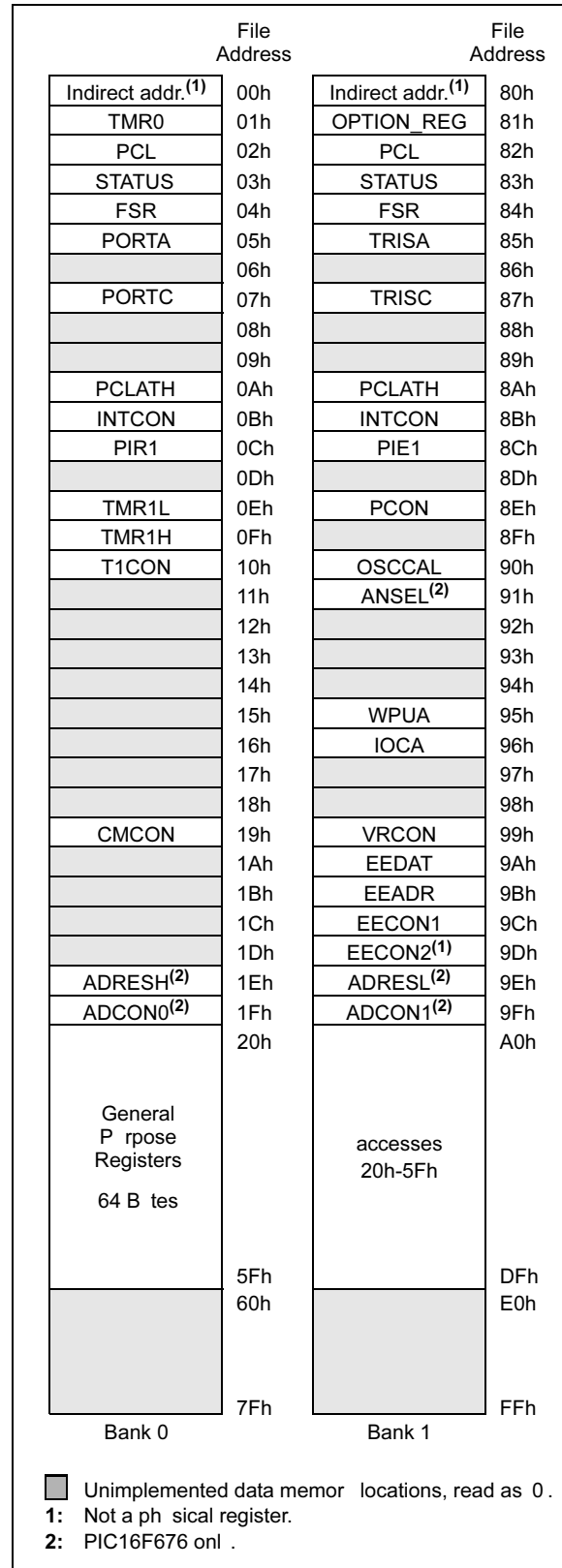
PIC16F630/676

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2:   DATA MEMORY MAP OF THE PIC16F630/676

File Address		File Address	
Indirect addr.[1]	00h	Indirect addr.[1]	80h
TMR0	01h	OPTION_REG	81h
PCL	02h	PCL	82h
STATUS	03h	STATUS	83h
FSR	04h	FSR	84h
PORTA	05h	TRISA	85h
	06h		86h
PORTC	07h	TRISC	87h
	08h		88h
	09h		89h
PCLATH	0Ah	PCLATH	8Ah
INTCON	0Bh	INTCON	8Bh
PIR1	0Ch	PIE1	8Ch
	0Dh		8Dh
TMR1L	0Eh	PCON	8Eh
TMR1H	0Fh		8Fh
T1CON	10h	OSCCAL	90h
	11h	ANSEL[2]	91h
	12h		92h
	13h		93h
	14h		94h
	15h	WPUA	95h
	16h	IOCA	96h
	17h		97h
	18h		98h
CMCON	19h	VRCON	99h
	1Ah	EEDAT	9Ah
	1Bh	EEADR	9Bh
	1Ch	EECON1	9Ch
	1Dh	EECON2[1]	9Dh
ADRESH[2]	1Eh	ADRESL[2]	9Eh
ADCON0[2]	1Fh	ADCON1[2]	9Fh
	20h		A0h
General Purpose Registers 64 Bytes		accesses 20h-5Fh	
	5Fh		DFh
	60h		E0h
	7Fh		FFh
Bank 0		Bank 1	

Unimplemented data memory locations, read as '0'.
1: Not a physical register.
2: PIC16F676 only.

TABLE 2-1: **PIC16F630/676 SPECIAL REGISTERS SUMMARY BANK 0**

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	18,61
01h	TMR0	Timer0 Module's Register								xxxx xxxx	29
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17
03h	STATUS	IRP[2]	RP1[2]	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	11
04h	FSR	Indirect data memory address pointer								xxxx xxxx	18
05h	PORTA	—	—	I/O Control Registers						--xx xxxx	19
06h	—	Unimplemented								—	—
07h	PORTC	—	—	I/O Control Registers						--xx xxxx	26
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	17
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	13
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	15
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	32
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	32
10h	T1CON	—	T1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	-000 0000	34
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	—	Unimplemented								—	—
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	37
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH[3]	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	44
1Fh	ADCON0[3]	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	00-0 0000	45,61

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

2: IRP & RP1 bits are reserved, always maintain these bits clear.

3: PIC16F676 only.

TABLE 2-2: PIC16F630/676 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	18,61
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	12,30
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17
83h	STATUS	IRP[2]	RP1[2]	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	11
84h	FSR	Indirect data memory address pointer								xxxx xxxx	18
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	19
86h	—	Unimplemented								—	—
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	17
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	13
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0	14
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOD}$	---- --qq	16
8Fh	—									—	—
90h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	16
91h	ANSEL[3]	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	46
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	WPUA	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	20
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	21
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	42
9Ah	EEDAT	EEPROM data register								0000 0000	49
9Bh	EEADR	—	EEPROM address register							0000 0000	49
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	50
9Dh	EECON2	EEPROM control register 2 (not a physical register)								---- ----	49
9Eh	ADRESL[3]	Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result								xxxx xxxx	44
9Fh	ADCON1[3]	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	45,61

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.
    2: IRP & RP1 bits are reserved, always maintain these bits clear.
    3: PIC16F676 only.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

• the arithmetic status of the ALU
• the RESET status
• the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any STATUS bits. For other instructions not affecting any STATUS bits, see the "Instruction Set Summary".

> **Note 1:** Bits IRP and RP1 (STATUS<7:6>) are not used by the PIC16F630/676 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
>
> **2:** The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1: STATUS — STATUS REGISTER (ADDRESS: 03h OR 83h)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C

bit 7   bit 0

bit 7   **IRP:** This bit is reserved and should be maintained as '0'

bit 6   **RP1:** This bit is reserved and should be maintained as '0'

bit 5   **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h - FFh)
0 = Bank 0 (00h - 7Fh)

bit 4   **$\overline{\text{TO}}$:** Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3   **$\overline{\text{PD}}$:** Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2   **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1   **DC:** Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
For borrow, the polarity is reversed.
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0   **C:** Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

> **Note:** For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC16F630/676

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- TMR0/WDT prescaler
- External RA2/INT interrupt
- TMR0
- Weak pull-ups on PORTA

Note:	To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' (OPTION<3>). See Section 4.4.

REGISTER 2-2:   OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7   **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual port latch values

bit 6   **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/INT pin
0 = Interrupt on falling edge of RA2/INT pin

bit 5   **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4   **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/T0CKI pin
0 = Increment on low-to-high transition on RA2/T0CKI pin

bit 3   **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0   **PS2:PS0:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

> **Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON — INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh OR 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF

bit 7   bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RA2/INT External Interrupt Enable bit
1 = Enables the RA2/INT external interrupt
0 = Disables the RA2/INT external interrupt

bit 3 **RAIE:** Port Change Interrupt Enable bit[1]
1 = Enables the PORTA change interrupt
0 = Disables the PORTA change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit[2]
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RA2/INT External Interrupt Flag bit
1 = The RA2/INT external interrupt occurred (must be cleared in software)
0 = The RA2/INT external interrupt did not occur

bit 0 **RAIF:** Port Change Interrupt Flag bit
1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software)
0 = None of the PORTA <5:0> pins have changed state

Note 1: IOCA register must also be enabled.

2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on RESET and should be initialized before clearing T0IF bit.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

> **Note:** Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1 — PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS: 8Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
EEIE	ADIE	—	—	CMIE	—	—	TMR1IE
bit 7							bit 0

bit 7   **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6   **ADIE:** A/D Converter Interrupt Enable bit (PIC16F676 only)
1 = Enables the A/D converter interrupt
0 = Disables the A/D converter interrupt

bit 5-4   **Unimplemented:** Read as '0'

bit 3   **CMIE:** Comparator Interrupt Enable bit
1 = Enables the comparator interrupt
0 = Disables the comparator interrupt

bit 2-1   **Unimplemented:** Read as '0'

bit 0   **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: **PIR1 — PERIPHERAL INTERRUPT REGISTER 1 (ADDRESS: 0Ch)**

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
EEIF	ADIF	—	—	CMIF	—	—	TMR1IF
bit 7							bit 0

bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started

bit 6 **ADIF:** A/D Converter Interrupt Flag bit (PIC16F676 only)
1 = The A/D conversion is complete (must be cleared in software)
0 = The A/D conversion is not complete

bit 5-4 **Unimplemented**: Read as '0'

bit 3 **CMIF**: Comparator Interrupt Flag bit
1 = Comparator input has changed (must be cleared in software)
0 = Comparator input has not changed

bit 2-1 **Unimplemented**: Read as '0'

bit 0 **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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2.2.2.6 PCON Register

The Power Control (PCON) register contains flag bits
to differentiate between a:

- Power-on Reset (POR)
- Brown-out Detect (BOD)
- Watchdog Timer Reset (WDT)
- External $\overline{\text{MCLR}}$ Reset

The PCON Register bits are shown in Register 2-6.

REGISTER 2-6:   PCON — POWER CONTROL REGISTER (ADDRESS: 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-x
—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOD}}$

bit 7   bit 0

bit 7-2	**Unimplemented:** Read as '0'
bit 1	**$\overline{\text{POR}}$:** Power-on Reset STATUS bit
	`1` = No Power-on Reset occurred
	`0` = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
bit 0	**$\overline{\text{BOD}}$:** Brown-out Detect STATUS bit
	`1` = No Brown-out Detect occurred
	`0` = A Brown-out Detect occurred (must be set in software after a Brown-out Detect occurs)

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.2.2.7 OSCCAL Register

The Oscillator Calibration register (OSCCAL) is used to
calibrate the internal 4 MHz oscillator. It contains 6 bits
to adjust the frequency up or down to achieve 4 MHz.

The OSCCAL register bits are shown in Register 2-7.

REGISTER 2-7:   OSCCAL — INTERNAL OSCILLATOR CALIBRATION REGISTER (ADDRESS: 90h)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—

bit 7   bit 0

bit 7-2	**CAL5:CAL0:** 6-bit Signed Oscillator Calibration bits
	`111111` = Maximum frequency
	`100000` = Center frequency
	`000000` = Minimum frequency
bit 1-0	**Unimplemented:** Read as '0'

| Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: **LOADING OF PC IN DIFFERENT SITUATIONS**
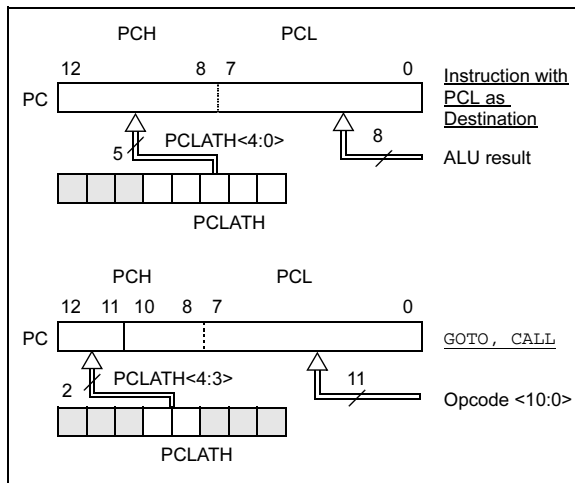
2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note *"Implementing a Table Read"* (AN556).

2.3.2 STACK

The PIC16F630/676 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

> **Note 1:** There are no STATUS bits to indicate stack overflow or stack underflow conditions.
>
> **2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although STATUS bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
         movlw   0x20   ;initialize pointer
         movwf   FSR    ;to RAM
NEXT     clrf    INDF   ;clear INDF register
         incf    FSR    ;inc pointer
         btfss   FSR,4  ;all done?
         goto    NEXT   ;no clear next
CONTINUE                ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F630/676

For memor map detail see Fig re 2-2.

Note 1: The RP1 and IRP bits are reser ed; al a s maintain these bits clear.

PIC16F630/676
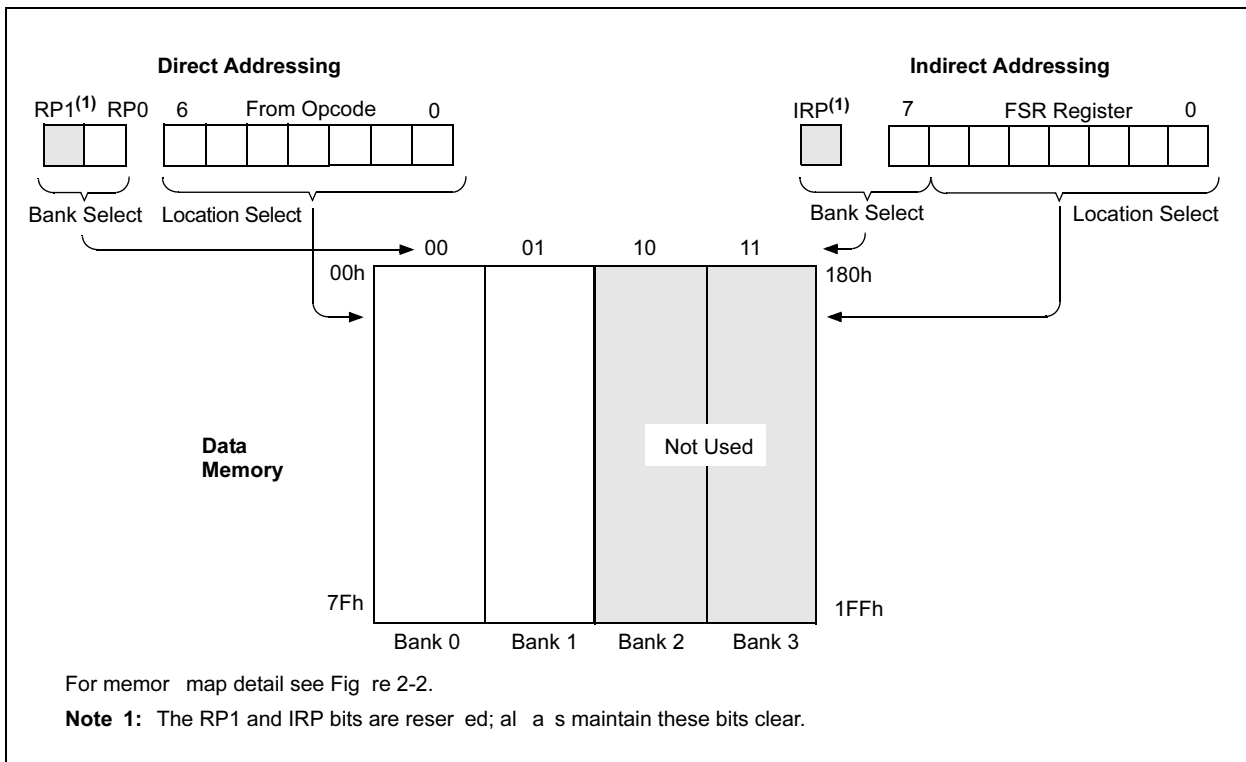
3.0 PORTS A AND C

There are as many as twelve general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

> **Note:** Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023)

3.1 PORTA and the TRISA Registers

PORTA is an 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 3-1 shows how to initialize PORTA.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch. RA3 reads '0' when MCLREN = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA

register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

> **Note:** The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

EXAMPLE 3-1: INITIALIZING PORTA

```
bcf     STATUS,RP0   ;Bank 0
clrf    PORTA        ;Init PORTA
movlw   05h          ;Set RA<2:0> to
movwf   CMCON        ;digital I/O
bsf     STATUS,RP0   ;Bank 1
clrf    ANSEL        ;digital I/O
movlw   0Ch          ;Set RA<3:2> as inputs
movwf   TRISA        ;and set RA<5:4,1:0>
                     ;as outputs
bcf     STATUS,RP0   ;Bank 0
```

3.2 Additional Pin Functions

Every PORTA pin on the PIC16F630/676 has an interrupt-on-change option and every PORTA pin, except RA3, has a weak pull-up option. The next two sections describe these functions.

3.2.1 WEAK PULL-UP

Each of the PORTA pins, except RA3, has an individually configurable weak internal pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 3-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{RAPU}$ bit (OPTION<7>).

REGISTER 3-1: PORTA — PORTA REGISTER (ADDRESS: 05h)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0

bit 7   bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5-0: **PORTA<5:0>**: PORTA I/O pin

1 = Port pin is >V_{IH}
0 = Port pin is <V_{IL}

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 3-2: **TRISA — PORTA TRISTATE REGISTER (ADDRESS: 85h)**

U-0	U-0	R/W-x	R/W-x	R-1	R/W-x	R/W-x	R/W-x
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0

bit 7   bit 0

bit 7-6:   **Unimplemented**: Read as '0'

bit 5-0:   **TRISA<5:0>**: PORTA Tri-State Control bit

                 1 = PORTA pin configured as an input (tri-stated)

                 0 = PORTA pin configured as an output

          Note: TRISA<3> always reads 1.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 3-3: **WPUA — WEAK PULL-UP REGISTER (ADDRESS: 95h)**

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0

bit 7   bit 0

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **WPUA<5:4>:** Weak Pull-up Register bit

                 1 = Pull-up enabled

                 0 = Pull-up disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **WPUA<2:0>:** Weak Pull-up Register bit

                 1 = Pull-up enabled

                 0 = Pull-up disabled

          Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.

                  2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

3.2.2 INTERRUPT-ON-CHANGE

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCAx enable or disable the interrupt function for each pin. Refer to Register 3-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt flag bit (RAIF) in the INTCON register.

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTA. This will end the mismatch condition.

b) Clear the flag bit RAIF.

A mismatch condition will continue to set flag bit RAIF. Reading PORTA will end the mismatch condition and allow flag bit RAIF to be cleared.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

REGISTER 3-4: **IOCA — INTERRUPT-ON-CHANGE PORTA REGISTER (ADDRESS: 96h)**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0

bit 7   bit 0

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **IOCA<5:0>:** Interrupt-on-Change PORTA Control bit
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note: Global interrupt enable (GIE) must be enabled for individual interrupts to be recognized.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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3.2.3 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this Data Sheet.
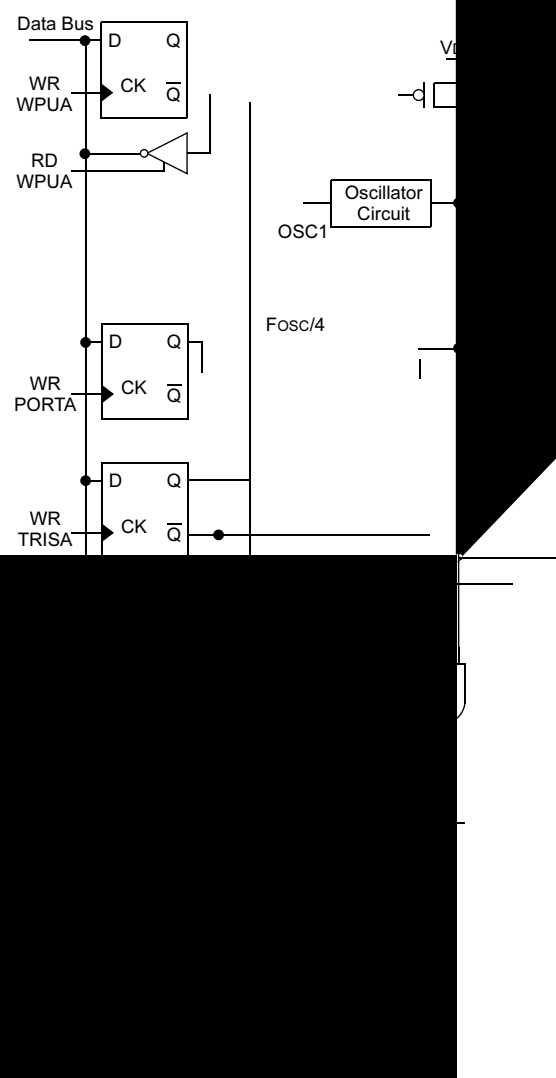
3.2.3.1 RA0/AN0/CIN+

Figure 3-1 shows the diagram for this pin. The RA0 pin is configurable to function as one of the following:

• a general purpose I/O
• an analog input for the A/D (PIC16F676 only)
• an analog input to the comparator

3.2.3.2 RA1/AN1/CIN-/VREF

Figure 3-1 shows the diagram for this pin. The RA1 pin is configurable to function as one of the following:

• as a general purpose I/O
• an analog input for the A/D (PIC16F676 only)
• an analog input to the comparator
• a voltage reference input for the A/D (PIC16F676 only)

FIGURE 3-1: **BLOCK DIAGRAM OF RA0 AND RA1 PINS**
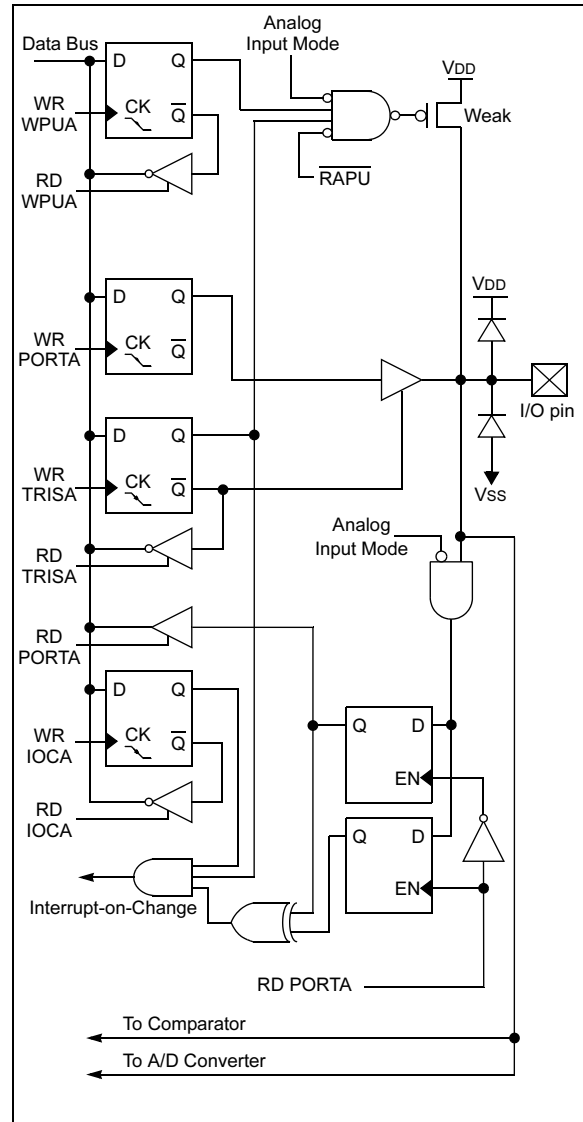
3.2.3.3 RA2/AN2/T0CKI/INT/COUT

Figure 3-2 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D (PIC16F676 only)
- a digital output from the comparator
- the clock input for TMR0
- an external edge triggered interrupt

FIGURE 3-2:   BLOCK DIAGRAM OF RA2
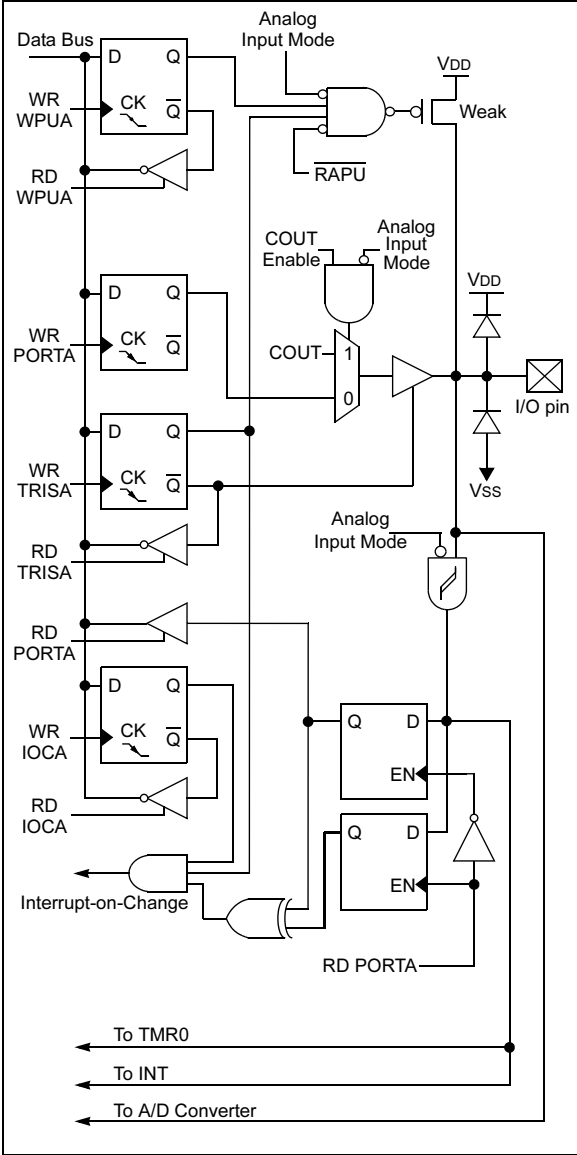
3.2.3.4   RA3/$\overline{\text{MCLR}}$/VPP

Figure 3-3 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset

FIGURE 3-3:   BLOCK DIAGRAM OF RA3
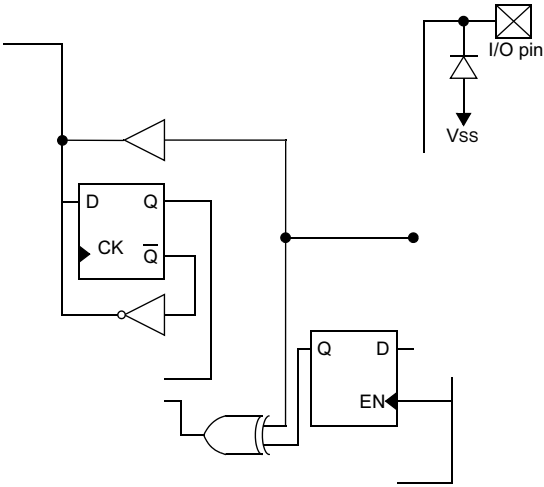
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3.2.3.5 RA4/AN3/$\overline{T1G}$/OSC2/CLK...

Figure 3-4 shows the diagram for this pin. T...
is configurable to function as one of the fol...

- a general purpose I/O
- an analog input for the A/D (PIC16F676...
- a TMR1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 3-4: BLOCK DIAGRA...

RA5/T1CKI/OSC1/CLKIN

...shows the diagram for this pin. The RA5 pin
...able to function as one of the following:

- ...l purpose I/O
- ...clock input
- ...resonator connection
- ...put

...-5: BLOCK DIAGRAM OF RA5

TABLE 3-1: **SUMMARY OF REGISTERS ASSOCIATED WITH PORTA**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other RESETS
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 000u
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
91h	ANSEL[1]	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
95h	WPUA	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000

Note 1: PIC16F676 onl .

Legend: x = nkno n, u = nchanged, – = nimplemented locations read as 0 . Shaded cells are not sed b PORTA.

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3.3 PORTC

PORTC is a general purpose I/O port consisting of 6 bi-directional pins. The pins can be configured for either digital I/O or analog input to A/D converter. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this Data Sheet.

> **Note:** The ANSEL register (9Fh) must be clear to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

EXAMPLE 3-2: INITIALIZING PORTC

```
bcf     STATUS,RP0      ;Bank 0
clrf    PORTC           ;Init PORTC
bsf     STATUS,RP0      ;Bank 1
clrf    ANSEL           ;digital I/O
movlw   0Ch             ;Set RC<3:2> as inputs
movwf   TRISC           ;and set RC<5:4,1:0>
                        ;as outputs
bcf     STATUS,RP0      ;Bank 0
```

3.3.1 RC0/AN4, RC1/AN5, RC2/AN6, RC3/AN7

The RC0/RC1/RC2/RC3 pins are configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D Converter (PIC16F676 only)

FIGURE 3-6: BLOCK DIAGRAM OF RC0/RC1/RC2/RC3 PINs
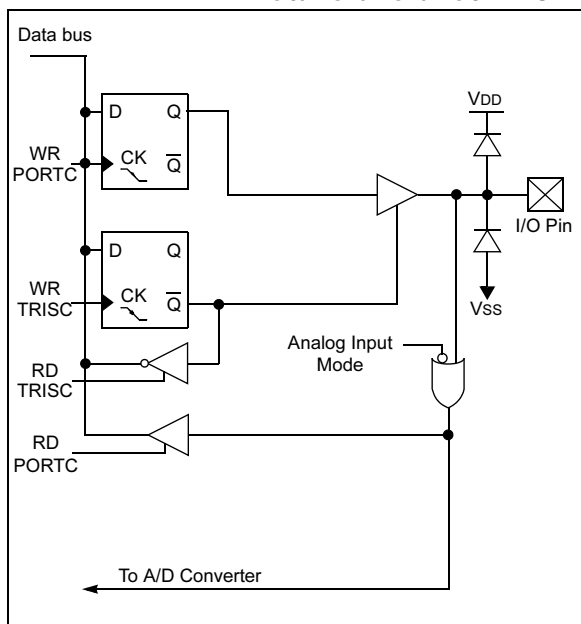
3.3.2 RC4 AND RC5

The RC4 and RC5 pins are configurable to function as a general purpose I/Os.

FIGURE 3-7: BLOCK DIAGRAM OF RC4 AND RC5 PINS
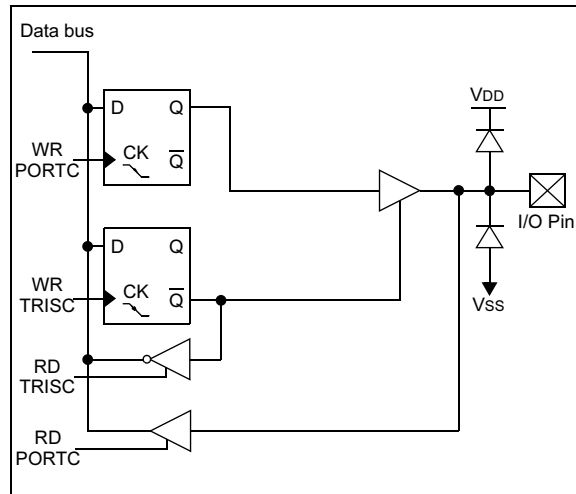
REGISTER 3-5: **PORTC — PORTC REGISTER (ADDRESS: 07h)**

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	RC5	RC4	RC3	RC2	RC1	RC0

bit 7   bit 0

bit 7-6:   **Unimplemented**: Read as '0'

bit 5-0:   **PORTC<5:0>**: General Purpose I/O pin

1 = Port pin is >V_{IH}
0 = Port pin is <V_{IL}

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 3-6: **TRISC — PORTC TRISTATE REGISTER (ADDRESS: 87h)**

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0

bit 7   bit 0

bit 7-6:   **Unimplemented**: Read as '0'

bit 5-0:   **TRISC<5:0>**: PORTC Tri-State Control bit

1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

TABLE 3-2: **SUMMARY OF REGISTERS ASSOCIATED WITH PORTC**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other RESETS
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
91h	ANSEL[1]	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111

Note 1: PIC16F676 onl .

Legend: x = unknown, u = nchanged, – = nimplemented locations read as 0 . Shaded cells are not sed b PORTC.

NOTES:

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 4-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

> **Note:** Additional information on the Timer0 module is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin RA2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

> **Note:** Counter mode has specific external clock requirements. Additional information on these requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut-off during SLEEP.

FIGURE 4-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

Note 1: T0SE, T0CS, PSA, PS0-PS2 are bits in the Option register.
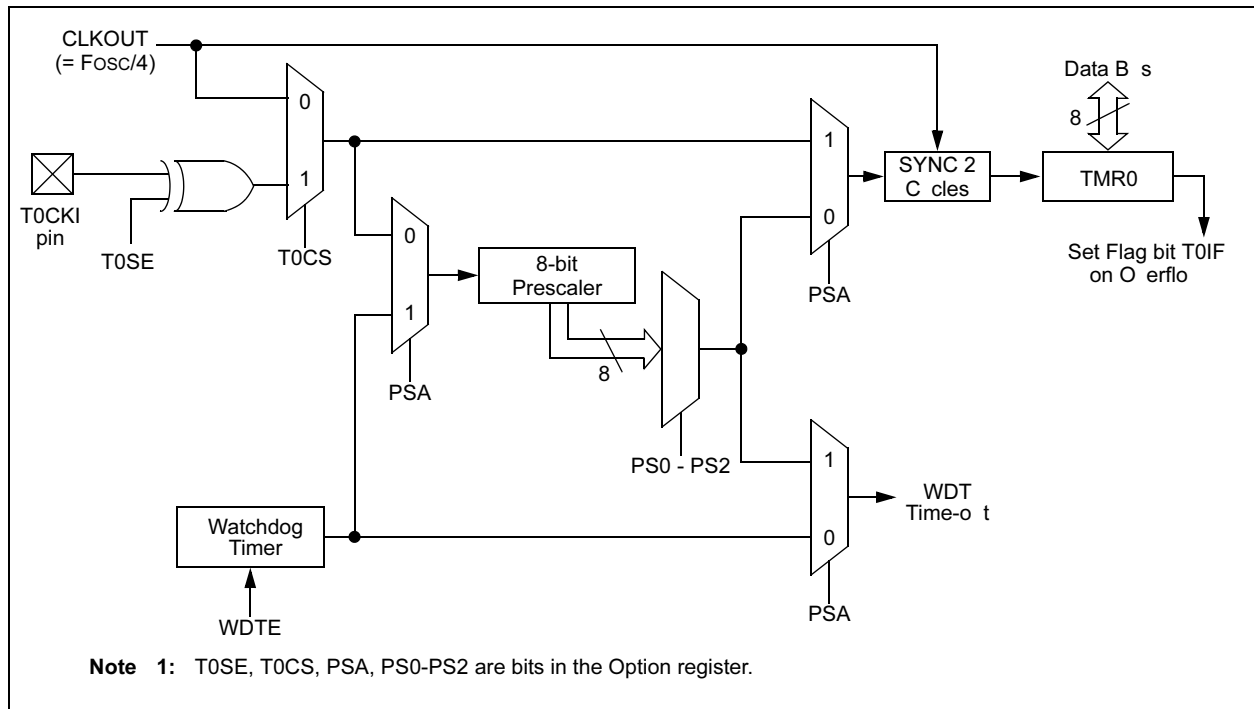
4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and

a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

> **Note:** The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

REGISTER 4-1:   OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

bit 7   bit 0

bit 7   **RAPU:** PORTA Pull-up Enable bit
          1 = PORTA pull-ups are disabled
          0 = PORTA pull-ups are enabled by individual port latch values

bit 6   **INTEDG:** Interrupt Edge Select bit
          1 = Interrupt on rising edge of RA2/INT pin
          0 = Interrupt on falling edge of RA2/INT pin

bit 5   **T0CS:** TMR0 Clock Source Select bit
          1 = Transition on RA2/T0CKI pin
          0 = Internal instruction cycle clock (CLKOUT)

bit 4   **T0SE:** TMR0 Source Edge Select bit
          1 = Increment on high-to-low transition on RA2/T0CKI pin
          0 = Increment on low-to-high transition on RA2/T0CKI pin

bit 3   **PSA:** Prescaler Assignment bit
          1 = Prescaler is assigned to the WDT
          0 = Prescaler is assigned to the Timer0 module

bit 2-0   **PS2:PS0:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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## 5.0 TIMER1 MODULE WITH GATE CONTROL

The PIC16F630/676 devices have a 16-bit timer. Figure 5-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input ($\overline{\text{T1G}}$)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 5-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note:	Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

FIGURE 5-1: TIMER1 BLOCK DIAGRAM
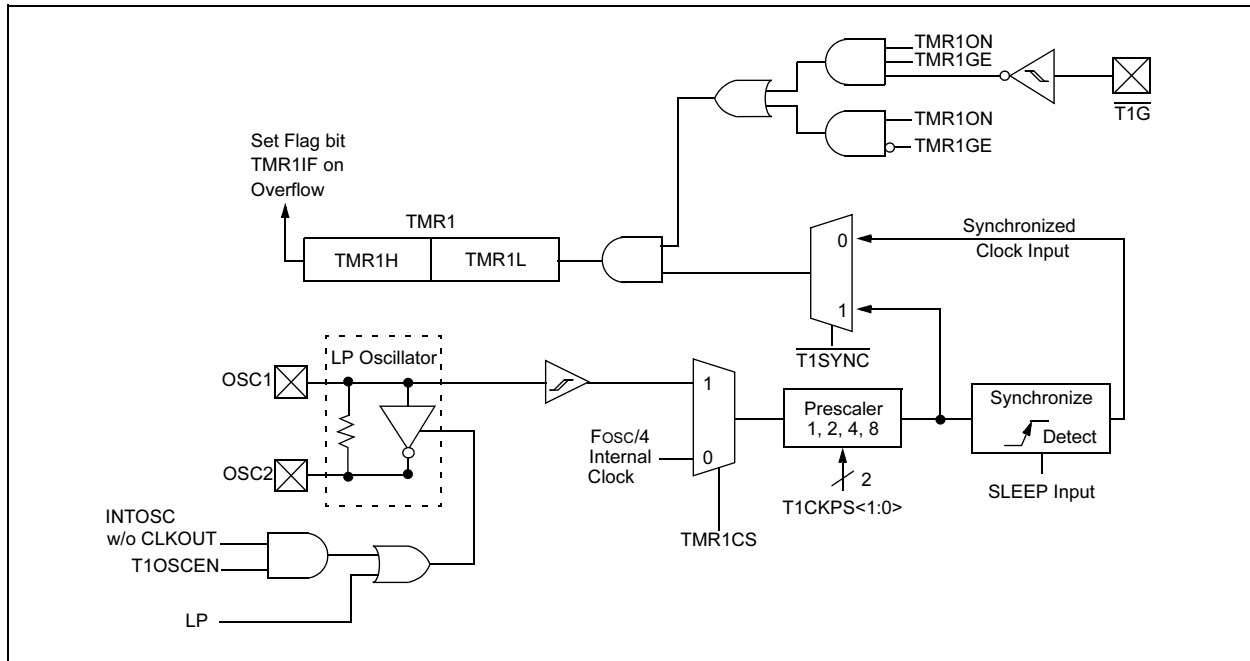
5.1 Timer1 Modes of Operation

Timer1 can operate in one of three modes:

• 16-bit timer with prescaler
• 16-bit synchronous counter
• 16-bit asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the T1G input.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

> **Note:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

5.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (PIR1<0>) is set. To enable the interrupt on rollover, you must set these bits:

• Timer1 interrupt Enable bit (PIE1<0>)
• PEIE bit (INTCON<6>)
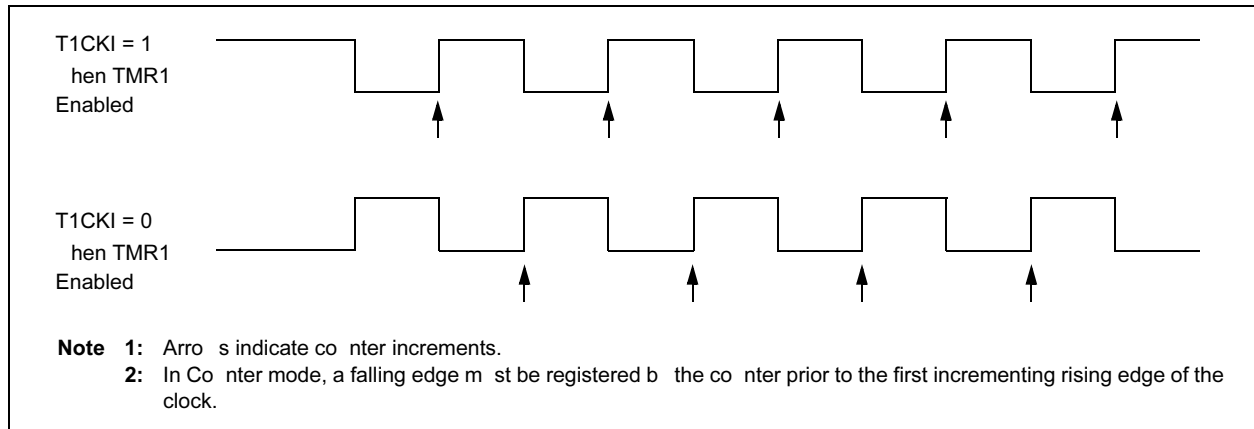• GIE bit (INTCON<7>).

The interrupt is cleared by clearing the TMR1IF in the Interrupt Service Routine.

> **Note:** The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

5.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4, or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

FIGURE 5-2: **TIMER1 INCREMENTING EDGE**

T1CKI = 1
 hen TMR1
Enabled

T1CKI = 0
 hen TMR1
Enabled

Note 1: Arro s indicate co nter increments.
2: In Co nter mode, a falling edge m st be registered b the co nter prior to the first incrementing rising edge of the clock.

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REGISTER 5-1: T1CON — TIMER1 CONTROL REGISTER (ADDRESS: 10h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON

bit 7   bit 0

bit 7   **Unimplemented:** Read as '0'

bit 6   **TMR1GE:** Timer1 Gate Enable bit
<u>If TMR1ON = 0:</u>
This bit is ignored
<u>If TMR1ON = 1:</u>
1 = Timer1 is on if $\overline{\text{T1G}}$ pin is low
0 = Timer1 is on

bit 5-4   **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3   **T1OSCEN:** LP Oscillator Enable Control bit
<u>If INTOSC without CLKOUT oscillator is active:</u>
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
<u>Else:</u>
This bit is ignored

bit 2   **T1SYNC:** Timer1 External Clock Input Synchronization Control bit
<u>TMR1CS = 1:</u>
1 = Do not synchronize external clock input
0 = Synchronize external clock input
<u>TMR1CS = 0:</u>
This bit is ignored. Timer1 uses the internal clock.

bit 1   **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1OSO/T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0   **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5.4 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 5.4.1).

> **Note:** The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

5.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples 12-2 and 12-3 in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

5.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 32 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 9-2 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

TRISA5 and TRISA4 bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as '0' and TRISA5 and TRISA4 bits read as '1'.

> **Note:** The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

5.6 Timer1 Operation During SLEEP

Timer1 can only operate during SLEEP when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

• Timer1 must be on (T1CON<0>)
• TMR1IE bit (PIE1<0>) must be set
• PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine on an overflow.

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 000x
0Ch	PIR1	EEIF	ADIF			CMIF			TMR1IF	00-- 0--0	00-- 0--0
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register									xxxx xxxx
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register									xxxx xxxx
10h	T1CON		TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	-000 0000	-uuu uuuu
8Ch	PIE1	EEIE	ADIE			CMIE			TMR1IE	00-- 0--0	00-- 0--0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

NOTES:

6.0 COMPARATOR MODULE

The PIC16F630/676 devices have one analog comparator. The inputs to the comparator are multiplexed with the RA0 and RA1 pins. There is an on-chip Comparator Voltage Reference that can also be applied to an input of the comparator. In addition, RA2 can be configured as the comparator output. The Comparator Control Register (CMCON), shown in Register 6-1, contains the bits to control the comparator.

REGISTER 6-1: **CMCON — COMPARATOR CONTROL REGISTER (ADDRESS: 19h)**

U-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COUT	—	CINV	CIS	CM2	CM1	CM0

bit 7   bit 0

bit 7   **Unimplemented**: Read as '0'

bit 6   **COUT**: Comparator Output bit
<u>When CINV = 0:</u>
1 = V_{IN+} > V_{IN-}
0 = V_{IN+} < V_{IN-}
<u>When CINV = 1:</u>
1 = V_{IN+} < V_{IN-}
0 = V_{IN+} > V_{IN-}

bit 5   **Unimplemented**: Read as '0'

bit 4   **CINV**: Comparator Output Inversion bit
1 = Output inverted
0 = Output not inverted

bit 3   **CIS**: Comparator Input Switch bit
<u>When CM2:CM0 = 110 or 101:</u>
1 = V_{IN-} connects to CIN+
0 = V_{IN-} connects to CIN-

bit 2-0   **CM2:CM0**: Comparator Mode bits
Figure 6-2 shows the Comparator modes and CM2:CM0 bit settings

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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6.1 Comparator Operation

A single comparator is shown in Figure 6-1, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN}+ is less than the analog input V_{IN}-, the output of the comparator is a digital low level. When the analog input at V_{IN}+ is greater than the analog input V_{IN}-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 6-1 represent the uncertainty due to input offsets and response time.

Note:	To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be programmed in the CMCON (19h) register.

The polarity of the comparator output can be inverted by setting the CINV bit (CMCON<4>). Clearing CINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 6-1.

TABLE 6-1: OUTPUT STATE VS. INPUT CONDITIONS

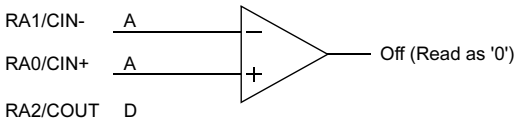| Input Conditions	CINV	COUT
V_{IN}- > V_{IN}+	0	0
V_{IN}- < V_{IN}+	0	1
V_{IN}- > V_{IN}+	1	1
V_{IN}- < V_{IN}+	1	0

FIGURE 6-1: SINGLE COMPARATOR

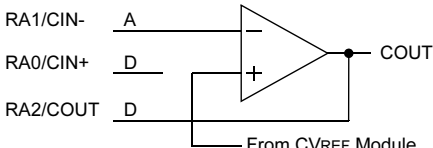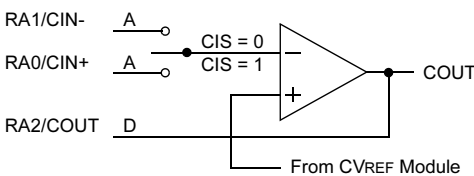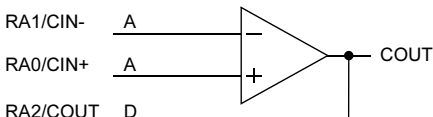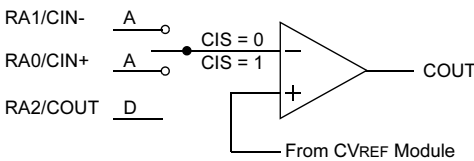| **Note:**	CINV bit (CMCON<4>) is clear.
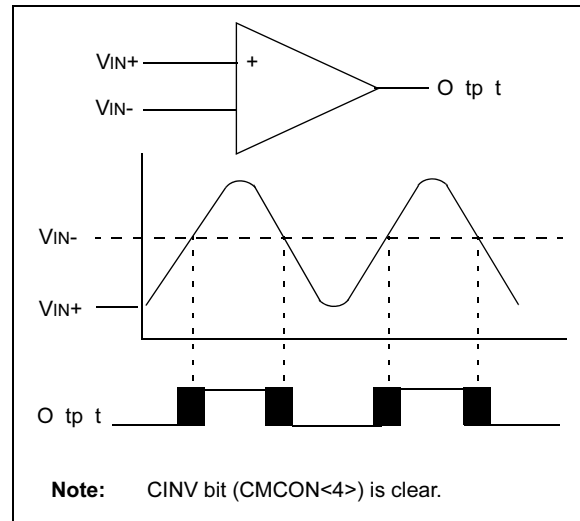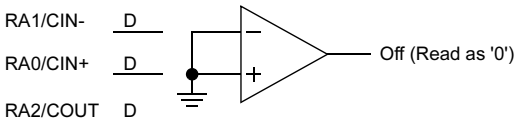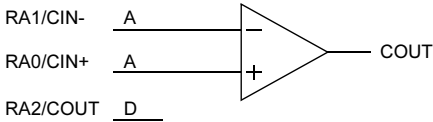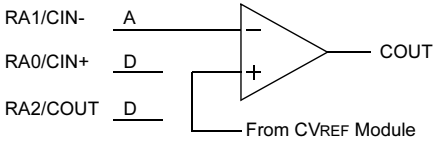
6.2   Comparator Configuration

There are eight modes of operation for the comparator. The CMCON register, shown in Register 6-1, is used to select the mode. Figure 6-2 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the

Comparator mode is changed, the comparator output level may not be valid for a specified period of time. Refer to the specifications in Section 12.0.

> **Note:** Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

FIGURE 6-2:   COMPARATOR I/O OPERATING MODES

Comparator Reset (POR Default Value - low power)
CM2:CM0 = 000

Comparator Off (Lowest power)
CM2:CM0 = 111

Comparator without Output
CM2:CM0 = 010

Comparator w/o Output and with Internal Reference
CM2:CM0 = 100

Comparator with Output and Internal Reference
CM2:CM0 = 011

Multiplexed Input with Internal Reference and Output
CM2:CM0 = 101

Comparator with Output
CM2:CM0 = 001

Multiplexed Input with Internal Reference
CM2:CM0 = 110

A = Analog Input, ports always reads '0'

D = Digital Input

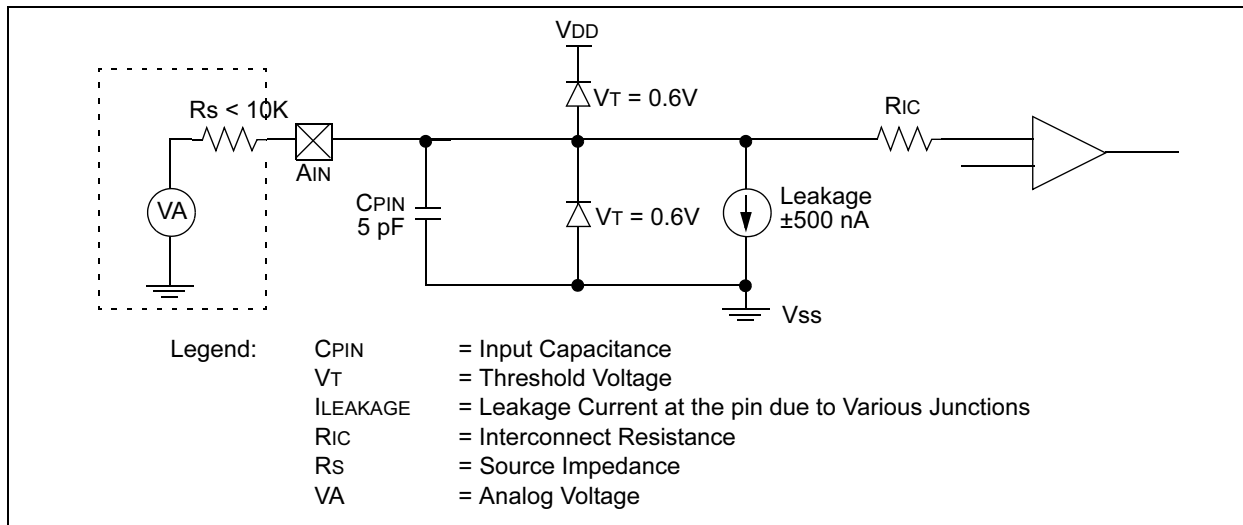CIS = Comparator Input Switch (CMCON<3>)

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6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to V_{DD} and V_{SS}. The analog input, therefore, must be between V_{SS} and V_{DD}. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 6-3: ANALOG INPUT MODE

Legend:
	C_{PIN}	= Input Capacitance
	V_T	= Threshold Voltage
	$I_{LEAKAGE}$	= Leakage Current at the pin due to Various Junctions
	R_{IC}	= Interconnect Resistance
	R_S	= Source Impedance
	V_A	= Analog Voltage

6.4 Comparator Output

The comparator output, COUT, is read through the CMCON register. This bit is read-only. The comparator output may also be directly output to the RA2 pin in three of the eight possible modes, as shown in Figure 6-2. When in one of these modes, the output on RA2 is asynchronous to the internal clock. Figure 6-4 shows the comparator output block diagram.

The TRISA<2> bit functions as an output enable/disable for the RA2 pin while the comparator is in an Output mode.

> **Note 1:** When reading the PORTA register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the TTL input specification.
>
> **2:** Analog levels on any pin that is defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 6-4: MODIFIED COMPARATOR OUTPUT BLOCK DIAGRAM
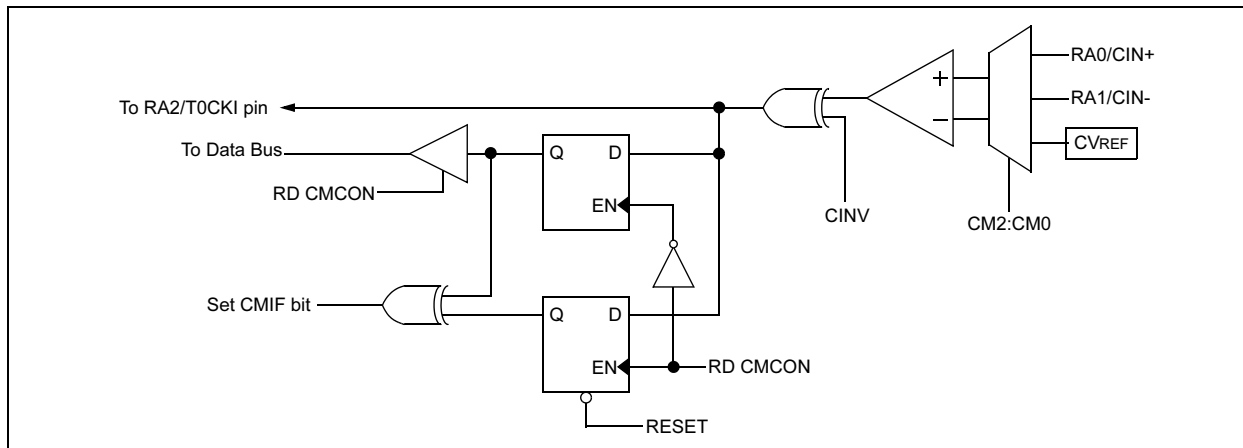
6.5 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for four of the eight Comparator modes. The VRCON register, Register 6-2, controls the voltage reference module shown in Figure 6-5.

6.5.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equations determine the output voltages:

$$VRR = 1 \text{ (low range): } CV_{REF} = (VR3:VR0 / 24) \text{ x } V_{DD}$$

$$VRR = 0 \text{ (high range): } CV_{REF} = (V_{DD} / 4) + (VR3:VR0 \text{ x } V_{DD} / 32)$$

6.5.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of V_{SS} to V_{DD} cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 6-5) keep CV_{REF} from approaching V_{SS} or V_{DD}. The Voltage Reference is V_{DD} derived and therefore, the CV_{REF} output changes with fluctuations in V_{DD}. The tested absolute accuracy of the Comparator Voltage Reference can be found in Section 12.0.

FIGURE 6-5: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM
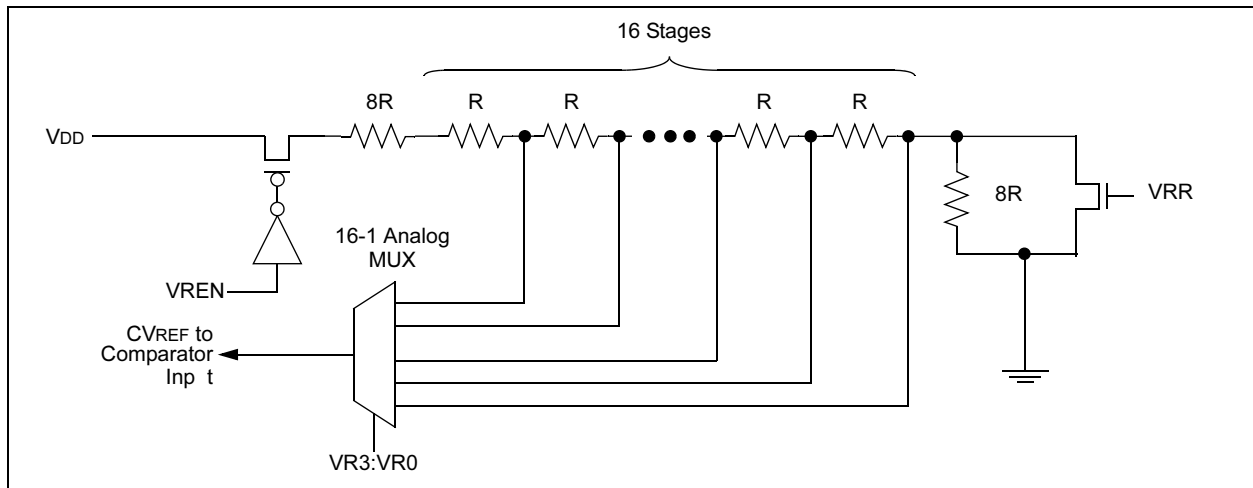
6.6 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 12-7).

6.7 Operation During SLEEP

Both the comparator and voltage reference, if enabled before entering SLEEP mode, remain active during SLEEP. This results in higher SLEEP currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in SLEEP mode, turn off the comparator, CM2:CM0 = 111, and voltage reference, VRCON<7> = 0.

While the comparator is enabled during SLEEP, an interrupt will wake-up the device. If the device wakes up from SLEEP, the contents of the CMCON and VRCON registers are not affected.

6.8 Effects of a RESET

A device RESET forces the CMCON and VRCON registers to their RESET states. This forces the comparator module to be in the Comparator Reset mode, CM2:CM0 = 000 and the voltage reference to its off state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.

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REGISTER 6-2: **VRCON — VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS: 99h)**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	—	VRR	—	VR3	VR2	VR1	VR0

bit 7   bit 0

bit 7   **VREN:** CV_{REF} Enable bit
                     1 = CV_{REF} circuit powered on
                     0 = CV_{REF} circuit powered down, no I_{DD} drain

bit 6   **Unimplemented:** Read as '0'

bit 5   **VRR:** CV_{REF} Range Selection bit
                     1 = Low range
                     0 = High range

bit 4   **Unimplemented:** Read as '0'

bit 3-0   **VR3:VR0:** CV_{REF} value selection $0 \leq VR [3:0] \leq 15$
                     When VRR = 1: CV_{REF} = (VR3:VR0 / 24) * V_{DD}
                     When VRR = 0: CV_{REF} = V_{DD}/4 + (VR3:VR0 / 32) * V_{DD}

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

6.9 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<6>, to determine the actual change that has occurred. The CMIF bit, PIR1<3>, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<3>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON. This will end the mismatch condition.

b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition and allow flag bit CMIF to be cleared.

> **Note:** If a change in the CMCON register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<3>) interrupt flag may not get set.

TABLE 6-2: **REGISTERS ASSOCIATED WITH COMPARATOR MODULE**

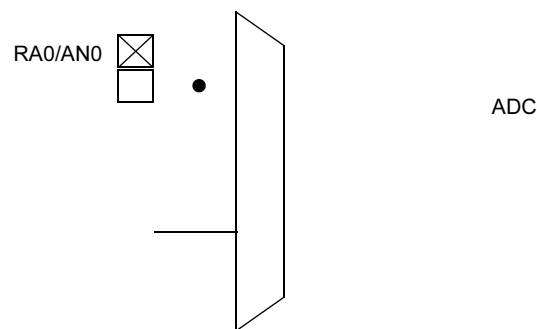| Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 000.
0Ch	PIR1	EEIF	ADIF			CMIF			TMR1IF	00-- 0--0	00-- 0--0
19h	CMCON		COUT		CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
8Ch	PIE1	EEIE	ADIE			CMIE			TMR1IE	00-- 0--0	00-- 0--0
85h	TRISA			TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
99h	VRCON	VREN		VRR		VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000

Legend: = nkno n,   = nchanged, - = nimplemented, read as '0'. Shaded cells are not sed b the comparator mod le.

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE (PIC16F676 ONLY)

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC16F676 has eight analog inputs, multiplexed into one sample and hold circuit.

FIGURE 7-1: A/D BLOCK DIAGRAM

The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 7-1 shows the block diagram of the A/D on the PIC16F676.

7.1 A/D Configuration and Operation

There are three registers available to control the functionality of the A/D module:

1. ADCON0 (Register 7-1)
2. ADCON1 (Register 7-2)
3. ANSEL (Register 7-3)

7.1.1 ANALOG PORT PINS

The ANS7:ANS0 bits (ANSEL<7:0>) and the TRISA bits control the operation of the A/D port pins. Set the corresponding TRISA bits to set the pin output driver to its high impedance state. Likewise, set the corresponding ANS bit to disable the digital input buffer.

7.1.2 CHANNEL SELECTION

There are eight analog channels on the PIC16F676, AN0 through AN7. The CHS2:CHS0 bits (ADCON0<4:2>) control which channel is connected to the sample and hold circuit.

7.1.3 VOLTAGE REFERENCE

There are two options for the voltage reference to the A/D converter: either VDD is used, or an analog voltage applied to VREF is used. The VCFG bit (ADCON0<6>) controls the voltage reference selection. If VCFG is set, then the voltage on the VREF pin is the reference; otherwise, VDD is the reference.

7.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ADCON1<6:4>). There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of 1.6 µs. Table 7-1 shows a few TAD calculations for selected frequencies.

PIC16F630/676

TABLE 7-1: T_{AD} vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (T_{AD})		Device Frequency			
Operation	ADCS2:ADCS0	20 MHz	5 MHz	4 MHz	1.25 MHz
2 T_{OSC}	000	100 ns[2]	400 ns[2]	500 ns[2]	1.6 μs
4 T_{OSC}	100	200 ns[2]	800 ns[2]	1.0 μs[2]	3.2 μs
8 T_{OSC}	001	400 ns[2]	1.6 μs	2.0 μs	6.4 μs
16 T_{OSC}	101	800 ns[2]	3.2 μs	4.0 μs	12.8 μs[3]
32 T_{OSC}	010	1.6 μs	6.4 μs	8.0 μs[3]	25.6 μs[3]
64 T_{OSC}	110	3.2 μs	12.8 μs[3]	16.0 μs[3]	51.2 μs[3]
A/D RC	x11	2 - 6 μs[1,4]	2 - 6 μs[1,4]	2 - 6 μs[1,4]	2 - 6 μs[1,4]

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical T_{AD} time of 4 μs for V_{DD} > 3.0V.

2: These values violate the minimum required T_{AD} time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during SLEEP.

7.1.5   STARTING A CONVERSION

The A/D conversion is initiated by setting the GO/DONE bit (ADCON0<1>). When the conversion is complete, the A/D module:

• Clears the GO/DONE bit
• Sets the ADIF flag (PIR1<6>)
• Generates an interrupt (if enabled).

If the conversion must be aborted, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the previous conversion. After an aborted conversion, a 2 T_{AD} delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

> **Note:** The GO/DONE bit should not be set in the same instruction that turns on the A/D.

7.1.6   CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right shifted. The ADFM bit (ADCON0<7>) controls the output format. Figure 7-2 shows the output formats.

FIGURE 7-2:   10-BIT A/D RESULT FORMAT

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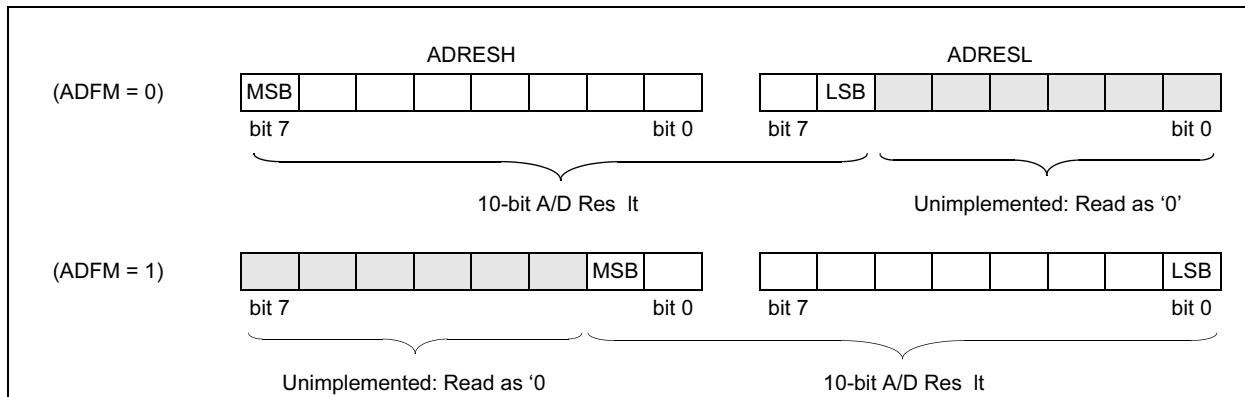
REGISTER 7-1: **ADCON0 — A/D CONTROL REGISTER (ADDRESS: 1Fh)**

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON

bit 7   bit 0

bit 7   **ADFM:** A/D Result Formed Select bit
            1 = Right justified
            0 = Left justified

bit 6   **VCFG:** Voltage Reference bit
            1 = V_{REF} pin
            0 = V_{DD}

bit 5   **Unimplemented:** Read as zero

bit 4-2   **CHS2:CHS0:** Analog Channel Select bits
            000 =Channel 00 (AN0)
            001 =Channel 01 (AN1)
            010 =Channel 02 (AN2)
            011 =Channel 03 (AN3)
            100 =Channel 04 (AN4)
            101 =Channel 05 (AN5)
            110 =Channel 06 (AN6)
            111 =Channel 07 (AN7)

bit 1   **GO/$\overline{\text{DONE}}$:** A/D Conversion STATUS bit
            1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
                 This bit is automatically cleared by hardware when the A/D conversion has completed.
            0 = A/D conversion completed/not in progress

bit 0   **ADON:** A/D Conversion STATUS bit
            1 = A/D converter module is operating
            0 = A/D converter is shut-off and consumes no operating current

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 7-2: **ADCON1 — A/D CONTROL REGISTER 1 (ADRESS: 9Fh)**

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—

bit 7   bit 0

bit 7:   **Unimplemented:** Read as '0'.

bit 6-4:   **ADCS<2:0>:** A/D Conversion Clock Select bits
            000 = $F_{OSC}/2$
            001 = $F_{OSC}/8$
            010 = $F_{OSC}/32$
             11 = F_{RC} (clock deri ed from a dedicated internal oscillator = 500 kH ma)
            100 = $F_{OSC}/4$
            101 = $F_{OSC}/16$
            110 = $F_{OSC}/64$

bit 3-0:   **Unimplemented:** Read as '0'.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 7-3:   **ANSEL — ANALOG SELECT REGISTER (ADRESS: 91h) (PIC16F676 ONLY)**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0

bit 7   bit 0

bit 7-0:   **ANS<7:0>**: Analog Select between analog or digital function on pins AN<7:0>, respectively.

1 = Analog input. Pin is assigned as analog input.[1]
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

7.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (C$_{HOLD}$) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-3. The source impedance (R$_S$) and the internal sampling switch (R$_{SS}$) impedance directly affect the time required to charge the capacitor C$_{HOLD}$. The sampling switch (R$_{SS}$) impedance varies over the device voltage (V$_{DD}$), see Figure 7-3. **The maximum recommended impedance for analog sources is 10 kΩ.** As the impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, T$_{ACQ}$, see the PICmicro™ Mid-Range Reference Manual (DS33023).

EQUATION 7-1: ACQUISITION TIME

$$
\begin{aligned}
T_{ACQ} =\ & \text{Amplifier Settling Time +} \\
& \text{Hold Capacitor Charging Time +} \\
& \text{Temperature Coefficient} \\[6pt]
=\ & T_{AMP} + T_C + T_{COFF} \\
=\ & 2\mu s + T_C + [(\text{Temperature -25°C})(0.05\mu s/°C)] \\
T_C =\ & C_{HOLD} (R_{IC} + R_{SS} + R_S) \ln(1/2047) \\
=\ & -120pF (1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\
=\ & 16.47\mu s \\
T_{ACQ} =\ & 2\mu s + 16.47\mu s + [(50°C -25°C)(0.05\mu s/°C)] \\
=\ & 19.72\mu s
\end{aligned}
$$

Note 1: The reference voltage (V$_{REF}$) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (C$_{HOLD}$) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 7-3: ANALOG INPUT MODEL
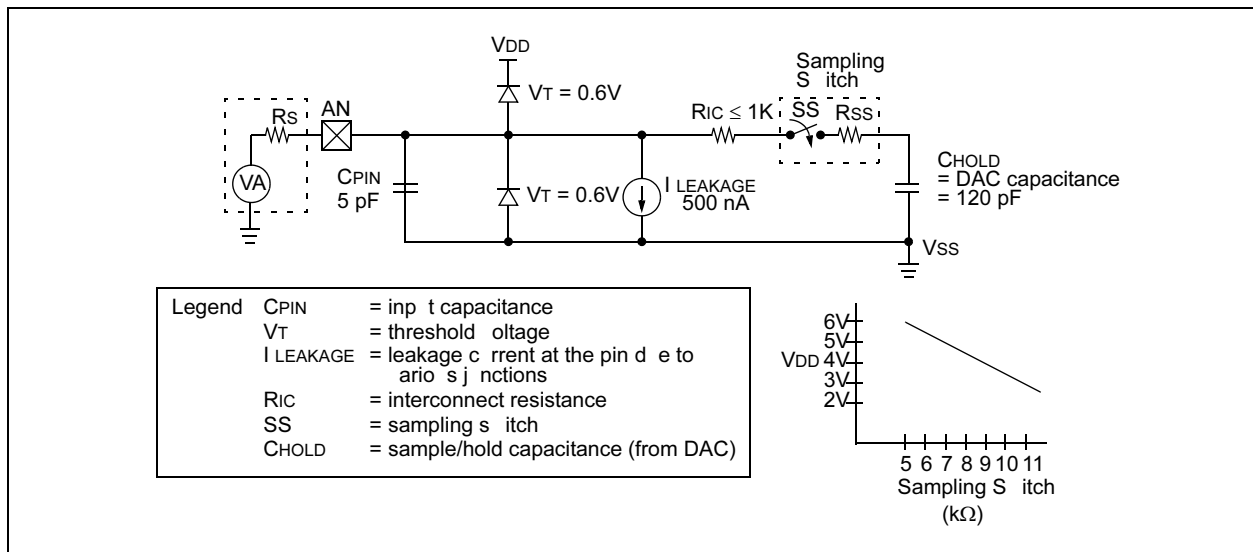
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7.3 A/D Operation During SLEEP

The A/D converter module can operate during SLEEP. This requires the A/D clock source to be set to the internal oscillator. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared, and the result is loaded into the ADRESH:ADRESL registers. If the A/D interrupt is enabled, the device awakens from SLEEP. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set.

When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted, and the A/D module is turned off. The ADON bit remains set.

7.4 Effects of RESET

A device RESET forces all registers to their RESET state. Thus, the A/D module is turned off and any pending conversion is aborted. The ADRESH:ADRESL registers are unchanged.

TABLE 7-2: SUMMARY OF A/D REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other RESETS
05h	PORTA			PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	--	--,, ,,,,
07h	PORTC			PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	--	--,, ,,,,
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 000.
0Ch	PIR1	EEIF	ADIF			CMIF			TMR1IF	00-- 0--0	00-- 0--0
1Eh	ADRESH	Most Significant 8 bits of the Left Shifted A/D res lt or 2 bits of the Right Shifted Res lt									,,,, ,,,,
1Fh	ADCON0	ADFM	VCFG		CHS2	CHS1	CHS0	GO	ADON	00-0 0000	00-0 0000
85h	TRISA			TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
87h	TRISC			TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
8Ch	PIE1	EEIE	ADIE			CMIE			TMR1IE	00-- 0--0	00-- 0--0
91h	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
9Eh	ADRESL	Least Significant 2 bits of the Left Shifted A/D Res lt or 8 bits of the Right Shifted Res lt									,,,, ,,,,
9Fh	ADCON1		ADCS2	ADCS1	ADCS0					-000 ----	-000 ----

Legend: x = nkno n, u = nchanged, - = nimplemented read as 0. Shaded cells are not sed for A/D con erter mod le.

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8.0   DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full V$_{DD}$ range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

• EECON1
• EECON2 (not a physically implemented register)
• EEDATA
• EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F630/676 devices have 128 bytes of data EEPROM with an address range from 0h to 7Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip to chip. Please refer to AC Specifications for exact limits.

When the data memory is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

REGISTER 8-1:   EEDAT — EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

bit 7-0   **EEDATn**: Byte value to write to or read from Data EEPROM

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 8-2:   EEADR — EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
bit 7							bit 0

bit 7   **Unimplemented**: Should be set to '0'

bit 6-0   **EEADR**: Specifies one of 128 locations for EEPROM Read/Write Operation

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

8.1 EEADR

The EEADR register can address up to a maximum of 128 bytes of data EEPROM. Only seven of the eight bits in the register (EEADR<6:0>) are required. The MSb (bit 7) is ignored.

The upper bit should always be '0' to remain upward compatible with devices that have more data EEPROM memory.

8.2 EECON1 AND EECON2 REGISTERS

EECON1 is the control register with four low order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{MCLR}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following RESET, the user can check the WRERR bit, clear it, and rewrite the location. The data and address will be cleared, therefore, the EEDATA and EEADR registers will need to be re-initialized.

Interrupt flag bit EEIF in the PIR1 register is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the Data EEPROM write sequence.

REGISTER 8-3:   EECON1 — EEPROM CONTROL REGISTER (ADDRESS: 9Ch)

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD

bit 7   bit 0

bit 7-4   **Unimplemented:** Read as '0'

bit 3   **WRERR:** EEPROM Error Flag bit
            1 = A write operation is prematurely terminated (any $\overline{MCLR}$ Reset, any WDT Reset during normal operation or BOD detect)
            0 = The write operation completed

bit 2   **WREN:** EEPROM Write Enable bit
            1 = Allows write cycles
            0 = Inhibits write to the data EEPROM

bit 1   **WR:** Write Control bit
            1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
            0 = Write cycle to the data EEPROM is complete

bit 0   **RD:** Read Control bit
            1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
            0 = Does not initiate an EEPROM read

Legend:		
S = Bit can only be set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

8.3 READING THE EEPROM DATA MEMORY

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>), as shown in Example 8-1. The data is available, in the very next cycle, in the EEDATA register. Therefore, it can be read in the next instruction. EEDATA holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 8-1: DATA EEPROM READD

```
    b f    STATUS,RP0    ;Bank 1
    mo l   CONFIG_ADDR   ;
    mo f   EEADR         ;Add e   o ead
    b f    EECON1,RD     ;EE Read
    mo f   EEDATA,W      ;Mo e da a  o W
```

8.4 WRITING TO THE EEPROM DATA MEMORY

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 8-2.

EXAMPLE 8-2: DATA EEPROM WRITE

```
    b f    STATUS,RP0    ;Bank 1
    b f    EECON1,WREN   ;Enable  i e
    bcf    INTCON,GIE    ;Di able INT
    mo l   55h           ;Unlock  i e
    mo f   EECON2        ;
    mo l   AAh           ;
    mo f   EECON2        ;
    b f    EECON1,WR     ;S a   he  i e
    b f    INTCON,GIE    ;Enable INTS
```
Required Sequence

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit (PIR<7>) register must be cleared by software.

8.5 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (see Example 8-3) to the desired value to be written.

EXAMPLE 8-3: WRITE VERIFY

```
    bcf    STATUS,RP0    ;Bank 0
    :                    ;An  code
    b f    STATUS,RP0    ;Bank 1 READ
    mo f   EEDATA,W      ;EEDATA no  changed
                         ;f om p e io   i e
    b f    EECON1,RD     ;YES, Read  he
                         ; al e  i  en
    o f    EEDATA,W
    b f    STATUS,Z      ;I  da a  he  ame
    go o   WRITE_ERR     ;No, handle e  o
    :                    ;Ye , con in e
```

8.5.1 USING THE DATA EEPROM

The Data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). Frequently changing values will typically be updated more often than specifications D120 or D120A. If this is not the case, an array refresh must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in FLASH program memory.

8.6 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

• brown-out
• power glitch
• software malfunction

8.7 DATA EEPROM OPERATION DURING CODE PROTECT

Data memory can be code protected by programming the CPD bit to '0'.

When the data memory is code protected, the CPU is able to read and write data to the Data EEPROM. It is recommended to code protect the program memory when code protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations to '0' will also help prevent data memory code protection from becoming breached.

TABLE 8-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Ch	PIR1	EEIF	ADIF			CMIF			TMR1IF	00-- 0--0	00-- 0--0
9Ah	EEDATA	EEPROM Data Register								0000 0000	0000 0000
9Bh	EEADR		EEPROM Address Register							-000 0000	-000 0000
9Ch	EECON1					WRERR	WREN	WR	RD	---- 000	---- q000
9Dh	EECON2[1]	EEPROM Control Register 2								---- ----	---- ----

Legend: = nkno n, u = nchanged, - = nimplemented read as 0, q = al e depends pon condition.
Shaded cells are not sed b Data EEPROM mod le.

Note 1: EECON2 is not a ph sical register.

9.0 SPECIAL FEATURES OF THE CPU

Certain special circuits that deal with the needs of real time applications are what sets a microcontroller apart from other processors. The PIC16F630/676 family has a host of such features intended to:

- maximize system reliability
- minimize cost through elimination of external components
- provide power saving operating modes and offer code protection.

These features are:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC16F630/676 has a Watchdog Timer that is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can provide at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through:

- External RESET
- Watchdog Timer wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 9-1).

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9.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations, as shown in Register 9-1. These bits are mapped in program memory location 2007h.

> **Note:** Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h - 3FFFh), which can be accessed only during programming. See PIC16F630/676 Programming Specification for more information.

REGISTER 9-1: CONFIG — CONFIGURATION WORD (ADDRESS: 2007h)

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
BG1	BG0	—	—	—	$\overline{CPD}$	$\overline{CP}$	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	F0SC2	F0SC1	F0SC0

bit 13 .... bit 0

bit 13-12 **BG1:BG0:** Bandgap Calibration bits for BOD and POR voltage[1]
  00 = Lowest bandgap voltage
  11 = Highest bandgap voltage

bit 11-9 **Unimplemented**: Read as '0'

bit 8 **$\overline{CPD}$:** Data Code Protection bit[2]
  1 = Data memory code protection is disabled
  0 = Data memory code protection is enabled

bit 7 **$\overline{CP}$**: Code Protection bit[3]
  1 = Program Memory code protection is disabled
  0 = Program Memory code protection is enabled

bit 6 **BODEN**: Brown-out Detect Enable bit[4]
  1 = BOD enabled
  0 = BOD disabled

bit 5 **MCLRE**: RA3/$\overline{MCLR}$ pin function select[5]
  1 = RA3/$\overline{MCLR}$ pin function is $\overline{MCLR}$
  0 = RA3/$\overline{MCLR}$ pin function is digital I/O, $\overline{MCLR}$ internally tied to V_{DD}

bit 4 **$\overline{PWRTE}$**: Power-up Timer Enable bit
  1 = PWRT disabled
  0 = PWRT enabled

bit 3 **WDTE**: Watchdog Timer Enable bit
  1 = WDT enabled
  0 = WDT disabled

bit 2-0 **FOSC2:FOSC0**: Oscillator Selection bits
  111 = RC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN
  110 = RC oscillator: I/O function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN
  101 = INTOSC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN
  100 = INTOSC oscillator: I/O function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN
  011 = EC: I/O function on RA4/OSC2/CLKOUT pin, CLKIN on RA5/OSC1/CLKIN
  010 = HS oscillator: High speed crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN
  001 = XT oscillator: Crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN
  000 = LP oscillator: Low power crystal on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN

Note 1: The Bandgap Calibration bits are factory programmed and must be read and saved prior to erasing the device as specified in the PIC16F630/676 Programming Specification. These bits are reflected in an export of the configuration word. Microchip Development Tools maintain all calibration bits to factory settings.
  2: The entire data EEPROM will be erased when the code protection is turned off.
  3: The entire program memory will be erased, including OSCCAL value, when the code protection is turned off.
  4: Enabling Brown-out Detect does not automatically enable Power-up Timer.
  5: When $\overline{MCLR}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

Legend:		
P = Programmed using ICSP		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared x = bit is unknown

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9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC16F630/676 can be operated in eight different Oscillator Option modes. The user can program three configuration bits (FOSC2 through FOSC0) to select one of these eight modes:

- LP   Low Power Crystal
- XT   Crystal/Resonator
- HS   High Speed Crystal/Resonator
- RC   External Resistor/Capacitor (2 modes)
- INTOSC Internal Oscillator (2 modes)
- EC   External Clock In

> **Note:** Additional information on oscillator configurations is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (see Figure 9-1). The PIC16F630/676 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may yield a frequency outside of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (see Figure 9-2).

FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)

Note 1: See Table 9-1 and Table 9-2 for recommended values of C1 and C2.
2: A series resistor may be required for AT strip cut crystals.
3: RF varies with the Oscillator mode selected (Approx. value = 10 MΩ).
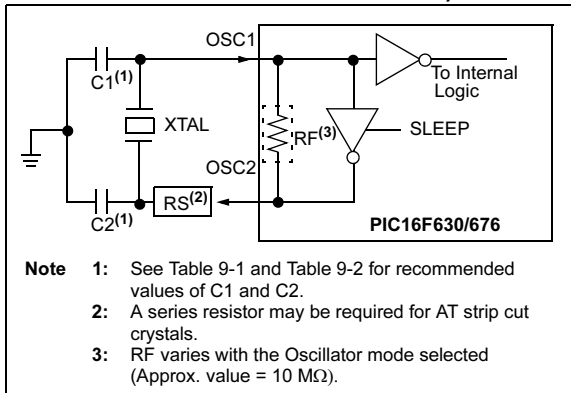
FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT, EC, OR LP OSC CONFIGURATION)

Note 1: Functions as RA4 in EC Osc mode.
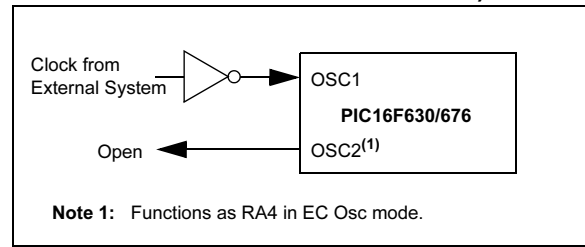
TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Characterized:			
Mode	Freq	OSC1(C1)	OSC2(C2)
XT	455 kHz	68 - 100 pF	68 - 100 pF
	2.0 MHz	15 - 68 pF	15 - 68 pF
	4.0 MHz	15 - 68 pF	15 - 68 pF
HS	8.0 MHz	10 - 68 pF	10 - 68 pF
	16.0 MHz	10 - 22 pF	10 - 22 pF

Note 1: Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1(C1)	OSC2(C2)
LP	32 kHz	68 - 100 pF	68 - 100 pF
XT	100 kHz	68 - 150 pF	150 - 200 pF
	2 MHz	15 - 30 pF	15 - 30 pF
	4 MHz	15 - 30 pF	15 - 30 pF
HS	8 MHz	15 - 30 pF	15 - 30 pF
	10 MHz	15 - 30 pF	15 - 30 pF
	20 MHz	15 - 30 pF	15 - 30 pF

Note 1: Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

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9.2.3 EXTERNAL CLOCK IN

For applications where a clock is already available elsewhere, users may directly drive the PIC16F630/676 provided that this external clock source meets the AC/DC timing requirements listed in Section 12.0. Figure 9-2 shows how an external clock circuit should be configured.

9.2.4 RC OSCILLATOR

For applications where precise timing is not a requirement, the RC oscillator option is available. The operation and functionality of the RC oscillator is dependent upon a number of variables. The RC oscillator frequency is a function of:

• Supply voltage
• Resistor (R_{EXT}) and capacitor (C_{EXT}) values
• Operating temperature.

The oscillator frequency will vary from unit to unit due to normal process parameter variation. The difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to account for the tolerance of the external R and C components. Figure 9-3 shows how the R/C combination is connected.

Two options are available for this Oscillator mode which allow RA4 to be used as a general purpose I/O or to output $F_{OSC}/4$.

FIGURE 9-3: RC OSCILLATOR MODE
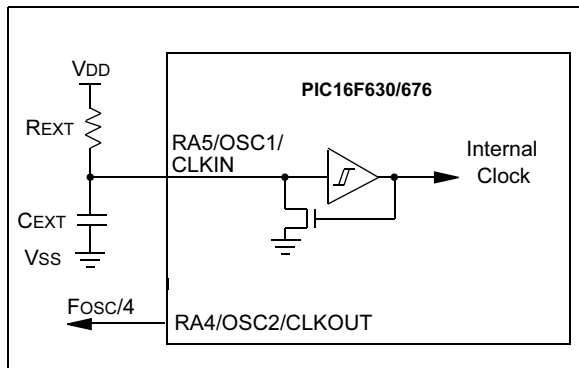
9.2.5 INTERNAL 4 MHz OSCILLATOR

When calibrated, the internal oscillator provides a fixed 4 MHz (nominal) system clock. See Electrical Specifications, Section 12.0, for information on variation over voltage and temperature.

Two options are available for this Oscillator mode which allow RA4 to be used as a general purpose I/O or to output $F_{OSC}/4$.

9.2.5.1 Calibrating the Internal Oscillator

A calibration instruction is programmed into the last location of program memory. This instruction is a `RETLW XX`, where the literal is the calibration value. The literal is placed in the OSCCAL register to set the calibration of the internal oscillator. Example 9-1 demonstrates how to calibrate the internal oscillator. For best operation, decouple (with capacitance) V_{DD} and V_{SS} as close to the device as possible.

Note: Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing part as specified in the PIC16F630/676 Programming specification. Microchip Development Tools maintain all calibration bits to factory settings.

EXAMPLE 9-1: CALIBRATING THE INTERNAL OSCILLATOR

```
b f    STATUS, RP0   ;Bank 1
call   3FFh          ;Ge  he cal  al e
mo  f  OSCCAL        ;Calib a e
bcf    STATUS, RP0   ;Bank 0
```

9.2.6 CLKOUT

The PIC16F630/676 devices can be configured to provide a clock out signal in the INTOSC and RC Oscillator modes. When configured, the oscillator frequency divided by four ($F_{OSC}/4$) is output on the RA4/OSC2/CLKOUT pin. $F_{OSC}/4$ can be used for test purposes or to synchronize other logic.

9.3   RESET

The PIC16F630/676 differentiates between various kinds of RESET:

a)   Power-on Reset (POR)

b)   WDT Reset during normal operation

c)   WDT Reset during SLEEP

d) $\overline{MCLR}$ Reset during normal operation

e) $\overline{MCLR}$ Reset during SLEEP

f)   Brown-out Detect (BOD)

Some registers are not affected in any RESET condition; their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on:

• Power-on Reset

• $\overline{MCLR}$ Reset

• WDT Reset

• WDT Reset during SLEEP

• Brown-out Detect (BOD)

They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different RESET situations as indicated in Table 9-4. These bits are used in software to determine the nature of the RESET. See Table 9-7 for a full description of RESET states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 9-4.

The $\overline{MCLR}$ Reset path has a noise filter to detect and ignore small pulses. See Table 12-4 in Electrical Specifications Section for pulse width specification.

FIGURE 9-4:   SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

Note   1:   This is a separate oscillator from the INTOSC/EC oscillator.
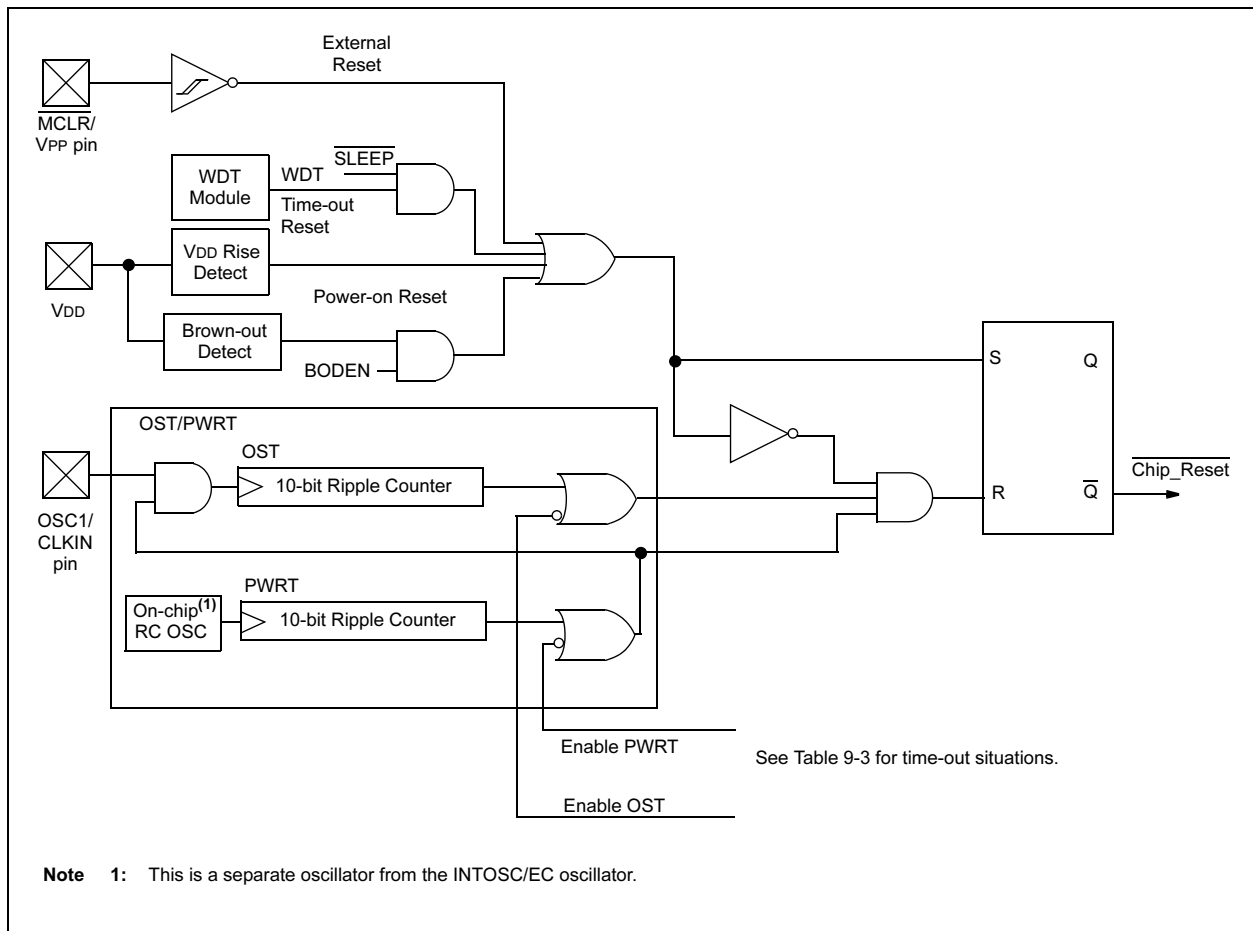
9.3.1 $\overline{\text{MCLR}}$

PIC16F630/676 devices have a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

The behavior of the ESD protection on the $\overline{\text{MCLR}}$ pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both $\overline{\text{MCLR}}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{\text{MCLR}}$ pin no longer be tied directly to V$_{DD}$. The use of an RC network, as shown in Figure 9-5, is suggested.

An internal $\overline{\text{MCLR}}$ option is enabled by setting the MCLRE bit in the configuration word. When enabled, $\overline{\text{MCLR}}$ is internally tied to V$_{DD}$. No internal pull-up option is available for the $\overline{\text{MCLR}}$ pin.

FIGURE 9-5: **RECOMMENDED $\overline{\text{MCLR}}$ CIRCUIT**
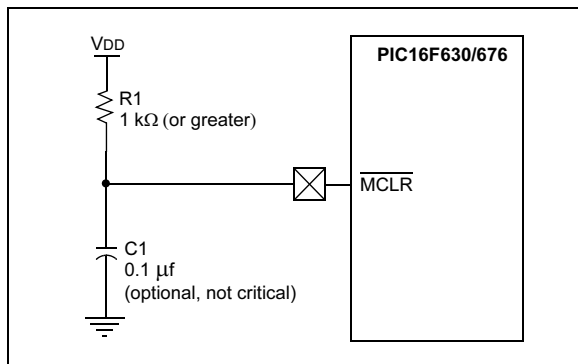
9.3.2 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until V$_{DD}$ has reached a high enough level for proper operation. To take advantage of the POR, simply tie the $\overline{\text{MCLR}}$ pin through a resistor to V$_{DD}$. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V$_{DD}$ is required. See Electrical Specifications for details (see Section 12.0). If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in RESET until V$_{DD}$ reaches V$_{BOD}$ (see Section 9.3.5).

> **Note:** The POR circuit does not produce an internal RESET when V$_{DD}$ declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607 *"Power-up Trouble Shooting"*.

9.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Detect. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the V$_{DD}$ to rise to an acceptable level. A configuration bit, $\overline{\text{PWRTE}}$ can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Detect is enabled.

The Power-up Time delay will vary from chip to chip and due to:

• V$_{DD}$ variation
• Temperature variation
• Process variation.

See DC parameters for details (Section 12.0).

9.3.4 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

9.3.5 BROWN-OUT DETECT (BOD)

The PIC16F630/676 members have on-chip Brown-out Detect circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Detect circuitry. If VDD falls below VBOD for greater than parameter (TBOD) in Table 12-4 (see Section 12.0), the Brown-out situation will reset the device. This will occur regardless of VDD slew-rate. A RESET is not guaranteed to occur if VDD falls below VBOD for less than parameter (TBOD).

On any RESET (Power-on, Brown-out Detect, Watchdog, etc.), the chip will remain in RESET until VDD rises above BVDD (see Figure 9-6). The Power-up Timer will now be invoked, if enabled, and will keep the chip in RESET an additional 72 ms.

> **Note:** A Brown-out Detect does not enable the Power-up Timer if the PWRTE bit in the configuration word is set.

If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Detect and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms RESET.

FIGURE 9-6:   BROWN-OUT SITUATIONS

Note   1: 72 ms dela   onl   if PWRTE bit is programmed to '0'.
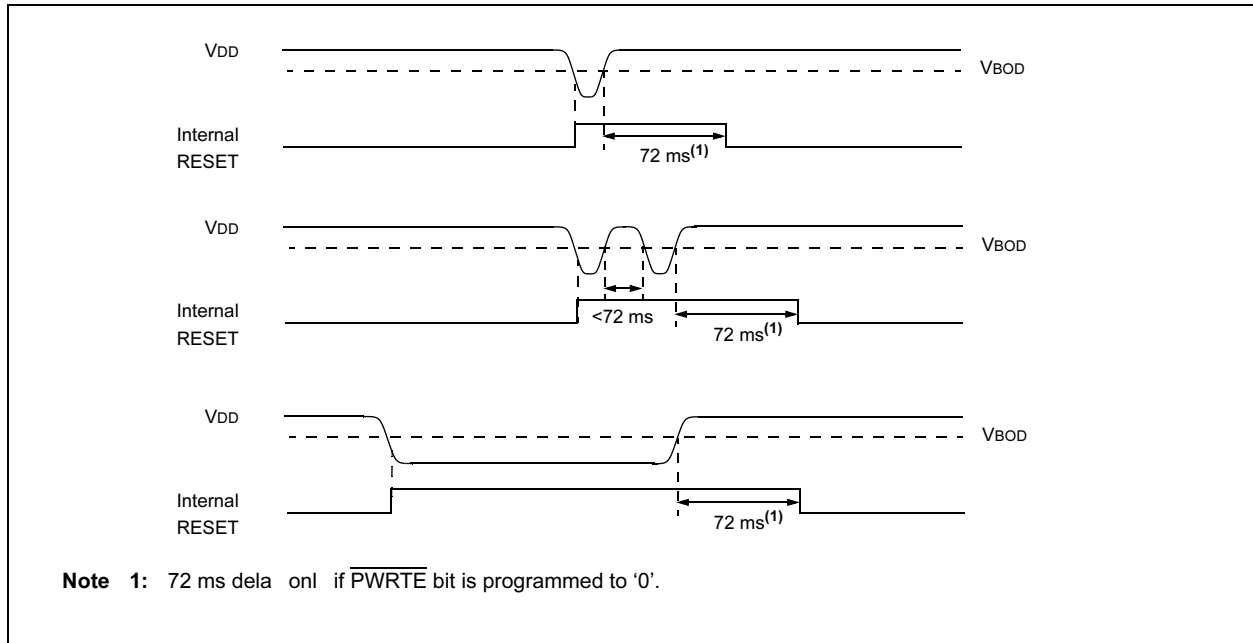
9.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired. Then, OST is activated. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 9-7, Figure 9-8 and Figure 9-9 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (see Figure 9-8). This is useful for testing purposes or to synchronize more than one PIC16F630/676 device operating in parallel.

Table 9-6 shows the RESET conditions for some special registers, while Table 9-7 shows the RESET conditions for all the registers.

9.3.7 POWER CONTROL (PCON) STATUS REGISTER

The power CONTROL/STATUS register, PCON (address 8Eh) has two bits.

Bit0 is BOD (Brown-out). BOD is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if BOD = 0, indicating that a brown-out has occurred. The BOD STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (i.e., VDD may have gone too low).

TABLE 9-3: **TIME-OUT IN VARIOUS SITUATIONS**

Oscillator Configuration	Power-up		Brown-out Detect		Wake-up from SLEEP
	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	
XT, HS, LP	T_{PWRT} + 1024•T_{OSC}	1024•T_{OSC}	T_{PWRT} + 1024•T_{OSC}	1024•T_{OSC}	1024•T_{OSC}
RC, EC, INTOSC	T_{PWRT}	—	T_{PWRT}	—	—

TABLE 9-4: **STATUS/PCON BITS AND THEIR SIGNIFICANCE**

$\overline{POR}$	$\overline{BOD}$	$\overline{TO}$	$\overline{PD}$	
0	u	1	1	Power-on Reset
1	0	1	1	Brown-out Detect
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{MCLR}$ Reset during normal operation
u	u	1	0	$\overline{MCLR}$ Reset during SLEEP

Legend: u = unchanged, x = unknown

TABLE 9-5: **SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS[1]
03h	STATUS	IRP	RP1	RPO	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOD}$	---- --0x	---- --uq

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.
Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

TABLE 9-6: **INITIALIZATION CONDITION FOR SPECIAL REGISTERS**

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Detect	000h	0001 1uuu	---- --10
Interrupt Wake-up from SLEEP	PC + 1[1]	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.
Note 1: When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 9-7: **INITIALIZATION CONDITION FOR REGISTERS**

Register	Address	Power-on Reset	• MCLR Reset • WDT Reset • Brown-out Detect[1]	• Wake-up from SLEEP through interrupt • Wake-up from SLEEP through WDT time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	—	—	—
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1[3]
STATUS	03h/83h	0001 1xxx	000q quuu[4]	uuuq quuu[4]
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORTC	07h	--xx xxxx	--uu uuuu	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 000u	uuuu uuqq[2]
PIR1	0Ch	00-- 0--0	00-- 0--0	qq-- q--q[2,5]
T1CON	10h	-000 0000	-uuu uuuu	-uuu uuuu
CMCON	19h	-0-0 0000	-0-0 0000	-u-u uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	00-0 0000	00-0 0000	uu-u uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISC	87h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	00-- 0--0	00-- 0--0	uu-- u--u
PCON	8Eh	---- --0x	---- --uu[1,6]	---- --uu
OSCCAL	90h	1000 00--	1000 00--	uuuu uu--
ANSEL	91h	1111 1111	1111 1111	uuuu uuuu
WPUA	95h	--11 -111	--11 -111	uuuu uuuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDATA	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	-000 0000	-000 0000	-uuu uuuu
EECON1	9Ch	---- x000	---- q000	---- uuuu
EECON2	9Dh	---- ----	---- ----	---- ----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000 ----	-000 ----	-uuu ----

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.
    2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
    3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
    4: See Table 9-6 for RESET value for specific condition.
    5: If wake-up was due to data EEPROM write completing, bit 7 = 1; A/D conversion completing, bit 6 = 1; Comparator input changing, bit 3 = 1; or Timer1 rolling over, bit 0 = 1. All other interrupts generating a wake-up will cause these bits to = u.
    6: If RESET was due to brown-out, then bit 0 = 0. All other RESETS will cause bit 0 = u.

FIGURE 9-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V$_{DD}$): CASE 1
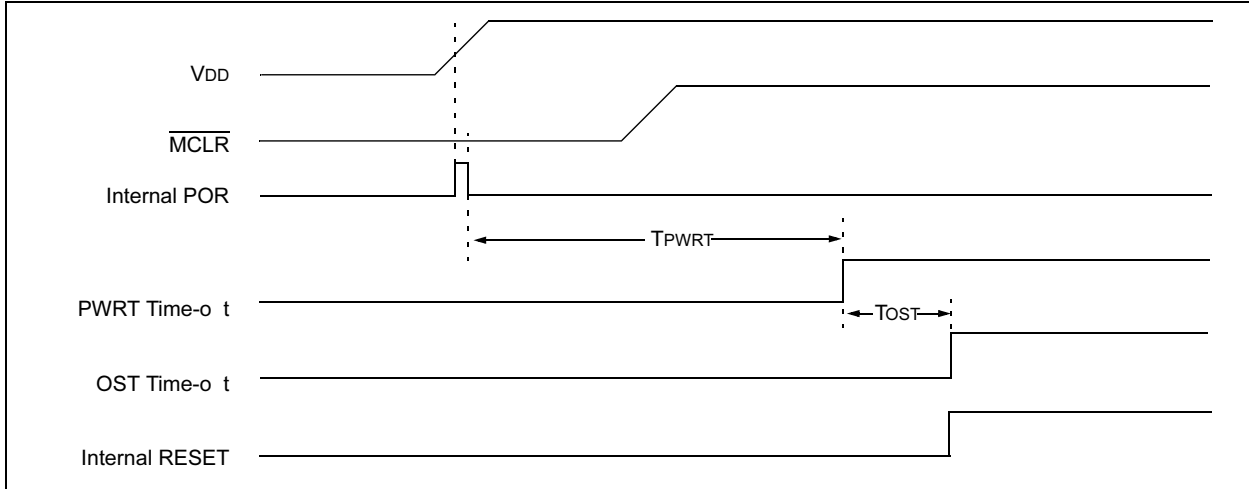

FIGURE 9-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V$_{DD}$): CASE 2
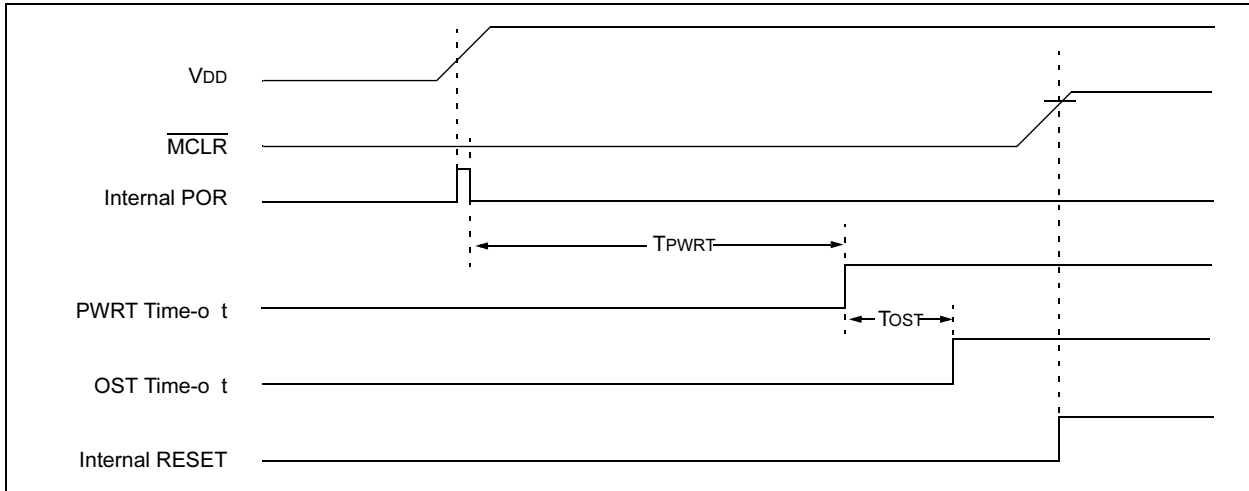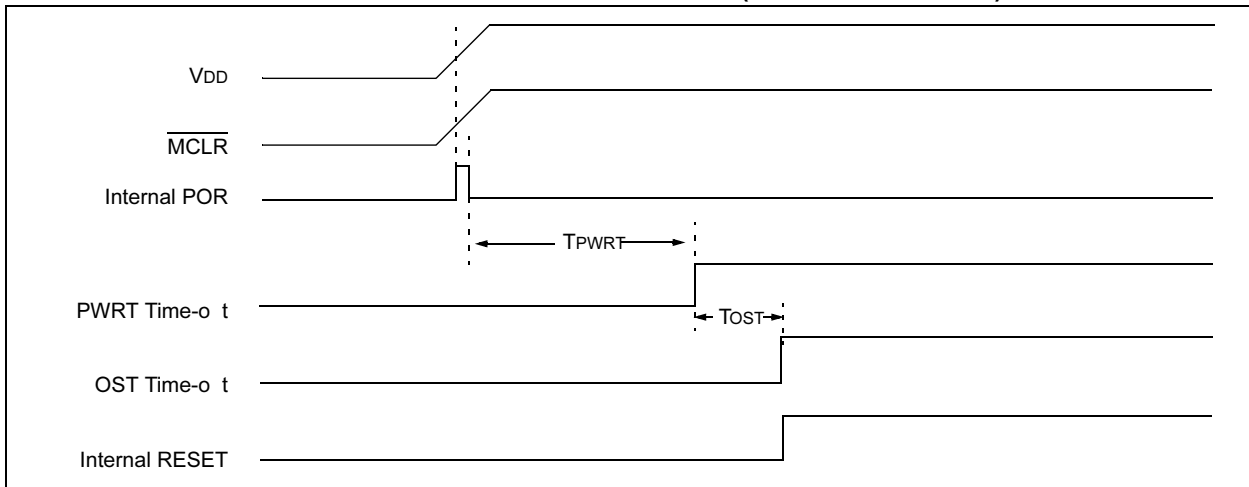

FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V$_{DD}$)

9.4 Interrupts

The PIC16F630/676 has 7 sources of interrupt:

- External Interrupt RA2/INT
- TMR0 Overflow Interrupt
- PORTA Change Interrupts
- Comparator Interrupt
- A/D Interrupt (PIC16F676 only)
- TMR1 Overflow Interrupt
- EEPROM Data Write Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt register (PIR) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register and PIE register. GIE is cleared on RESET.

The return from interrupt instruction, RETFIE, exits interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT pin interrupt
- PORTA change interrupt
- TMR0 overflow interrupt

The peripheral interrupt flags are contained in the special register PIR1. The corresponding interrupt enable bit is contained in Special Register PIE1.

The following interrupt flags are contained in the PIR register:

- EEPROM data write interrupt
- A/D interrupt
- Comparator interrupt
- Timer1 overflow interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt
- The return address is pushed onto the stack
- The PC is loaded with 0004h

Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid RA2/INT recursive interrupts.

For external interrupt events, such as the INT pin, or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 9-11). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The

interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.

FIGURE 9-10: **INTERRUPT LOGIC**
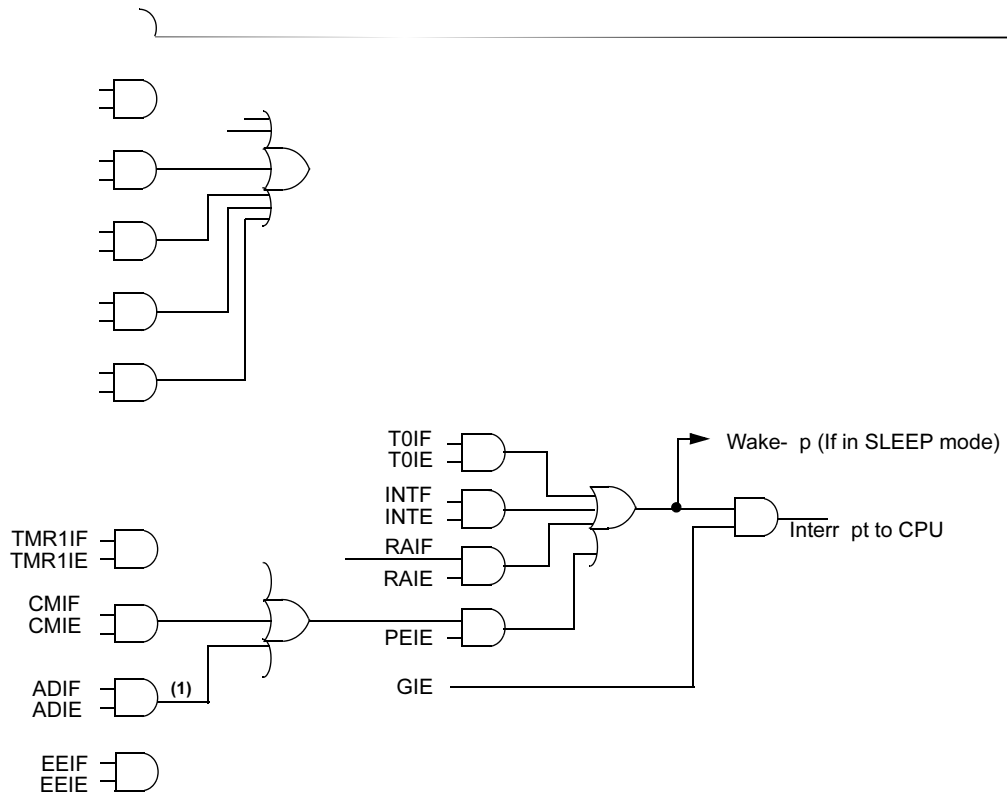
9.4.1   RA2/INT INTERRUPT

External interrupt on RA2/INT pin is edge-triggered; either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from SLEEP if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.7 for details on SLEEP and Figure 9-13 for timing of wake-up from SLEEP through RA2/INT interrupt.

> **Note:**   The ANSEL 9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

9.4.2   TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 4.0.

9.4.3   PORTA INTERRUPT

An input change on PORTA change sets the RAIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RAIE (INTCON<3>) bit. Plus individual pins can be configured through the IOCA register.

> **Note:**   If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

9.4.4   COMPARATOR INTERRUPT

See Section 6.9 for description of comparator interrupt.

9.4.5   A/D CONVERTER INTERRUPT

After a conversion is complete, the ADIF flag (PIR<6>) is set. The interrupt can be enabled/disabled by setting or clearing ADIE (PIE<6>).

See Section 7.0 for operation of the A/D converter interrupt.

FIGURE 9-11:   INT PIN INTERRUPT TIMING
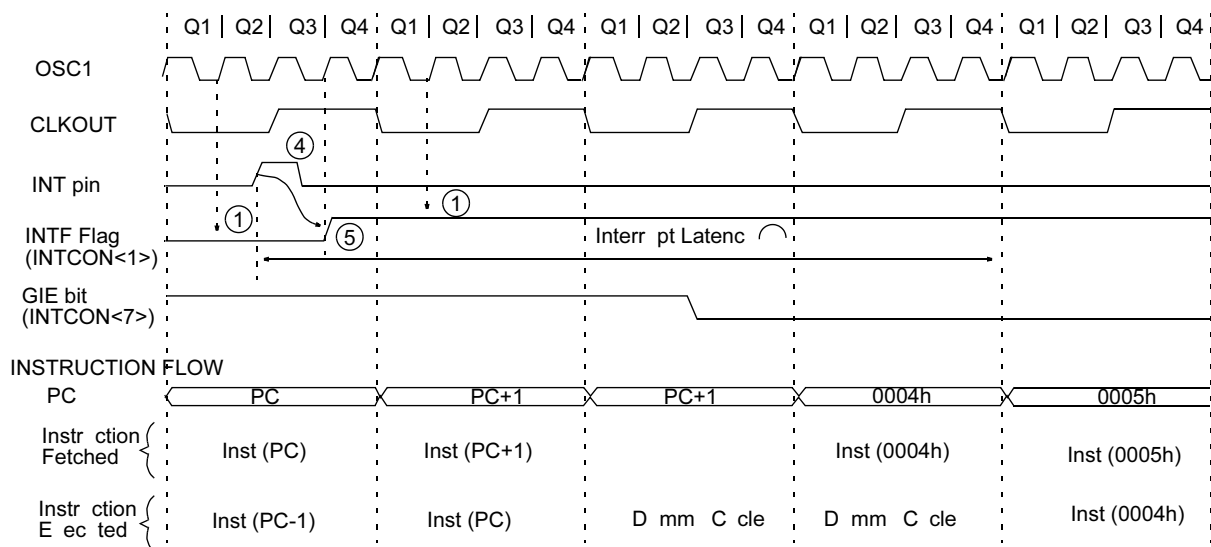
TABLE 9-8: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 000.
0Ch	PIR1	EEIF	ADIF			CMIF			TMR1IF	00-- 0--0	00-- 0--0
8Ch	PIE1	EEIE	ADIE			CMIE			TMR1IE	00-- 0--0	00-- 0--0

Legend: = nkno n, = nchanged, - = nimplemented read as 0, q = al e depends pon condition.
Shaded cells are not sed b the Interr pt mod le.

9.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W register and STATUS register). This must be implemented in software.

Example 9-2 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-2:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 9-2: SAVING THE STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP       ;copy W to temp register,
                     could be in either bank
SWAPF   STATUS,W     ;swap status to be saved into W
BCF     STATUS,RP0   ;change to bank 0 regardless of
                     current bank
MOVWF   STATUS_TEMP  ;save status to bank 0 register
    :
    :(ISR)
    :
SWAPF   STATUS_TEMP,W;swap STATUS_TEMP register into
                     W, sets bank to original state
MOVWF   STATUS       ;move W into STATUS register
SWAPF   W_TEMP,F     ;swap W_TEMP
SWAPF   W_TEMP,W     ;swap W_TEMP into W
```

9.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (i.e., V_{DD} = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time-out occurs.
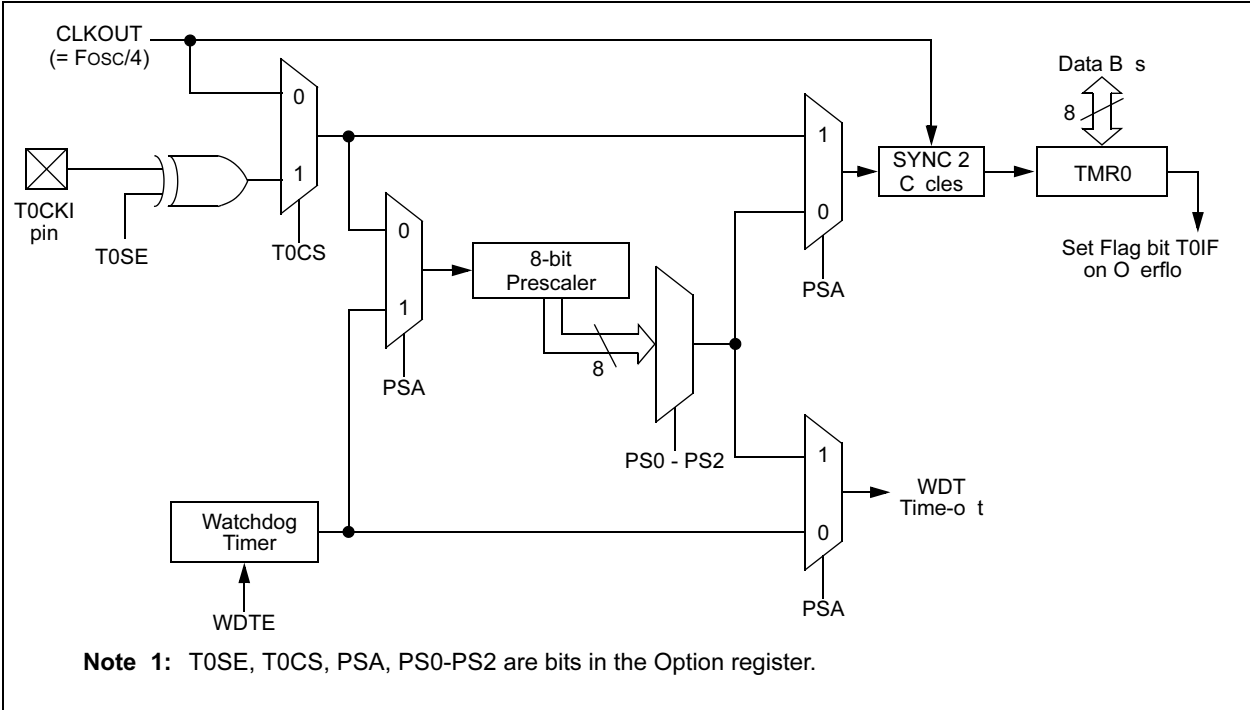
FIGURE 9-12: **WATCHDOG TIMER BLOCK DIAGRAM**

Note 1: T0SE, T0CS, PSA, PS0-PS2 are bits in the Option register.

TABLE 9-9: **SUMMARY OF WATCHDOG TIMER REGISTERS**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
81h	OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
2007h	Config. bits	CP	BODEN	MCLRE	PWRTE	WDTE	F0SC2	F0SC1	F0SC0	....	....

Legend: = Unchanged, shaded cells are not used by the Watchdog Timer.

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9.7 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a `SLEEP` instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running
- $\overline{PD}$ bit in the STATUS register is cleared
- $\overline{TO}$ bit is set
- Oscillator driver is turned off
- I/O ports maintain the status they had before `SLEEP` was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

> **Note:** It should be noted that a RESET generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

9.7.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External RESET input on $\overline{MCLR}$ pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RA2/INT pin, PORTA change, or a peripheral interrupt.

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device RESET. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. $\overline{TO}$ bit is cleared if WDT Wake-up occurred.

When the `SLEEP` instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have an `NOP` after the `SLEEP` instruction.

> **Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The `SLEEP` instruction is completely executed.
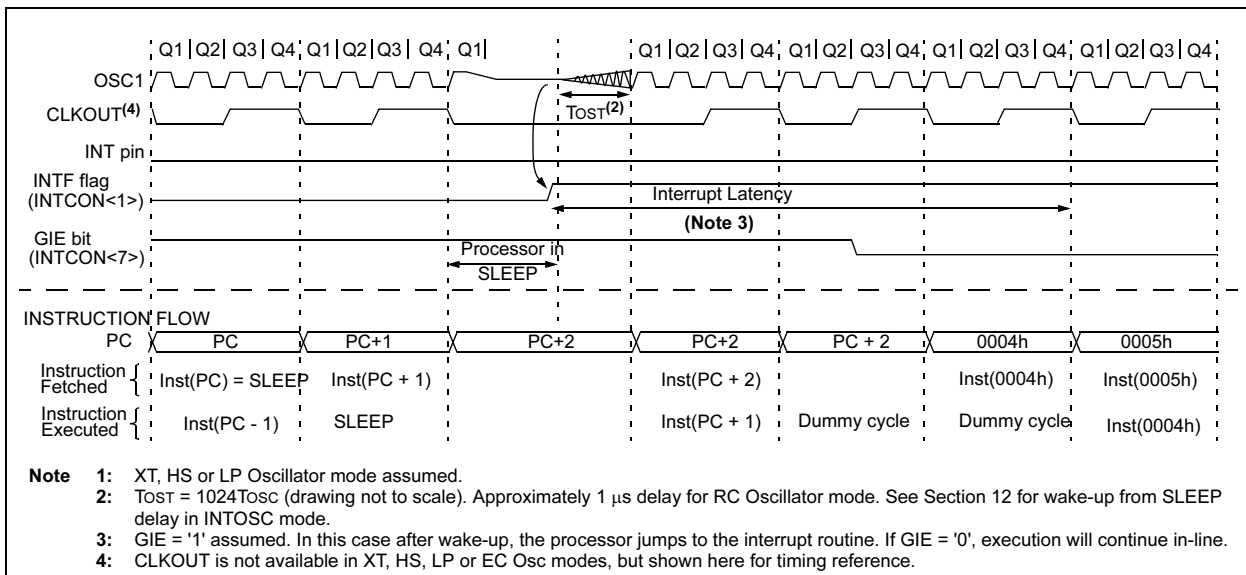
The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

FIGURE 9-13: WAKE-UP FROM SLEEP THROUGH INTERRUPT

Note 1: XT, HS or LP Oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale). Approximately 1 μs delay for RC Oscillator mode. See Section 12 for wake-up from SLEEP delay in INTOSC mode.
3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in XT, HS, LP or EC Osc modes, but shown here for timing reference.

9.8   Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

> **Note:** The entire data EEPROM and FLASH program memory will be erased when the code protection is turned off. The INTOSC calibration data is also erased. See PIC16F630/676 Programming Specification for more information.

9.9   ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify. Only the Least Significant 7 bits of the ID locations are used.

9.10   In-Circuit Serial Programming

The PIC16F630/676 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for:

• power
• ground
• programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the micro-controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH (see Programming Specification). RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After RESET, to place the device into Programming/Verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the PIC16F630/676 Programming Specification.

A typical In-Circuit Serial Programming connection is shown in Figure 9-14.

FIGURE 9-14:   TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION
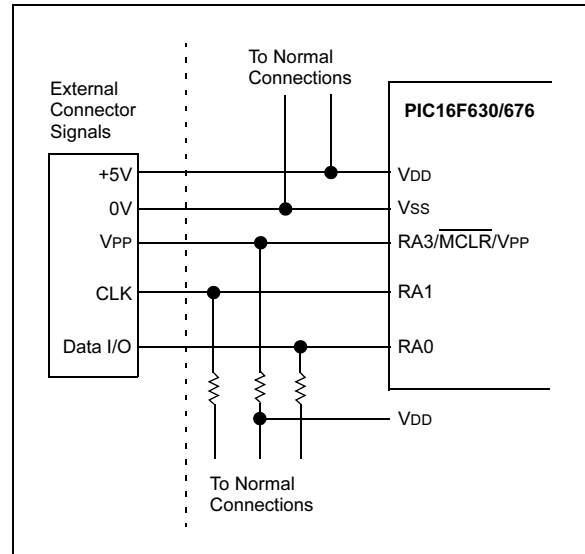
9.11   In-Circuit Debugger

Since in-circuit debugging requires the loss of clock, data and MCLR pins, MPLAB® ICD 2 development with an 14-pin device is not practical. A special 20-pin PIC16F676-ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

This special ICD device is mounted on the top of the header and its signals are routed to the MPLAB ICD 2 connector. On the bottom of the header is an 14-pin socket that plugs into the user's target via the 14-pin stand-off connector.

When the ICD pin on the PIC16F676-ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 9-10 shows which features are consumed by the background debugger:

TABLE 9-10:   DEBUGGER RESOURCES

I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be NOP 300h - 3FEh

For more information, see 14-Pin MPLAB ICD 2 Header Information Sheet (DS51299) available on Microchip's website (www.microchip.com).

NOTES:

10.0   INSTRUCTION SET SUMMARY

The PIC16F630/676 instruction set is highly orthogonal and is comprised of three basic categories:

• **Byte-oriented** operations

• **Bit-oriented** operations

• **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type, and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 10-1, while the various opcode fields are summarized in Table 10-1.

Table 10-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the PICmicro™ Mid-Range Reference Manual (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

> **Note:** To maintain upward compatibility with future products, <u>do not use</u> the OPTION and TRIS instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

10.1   READ-MODIFY-WRITE OPERATIONS

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended result of clearing the condition that set the RAIF flag.

TABLE 10-1:   OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 10-1:   GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

```
13              8  7 6              0
┌───────────────┬──┬────────────────┐
│    OPCODE     │ d│   f (FILE #)   │
└───────────────┴──┴────────────────┘
```

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

```
13          10 9    7 6              0
┌───────────┬───────┬────────────────┐
│   OPCODE  │b (BIT #)│  f (FILE #)  │
└───────────┴───────┴────────────────┘
```

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

```
13              8  7                 0
┌───────────────┬───────────────────┐
│    OPCODE     │     k (literal)   │
└───────────────┴───────────────────┘
```

k = 8-bit immediate al e

CALL and GOTO instr ctions onl

```
13         11 10                     0
┌───────────┬───────────────────────┐
│   OPCODE  │      k (literal)      │
└───────────┴───────────────────────┘
```

k = 11-bit immediate al e

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TABLE 10-2: PIC16F630/676 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb	LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00 0111 dfff	ffff	C,DC,Z	**1,2**
ANDWF	f, d	AND W ith f	1	00 0101 dfff	ffff	Z	**1,2**
CLRF	f	Clear f	1	00 0001 lfff	ffff	Z	**2**
CLRW	-	Clear W	1	00 0001 0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff	ffff	Z	**1,2**
DECF	f, d	Decrement f	1	00 0011 dfff	ffff	Z	**1,2**
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff	ffff		**1,2,3**
INCF	f, d	Increment f	1	00 1010 dfff	ffff	Z	**1,2**
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff	ffff		**1,2,3**
IORWF	f, d	Incl si e OR W ith f	1	00 0100 dfff	ffff	Z	**1,2**
MOVF	f, d	Mo e f	1	00 1000 dfff	ffff	Z	**1,2**
MOVWF	f	Mo e W to f	1	00 0000 lfff	ffff		
NOP	-	No Operation	1	00 0000 0xx0	0000		
RLF	f, d	Rotate Left f thro gh Carr	1	00 1101 dfff	ffff	C	**1,2**
RRF	f, d	Rotate Right f thro gh Carr	1	00 1100 dfff	ffff	C	**1,2**
SUBWF	f, d	S btract W from f	1	00 0010 dfff	ffff	C,DC,Z	**1,2**
SWAPF	f, d	S ap nibbles in f	1	00 1110 dfff	ffff		**1,2**
XORWF	f, d	E cl si e OR W ith f	1	00 0110 dfff	ffff	Z	**1,2**
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01 00bb bfff	ffff		**1,2**
BSF	f, b	Bit Set f	1	01 01bb bfff	ffff		**1,2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS							
ADDLW	k	Add literal and W	1	11 111x kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal ith W	1	11 1001 kkkk	kkkk	Z	
CALL	k	Call s bro tine	2	10 0kkk kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110	0100	$\overline{TO},\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk	kkkk		
IORLW	k	Incl si e OR literal ith W	1	11 1000 kkkk	kkkk	Z	
MOVLW	k	Mo e literal to W	1	11 00xx kkkk	kkkk		
RETFIE	-	Ret rn from interr pt	2	00 0000 0000	1001		
RETLW	k	Ret rn ith literal in W	2	11 01xx kkkk	kkkk		
RETURN	-	Ret rn from S bro tine	2	00 0000 0000	1000		
SLEEP	-	Go into Standb mode	1	00 0000 0110	0011	$\overline{TO},\overline{PD}$	
SUBLW	k	S btract W from literal	1	11 110x kkkk	kkkk	C,DC,Z	
XORLW	k	E cl si e OR literal ith W	1	11 1010 kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a f nction of itself (e.g., `MOVF PORTA, 1`), the al e sed ill be that al e present on the pins themsel es. For e ample, if the data latch is 1 for a pin config red as inp t and is dri en lo b an e ternal de ice, the data ill be ritten back ith a 0 .

2: If this instr ction is e ec ted on the TMR0 register (and, here applicable, d = 1), the prescaler ill be cleared if assigned to the Timer0 mod le.

3: If Program Co nter (PC) is modified, or a conditional test is tr e, the instr ction req ires t o c cles. The second c cle is e ec ted as a `NOP`.

> **Note:** Additional information on the mid-range instruction set is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

10.2 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow (destination)$
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) .AND. (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(W) .AND. (f) \rightarrow (destination)$
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	$0 \rightarrow (f<b>)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	$1 \rightarrow (f<b>)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if $(f<b>) = 1$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a `NOP` is executed instead, making this a 2-cycle instruction.

BTFSC	Bit Test, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	skip if $(f<b>) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a `NOP` is executed instead, making this a 2-cycle instruction.

CALL	**Call Subroutine**
Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	$(PC)+ 1 \rightarrow TOS$, $k \rightarrow PC<10:0>$, $(PCLATH<4:3>) \rightarrow PC<12:11>$
Status Affected:	None
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRWDT	**Clear Watchdog Timer**
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	$00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$
Status Affected:	$\overline{TO}, \overline{PD}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits $\overline{TO}$ and $\overline{PD}$ are set.

CLRF	**Clear f**
Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	$00h \rightarrow (f)$ $1 \rightarrow Z$
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

COMF	**Complement f**
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow (destination)$
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

CLRW	**Clear W**
Syntax:	[*label*] CLRW
Operands:	None
Operation:	$00h \rightarrow (W)$ $1 \rightarrow Z$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECF	**Decrement f**
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (destination)$
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

DECFSZ	**Decrement f, Skip if 0**
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2-cycle instruction.

INCFSZ	**Increment f, Skip if 0**
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2-cycle instruction.

GOTO	**Unconditional Branch**
Syntax:	[*label*] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	k $\rightarrow$ PC<10:0> PCLATH<4:3> $\rightarrow$ PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

IORLW	**Inclusive OR Literal with W**
Syntax:	[*label*] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .OR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

INCF	**Increment f**
Syntax:	[*label*] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

IORWF	**Inclusive OR W with f**
Syntax:	[*label*] IORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	k $\rightarrow$ (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	(W) $\rightarrow$ (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS $\rightarrow$ PC, 1 $\rightarrow$ GIE
Status Affected:	None

RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	k $\rightarrow$ (W); TOS $\rightarrow$ PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS $\rightarrow$ PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RRF	Rotate Right f through Carry
Syntax:	[*label*] RRF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

SLEEP	
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h $\rightarrow$ WDT, 0 $\rightarrow$ WDT prescaler, 1 $\rightarrow$ $\overline{TO}$, 0 $\rightarrow$ $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down STATUS bit, $\overline{PD}$ is cleared. Time-out STATUS bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.

SUBLW	Subtract W from Literal
Syntax:	[*label*] SUBLW k
Operands:	$0 \leq k \leq 255$
Operation:	k - (W) $\rightarrow$ (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) - (W) $\rightarrow$ (destination)
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

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SWAPF   **Swap Nibbles in f**

Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.

XORLW   **Exclusive OR Literal with W**

Syntax:	[*label*] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF   **Exclusive OR W with f**

Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

11.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
  - MPLAB dsPIC30 Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM.net™ Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
- Evaluation Kits
  - KEELOQ®
  - PICDEM MSC
  - microID®
  - CAN
  - PowerSmart®
  - Analog

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit micro-controller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - absolute listing file (mixed assembly and C)
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

11.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contains source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

• Efficient linking of single libraries instead of many smaller files
• Enhanced code maintainability by grouping related modules together
• Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

11.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce it's object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

• Support for the entire dsPIC30F instruction set
• Support for fixed-point and floating-point data
• Command line interface
• Rich directive set
• Flexible macro language
• MPLAB IDE compatibility

11.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

11.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

11.9 MPLAB ICE 2000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.10 MPLAB ICE 4000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at V$_{DDMIN}$ and V$_{DDMAX}$ for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

11.14 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer, or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs.

11.15 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface, and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

11.16 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18-, 28-, and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs, and sample PIC18F452 and PIC16F877 FLASH microcontrollers.

11.17 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

11.18 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board FLASH memory. A generous prototype area is available for user hardware expansion.

11.19 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

11.20 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three micro-controllers are programmed with firmware to provide LIN bus communication.

11.21 PICkit™ 1 FLASH Starter Kit

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC® microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB® IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC® Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

11.22 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

11.23 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA® development kit
- microID development and rfLab™ development software
- SEEVAL® designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits.

NOTES:

12.0   ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias..-40 to +125°C

Storage temperature .... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... -0.3 to +6.5V

Voltage on $\overline{MCLR}$ with respect to Vss ....-0.3 to +13.5V

Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)

Total power dissipation[1] ....800 mW

Maximum current out of V_{SS} pin .... 300 mA

Maximum current into V_{DD} pin .... 250 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})..± 20 mA

Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD})...± 20 mA

Maximum output current sunk by any I/O pin... 25 mA

Maximum output current sourced by any I/O pin .... 25 mA

Maximum current sunk by PORTA and PORTC (combined) .... 200 mA

Maximum current sourced PORTA and PORTC (combined)... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD}$ x {I_{DD} - $\sum I_{OH}$} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OI} x I_{OL}).

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† NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

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FIGURE 12-1: PIC16F630/676 WITH A/D DISABLED VOLTAGE-FREQUENCY GRAPH,
-40°C $\leq$ TA $\leq$ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
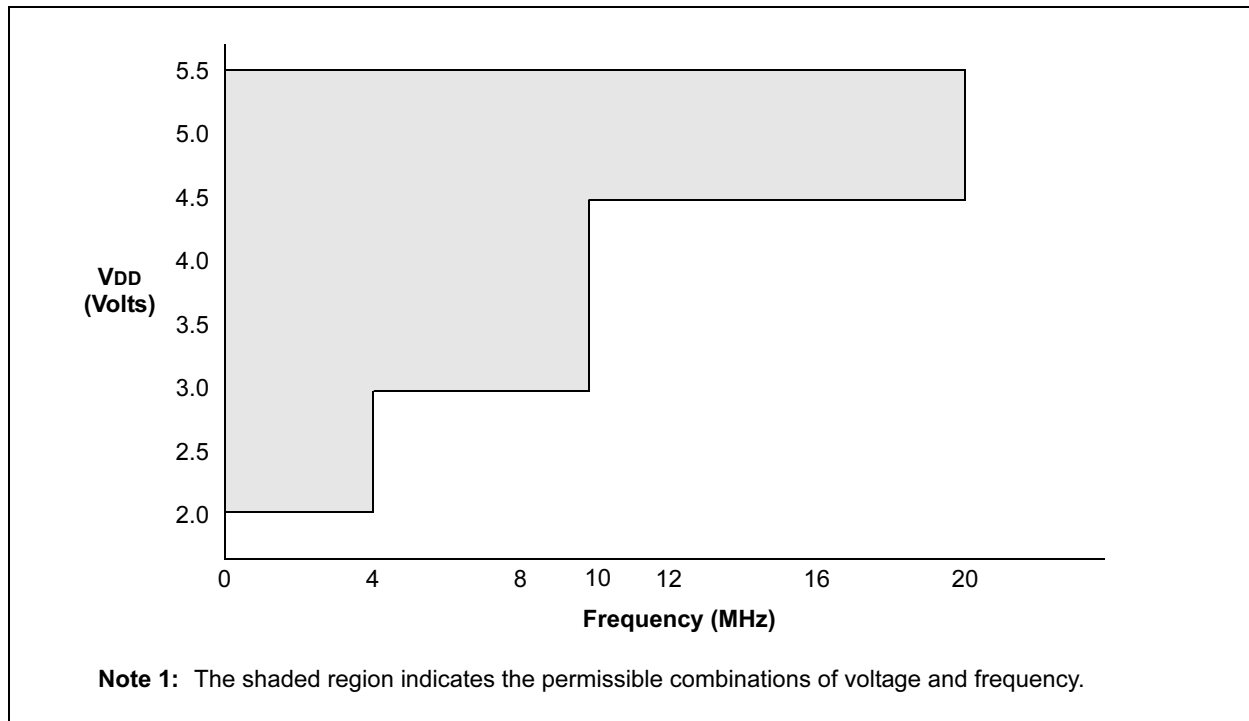
FIGURE 12-2: PIC16F676 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH,
-40°C $\leq$ TA $\leq$ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
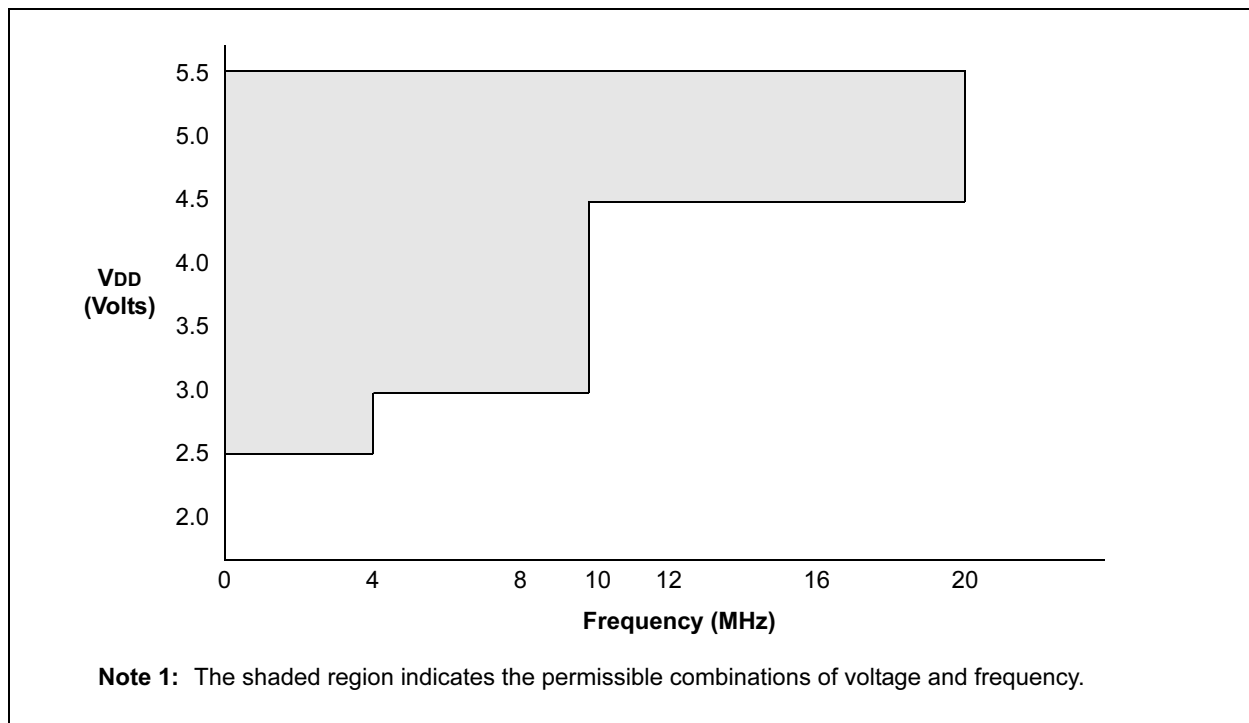
FIGURE 12-3: **PIC16F676 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH,**
0°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

12.1 DC Characteristics: PIC16F630/676-I (Industrial), PIC16F630/676-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A D001B D001C D001D	VDD	**Supply Voltage**	2.0 2.2 2.5 3.0 4.5	— — — — —	5.5 5.5 5.5 5.5 5.5	V V V V V	FOSC < = 4 MHz: PIC16F630/676 with A/D off PIC16F676 with A/D on, 0°C to +125°C PIC16F676 with A/D on, -40°C to +125°C 4 MHz < FOSC < = 10 MHz
D002	VDR	**RAM Data Retention Voltage**[1]	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOD		—	2.1	—	V	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

12.2 DC Characteristics: PIC16F630/676-I (Industrial)

Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	**Supply Current (IDD)**	—	9	16	μA	2.0	FOSC = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011		—	110	150	μA	2.0	FOSC = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012		—	220	280	μA	2.0	FOSC = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013		—	70	110	μA	2.0	FOSC = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014		—	180	250	μA	2.0	FOSC = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015		—	340	450	μA	2.0	FOSC = 4 MHz INTOSC Mode
		—	500	780	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016		—	180	250	μA	2.0	FOSC = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017		—	2.1	2.95	mA	4.5	FOSC = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

12.3 DC Characteristics: PIC16F630/676-I (Industrial)

Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	Power-down Base Current (IPD)	—	0.99	700	nA	2.0	WDT, BOD, Comparators, VREF, and T1OSC disabled
		—	1.2	770	nA	3.0	
		—	2.9	995	nA	5.0	
D021		—	0.3	1.5	μA	2.0	WDT Current[1]
		—	1.8	3.5	μA	3.0	
		—	8.4	17	μA	5.0	
D022		—	58	70	μA	3.0	BOD Current[1]
		—	109	130	μA	5.0	
D023		—	3.3	6.5	μA	2.0	Comparator Current[1]
		—	6.1	8.5	μA	3.0	
		—	11.5	16	μA	5.0	
D024		—	58	70	μA	2.0	CVREF Current[1]
		—	85	100	μA	3.0	
		—	138	160	μA	5.0	
D025		—	4.0	6.5	μA	2.0	T1 OSC Current[1]
		—	4.6	7.0	μA	3.0	
		—	6.0	10.5	μA	5.0	
D026		—	1.2	755	nA	3.0	A/D Current[1]
		—	0.0022	1.0	μA	5.0	

Standard Operating Conditions (unless otherwise stated)
Operating temperature $-40°C \leq T_A \leq +85°C$ for industrial

†   Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2:   The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD.

12.4 DC Characteristics: PIC16F630/676-E (Extended)

Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions VDD	Conditions Note
D010E	**Supply Current (IDD)**	—	9	16	µA	2.0	FOSC = 32 kHz LP Oscillator Mode
		—	18	28	µA	3.0	
		—	35	54	µA	5.0	
D011E		—	110	150	µA	2.0	FOSC = 1 MHz XT Oscillator Mode
		—	190	280	µA	3.0	
		—	330	450	µA	5.0	
D012E		—	220	280	µA	2.0	FOSC = 4 MHz XT Oscillator Mode
		—	370	650	µA	3.0	
		—	0.6	1.4	mA	5.0	
D013E		—	70	110	µA	2.0	FOSC = 1 MHz EC Oscillator Mode
		—	140	250	µA	3.0	
		—	260	390	µA	5.0	
D014E		—	180	250	µA	2.0	FOSC = 4 MHz EC Oscillator Mode
		—	320	470	µA	3.0	
		—	580	850	µA	5.0	
D015E		—	340	450	µA	2.0	FOSC = 4 MHz INTOSC Mode
		—	500	780	µA	3.0	
		—	0.8	1.1	mA	5.0	
D016E		—	180	250	µA	2.0	FOSC = 4 MHz EXTRC Mode
		—	320	450	µA	3.0	
		—	580	800	µA	5.0	
D017E		—	2.1	2.95	mA	4.5	FOSC = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

12.5 DC Characteristics: PIC16F630/676-E (Extended)

Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						Standard Operating Conditions (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +125°C$ for extended	
						V_{DD}	Note
D020E	Power-down Base Current (I_{PD})	—	0.00099	3.5	μA	2.0	WDT, BOD, Comparators, V_{REF}, and T1OSC disabled
		—	0.0012	4.0	μA	3.0	
		—	0.0029	8.0	μA	5.0	
D021E		—	0.3	6.0	μA	2.0	WDT Current[1]
		—	1.8	9.0	μA	3.0	
		—	8.4	20	μA	5.0	
D022E		—	58	70	μA	3.0	BOD Current[1]
		—	109	130	μA	5.0	
D023E		—	3.3	10	μA	2.0	Comparator Current[1]
		—	6.1	13	μA	3.0	
		—	11.5	24	μA	5.0	
D024E		—	58	70	μA	2.0	CV_{REF} Current[1]
		—	85	100	μA	3.0	
		—	138	165	μA	5.0	
D025E		—	4.0	10	μA	2.0	T1 O_{SC} Current[1]
		—	4.6	12	μA	3.0	
		—	6.0	20	μA	5.0	
D026E		—	0.0012	6.0	μA	3.0	A/D Current[1]
		—	0.0022	8.5	μA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{DD} or I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD}.

12.6 DC Characteristics: PIC16F630/676-I (Industrial), PIC16F630/676-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	V$_{IL}$	**Input Low Voltage** I/O ports					
D030		with TTL buffer	Vss		0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			Vss		0.15 VDD	V	Otherwise
D031		with Schmitt Trigger buffer	Vss		0.2 VDD	V	Entire range
D032		$\overline{MCLR}$, OSC1 (RC mode)	Vss		0.2 VDD	V	
D033		OSC1 (XT and LP modes)	Vss		0.3	V	**(Note 1)**
D033A		OSC1 (HS mode)	Vss		0.3 VDD	V	**(Note 1)**
	V$_{IH}$	**Input High Voltage** I/O ports					
D040		with TTL buffer	2.0		VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25 VDD+0.8)		VDD	V	otherwise
D041		with Schmitt Trigger buffer	0.8 VDD		VDD		entire range
D042		$\overline{MCLR}$	0.8 VDD		VDD	V	
D043		OSC1 (XT and LP modes)	1.6		VDD	V	**(Note 1)**
D043A		OSC1 (HS mode)	0.7 VDD		VDD	V	**(Note 1)**
D043B		OSC1 (RC mode)	0.9 VDD		VDD	V	
D070	I$_{PUR}$	**PORTA Weak Pull-up Current**	50*	250	400*	μA	VDD = 5.0V, VPIN = Vss
	I$_{IL}$	**Input Leakage Current[3]**					
D060		I/O ports		± 0.1	± 1	μA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A		Analog inputs		± 0.1	± 1	μA	Vss ≤ VPIN ≤ VDD
D060B		V$_{REF}$		± 0.1	± 1	μA	Vss ≤ VPIN ≤ VDD
D061		$\overline{MCLR}$[2]		± 0.1	± 5	μA	Vss ≤ VPIN ≤ VDD
D063		OSC1		± 0.1	± 5	μA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	V$_{OL}$	**Output Low Voltage** I/O ports					
D080		I/O ports			0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
D083		OSC2/CLKOUT (RC mode)			0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.) IOL = 1.2 mA, VDD = 4.5V (Ext.)
	V$_{OH}$	**Output High Voltage** I/O ports					
D090		I/O ports	VDD - 0.7			V	IOH = -3.0 mA, VDD = 4.5V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD - 0.7			V	IOH = -1.3 mA, VDD = 4.5V (Ind.) IOH = -1.0 mA, VDD = 4.5V (Ext.)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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12.7 DC Characteristics: PIC16F630/676-I (Industrial), PIC16F630/676-E (Extended) (Cont.)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh[1]	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program FLASH Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

*   These parameters are characterized but not tested.

†   Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See Section 8.5.1 for additional information.

12.8   TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T				
F	Frequency		T	Time

Lowercase letters (pp) and their meanings:

pp				
cc	CCP1		osc	OSC1
ck	CLKOUT		rd	$\overline{RD}$
cs	$\overline{CS}$		rw	$\overline{RD}$ or $\overline{WR}$
di	SDI		sc	SCK
do	SDO		ss	$\overline{SS}$
dt	Data in		t0	T0CKI
io	I/O port		t1	T1CKI
mc	$\overline{MCLR}$		wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
F	Fall		P	Period
H	High		R	Rise
I	Invalid (Hi-impedance)		V	Valid
L	Low		Z	Hi-impedance

FIGURE 12-4:   LOAD CONDITIONS
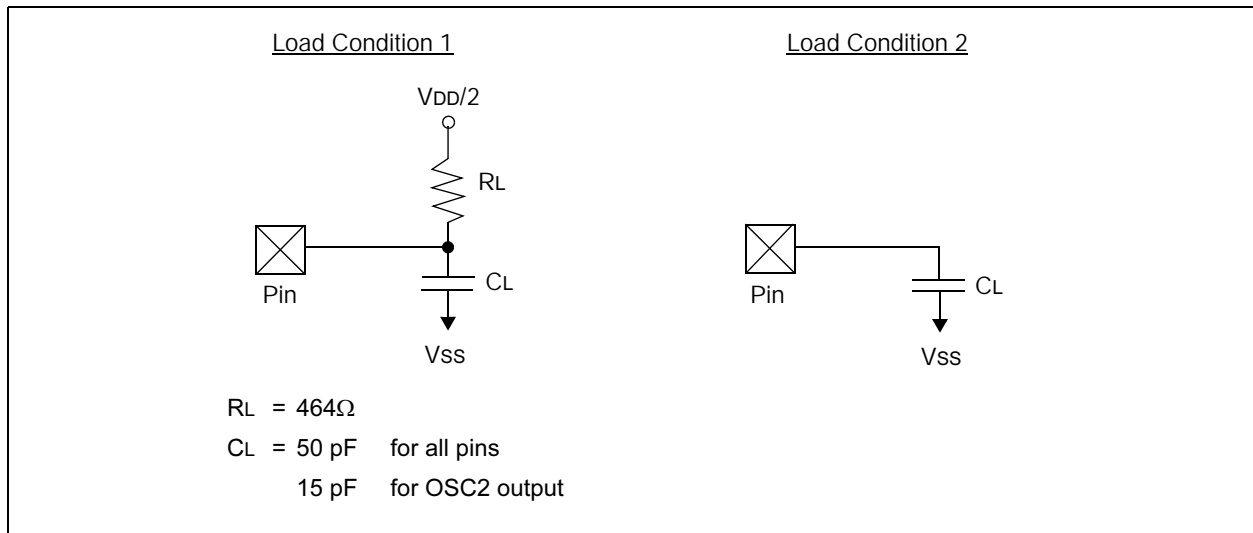
PIC16F630/676

12.9 AC CHARACTERISTICS: PIC16F630/676 (INDUSTRIAL, EXTENDED)

FIGURE 12-5: EXTERNAL CLOCK TIMING
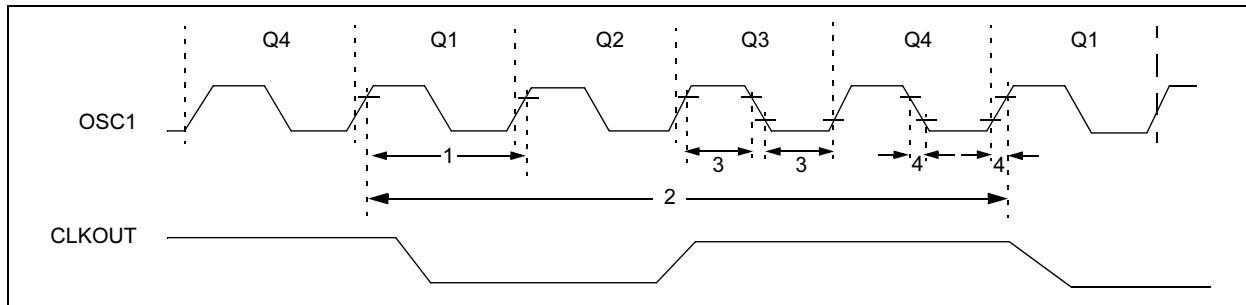
TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency[1]	DC	—	37	kHz	LP Osc mode
			DC	—	4	MHz	XT mode
			DC	—	20	MHz	HS mode
			DC	—	20	MHz	EC mode
		Oscillator Frequency[1]	5	—	37	kHz	LP Osc mode
			—	4	—	MHz	INTOSC mode
			DC	—	4	MHz	RC Osc mode
			0.1	—	4	MHz	XT Osc mode
			1	—	20	MHz	HS Osc mode
1	TOSC	External CLKIN Period[1]	27	—	∞	μs	LP Osc mode
			50	—	∞	ns	HS Osc mode
			50	—	∞	ns	EC Osc mode
			250	—	∞	ns	XT Osc mode
		Oscillator Period[1]	27	—	200	μs	LP Osc mode
			—	250	—	ns	INTOSC mode
			250	—	—	ns	RC Osc mode
			250	—	10,000	ns	XT Osc mode
			50	—	1,000	ns	HS Osc mode
2	TCY	Instruction Cycle Time[1]	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL, TosH	External CLKIN (OSC1) High External CLKIN Low	2*	—	—	μs	LP oscillator, TOSC L/H duty cycle
			20*	—	—	ns	HS oscillator, TOSC L/H duty cycle
			100 *	—	—	ns	XT oscillator, TOSC L/H duty cycle
4	TosR, TosF	External CLKIN Rise External CLKIN Fall	—	—	50*	ns	LP oscillator
			—	—	25*	ns	XT oscillator
			—	—	15*	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

TABLE 12-2: **PRECISION INTERNAL OSCILLATOR PARAMETERS**

Param No.	Sym	Characteristic	Freq Tolerance	Min	Typ†	Max	Units	Conditions
F10	F_{OSC}	Internal Calibrated INTOSC Frequency	±1	3.96	4.00	4.04	MHz	VDD = 3.5V, 25°C
			±2	3.92	4.00	4.08	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			±5	3.80	4.00	4.20	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (IND) -40°C ≤ TA ≤ +125°C (EXT)
F14	T_{IOSC} ST	Oscillator Wake-up from SLEEP start-up time*	—	—	6	8	μs	VDD = 2.0V, -40°C to +85°C
			—	—	4	6	μs	VDD = 3.0V, -40°C to +85°C
			—	—	3	5	μs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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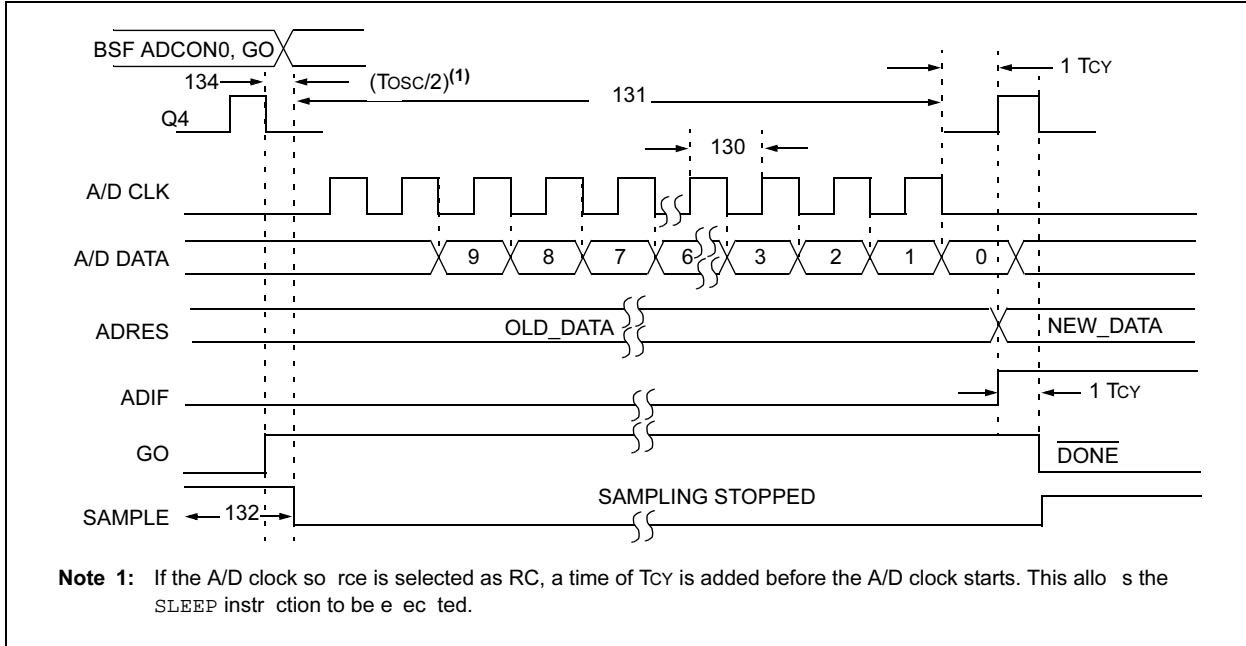**FIGURE 12-6:** CLKOUT AND I/O TIMING
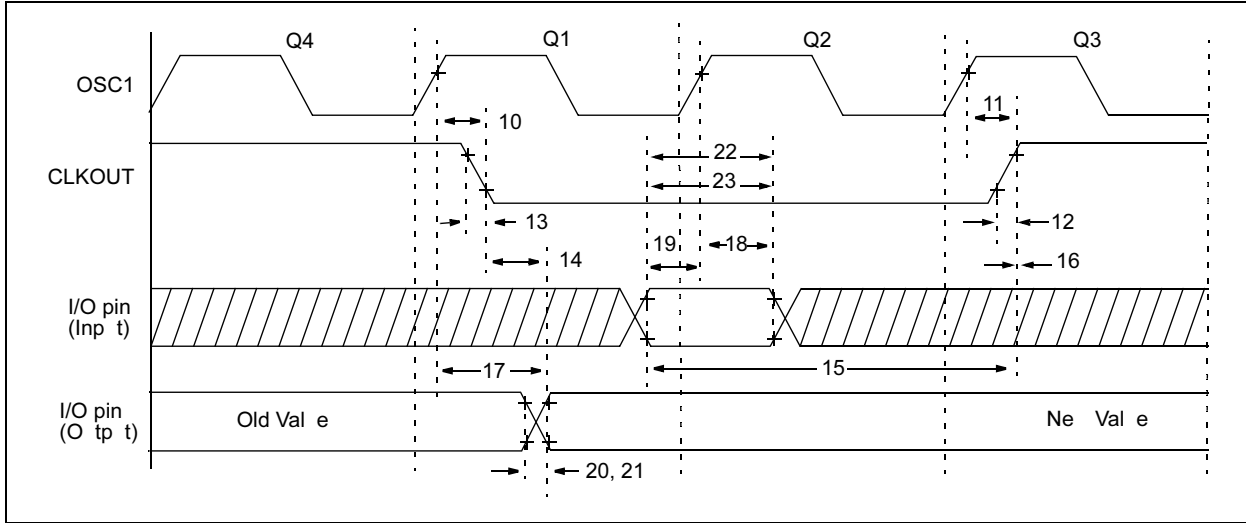
TABLE 12-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLOUT↓	—	75	200	ns	**(Note 1)**
11	TosH2ckH	OSC1↑ to CLOUT↑	—	75	200	ns	**(Note 1)**
12	TckR	CLKOUT rise time	—	35	100	ns	**(Note 1)**
13	TckF	CLKOUT fall time	—	35	100	ns	**(Note 1)**
14	TckL2ioV	CLKOUT↓ to Port out valid	—	—	20	ns	**(Note 1)**
15	TioV2ckH	Port in valid before CLKOUT↑	T$_{OSC}$ + 200 ns	—	—	ns	**(Note 1)**
16	TckH2ioI	Port in hold after CLKOUT↑	0	—	—	ns	**(Note 1)**
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150 *	ns	
			—	—	300	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TioR	Port output rise time	—	10	40	ns	
21	TioF	Port output fall time	—	10	40	ns	
22	Tinp	INT pin high or low time	25	—	—	ns	
23	Trbp	PORTA change INT high or low time	T$_{CY}$	—	—	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4xT$_{OSC}$.

FIGURE 12-7: **RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**
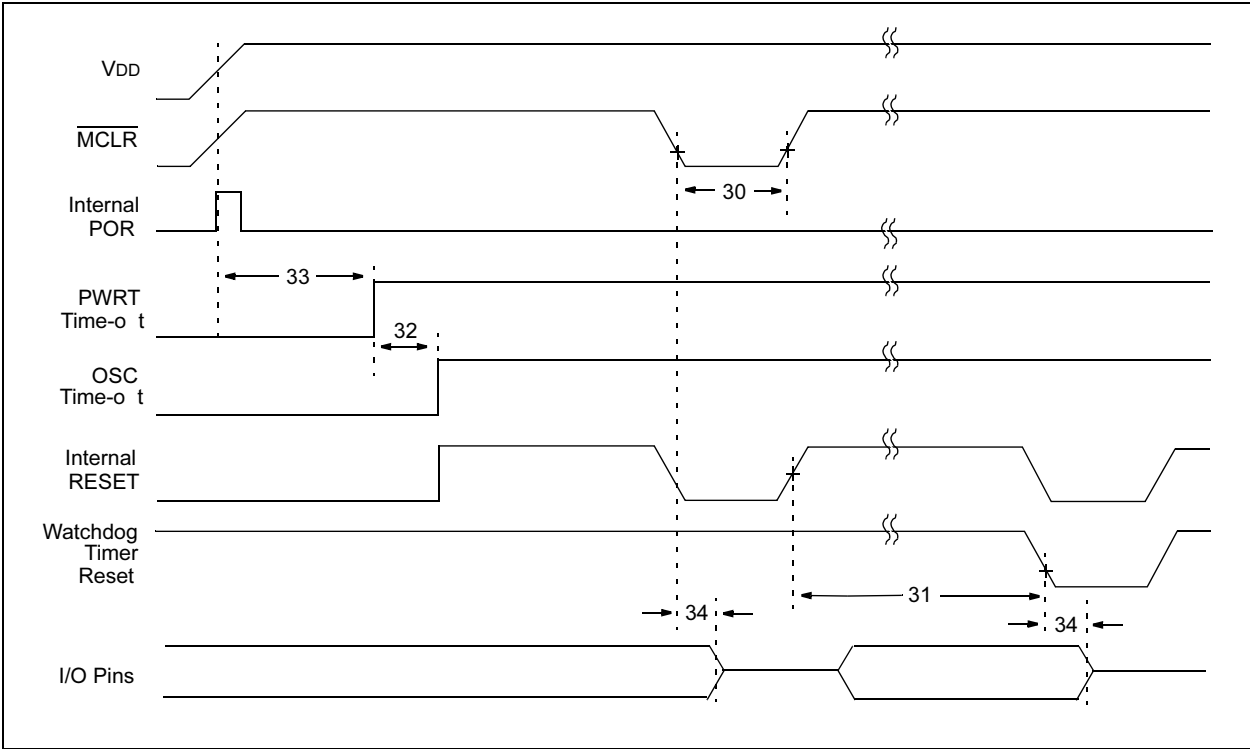
FIGURE 12-8: **BROWN-OUT DETECT TIMING AND CHARACTERISTICS**

Note 1: 72 ms dela onl if $\overline{\text{PWRTE}}$ bit in config ration ord is programmed to '0'.
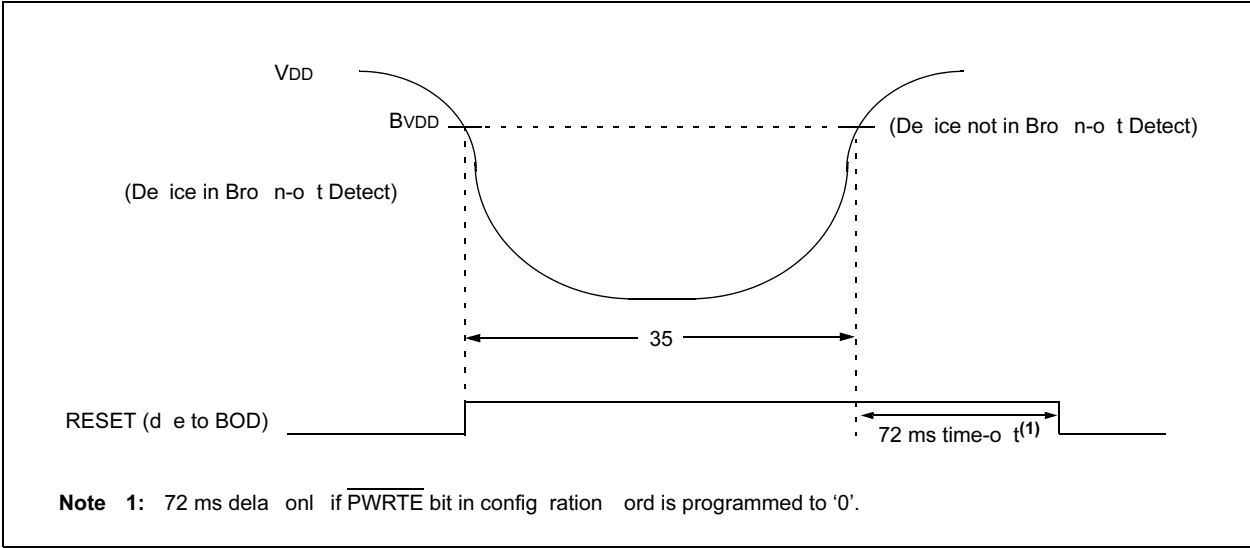
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TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	T_{MCL}	$\overline{MCLR}$ Pulse Width (low)	2 11	— 18	— 24	μs ms	V_{DD} = 5V, -40°C to +85°C Extended temperature
31	T_{WDT}	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	V_{DD} = 5V, -40°C to +85°C Extended temperature
32	T_{OST}	Oscillation Start-up Timer Period	—	1024T_{OSC}	—	—	T_{OSC} = OSC1 period
33*	T_{PWRT}	Power-up Timer Period	28* TBD	72 TBD	132* TBD	ms ms	V_{DD} = 5V, -40°C to +85°C Extended Temperature
34	T_{IOZ}	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	μs	
	B_{VDD}	Brown-out Detect Voltage	2.025	—	2.175	V	
		Brown-out Hysteresis	TBD	—	—	—	
35	T_{BOD}	Brown-out Detect Pulse Width	100*	—	—	μs	$V_{DD} \leq B_{VDD}$ (D005)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS
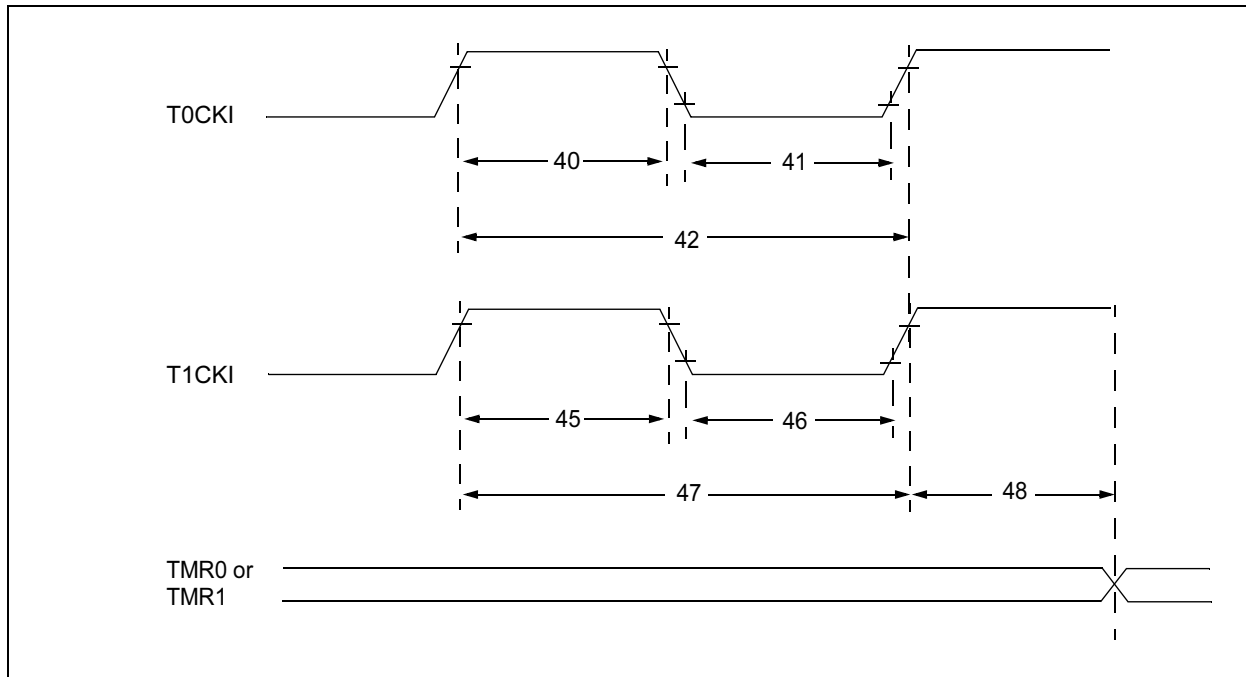
TABLE 12-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20			ns	
			With Prescaler	10			ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20			ns	
			With Prescaler	10			ns	
42*	Tt0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$			ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20			ns	
			Synchronous, with Prescaler	15			ns	
			Asynchronous	30			ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20			ns	
			Synchronous, with Prescaler	15			ns	
			Asynchronous	30			ns	
47*	Tt1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$			ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60			ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC		200*	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment		2 TOSC*		7 TOSC*		

* These parameters are characterized but not tested.
Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are
not tested.

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TABLE 12-6: COMPARATOR SPECIFICATIONS

Comparator Specifications		Standard Operating Conditions -40°C to +125°C (unless otherwise stated)				
Sym	Characteristics	Min	Typ	Max	Units	Comments
VOS	Input Offset Voltage	—	± 5.0	± 10	mV	
VCM	Input Common Mode Voltage	0	—	VDD - 1.5	V	
CMRR	Common Mode Rejection Ratio	+55*	—	—	db	
TRT	Response Time[1]	—	150	400*	ns	
TMC2COV	Comparator Mode Change to Output Valid	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD - 1.5V.

TABLE 12-7: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

Voltage Reference Specifications		Standard Operating Conditions -40°C to +125°C (unless otherwise stated)				
Sym	Characteristics	Min	Typ	Max	Units	Comments
	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Absolute Accuracy	— —	— —	± 1/2* ± 1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Unit Resistor Value (R)	—	2k*	—	Ω	
	Settling Time[1]	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from `0000` to `1111`.

TABLE 12-8: PIC16F676 A/D CONVERTER CHARACTERISTICS:

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	N$_R$	Resolution	—	—	10 bits	bit	
A02	E$_{ABS}$	Total Absolute Error*	—	—	±1	LSb	V$_{REF}$ = 5.0V
A03	E$_{IL}$	Integral Error	—	—	±1	LSb	V$_{REF}$ = 5.0V
A04	E$_{DL}$	Differential Error	—	—	±1	LSb	No missing codes to 10 bits V$_{REF}$ = 5.0V
A05	E$_{FS}$	Full Scale Range	2.2*	—	5.5*	V	
A06	E$_{OFF}$	Offset Error	—	—	±1	LSb	V$_{REF}$ = 5.0V
A07	E$_{GN}$	Gain Error	—	—	±1	LSb	V$_{REF}$ = 5.0V
A10	—	Monotonicity	—	g aranteed[3]	—	—	V$_{SS}$ ≤ V$_{AIN}$ ≤ V$_{REF}$+
A20 A20A	V$_{REF}$	Reference Voltage	2.0 2.5	—	— V$_{DD}$ + 0.3	V	Absolute minimum to ensure 10-bit accuracy
A21	V$_{REF}$	Reference V High (V$_{DD}$ or V$_{REF}$)	V$_{SS}$	—	V$_{DD}$	V	
A25	V$_{AIN}$	Analog Input Voltage	V$_{SS}$	—	V$_{REF}$	V	
A30	Z$_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	I$_{REF}$	V$_{REF}$ Input Current[2]	10	—	1000	μA	During V$_{AIN}$ acquisition. Based on differential of V$_{HOLD}$ to V$_{AIN}$.
			—	—	10	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: V$_{REF}$ current is from External V$_{REF}$ or V$_{DD}$ pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

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FIGURE 12-10: **PIC16F676 A/D CONVERSION TIMING (NORMAL MODE)**

Note 1: If the A/D clock source is selected as RC, a time of T$_{CY}$ is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 12-9: **PIC16F676 A/D CONVERSION REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	T$_{AD}$	A/D Clock Period	1.6	—	—	μs	T$_{OSC}$ based, V$_{REF}$ ≥ 3.0V
			3.0*	—	—	μs	T$_{OSC}$ based, V$_{REF}$ full range
130	T$_{AD}$	A/D Internal RC Oscillator Period	3.0*	6.0	9.0*	μs	ADCS<1:0> = 11 (RC mode) At V$_{DD}$ = 2.5V
			2.0*	4.0	6.0*	μs	At V$_{DD}$ = 5.0V
131	T$_{CNV}$	Conversion Time (not including Acquisition Time)[1]	—	11	—	T$_{AD}$	Set GO bit to new data in A/D result register
132	T$_{ACQ}$	Acquisition Time	(Note 2)	11.5	—	μs	
			5*	—	—	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on C$_{HOLD}$).
134	T$_{GO}$	Q4 to A/D Clock Start	—	T$_{OSC}$/2	—	—	If the A/D clock source is selected as RC, a time of T$_{CY}$ is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

 * These parameters are characterized but not tested.

 † Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T$_{CY}$ cycle.
  2: See Table 7-1 for minimum conditions.

FIGURE 12-11: **PIC16F676 A/D CONVERSION TIMING (SLEEP MODE)**

Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.
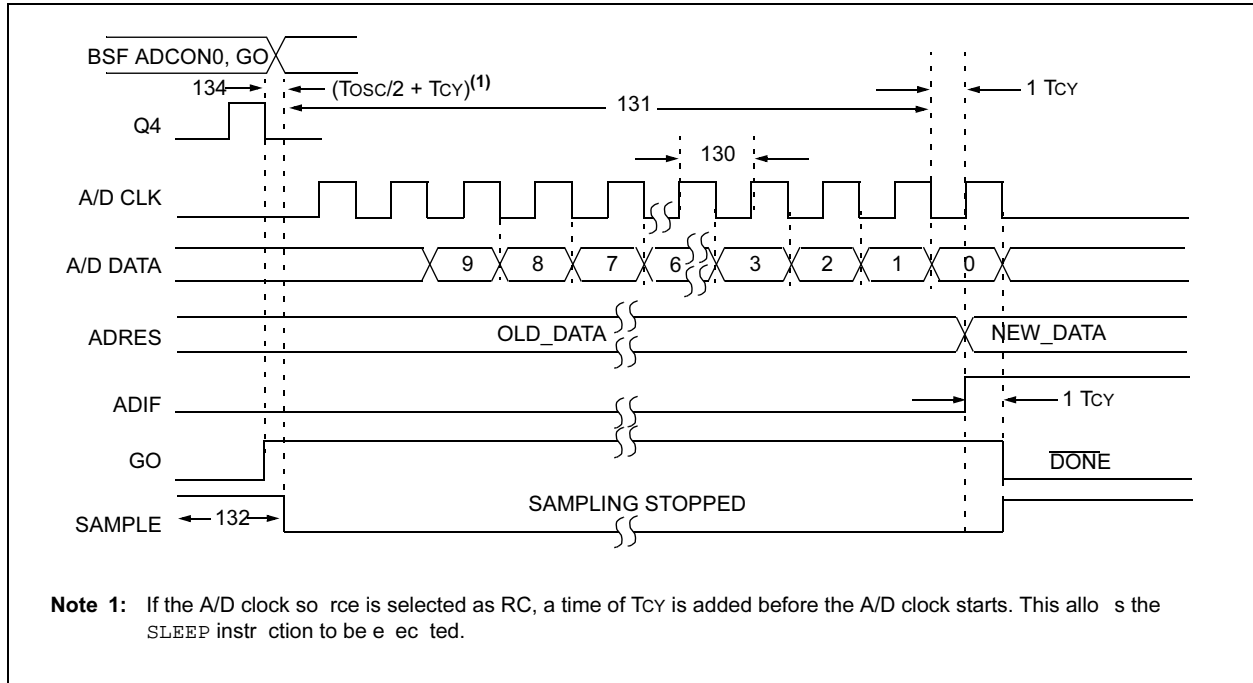
TABLE 12-10: PIC16F676 A/D CONVERSION REQUIREMENTS (SLEEP MODE)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	T_{AD}	A/D Clock Period	1.6	—	—	μs	$V_{REF} \geq 3.0V$
			3.0*	—	—	μs	V_{REF} full range
130	T_{AD}	A/D Internal RC Oscillator Period					ADCS<1:0> = `11` (RC mode)
			3.0*	6.0	9.0*	μs	At V_{DD} = 2.5V
			2.0*	4.0	6.0*	μs	At V_{DD} = 5.0V
131	T_{CNV}	Conversion Time (not including Acquisition Time)[1]	—	11	—	T_{AD}	
132	T_{ACQ}	Acquisition Time	**(Note 2)**	11.5	—	μs	
			5*	—	—	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on C_{HOLD}).
134	T_{GO}	Q4 to A/D Clock Start	—	$T_{OSC}/2 + T_{CY}$	—	—	If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

    * These parameters are characterized but not tested.

    † Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{CY} cycle.

    2: See Table 7-1 for minimum conditions.

NOTES:

13.0   DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C. 'Max' or 'min' represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.

FIGURE 13-1:   TYPICAL I_{PD} vs. V_{DD} OVER TEMP (-40°C TO +25°C)
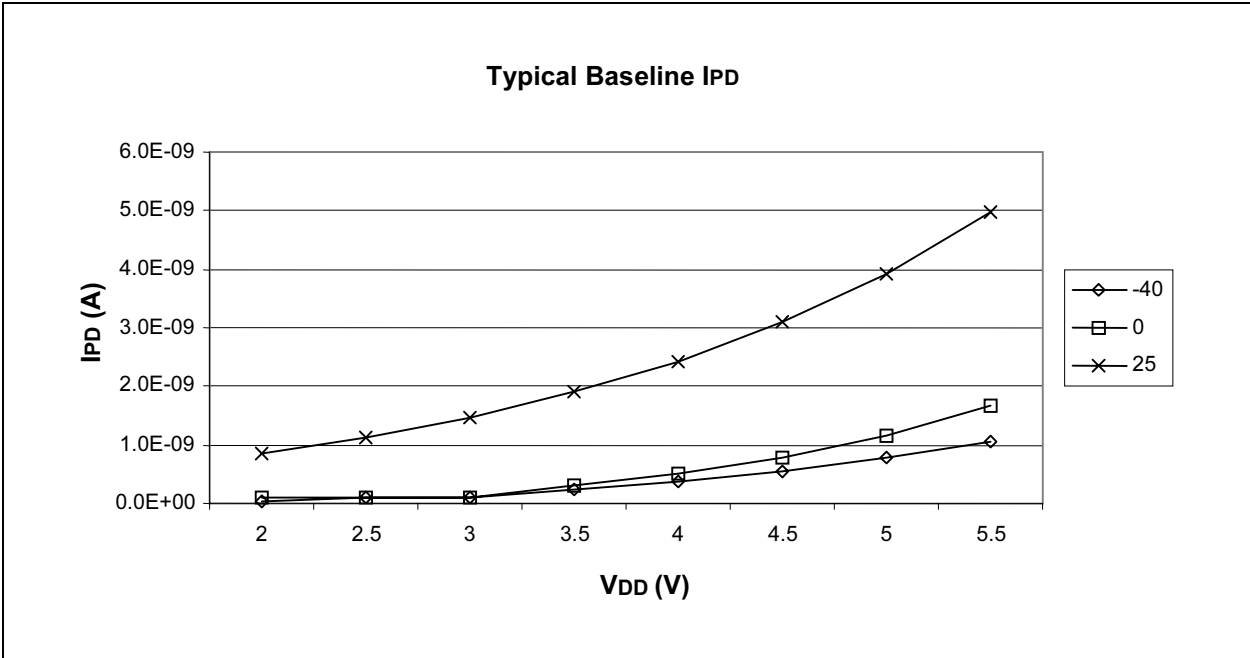
FIGURE 13-2:   TYPICAL I_{PD} vs. V_{DD} OVER TEMP (+85°C)
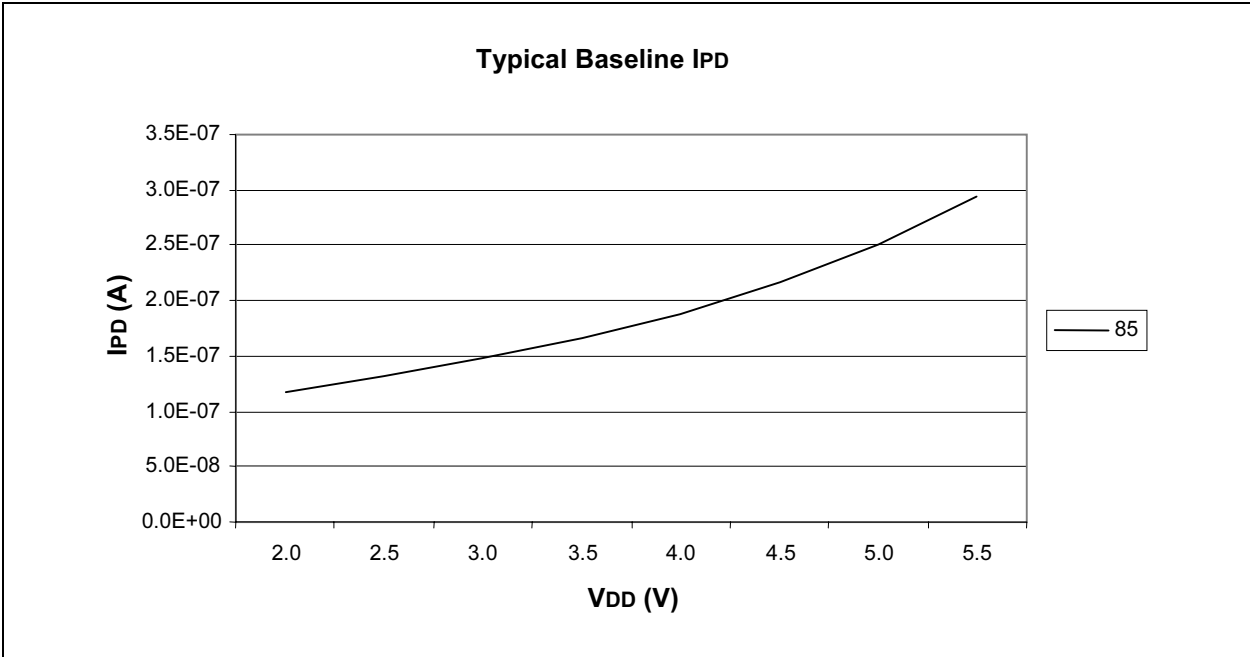
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FIGURE 13-3: **TYPICAL I_{PD} vs. V_{DD} OVER TEMP (+125°C)**

Typical Baseline I_{PD}
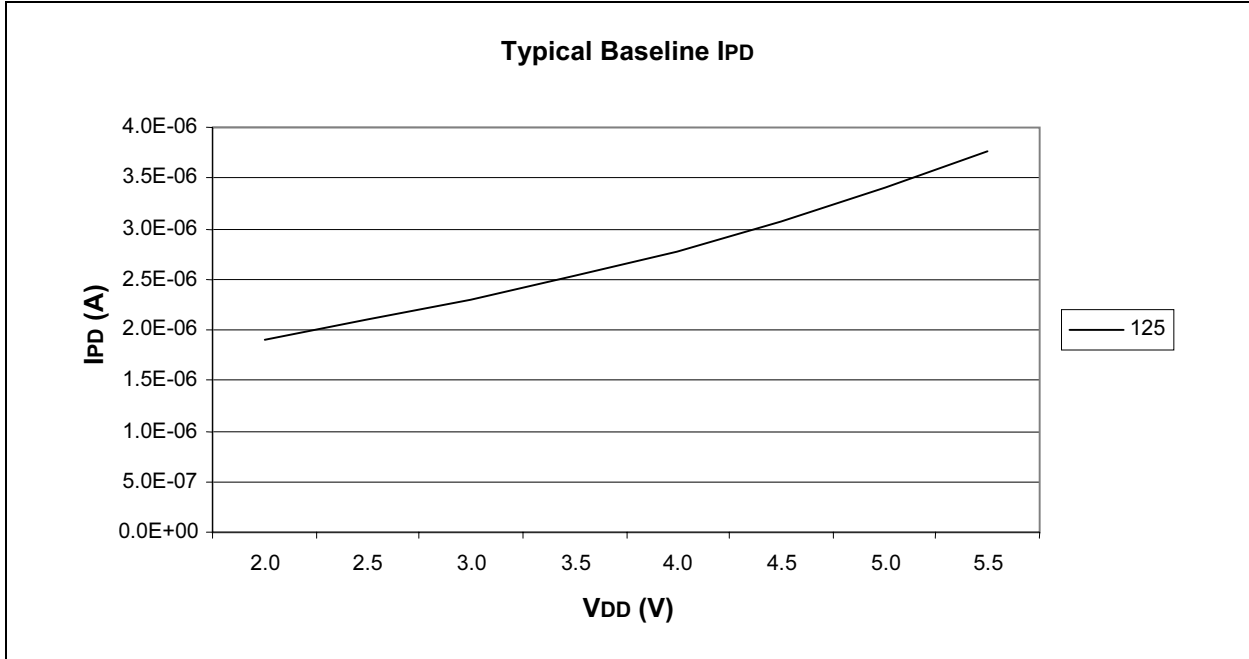
FIGURE 13-4: **MAXIMUM I_{PD} vs. V_{DD} OVER TEMP (-40°C TO +25°C)**

Maximum Baseline I_{PD}
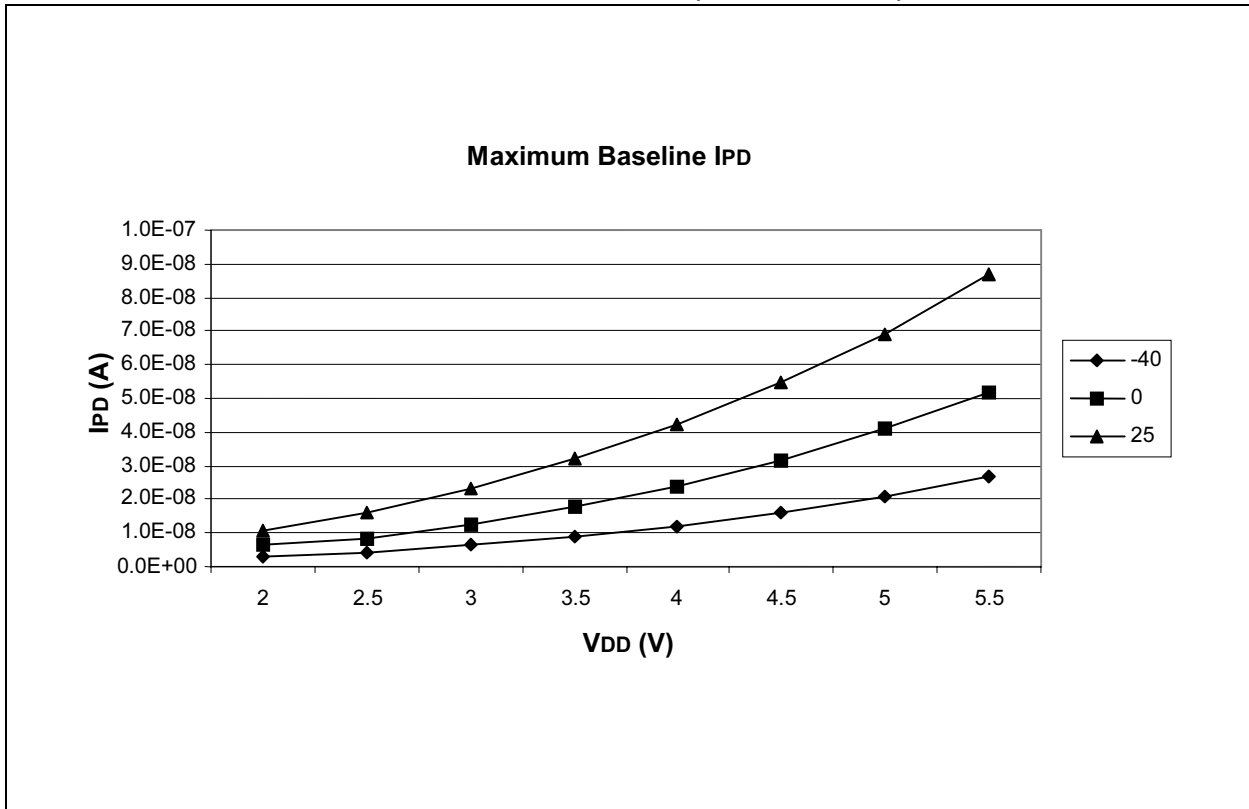
FIGURE 13-5: **MAXIMUM IPD vs. VDD OVER TEMP (+85°C)**

Maximum Baseline IPD
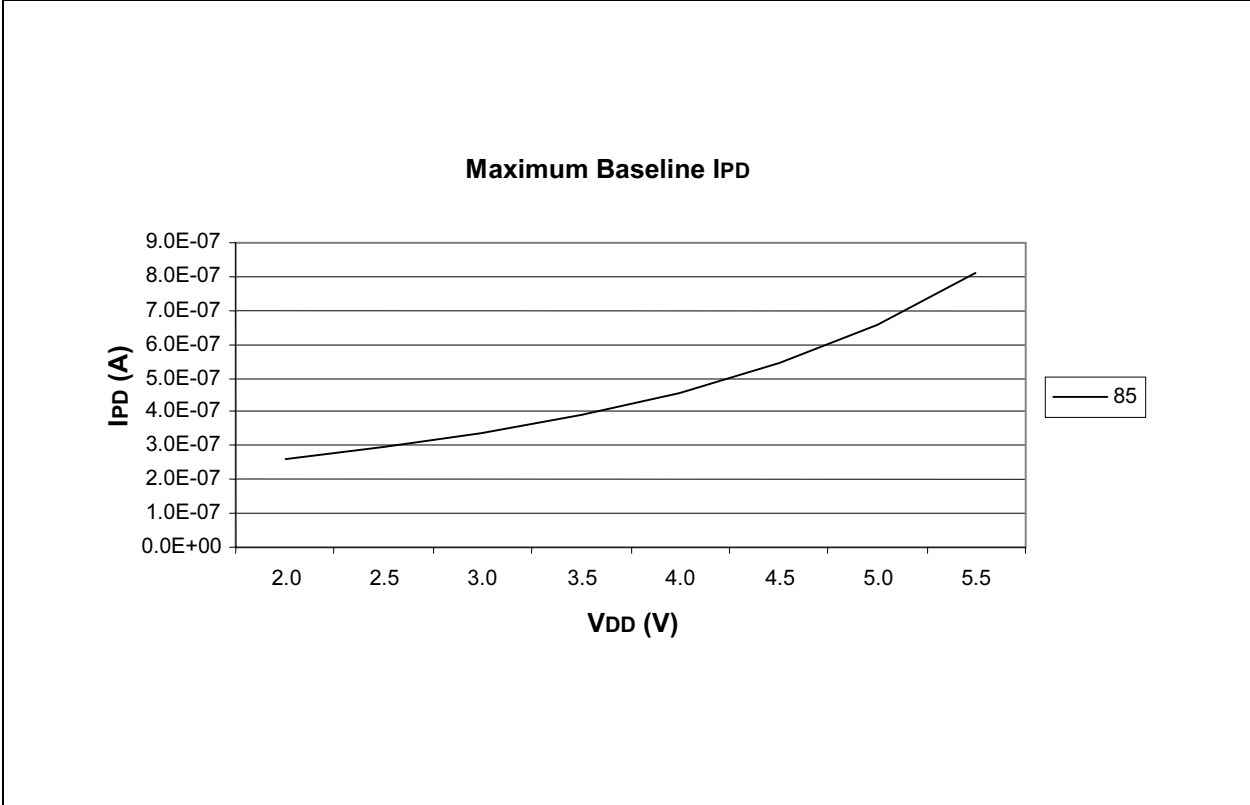
FIGURE 13-6: **MAXIMUM IPD vs. VDD OVER TEMP (+125°C)**
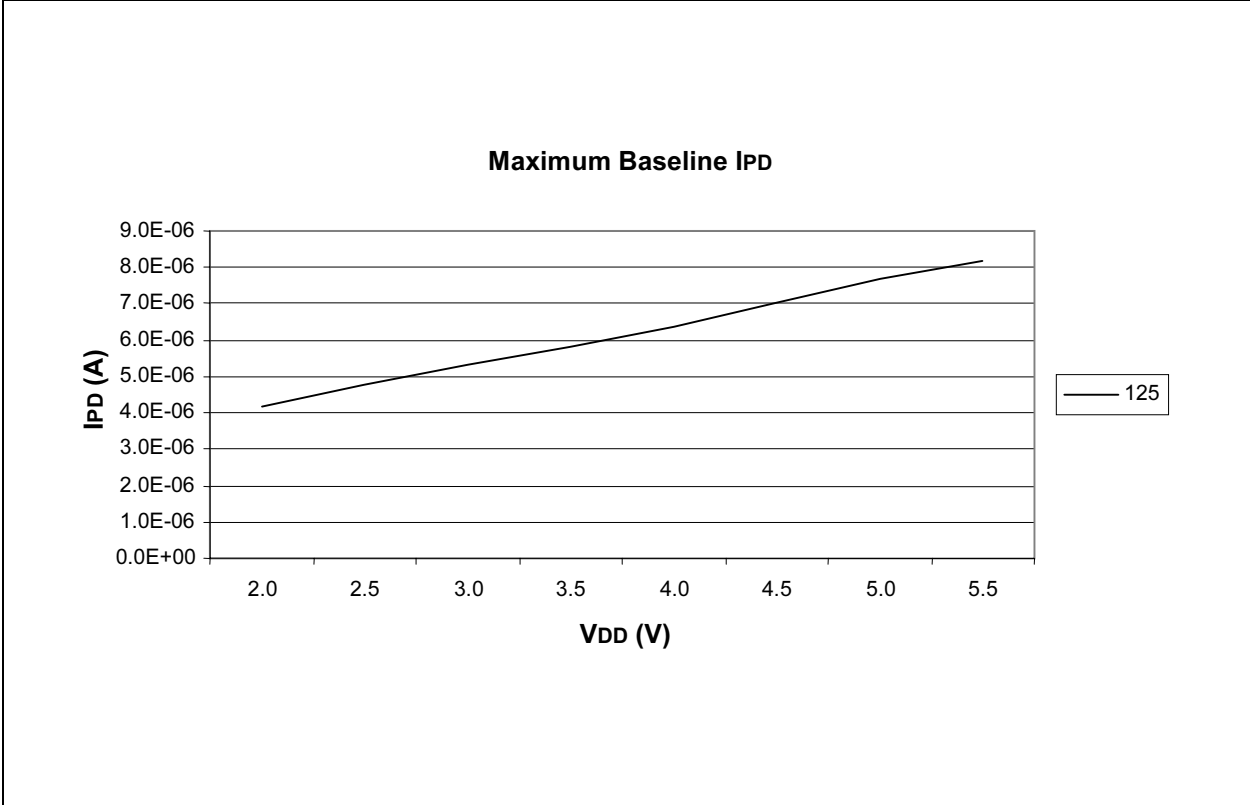
Maximum Baseline IPD

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Typical BOD I$_{PD}$

Typical Comparator I$_{PD}$
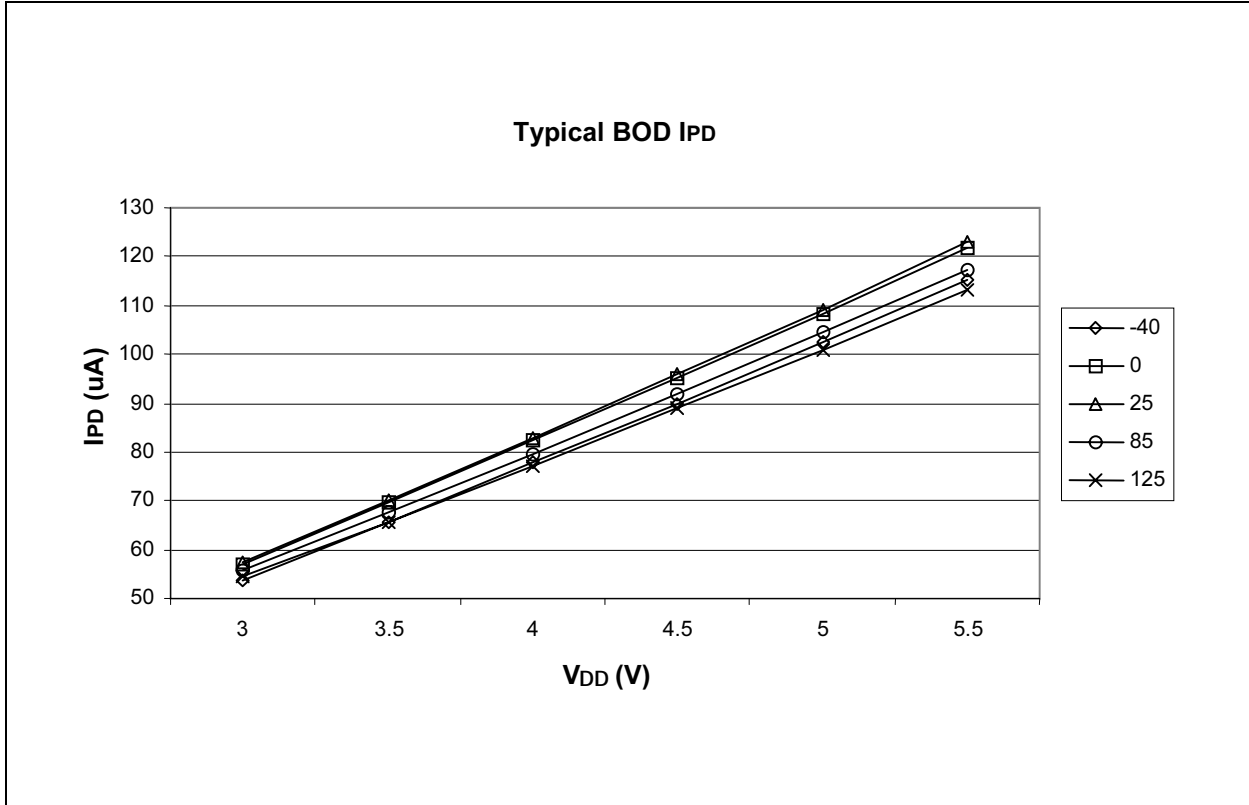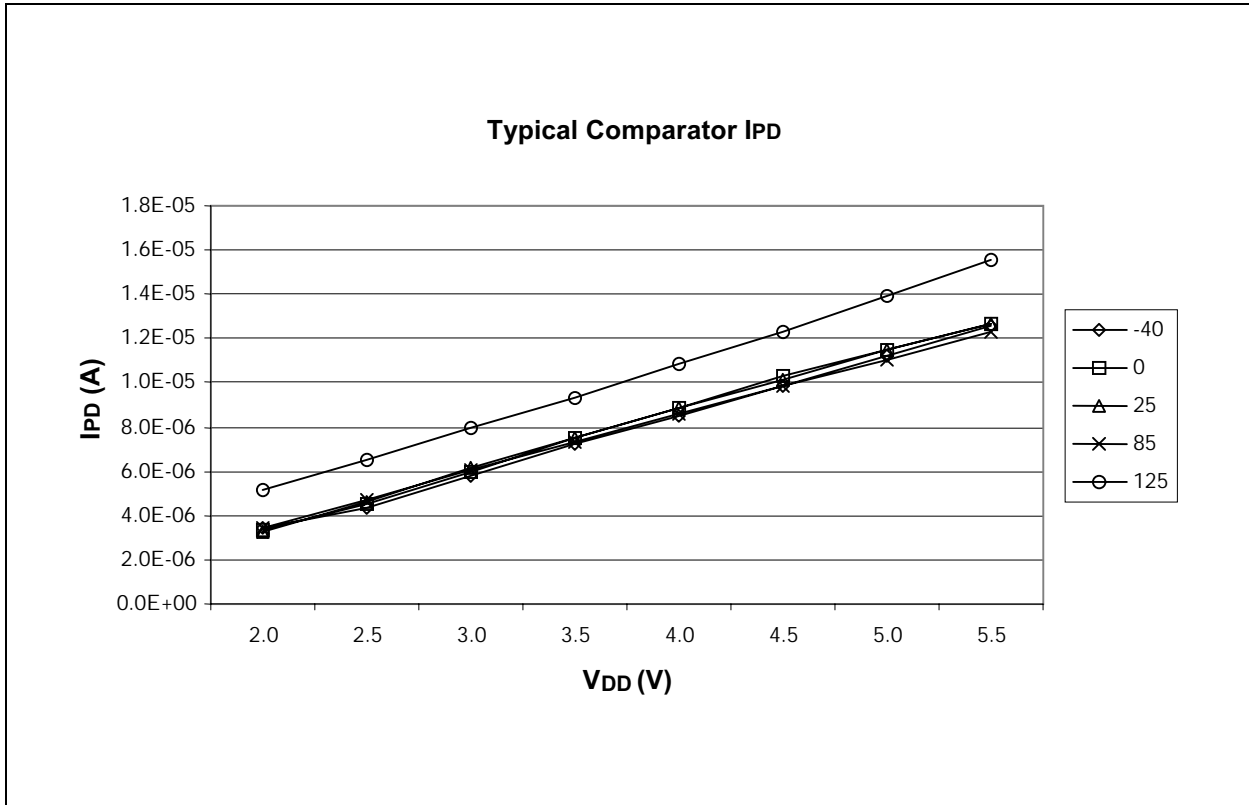
FIGURE 13-9: TYPICAL I_{PD} WITH A/D ENABLED vs. V_{DD} OVER TEMP (-40°C TO +25°C)

Typical A/D I_{PD}
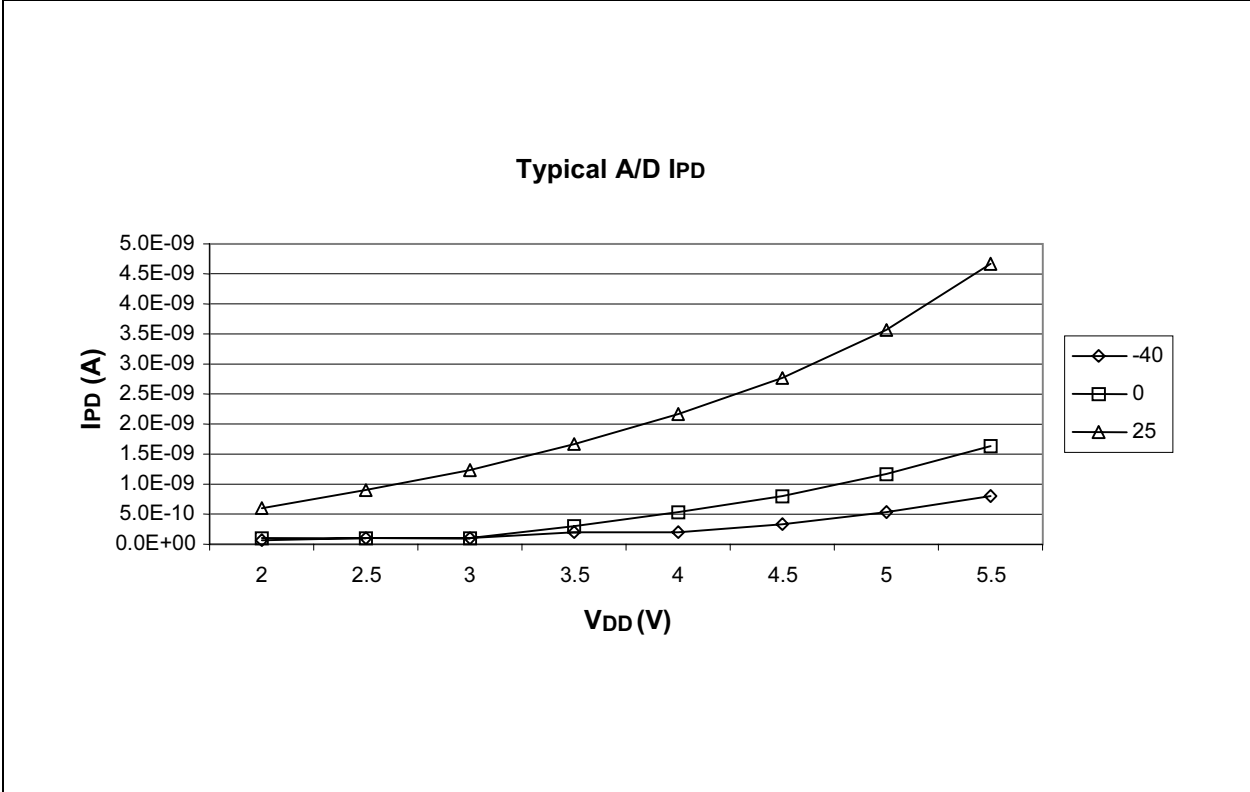
FIGURE 13-10: TYPICAL I_{PD} WITH A/D ENABLED vs. V_{DD} OVER TEMP (+85°C)

Typical A/D I_{PD}
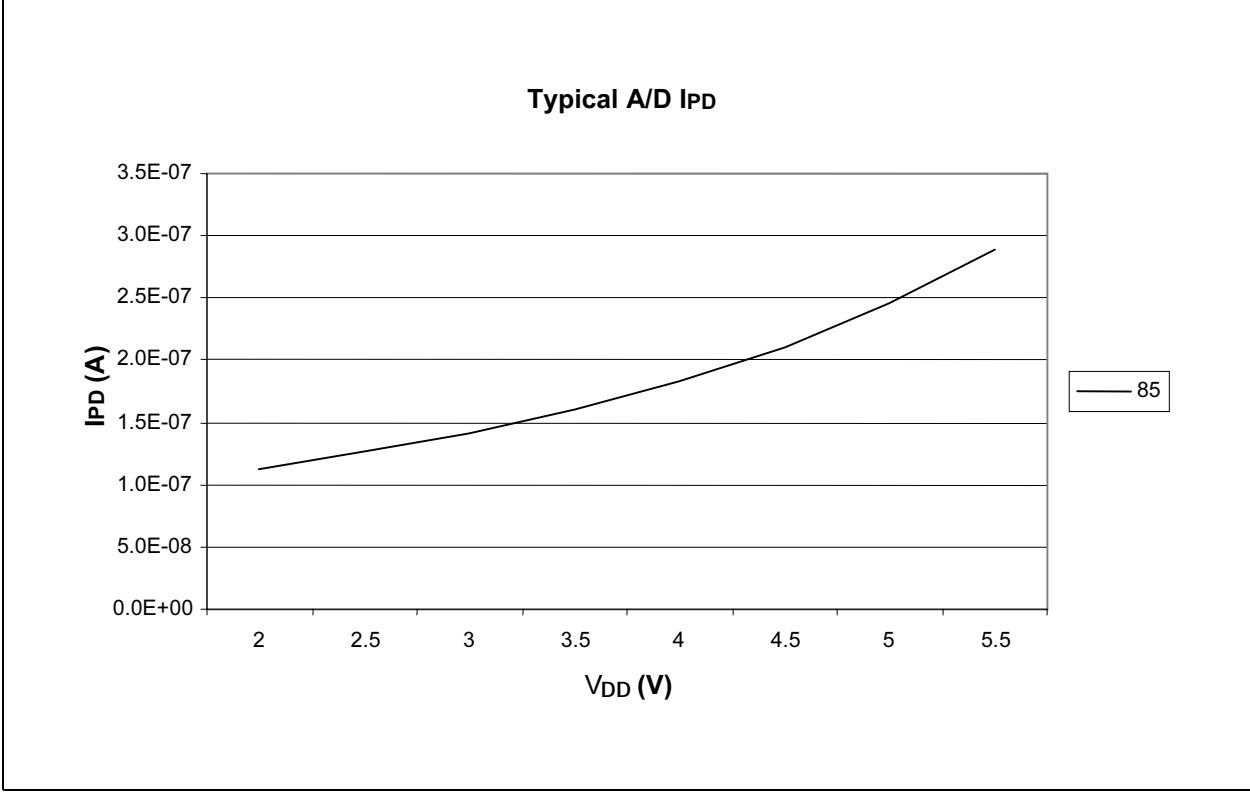
PIC16F630/676

FIGURE 13-11: **TYPICAL I**PD **WITH A/D ENABLED vs. V**DD **OVER TEMP (+125°C)**
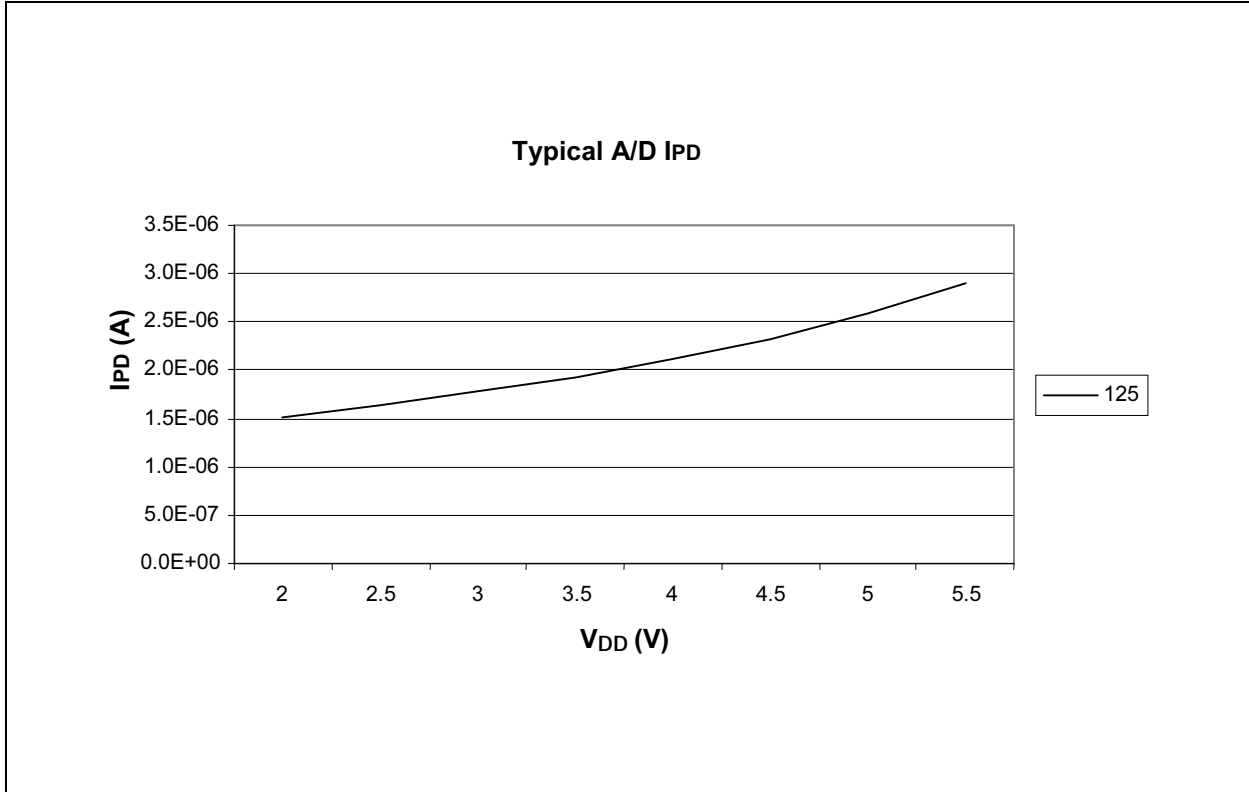
FIGURE 13-12: **TYPICAL I**PD **WITH T1 OSC ENABLED vs. V**DD **OVER TEMP (-40°C TO +125°C), 32 KHZ, C1 AND C2=50 pF)**
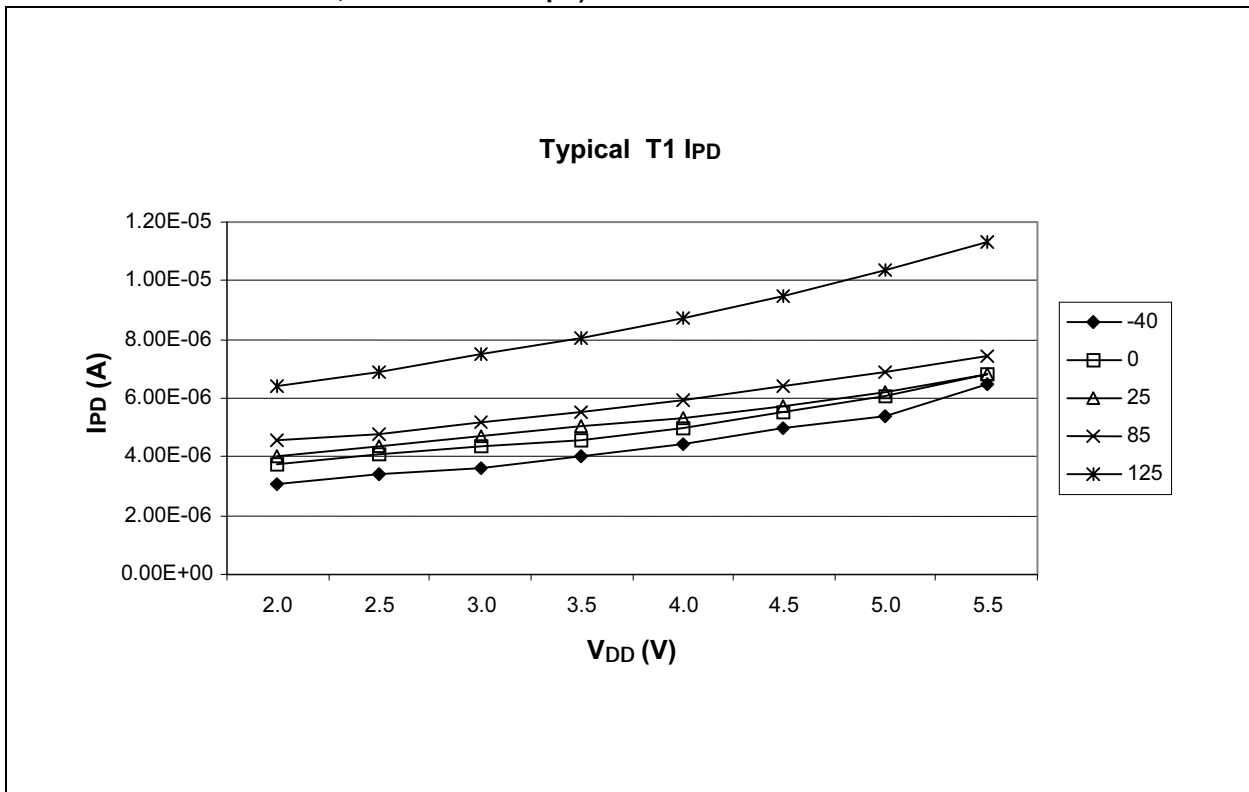
FIGURE 13-13: TYPICAL IPD WITH CVREF ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

Typical CVREF IPD
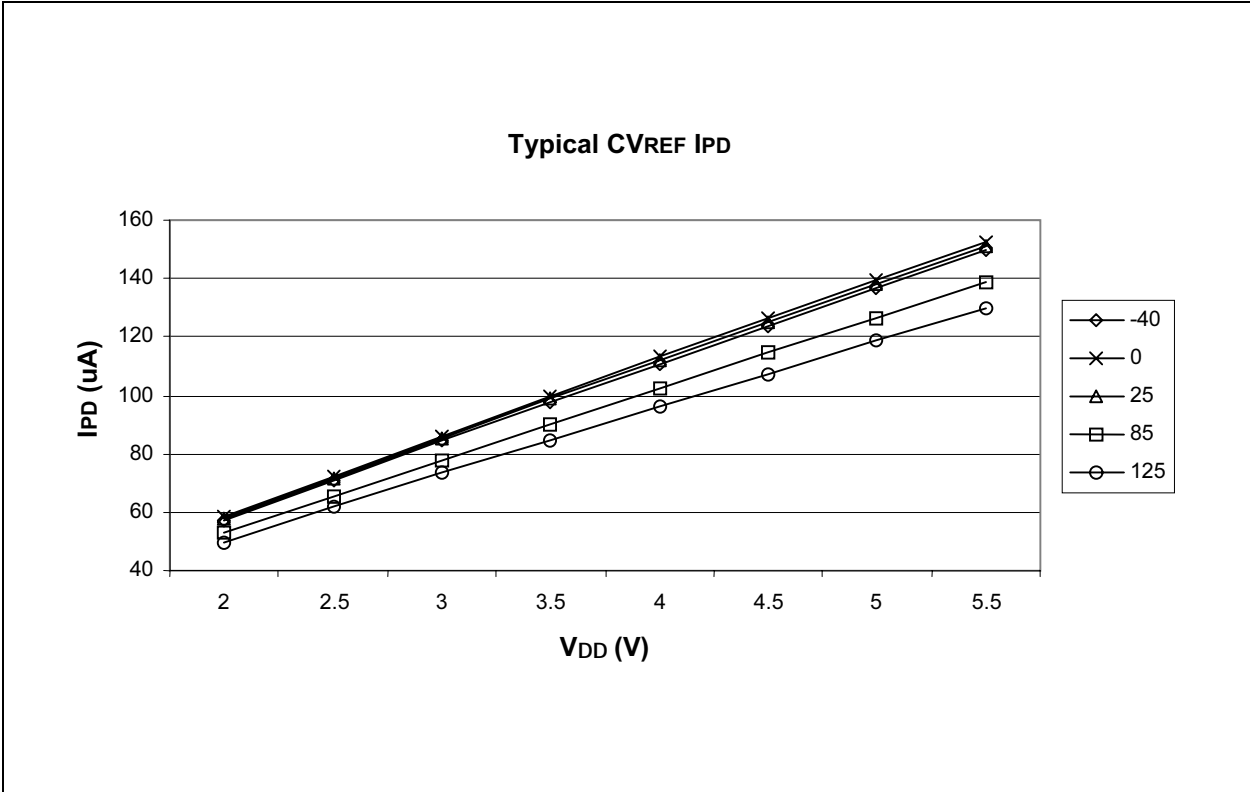
FIGURE 13-14: TYPICAL IPD WITH WDT ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)
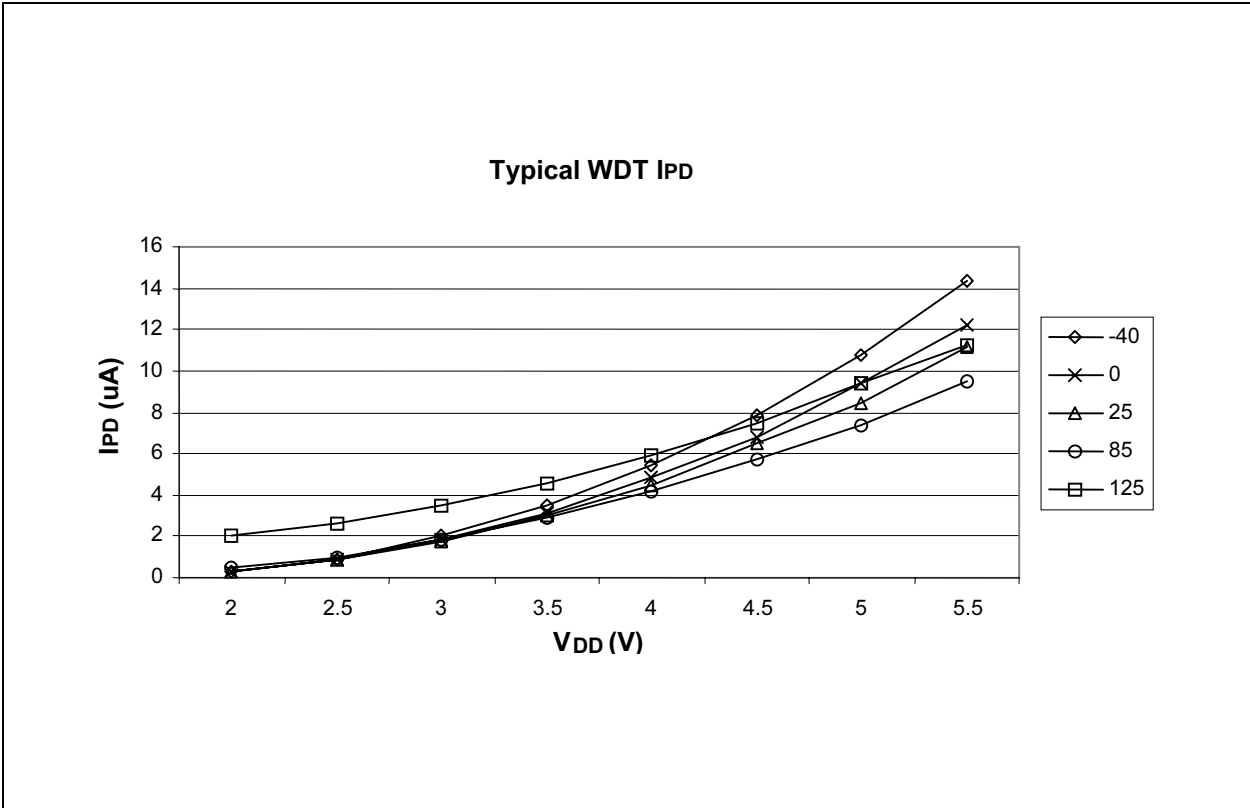
Typical WDT IPD

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FIGURE 13-15: **MAXIMUM AND MINIMUM INTOSC FREQ vs. TEMPERATURE WITH 0.1μF AND 0.01μF DECOUPLING (VDD = 3.5V)**
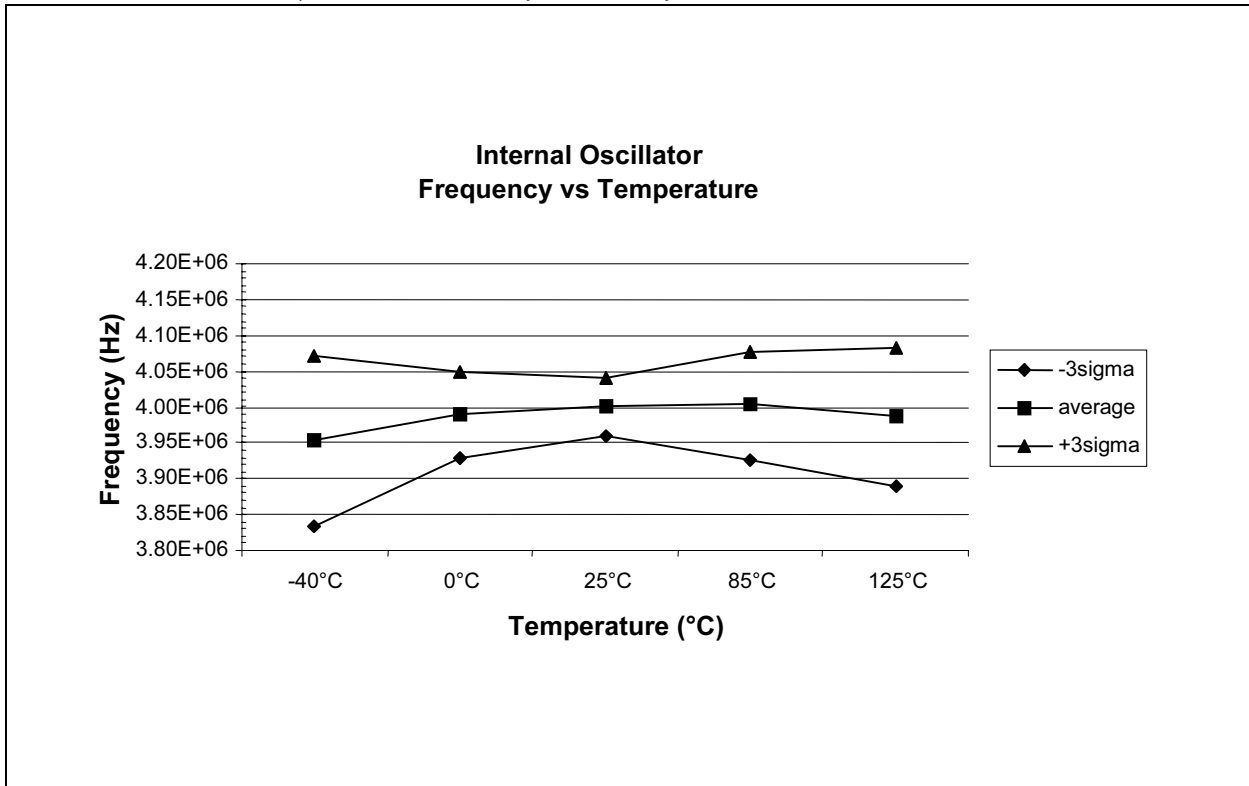
FIGURE 13-16: **MAXIMUM AND MINIMUM INTOSC FREQ vs. VDD WITH 0.1μF AND 0.01μF DECOUPLING (+25°C)**
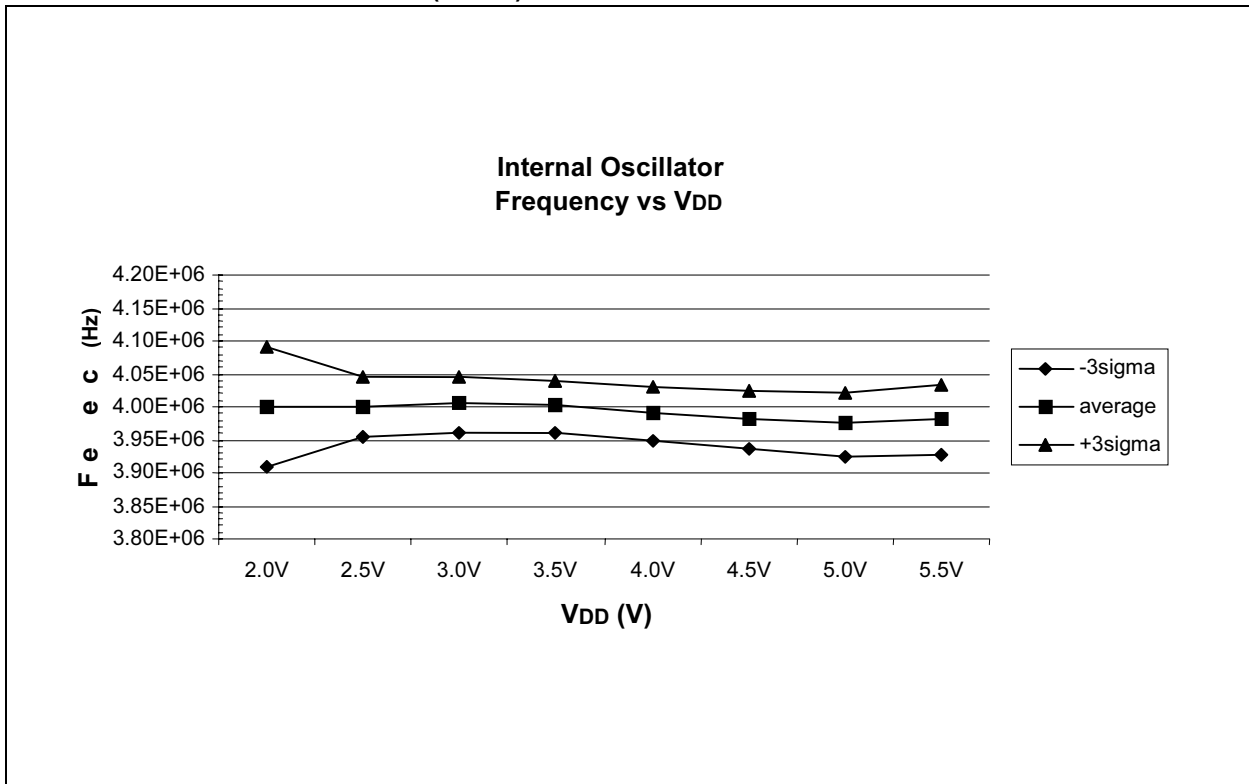
FIGURE 13-17: TYPICAL WDT PERIOD vs. V$_{DD}$ (-40°C TO +125°C)

WDT Time-out
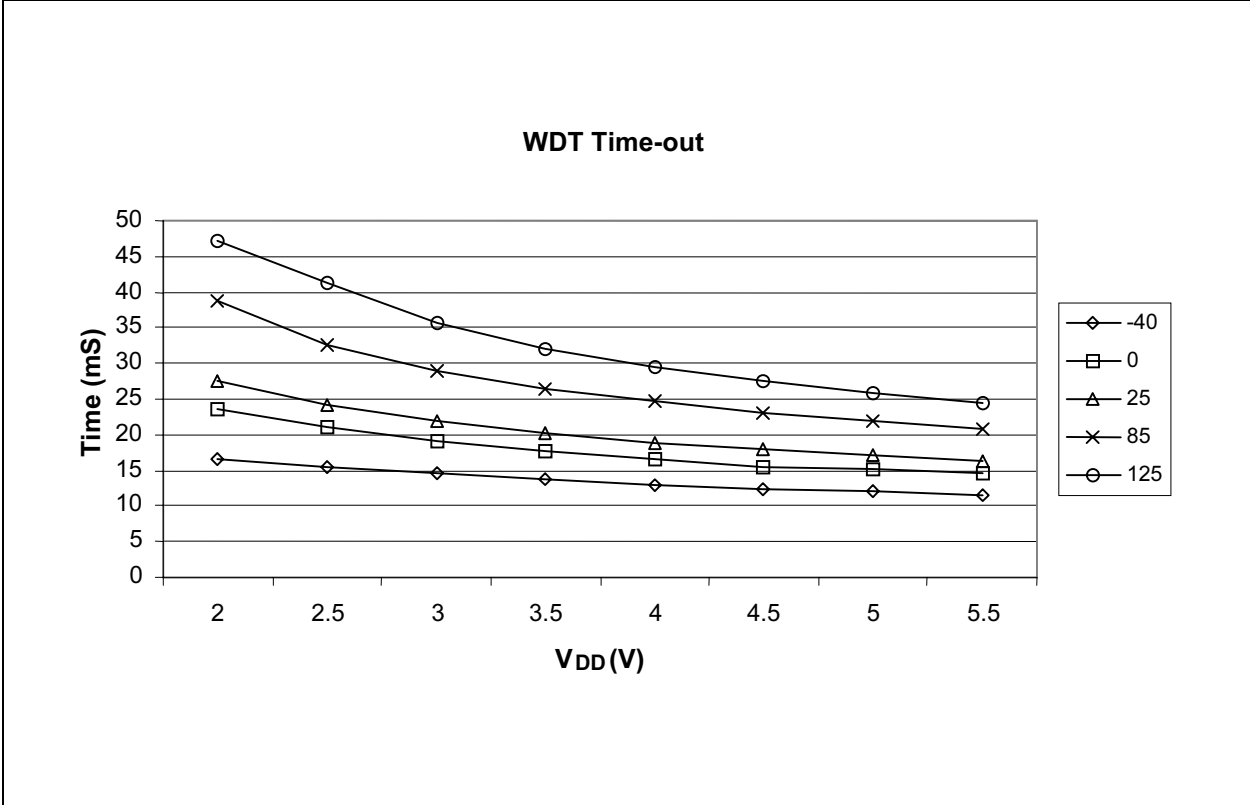
NOTES:

14.0   PACKAGING INFORMATION

14.1   Package Marking Information

14-Lead PDIP (Skinny DIP)

```
XXXXXXXXXXXXX
XXXXXXXXXXXXX
○ Ⓜ YYWWNNN
```

Example

```
16F630-I
○ Ⓜ 0215/017
```

14-Lead SOIC

```
XXXXXXXXXX
XXXXXXXXXX
○  Ⓜ YYWWNNN
```

Example

```
16F630-E
○  Ⓜ 0215/017
```

14-Lead TSSOP

```
XXXXXXX
Ⓜ YYWW
○  NNN
```

Example

```
16F630
Ⓜ 0215
○  017
```

Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

*   Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

14.2   Package Details

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)
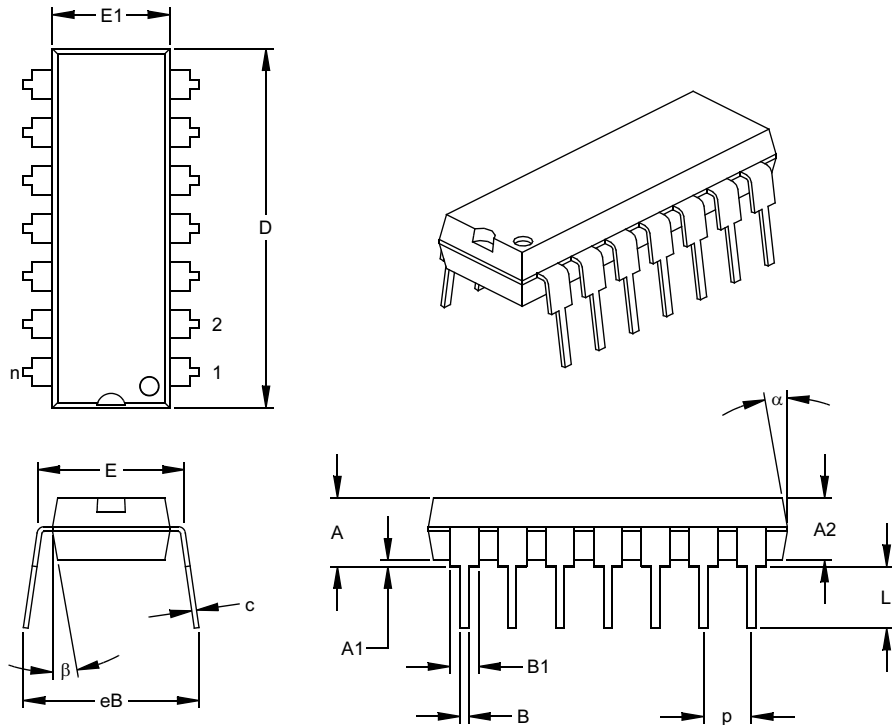
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)
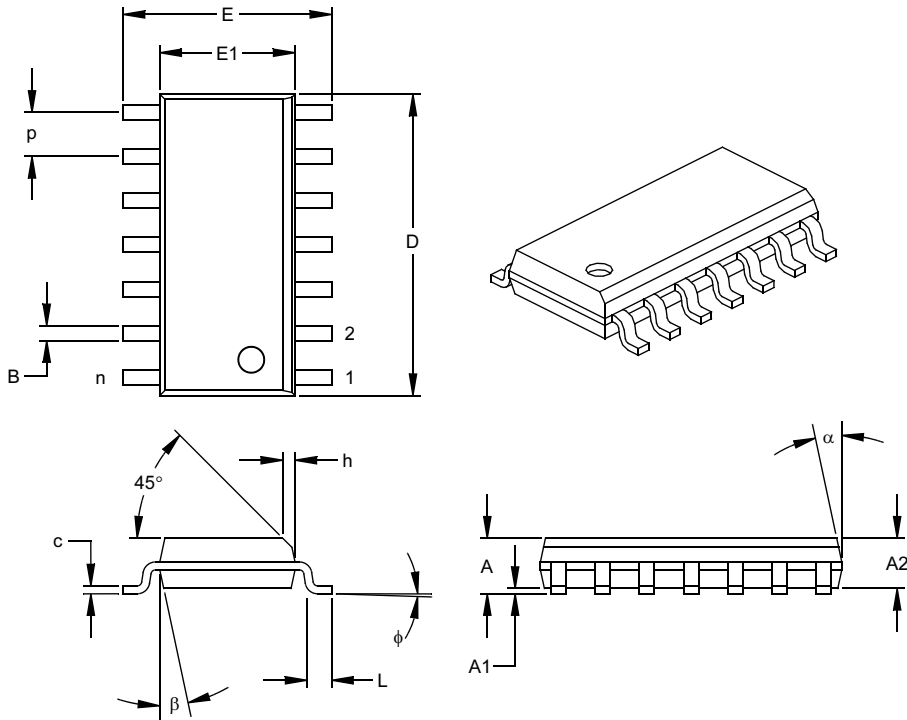
	Units		INCHES*			MILLIMETERS	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

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14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

Number of deo502 0 TD0 T206 0 TD-01 Package Length		14			0.tbss1.10	0.90
Pitch	p	.026			0.65	
Overall Height	A		.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

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APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Added characterization graphs.

Updated specifications.

Added notes to indicate Microchip programmers maintain all calibration bits to factory settings and the PIC16F676 ANSEL register must be initialized to configure pins as digital I/O.

APPENDIX B: DEVICE DIFFERENCES

The differences between the PIC16F630/676 devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Feature	PIC16F630	PIC16F676
A/D	No	Yes

PIC16F630/676

APPENDIX C: DEVICE MIGRATIONS

This section is intended to describe the functional and electrical specification differences when migrating between functionally similar devices (such as from a PIC16C74A to a PIC16C74B).

Not Applicable

APPENDIX D: MIGRATING FROM OTHER PICmicro® DEVICES

This discusses some of the issues in migrating from other PICmicro devices to the PIC16F6XX family of devices.

D.1   PIC12C67X to PIC12F6XX

TABLE 1:   FEATURE COMPARISON

Feature	PIC12C67X	PIC16F6XX
Max Operating Speed	10 MHz	20 MHz
Max Program Memory	2048 bytes	1024 bytes
A/D Resolution	8-bit	10-bit
Data EEPROM	16 bytes	64 bytes
Oscillator Modes	5	8
Brown-out Detect	N	Y
Internal Pull-ups	RA0/1/3	RA0/1/2/4/5
Interrupt-on-change	RA0/1/3	RA0/1/2/3/4/5
Comparator	N	Y

> **Note:** This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

INDEX

PIC16F630/676

NOTES:

SYSTEMS INFORMATION AND

PIC16F630/676

READER RESPONSE

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Device: PIC16F630/676   Literature Number: DS40039C

Questions:

1. What are the best features of this document?

   _____

   _____

2. How does this document meet your hardware and software development needs?

   _____

   _____

3. Do you find the organization of this document easy to follow? If not, why?

   _____

   _____

4. What additions to the document do you think would enhance the structure and subject?

   _____

   _____

5. What deletions from the document could be made without affecting the overall usefulness?

   _____

   _____

6. Is there any incorrect or misleading information (what and where)?

   _____

   _____

7. How would you improve this document?

   _____

   _____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or deli er , refer to the factor or the listed sales office.

PART NO.	X	/XX	XXX
Device	**Temperature Range**	**Package**	**Pattern**

Device	: Standard V$_{DD}$ range T: (Tape and Reel)		
Temperature Range	I =	-40°C to +85°C	
	E =	-40°C to +125°C	
Package	P =	PDIP	
	SN =	SOIC (Gull wing, 150 mil body)	
	ST =	TSSOP(4.4 mm)	
Pattern		3-Digit Pattern Code for QTP (blank otherwise)	

Examples:

a) PIC16F630 – E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301

b) PIC16F676 – I/SO = Industrial Temp., SOIC package, 20 MHz

* JW De ices are UV erasable and can be programmed to an de ice config ration. JW De ices meet the electrical req irement of each oscillator t pe.

Sales and Support

Data Sheets
Prod cts s pported b a preliminar Data Sheet ma ha e an errata sheet describing minor operational differences and recommended orkaro nds. To determine if an errata sheet e ists for a partic lar de ice, please contact one of the follo ing:

1. Yo r local Microchip sales office
2. The Microchip Corporate Literat re Center U.S. FAX: (480) 792-7277
3. The Microchip World ide Site (.microchip.com)

Please specif hich de ice, re ision of silicon and Data Sheet (incl de Literat re #) o are sing.

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