

8

7

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1

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JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	10-13	10-13	L.W.
B	MINOR CHANGES	02-14	L.W.

RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

16 MAY 14

TEMPLATE ENGINEER P. ALONGI	DATE 3/22/11	SCHEMATIC		
HARDWARE SERVICES -		AD9144 FMC EVALUATION BOARD		
HARDWARE SYSTEMS -		<PRODUCT>		
TEST ENGINEER -		<PRODUCT_1>		
COMPONENT ENGINEER -		<DRAWING_TITLE1>		
TEST PROCESS -		<DRAWING_TITLE2>		
HARDWARE RELEASE -		<DRAWING_TITLE3>		
DESIGNER -		<DRAWING_TITLE4>		
PTD ENGINEER <PTD_ENGINEER>		<DRAWING_TITLE5>		
CHECKER -		MASTER PROJECT TEMPLATE <DRAWING_TITLE6>	TESTER TEMPLATE -	DRAWING NO. HSC 13045
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		REV. B
		TOLERANCES		
DECIMALS X.XX +0.010 X.XXX +0.005	FRACTIONS +1/32	ANGLES +2		
SIZE D	SCALE <SCALE>-	CODE ID NO.	SHEET 1	OF 8

8

7

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2

1

D

C

B

A

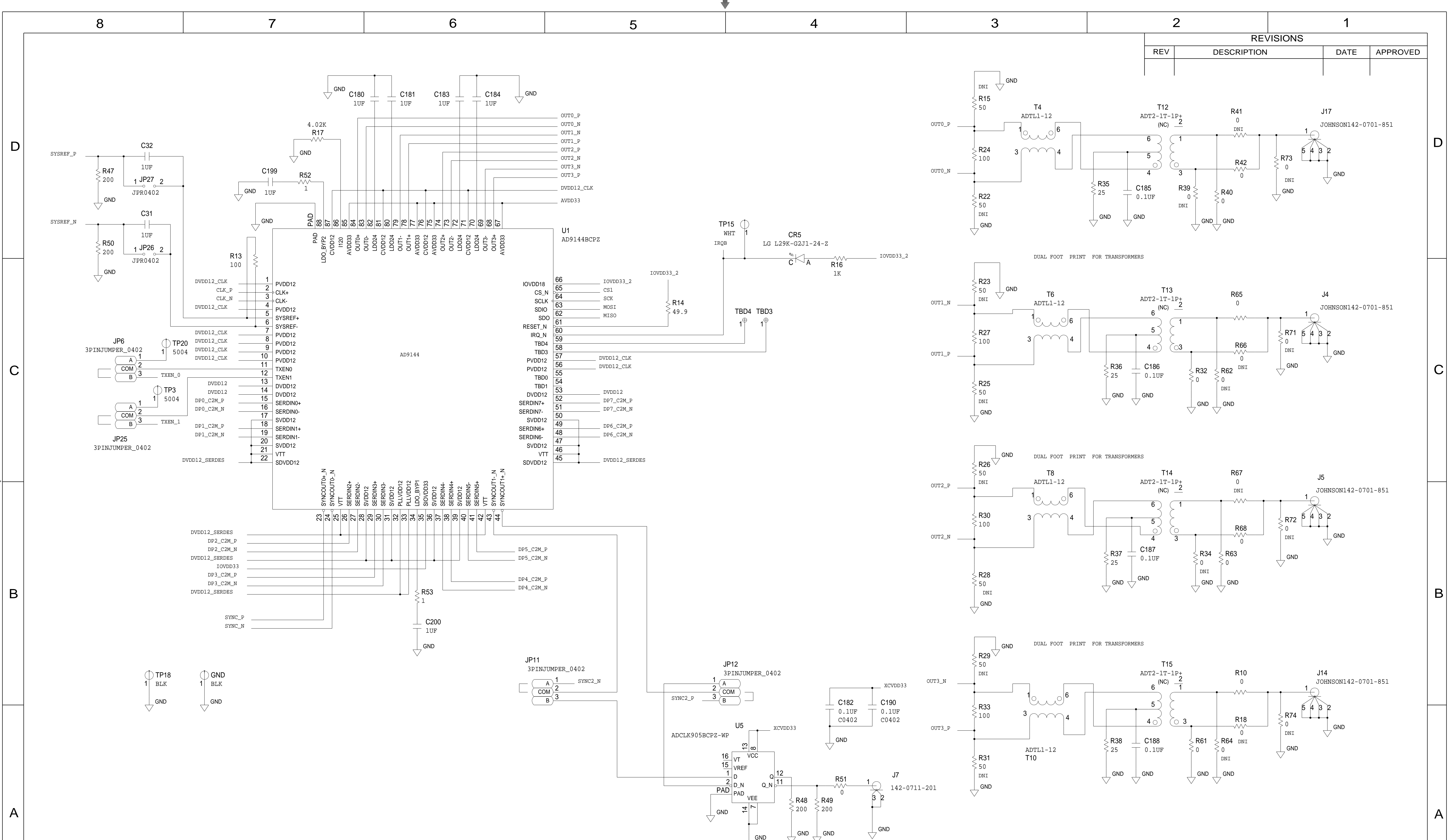
D

C

B

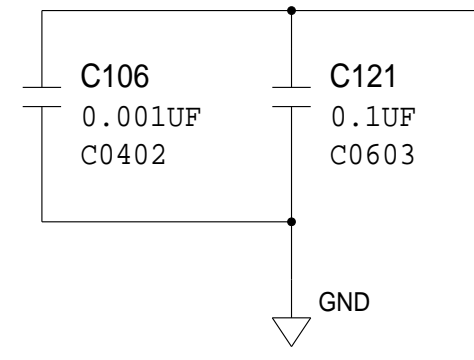
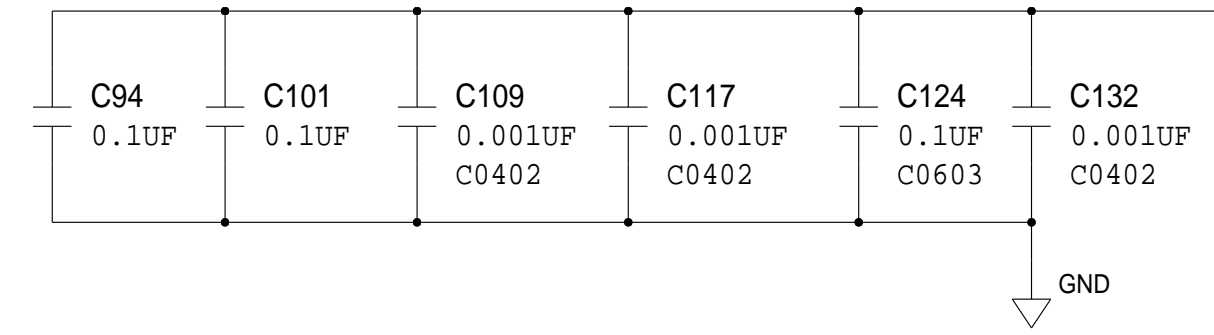
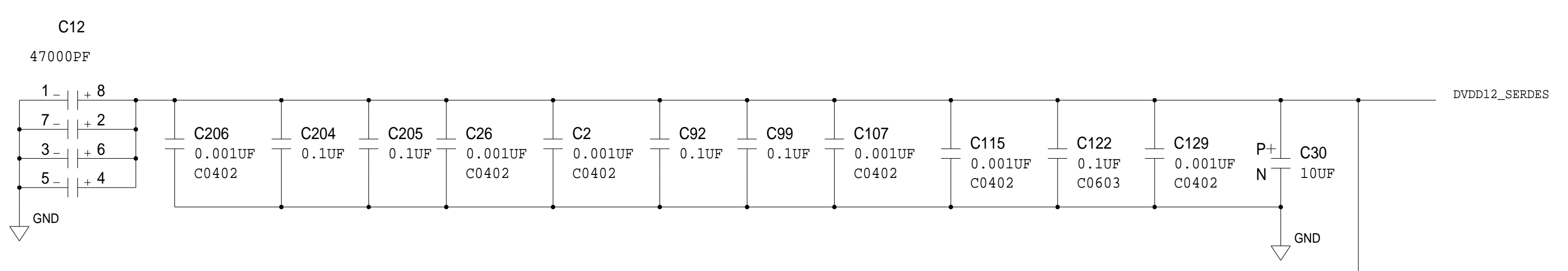
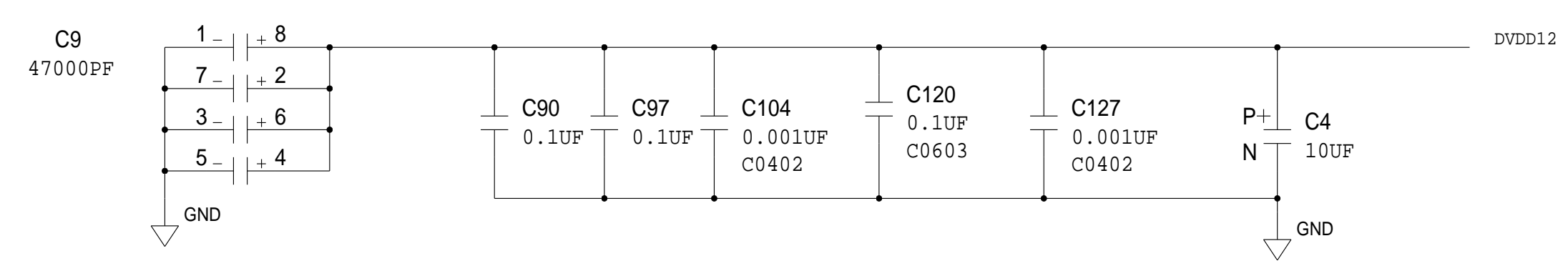
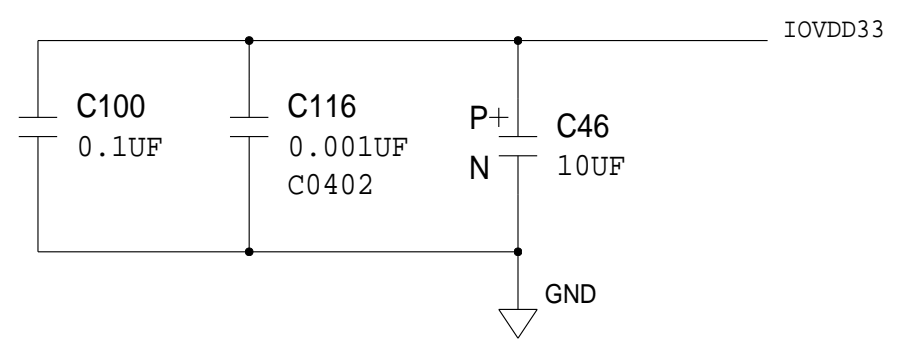
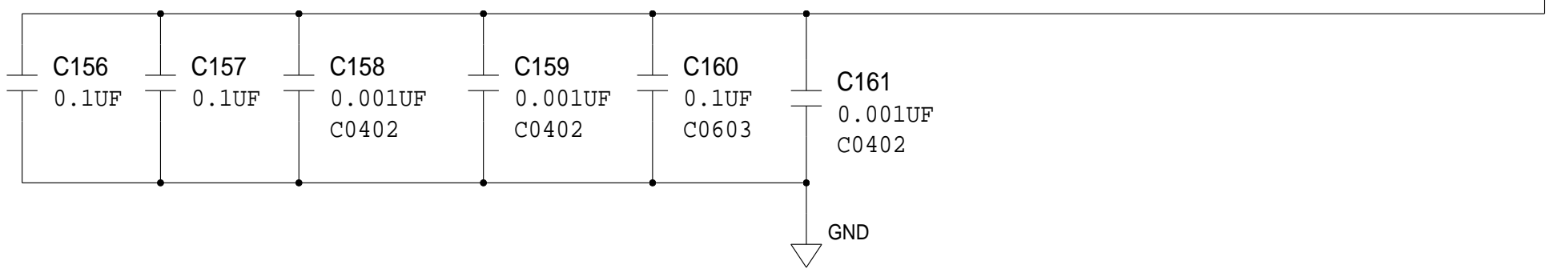
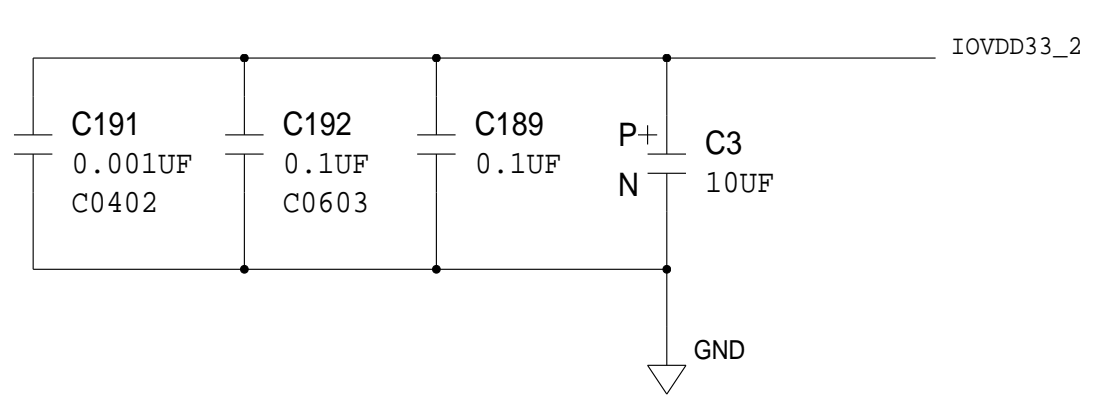
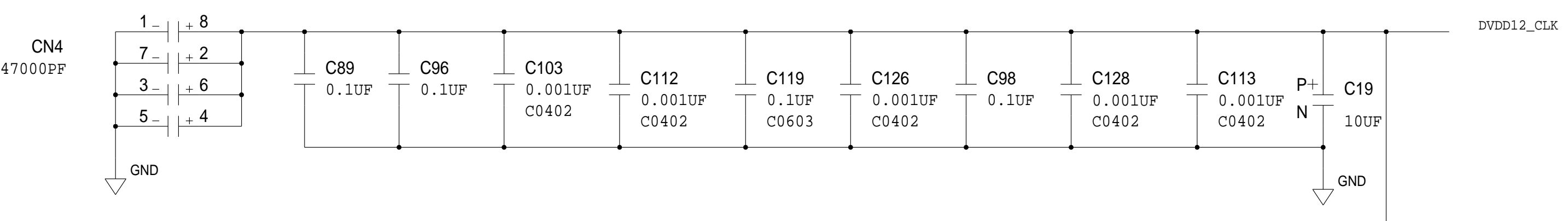
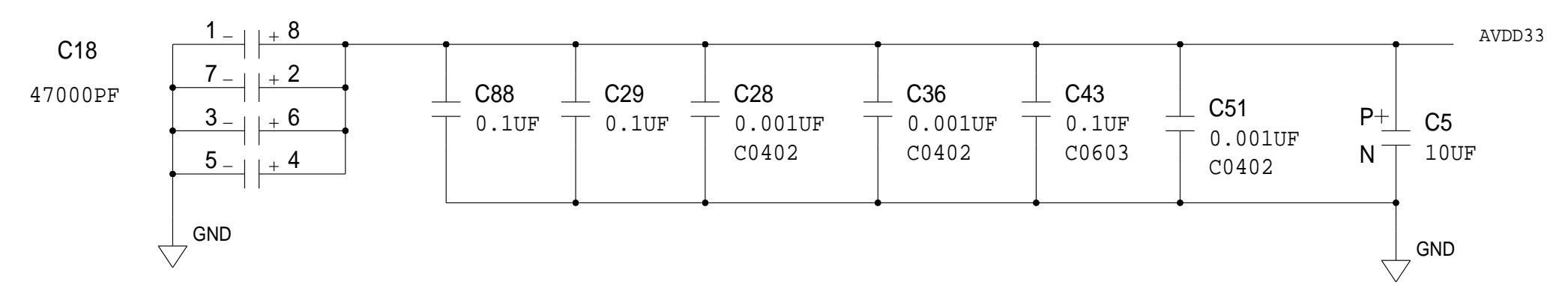
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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	<PRODUCT_1>		
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PTD ENGINEER	SCALE	SHEET 2 OF 8	
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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	AD9144 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	
		SHEET 3 OF 8	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FMC

D

C

B

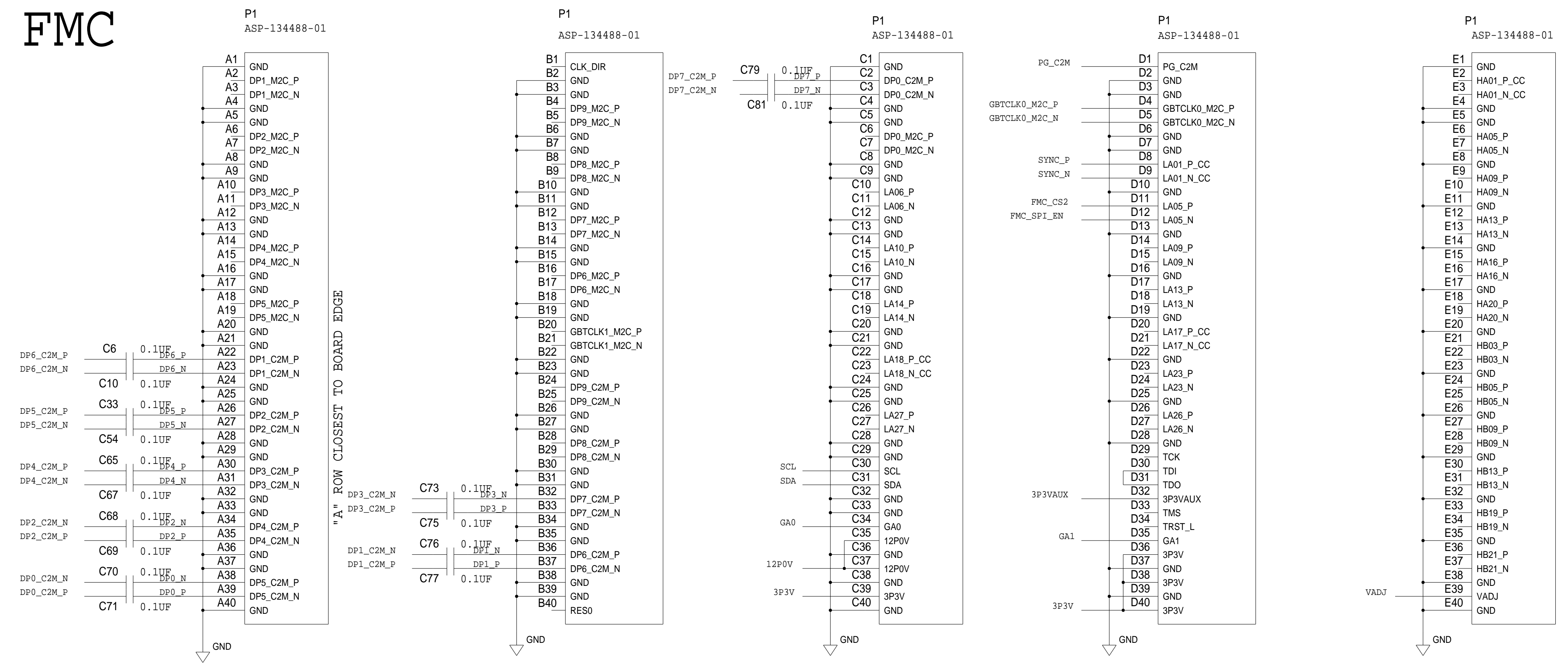
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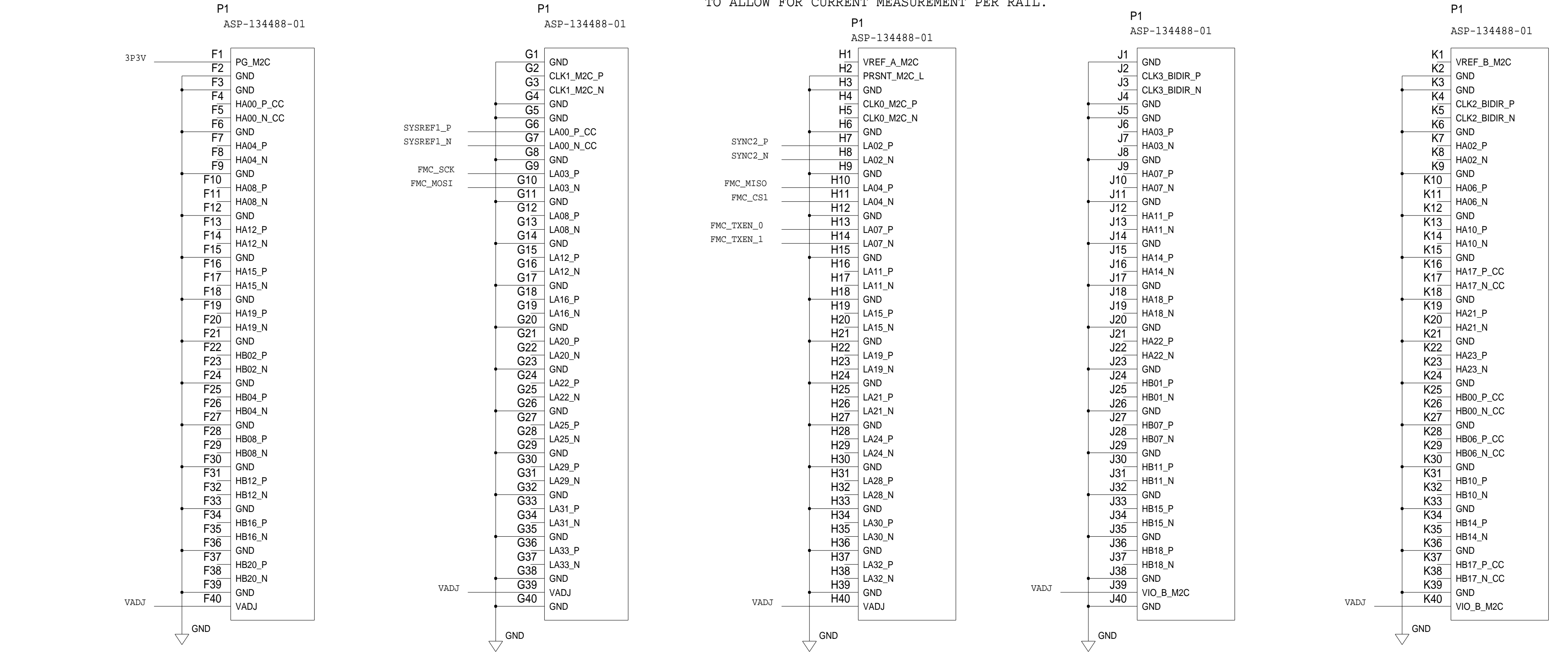
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B

A



ON 3P3V, 12P0V, AND VADJ, HAVE PIN-HEADER JUMPER BETWEEN FMC PINS AND REST OF BOARD, TO ALLOW FOR CURRENT MEASUREMENT PER RAIL.

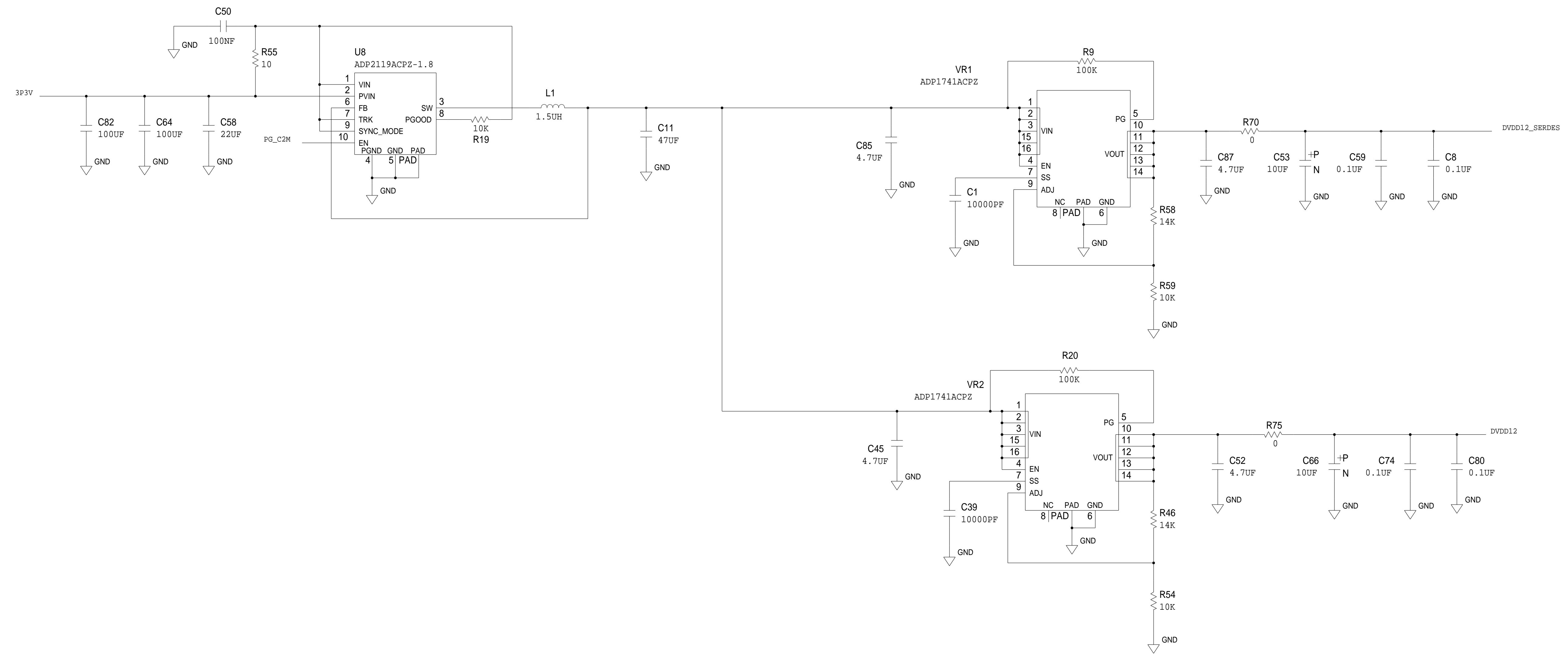


VIO_B_M2C PINS SHOULD HAVE WIDE ETCH CONNECTION TO VADJ PINS

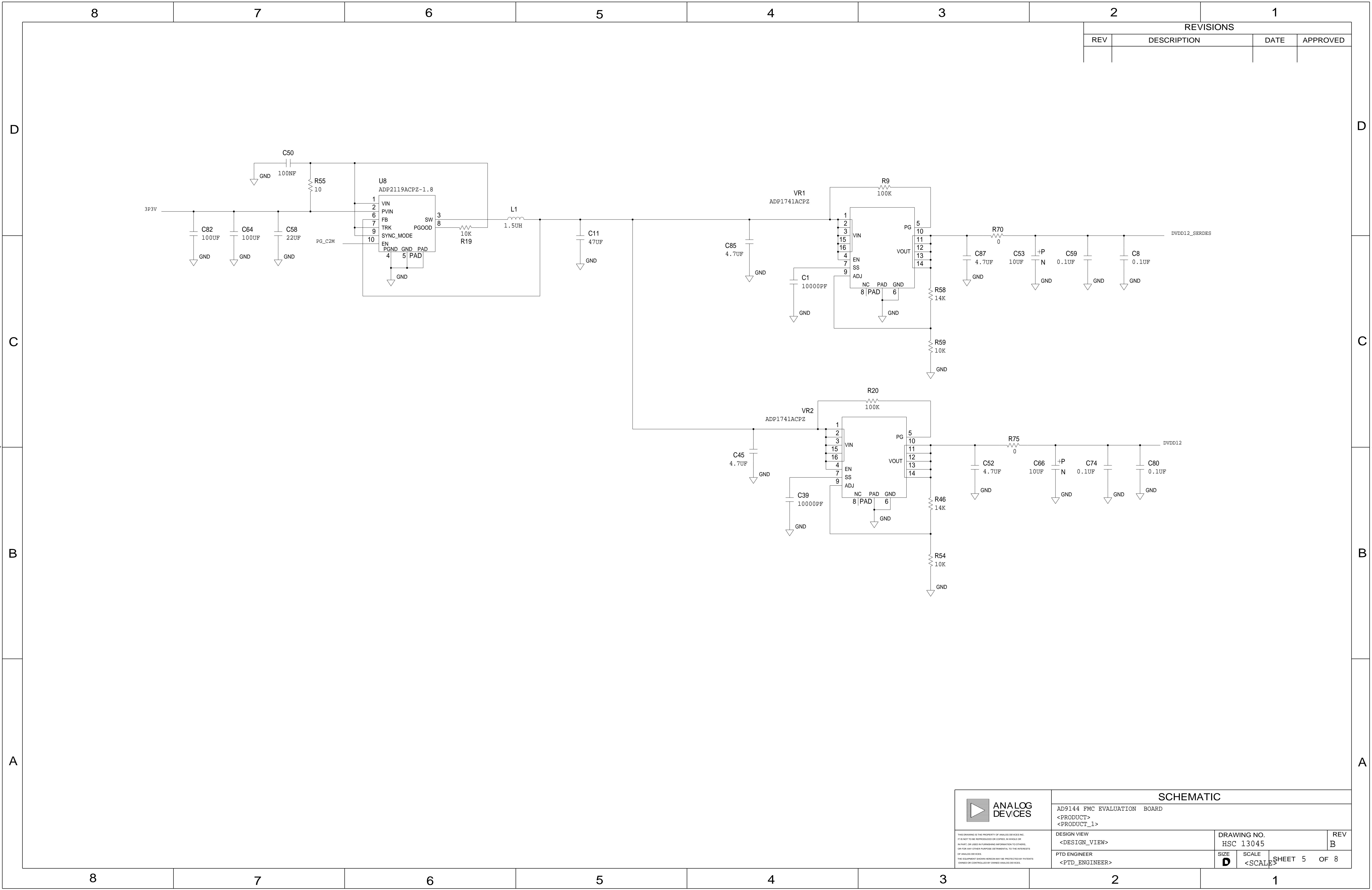
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PTD ENGINEER <PTD_ENGINEER>	SCALE <SCALE>	SHEET 4 OF 8	

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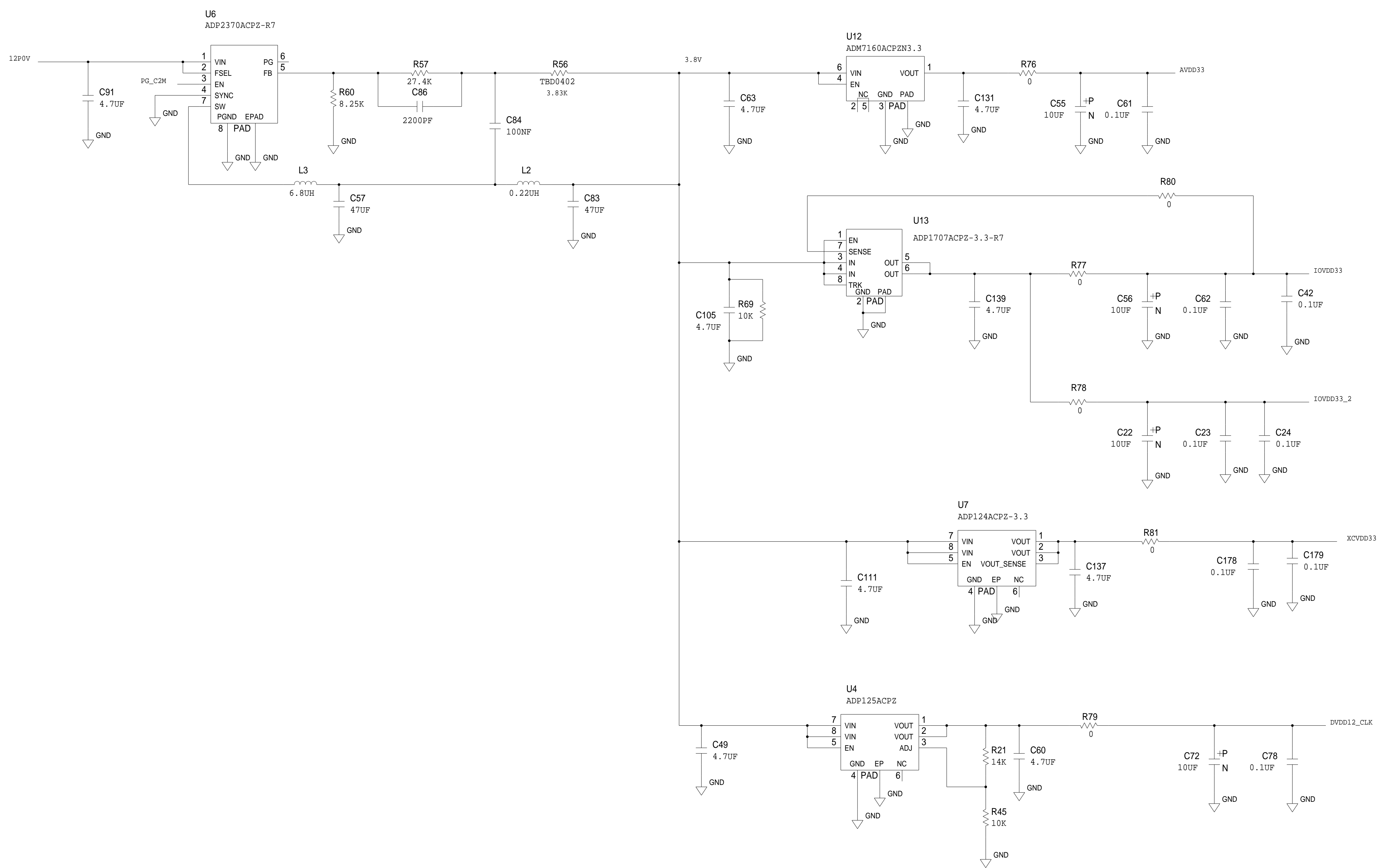
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REV	DESCRIPTION	DATE	APPROVED



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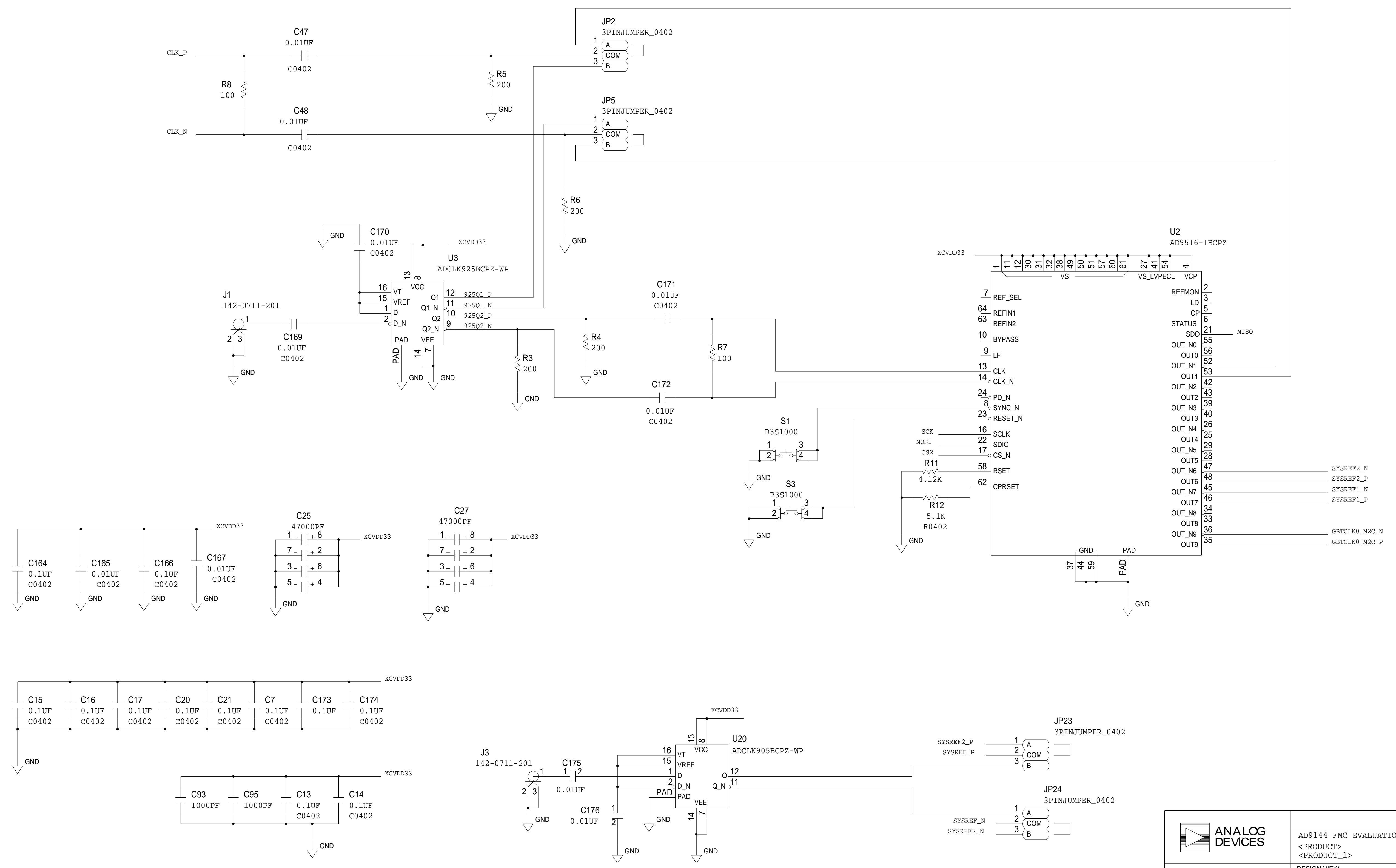


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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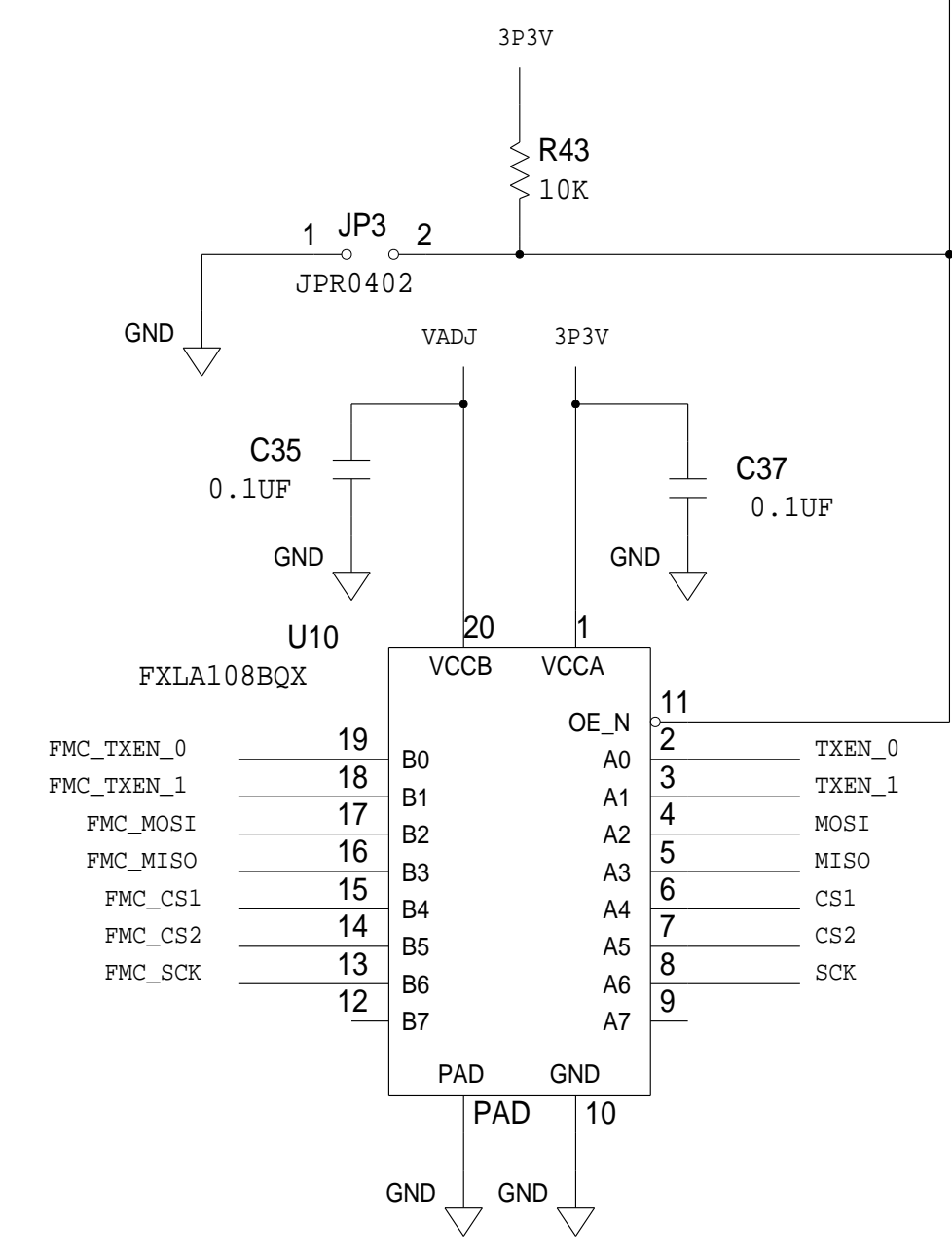
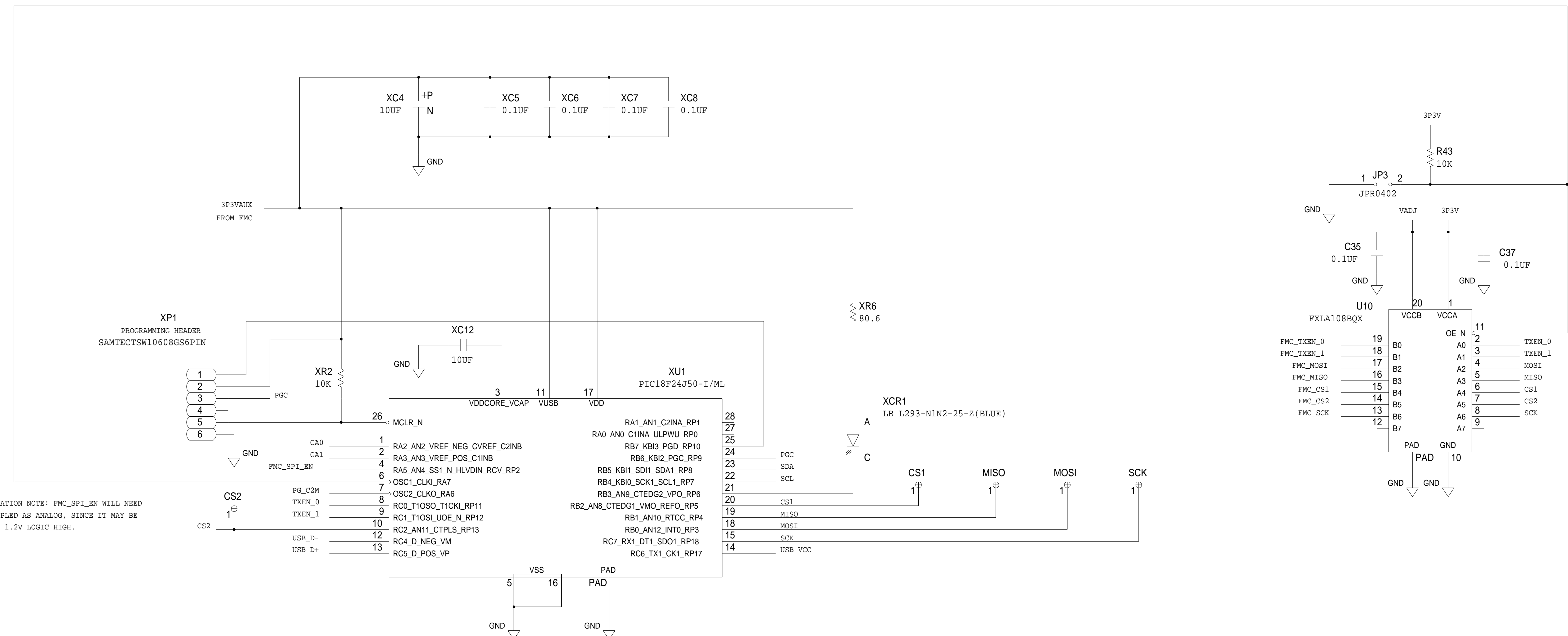
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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		SHEET 7 OF 8	

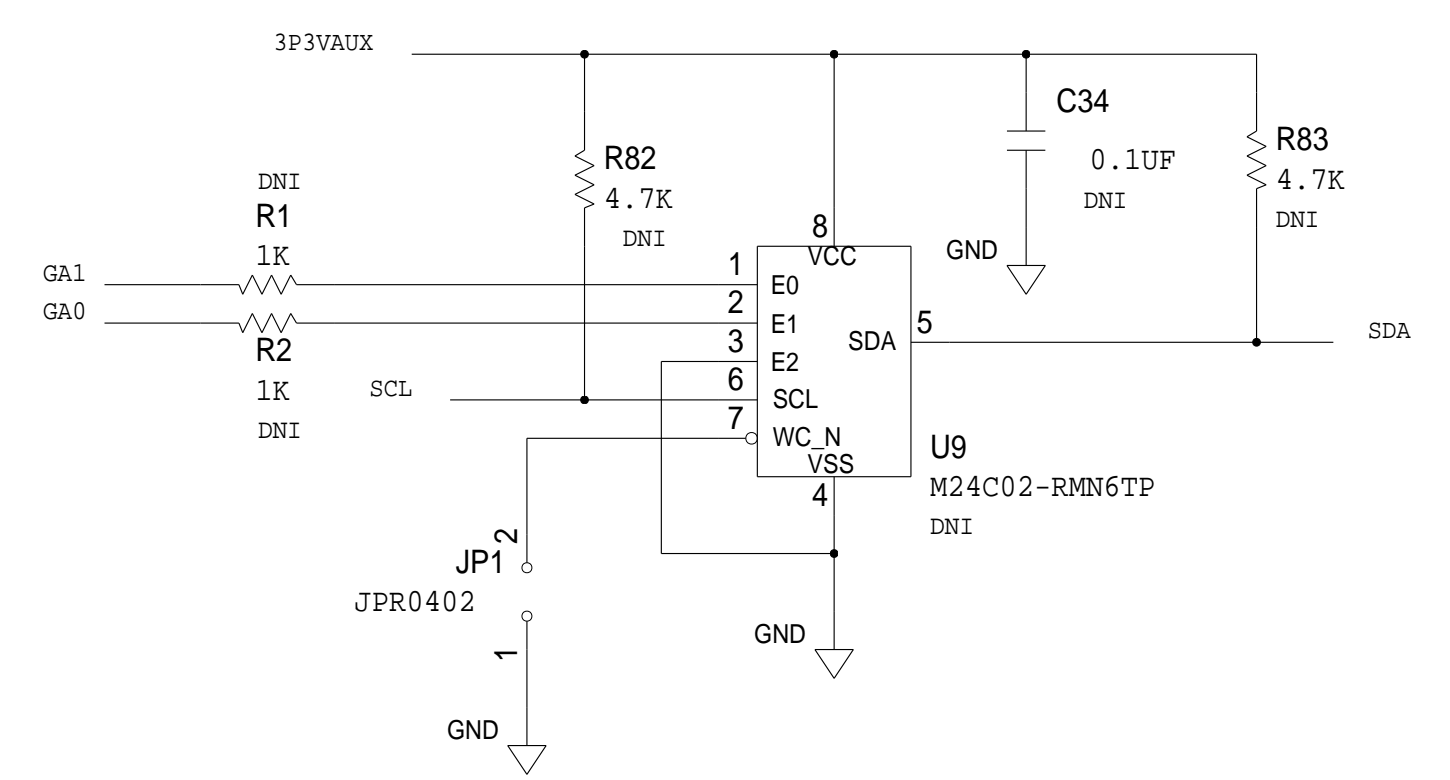
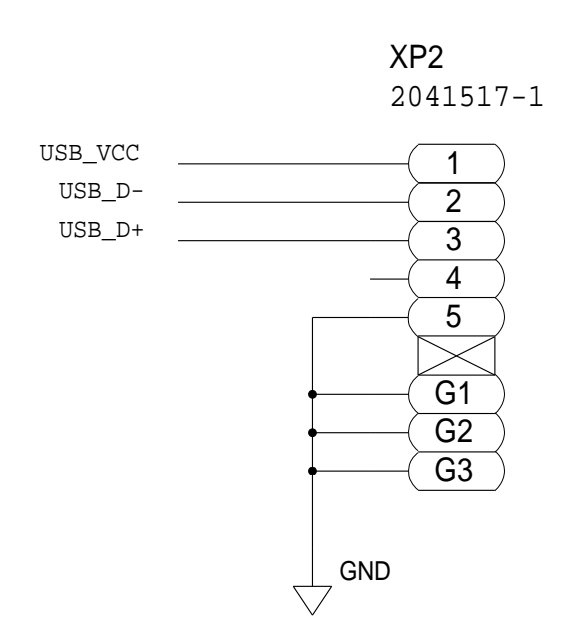
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IMPLEMENTATION NOTE: FMC_SPI_EN WILL NEED TO BE SAMPLED AS ANALOG, SINCE IT MAY BE AS LOW AS 1.2V LOGIC HIGH.

NOTE:
 IF USB CABLE IS PLUGGED IN PIC IS THE SOURCE OF SPI BUS AND TXEN SIGNALS
 IF USB IS UNPLUGGED FMC INTERFACE IS THE SOURCE OF SPI BUS AND TXEN SIGNAL.



	SCHEMATIC		
	AD9144 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13045	REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 8 OF 8

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