High Speed, Monolithic Pin Driver

The EL7154 three-state pin driver is particularly well suited
for ATE and level shifting applications. The 4A peak drive

Ordering Information

PART NUMBER	PART MARKING	TAPE AND REEL	PACKAGE	PKG. DWG. #
EL7154CN	EL7154CN	-	8 Ld PDIP	MDP0031
EL7154CNZ	EL7154CN Z	-	8 Ld PDIP* (Pb-free)	MDP0031
EL7154CS	7154CS	-	8 Ld SOIC	MDP0027
EL7154CS-T7	7154CS	7"	8 Ld SOIC	MDP0027
EL7154CS-T13	7154CS	13"	8 Ld SOIC	MDP0027
EL7154CSZ (See Note)	7154CSZ	-	8 Ld SOIC (Pb-free)	MDP0027
EL7154CSZ-T7 (See Note)	7154CSZ	7"	8 Ld SOIC (Pb-free)	MDP0027
EL7154CSZ-T13 (See Note)	7154CSZ	13"	8 Ld SOIC (Pb-free)	MDP0027

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Nominal Operating Voltage Range

PIN	MIN	MAX
V_L	-3	0
V_{DD} to V_L	5	15
V_H to V_L	2	15
V_{DD} to V_H	-0.5	15
V_{DD}	5	15

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Absolute Maximum Ratings (T$_A$ = +25°C)

Supply (V$_{DD}$ to V$_L$; V$_H$ to V$_L$, V$_H$ to GND),
V+ to V$_H$. 16.5V
V$_L$ to GND . . . . -5V
Input Pins. . . . . -0.3V below V$_L$ to +0.3V above V$_{DD}$
Peak Output Current 4A

Thermal Information

Storage Temperature Range . . . .-65°C to +150°C
Ambient Operating Temperature . . . .-40°C to +85°C
Operating Junction Temperature . . . .+125°C
Power Dissipation
    SOIC. 570mW
    PDIP* 1050mW
Pb-free reflow profile . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T$_J$ = T$_C$ = T$_A$
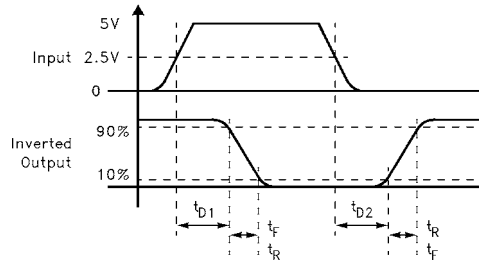
DC Electrical Specifications   T$_A$ = +25°C, V$_{DD}$ = +12V, V$_H$ = +12V, V$_L$ = -3V, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V$_{IH}$	Logic "1" Input Voltage		2.4			V
I$_{IH}$	Logic "1" Input Current	V$_{IH}$ = V$_{DD}$		0.1	10	µA
V$_{IL}$	Logic "0" Input Voltage				0.6	V
I$_{IL}$	Logic "0" Input Current	V$_{IL}$ = 0V		0.1	10	µA
V$_{HVS}$	Input Hysteresis			0.3		V
OUTPUT						
R$_{OH}$	Pull-Up Resistance	I$_{OUT}$ = -100mA		1.5	4	Ω
R$_{OL}$	Pull-Down Resistance	I$_{OUT}$ = +100mA		2	4	Ω
I$_{OUT}$	Output Leakage Current	V$_{DD}$/GND		0.2	10	µA
I$_{PK}$	Peak Output Current	Source/Sink		4.0		A
I$_{DC}$	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I$_S$	Power Supply Current	Inputs = V$_{DD}$		1	2.5	mA
V$_S$	Operating Voltage		4.5		16	V
I$_G$	Current to GND (Pin 4)			1	10	µA
I$_H$	Off Leakage at V$_H$	Pin 8 = 0V		1	10	µA

AC Electrical Specifications   T$_A$ = +25°C unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (V$_{DD}$ = V$_H$ = 12V; V$_L$ = -3V)						
t$_R$	Rise Time	C$_L$ = 100pF		4	25	ns
		C$_L$ = 2000pF		20		
t$_F$	Fall Time	C$_L$ = 100pF		4	25	ns
		C$_L$ = 2000pF		20		
t$_{D-1}$	Turn-Off Delay Time	C$_L$ = 2000pF		20	25	ns
t$_{D-2}$	Turn-On Delay Time	C$_L$ = 2000pF		10	25	ns
t$_{D-1}$	Three-State Delay				25	ns
t$_{D-2}$	Three-State Delay				25	ns

Timing Table

Standard Test Configuration
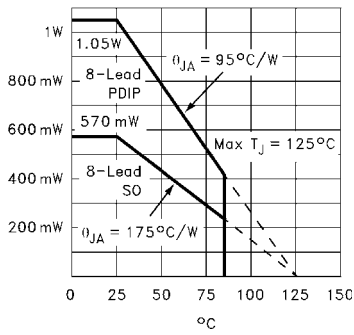
Typical Performance Curves

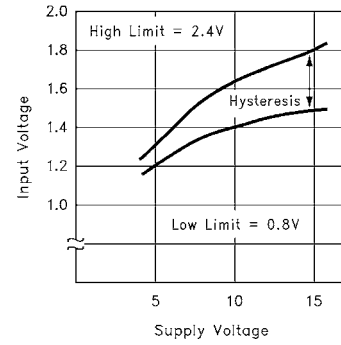**FIGURE 1. MAX POWER DERATING CURVES**

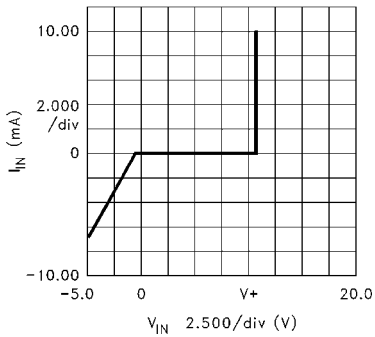**FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE**

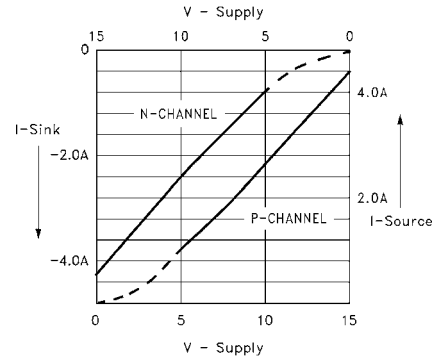**FIGURE 3. INPUT CURRENT vs VOLTAGE**

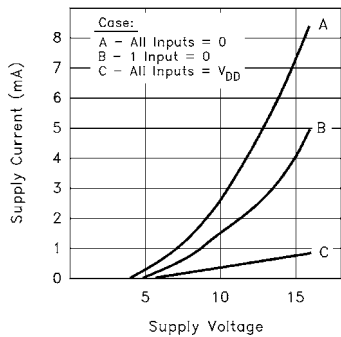
FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE
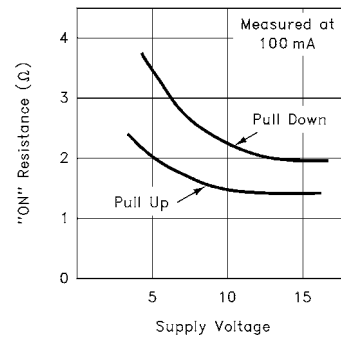

FIGURE 5. QUIESCENT SUPPLY CURRENT

FIGURE 6. "ON" RESISTANCE vs SUPPLY VOLTAGE

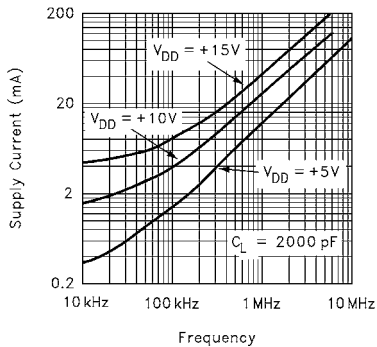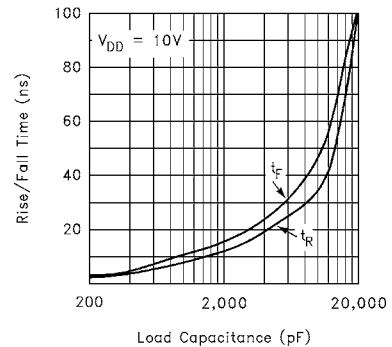**FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY**

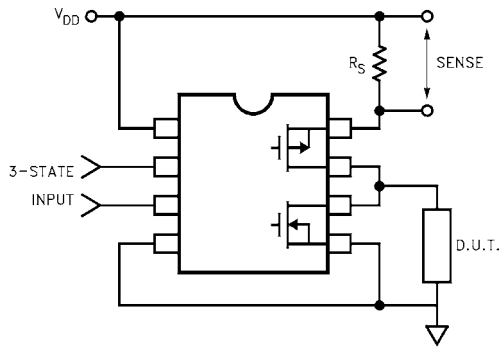**FIGURE 8. RISE/FALL TIME vs LOAD**

Typical Applications

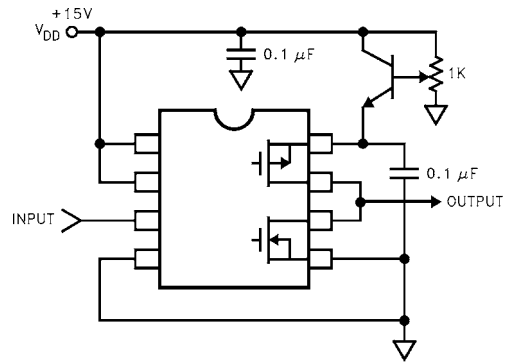**FIGURE 9. PIN DRIVER**
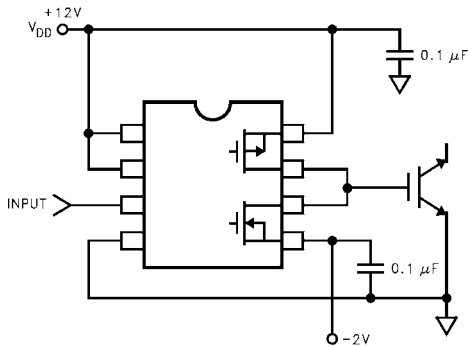

FIGURE 10. ADJUSTABLE AMPLITUDE PULSE GENERATOR

FIGURE 11. IGBT DRIVER WITH NEGATIVE SWING
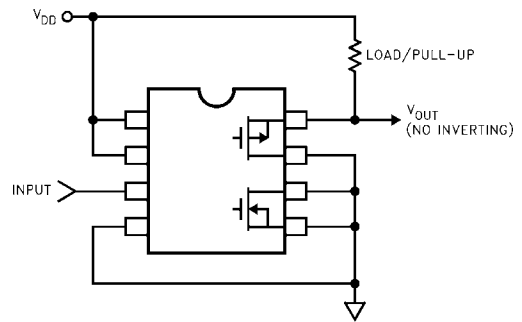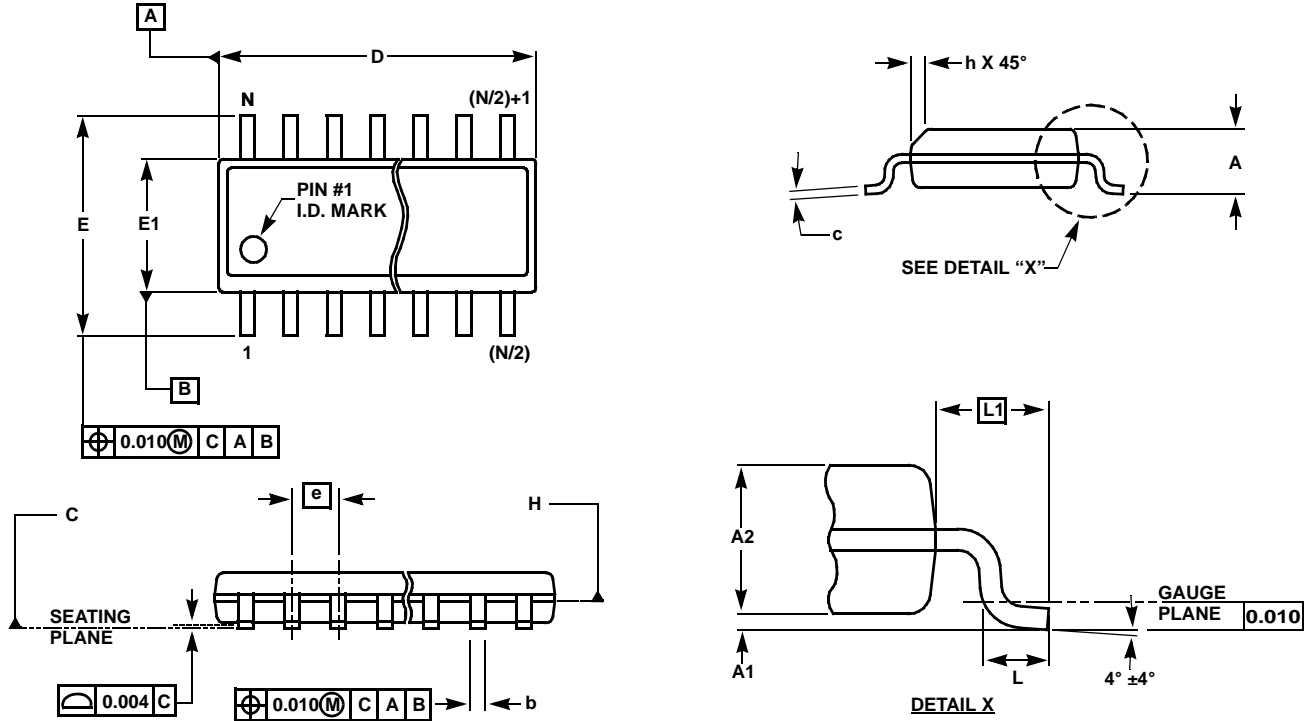

FIGURE 12. PMDS FOLLOWER

FIGURE 13. RESONANT GATE DRIVER

Small Outline Package Family (SO)
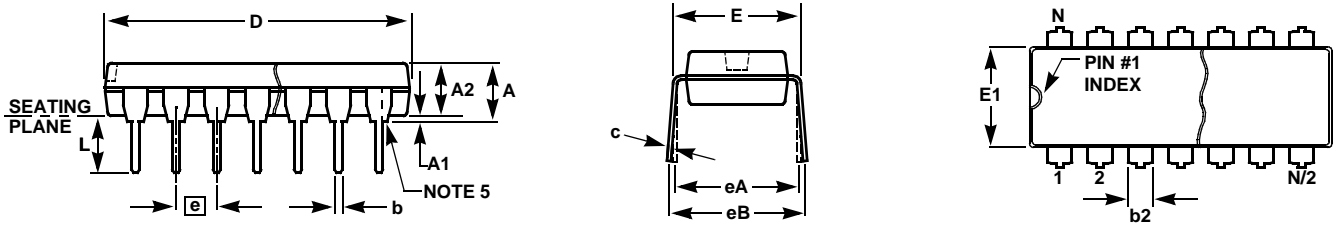

MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.

2. Plastic interlead protrusions of 0.010" maximum per side are not included.

3. Dimensions "D" and "E1" are measured at Datum Plane "H".

4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)

MDP0031
PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.

2. Plastic interlead protrusions of 0.010" maximum per side are not included.

3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.

4. Dimension eB is measured with the lead tips unconstrained.

5. 8 and 16 lead packages have half end-leads as shown.

For information regarding Intersil Corporation and its products, see www.intersil.com