FIGURE 9-2: RA2 AND RA3 BLOCK DIAGRAM

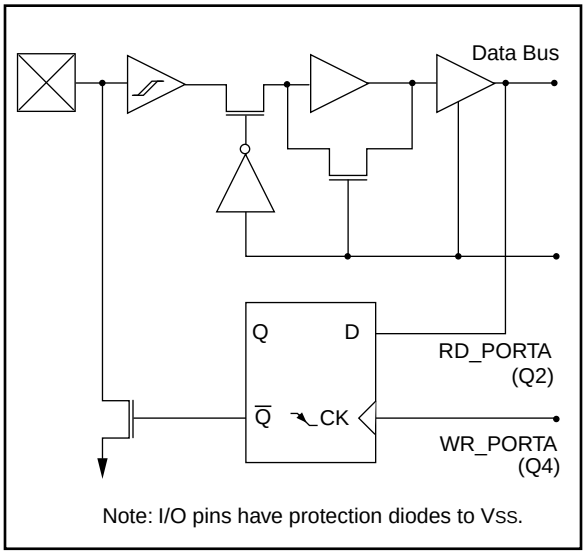


FIGURE 9-3: RA4 AND RA5 BLOCK DIAGRAM

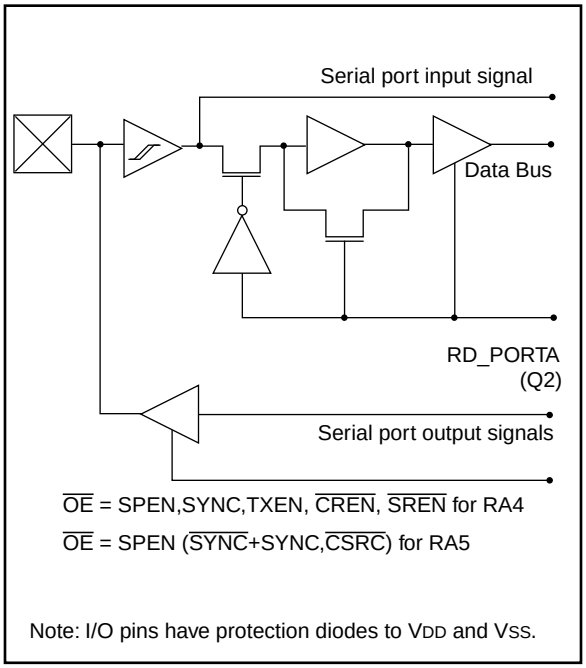


TABLE 9-1: PORTA FUNCTIONS

| Name | Bit0 | Buffer Type | Function |
|---|---|---|---|
| RA0/INT | bit0 | ST | Input or external interrupt input. |
| RA1/T0CKI | bit1 | ST | Input or clock input to the TMR0 timer/counter, and/or an external interrupt input. |
| RA2 | bit2 | ST | Input/Output. Output is open drain type. |
| RA3 | bit3 | ST | Input/Output. Output is open drain type. |
| RA4/RX/DT | bit4 | ST | Input or USART Asynchronous Receive or USART Synchronous Data. |
| RA5/TX/CK | bit5 | ST | Input or USART Asynchronous Transmit or USART Synchronous Clock. |
| RBPU | bit7 | Ñ | Control bit for PORTB weak pull-ups. |

Legend: ST = Schmitt Trigger input.

TABLE 9-2: REGISTERS/BITS ASSOCIATED WITH PORTA

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10h, Bank 0 | PORTA | RBPU | Ñ | RA5 | RA4 | RA3 | RA2 | RA1/T0CKI | RA0/INT | 0-xx xxxx | 0-uu uuuu |
| 05h, Unbanked | T0STA | INTEDG | T0SE | T0CS | PS3 | PS2 | PS1 | PS0 | Ñ | 0000 000- | 0000 000- |
| 13h, Bank 0 | RCSTA | SPEN | RC9 | SREN | CREN | Ñ | FERR | OERR | RC9D | 0000 -00x | 0000 -00u |
| 15h, Bank 0 | TXSTA | CSRC | TX9 | TXEN | SYNC | Ñ | Ñ | TRMT | TX9D | 0000 --1x | 0000 --1u |

Legend: x = unknown, u = unchanged, - = unimplemented reads as '0'. Shaded cells are not used by PORTA.
Note 1: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.


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## 9.2 PORTB and DDRB Register s

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is DDRB. A '1' in DDRB conÞgures the corresponding port pin as an input. A '0' in the DDRB register conÞgures the corresponding port pin as an output. Reading PORTB reads the status of the pins, whereas writing to it will write to the port latch.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (PORTA<7>) bit. The weak pull-up is automatically turned off when the port pin is conÞgured as an output. The pull-ups are enabled on any reset.

PORTB also has an interrupt on change feature. Only pins conÞgured as inputs can cause this interrupt to occur (i.e. any RB7:RB0 pin conÞgured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB0) are compared with the value in the PORTB data latch. The ÒmismatchÓ outputs of RB7:RB0 are ORÕed together to generate the PORTB Interrupt Flag RBIF (PIR<7>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt by:

a) Read-Write PORTB (such as; `MOVPF PORTB, PORTB`). This will end mismatch condition.

b) Then, clear the RBIF bit.

A mismatch condition will continue to set the RBIF bit. Reading then writing PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software conÞgurable pull-ups on this port, allows easy interface to a key pad and make it possible for wake-up on key-depression. For an example, refer to AN552 in the *Embedded Control Handbook*.

The interrupt on change feature is recommended for wake-up on operations where PORTB is only used for the interrupt on change feature and key depression operation.

FIGURE 9-4: BLOCK DIAGRAM OF RB<7:4> AND RB<1:0> PORT PINS

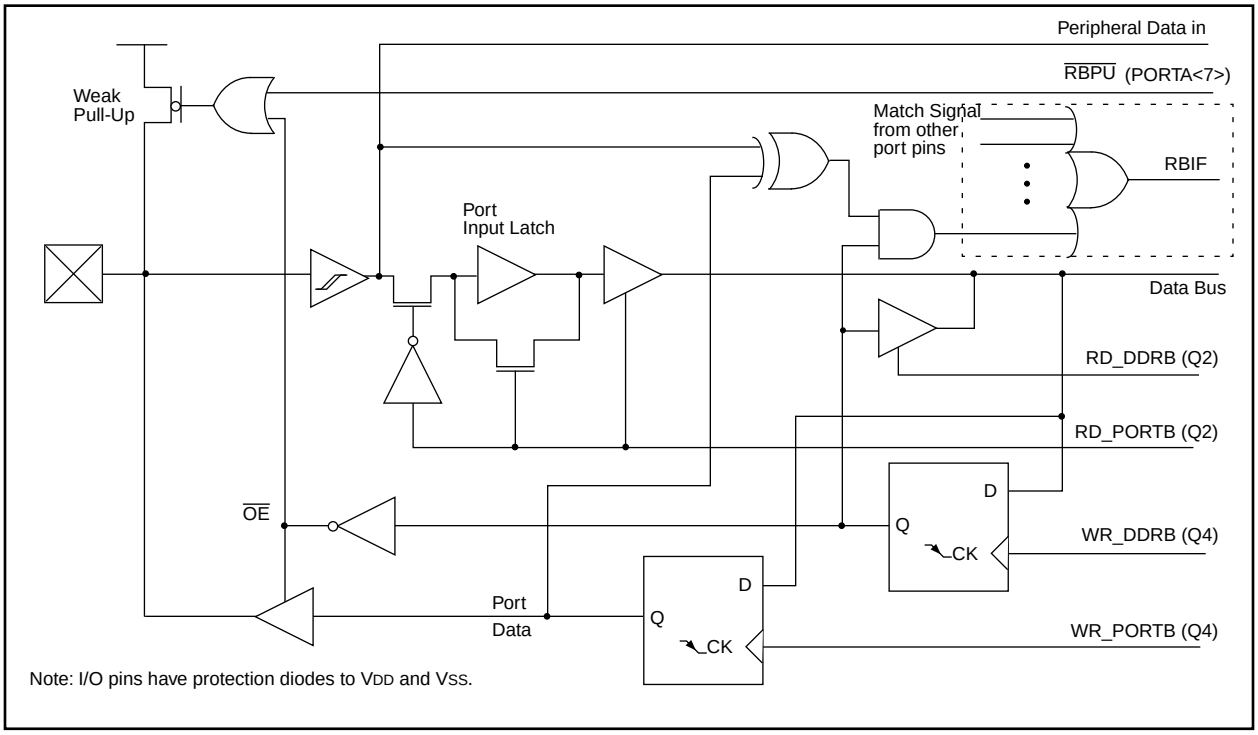
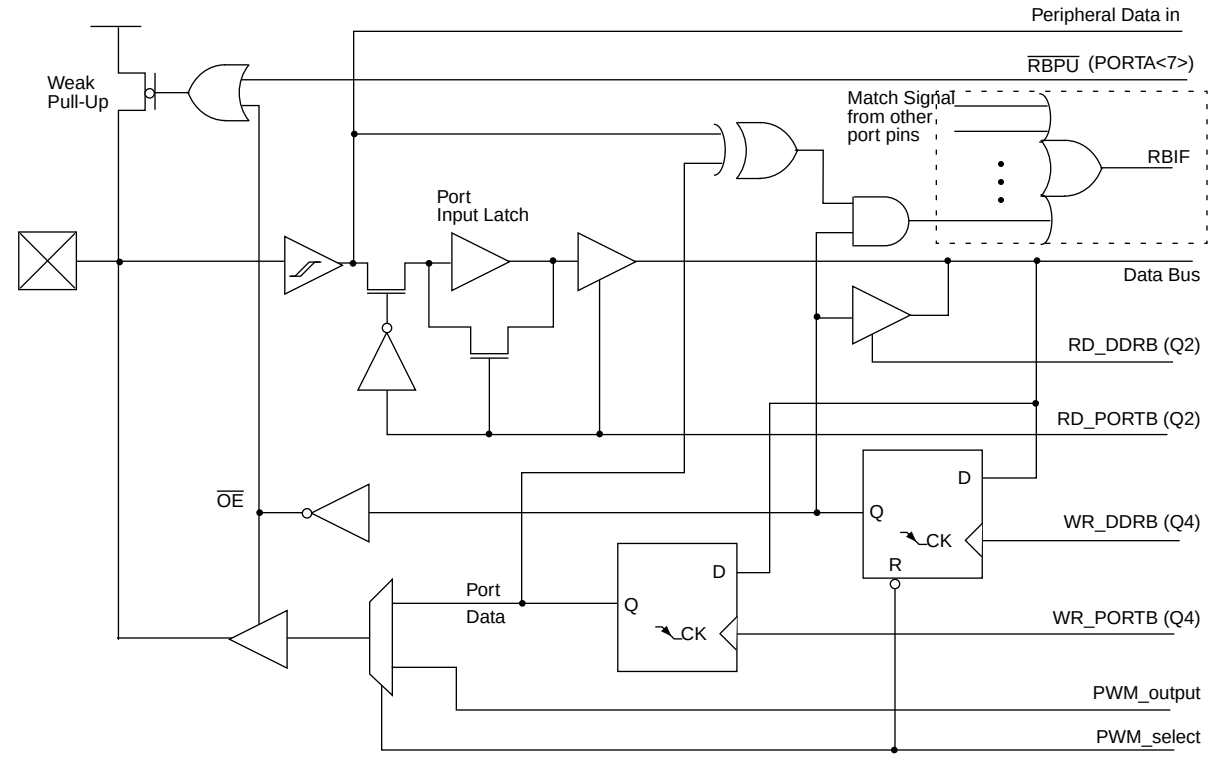


FIGURE 9-5: BLOCK DIAGRAM OF RB3 AND RB2 PORT PINS




Note: I/O pins have protection diodes to VDD and Vss.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Example 9-1 shows the instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized.

EXAMPLE 9-1: INITIALIZING PORTB

```
MOVLB 0         ; Select Bank 0
CLRF  PORTB     ; Initialize PORTB by clearing
                ;  output data latches
MOVLW 0xCF      ; Value used to initialize
                ;  data direction
MOVWF DDRB      ;  Set RB<3:0> as inputs
                ;   RB<5:4> as outputs
                ;   RB<7:6> as inputs
```

TABLE 9-3: PORTB FUNCTIONS

| Name | Bit | Buffer Type | Function |
|---|---|---|---|
| RB0/CAP1 | bit0 | ST | Input/Output or the RB0/CAP1 input pin. Software programmable weak pull-up and interrupt on change features. |
| RB1/CAP2 | bit1 | ST | Input/Output or the RB1/CAP2 input pin. Software programmable weak pull-up and interrupt on change features. |
| RB2/PWM1 | bit2 | ST | Input/Output or the RB2/PWM1 output pin. Software programmable weak pull-up and interrupt on change features. |
| RB3/PWM2 | bit3 | ST | Input/Output or the RB3/PWM2 output pin. Software programmable weak pull-up and interrupt on change features. |
| RB4/TCLK12 | bit4 | ST | Input/Output or the external clock input to Timer1 and Timer2. Software programmable weak pull-up and interrupt on change features. |
| RB5/TCLK3 | bit5 | ST | Input/Output or the external clock input to Timer3. Software programmable weak pull-up and interrupt on change features. |
| RB6 | bit6 | ST | Input/Output pin. Software programmable weak pull-up and interrupt on change features. |
| RB7 | bit7 | ST | Input/Output pin. Software programmable weak pull-up and interrupt on change features. |

Legend: ST = Schmitt Trigger input.

TABLE 9-4: REGISTERS/BITS ASSOCIATED WITH PORTB

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 12h, Bank 0 | PORTB | PORTB data latch | | | | | | | | xxxx xxxx | uuuu uuuu |
| 11h, Bank 0 | DDRB | Data direction register for PORTB | | | | | | | | 1111 1111 | 1111 1111 |
| 10h, Bank 0 | PORTA | $\overline{RBPU}$ | Ñ | RA5 | RA4 | RA3 | RA2 | RA1/T0CKI | RA0/INT | 0-xx xxxx | 0-uu uuuu |
| 06h, Unbanked | CPUSTA | Ñ | Ñ | STKAV | GLINTD | $\overline{TO}$ | $\overline{PD}$ | Ñ | Ñ | --11 11-- | --11 qq-- |
| 07h, Unbanked | INTSTA | PEIF | T0CKIF | T0IF | INTF | PEIE | T0CKIE | T0IE | INTE | 0000 0000 | 0000 0000 |
| 16h, Bank 1 | PIR | RBIF | TMR3IF | TMR2IF | TMR1IF | CA2IF | CA1IF | TXIF | RCIF | 0000 0010 | 0000 0010 |
| 17h, Bank 1 | PIE | RBIE | TMR3IE | TMR2IE | TMR1IE | CA2IE | CA1IE | TXIE | RCIE | 0000 0000 | 0000 0000 |
| 16h, Bank 3 | TCON1 | CA2ED1 | CA2ED0 | CA1ED1 | CA1ED0 | T16 | TMR3CS | TMR2CS | TMR1CS | 0000 0000 | 0000 0000 |
| 17h, Bank 3 | TCON2 | CA2OVF | CA1OVF | PWM2ON | PWM1ON | CA1/$\overline{PR3}$ | TMR3ON | TMR2ON | TMR1ON | 0000 0000 | 0000 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = Value depends on condition.
Shaded cells are not used by PORTB.

Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

## 9.3 PORTC and DDRC Register s

PORTC is an 8-bit bi-directional port. The corresponding data direction register is DDRC. A '1' in DDRC conÞgures the corresponding port pin as an input. A '0' in the DDRC register conÞgures the corresponding port pin as an output. Reading PORTC reads the status of the pins, whereas writing to it will write to the port latch. PORTC is multiplexed with the system bus. When operating as the system bus, PORTC is the low order byte of the address/data bus (AD7:AD0). The timing for the system bus is shown in the Electrical Characteristics section.

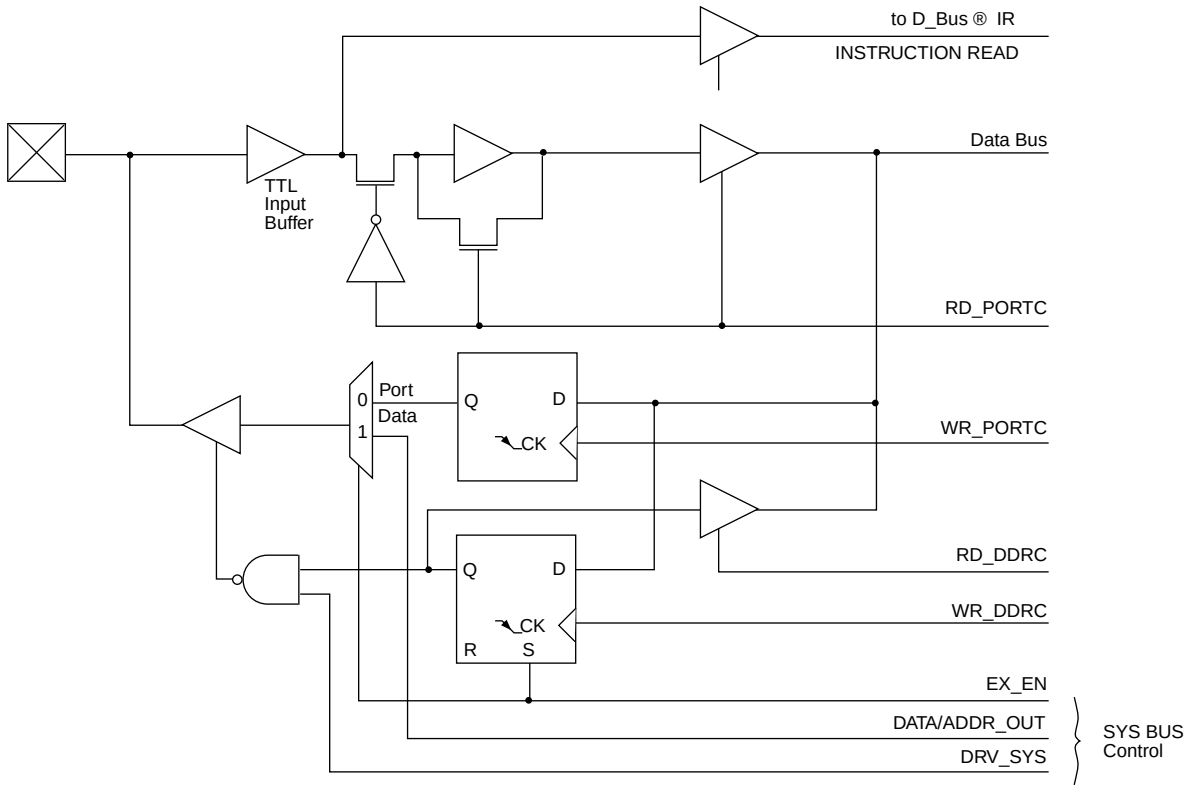
| Note: | This port is conÞgured as the system bus when the deviceÕs conÞguration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O. |
|---|---|

Example 9-2 shows the instruction sequence to initialize PORTC. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-2: INITIALIZING PORTC

```
MOVLB  1          ;  Select Bank 1
CLRF   PORTC      ;  Initialize PORTC data
                  ;   latches before setting
                  ;   the data direction
                  ;   register
MOVLW  0xCF       ;  Value used to initialize
                  ;   data direction
MOVWF  DDRC       ;  Set RC<3:0> as inputs
                  ;   RC<5:4> as outputs
                  ;   RC<7:6> as inputs
```

FIGURE 9-6: BLOCK DIAGRAM OF RC<7:0> PORT PINS




Note: I/O pins have protection diodes to VDD and Vss.


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TABLE 9-5: PORTC FUNCTIONS

| Name | Bit | Buffer Type | Function |
|---|---|---|---|
| RC0/AD0 | bit0 | TTL | Input/Output or system bus address/data pin. |
| RC1/AD1 | bit1 | TTL | Input/Output or system bus address/data pin. |
| RC2/AD2 | bit2 | TTL | Input/Output or system bus address/data pin. |
| RC3/AD3 | bit3 | TTL | Input/Output or system bus address/data pin. |
| RC4/AD4 | bit4 | TTL | Input/Output or system bus address/data pin. |
| RC5/AD5 | bit5 | TTL | Input/Output or system bus address/data pin. |
| RC6/AD6 | bit6 | TTL | Input/Output or system bus address/data pin. |
| RC7/AD7 | bit7 | TTL | Input/Output or system bus address/data pin. |

Legend: TTL = TTL input.

TABLE 9-6: REGISTERS/BITS ASSOCIATED WITH PORTC

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11h, Bank 1 | PORTC | RC7/ AD7 | RC6/ AD6 | RC5/ AD5 | RC4/ AD4 | RC3/ AD3 | RC2/ AD2 | RC1/ AD1 | RC0/ AD0 | xxxx xxxx | uuuu uuuu |
| 10h, Bank 1 | DDRC | Data direction register for PORTC | | | | | | | | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and the Watchdog Timer Reset.

## 9.4 PORTD and DDRD Register s

PORTD is an 8-bit bi-directional port. The corresponding data direction register is DDRD. A '1' in DDRD conÞgures the corresponding port pin as an input. A '0' in the DDRC register conÞgures the corresponding port pin as an output. Reading PORTD reads the status of the pins, whereas writing to it will write to the port latch. PORTD is multiplexed with the system bus. When operating as the system bus, PORTD is the high order byte of the address/data bus (AD15:AD8). The timing for the system bus is shown in the Electrical Characteristics section.

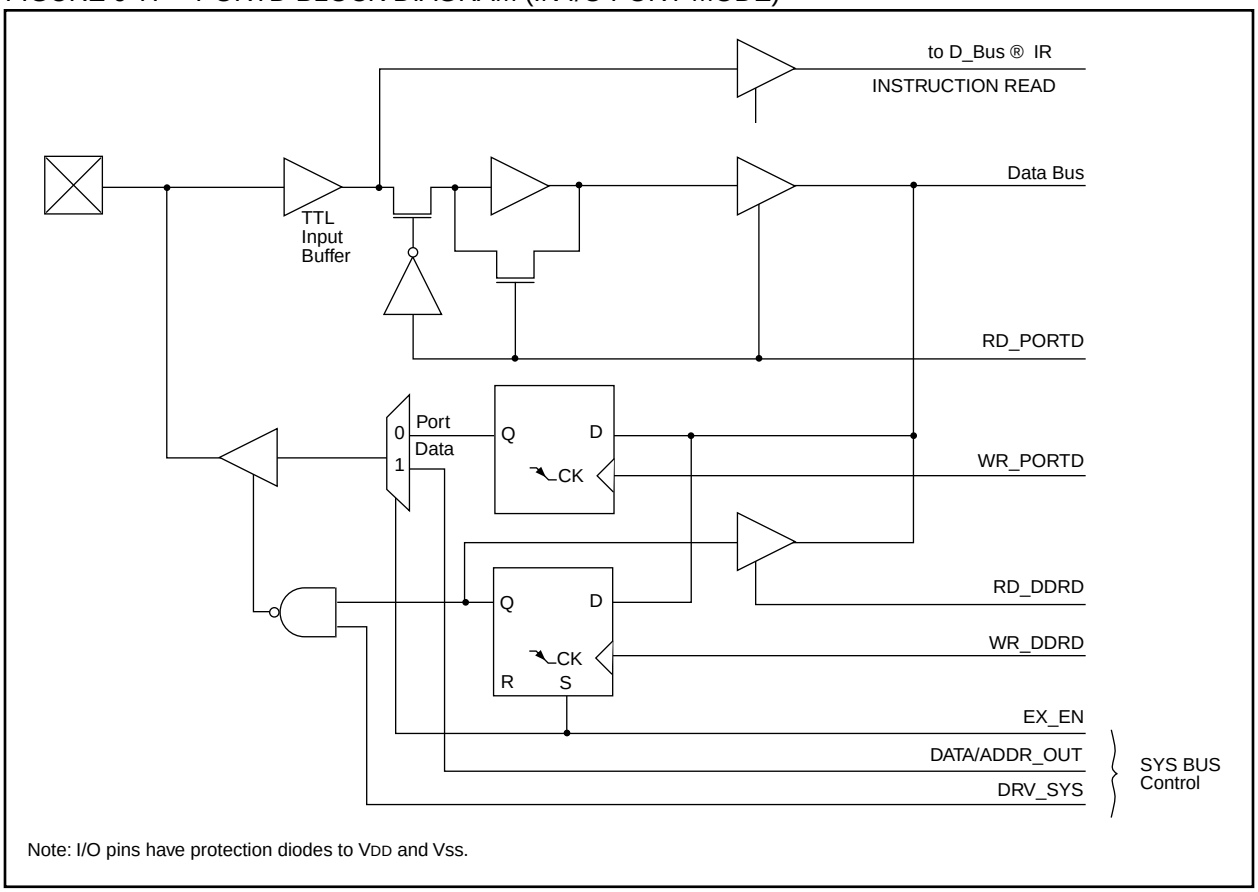
Note: This port is conÞgured as the system bus when the deviceÕs conÞguration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

Example 9-3 shows the instruction sequence to initialize PORTD. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-3: INITIALIZING PORTD

```
MOVLB  1          ;  Select Bank 1
CLRF   PORTD      ;  Initialize PORTD data
                  ;   latches before setting
                  ;   the data direction
                  ;   register
MOVLW  0xCF       ;  Value used to initialize
                  ;   data direction
MOVWF  DDRD       ;  Set RD<3:0> as inputs
                  ;   RD<5:4> as outputs
                  ;   RD<7:6> as inputs
```

FIGURE 9-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)




Note: I/O pins have protection diodes to VDD and Vss.


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TABLE 9-7: PORTD FUNCTIONS

| Name | Bit | Buffer Type | Function |
|---|---|---|---|
| RD0/AD8 | bit0 | TTL | Input/Output or system bus address/data pin. |
| RD1/AD9 | bit1 | TTL | Input/Output or system bus address/data pin. |
| RD2/AD10 | bit2 | TTL | Input/Output or system bus address/data pin. |
| RD3/AD11 | bit3 | TTL | Input/Output or system bus address/data pin. |
| RD4/AD12 | bit4 | TTL | Input/Output or system bus address/data pin. |
| RD5/AD13 | bit5 | TTL | Input/Output or system bus address/data pin. |
| RD6/AD14 | bit6 | TTL | Input/Output or system bus address/data pin. |
| RD7/AD15 | bit7 | TTL | Input/Output or system bus address/data pin. |

Legend: TTL = TTL input.

TABLE 9-8: REGISTERS/BITS ASSOCIATED WITH PORTD

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 13h, Bank 1 | PORTD | RD7/ AD15 | RD6/ AD14 | RD5/ AD13 | RD4/ AD12 | RD3/ AD11 | RD2/ AD10 | RD1/ AD9 | RD0/ AD8 | xxxx xxxx | uuuu uuuu |
| 12h, Bank 1 | DDRD | Data direction register for PORTD | | | | | | | | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and the Watchdog Timer Reset.

### 9.4.1 PORTE AND DDRE REGISTER

PORTE is a 3-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE conÞgures the corresponding port pin as an input. A '0' in the DDRE register conÞgures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to it will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable ($\overline{OE}$), and Write ($\overline{WR}$). The control signals $\overline{OE}$ and $\overline{WR}$ are active low signals. The timing for the system bus is shown in the Electrical Characteristics section.

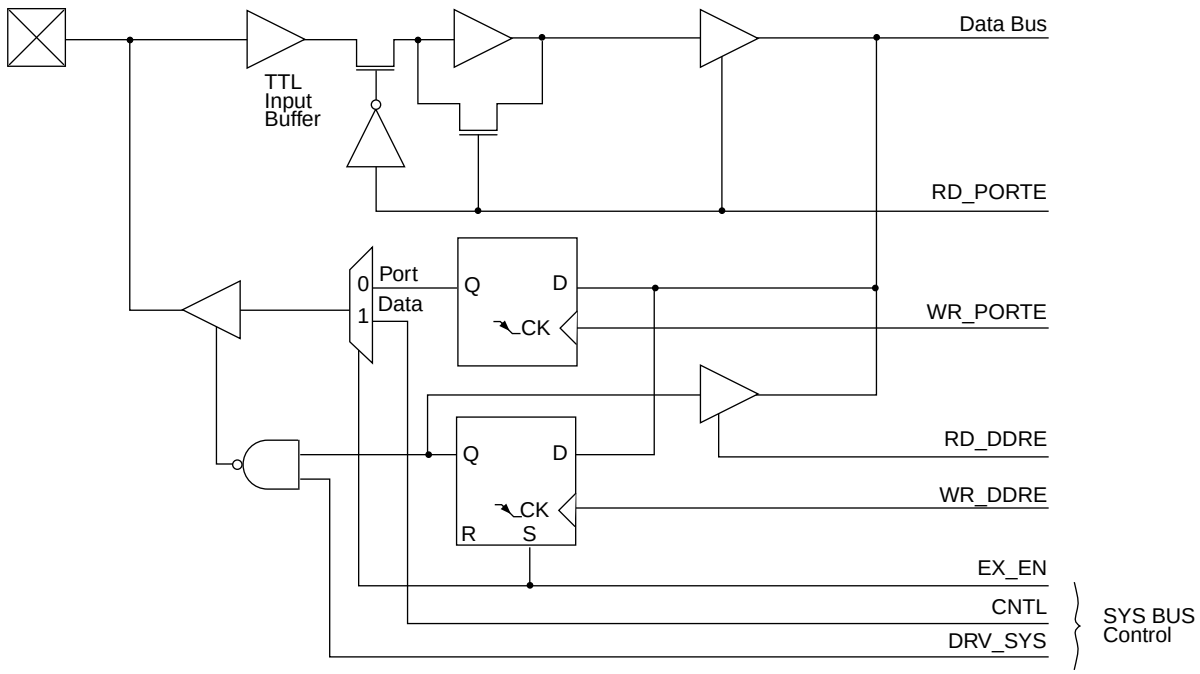
| Note: | This port is conÞgured as the system bus when the deviceÕs conÞguration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O. |
|---|---|

Example 9-4 shows the instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-4: INITIALIZING PORTE

```
MOVLB  1          ;  Select Bank 1
CLRF   PORTE      ;  Initialize PORTE data
                  ;   latches before setting
                  ;   the data direction
                  ;   register
MOVLW  0x03       ;  Value used to initialize
                  ;   data direction
MOVWF  DDRE       ;  Set RE<1:0> as inputs
                  ;   RE<2> as outputs
                  ;   RE<7:3> are always
                  ;   read as '0'
```

FIGURE 9-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)




Note: I/O pins have protection diodes to VDD and Vss.


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TABLE 9-9: PORTE FUNCTIONS

| Name | Bit | Buffer Type | Function |
|---|---|---|---|
| RE0/ALE | bit0 | TTL | Input/Output or system bus Address Latch Enable (ALE) control pin. |
| RE1/$\overline{OE}$ | bit1 | TTL | Input/Output or system bus Output Enable ($\overline{OE}$) control pin. |
| RE2/$\overline{WR}$ | bit2 | TTL | Input/Output or system bus Write ($\overline{WR}$) control pin. |

Legend: TTL = TTL input.

TABLE 9-10: REGISTERS/BITS ASSOCIATED WITH PORTE

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 15h, Bank 1 | PORTE | Ñ | Ñ | Ñ | Ñ | Ñ | RE2/$\overline{WR}$ | RE1/$\overline{OE}$ | RE0/ALE | ---- -xxx | ---- -uuu |
| 14h, Bank 1 | DDRE | Data direction register for PORTE | | | | | | | | ---- -111 | ---- -111 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTE.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

## 9.5 I/O Programming Considerations

### 9.5.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. For example, the BCF and BSF instructions read the register into the CPU, execute the bit operation, and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs deÞned. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g. bit0) and it is deÞned as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading a port reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (BCF, BSF, BTG, etc.) on a port, the value of the port pins is read, the desired operation is performed with this value, and the value is then written to the port latch.

Example 9-5 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 9-5: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

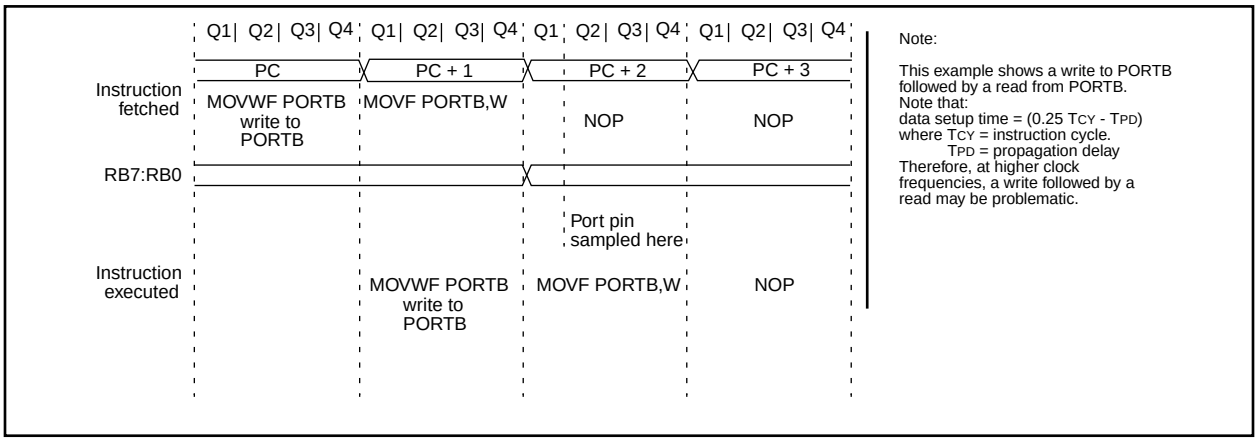
```
; Initial PORT settings: PORTB<7:4> Inputs
;                        PORTB<3:0> Outputs
; PORTB<7:6> have pull-ups and are
; not connected to other circuitry
;
;                       PORT latch  PORT pins
;                       ----------  ---------
;
   BCF   PORTB, 7       01pp pppp   11pp pppp
   BCF   PORTB, 6       10pp pppp   11pp pppp
;
   BCF   DDRB, 7        10pp pppp   11pp pppp
   BCF   DDRB, 6        10pp pppp   10pp pppp
;
; Note that the user may have expected the
; pin values to be 00pp pppp. The 2nd BCF
; caused RB7 to be latched as the pin value
; (High).
```

Note: A pin actively outputting a Low or High should not be driven from external devices in order to change the level on this pin (i.e. Òwired-orÓ, Òwired-andÓ). The resulting high output currents may damage the device.

### 9.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 9-9). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before executing the instruction that reads the values on that I/O port. Otherwise, the previous state of that pin may be read into the CPU rather than the ÒnewÓ state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 9-9: SUCCESSIVE I/O OPERATION





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## 10.0 OVERVIEW OF TIMER RESOURCES

The PIC17C4X has four timer modules. Each module can generate an interrupt to indicate that an event has occurred. These timers are called:

- ¥ Timer0 - 16-bit timer with programmable 8-bit prescaler
- ¥ Timer1 - 8-bit timer
- ¥ Timer2 - 8-bit timer
- ¥ Timer3 - 16-bit timer

For enhanced time-base functionality, two input Captures and two Pulse Width Modulation (PWM) outputs are possible. The PWMs use the TMR1 and TMR2 resources and the input Captures use the TMR3 resource.

### 10.1 Timer0 Overview

The Timer0 module is a simple 16-bit overßow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock.

The Timer0 module also has a programmable prescaler option. The PS3:PS0 bits (T0STA<4:1>) determine the prescaler value. TMR0 can increment at the following rates: 1:1, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, 1:256.

When TImer0Õs clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the deviceÕs frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

### 10.2 Timer1 Overview

The TImer0 module is an 8-bit timer/counter with an 8-bit period register (PR1). When the TMR1 value rolls over from the period match value to 0h, the TMR1IF ßag is set, and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB4/TCLK12 pin, which can also be selected to be the clock for the Timer2 module.

TMR1 can be concatenated to TMR2 to form a 16-bit timer. The TMR1 register is the LSB and TMR2 is the MSB. When in the 16-bit timer mode, there is a corresponding 16-bit period register (PR2:PR1). When the TMR2:TMR1 value rolls over from the period match value to 0h, the TMR1IF ßag is set, and an interrupt will be generated when enabled.

### 10.3 Timer2 Overview

The TMR2 module is an 8-bit timer/counter with an 8-bit period register (PR2). When the TMR2 value rolls over from the period match value to 0h, the TMR2IF ßag is set, and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB4/TCLK12 pin, which can also be selected to be the clock for the TMR1 module.

TMR1 can be concatenated to TMR2 to form a 16-bit timer. The TMR2 register is the MSB and TMR1 is the LSB. When in the 16-bit timer mode, there is a corresponding 16-bit period register (PR2:PR1). When the TMR2:TMR1 value rolls over from the period match value to 0h, the TMR1IF ßag is set, and an interrupt will be generated when enabled.

### 10.4 Timer3 Overview

The TImer3 module is a 16-bit timer/counter with a 16-bit period register. When the TMR3H:TMR3L value rolls over to 0h, the TMR3IF bit is set and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB5/TCLK3 pin.

When operating in the dual capture mode, the period registers become the second 16-bit capture register.

### 10.5 Role of the Timer/Counters

The timer modules are general purpose, but have dedicated resources associated with them. TImer1 and Timer2 are the time-bases for the two Pulse Width Modulation (PWM) outputs, while Timer3 is the time-base for the two input captures.



This document was created with FrameMaker 4.0.4

NOTES:


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## 11.0 TIMER0

The Timer0 module consists of a 16-bit timer/counter, TMR0. The high byte is TMR0H and the low byte is TMR0L. A software programmable 8-bit prescaler makes an effective 24-bit overßow timer. The clock source is also software programmable as either the internal instruction clock or the RA1/T0CKI pin. The control bits for this module are in register T0STA (Figure 11-1).

FIGURE 11-1: T0STA REGISTER (ADDRESS: 05h, UNBANKED)

| R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | U - 0 |
|---|---|---|---|---|---|---|---|
| INTEDG | T0SE | T0CS | PS3 | PS2 | PS1 | PS0 | Ñ |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented, Read as '0'
-n = Value at POR reset

bit 7: INTEDG: RA0/INT Pin Interrupt Edge Select bit
This bit selects the edge upon which the interrupt is detected
1 = Rising edge of RA0/INT pin generates interrupt
0 = Falling edge of RA0/INT pin generates interrupt

bit 6: T0SE: Timer0 Clock Input Edge Select bit
This bit selects the edge upon which TMR0 will increment
When T0CS = 0
1 = Rising edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
0 = Falling edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
When T0CS = 1
DonÕt care

bit 5: T0CS: Timer0 Clock Source Select bit
This bit selects the clock source for TMR0.
1 = Internal instruction clock cycle (TCY)
0 = T0CKI pin

bit 4-1: PS3:PS0: Timer0 Prescale Selection bits
These bits select the prescale value for TMR0.

| PS3:PS0 | Prescale Value |
|---|---|
| 0000 | 1:1 |
| 0001 | 1:2 |
| 0010 | 1:4 |
| 0011 | 1:8 |
| 0100 | 1:16 |
| 0101 | 1:32 |
| 0110 | 1:64 |
| 0111 | 1:128 |
| 1xxx | 1:256 |

bit 0: Unimplemented : Read as '0'



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## 11.1 Timer0 Operation

When the T0CS (T0STA<5>) bit is set, TMR0 increments on the internal clock. When T0CS is clear, TMR0 increments on the external clock (RA1/T0CKI pin). The external clock edge can be conÞgured in software. When the T0SE (T0STA<6>) bit is set, the timer will increment on the rising edge of the RA1/T0CKI pin. When T0SE is clear, the timer will increment on the falling edge of the RA1/T0CKI pin. The prescaler can be programmed to introduce a prescale of 1:1 to 1:256. The timer increments from 0000h to FFFFh and rolls over to 0000h. On overßow, the TMR0 Interrupt Flag bit (T0IF) is set. The TMR0 interrupt can be masked by clearing the corresponding TMR0 Interrupt Enable bit (T0IE). The TMR0 Interrupt Flag bit (T0IF) is automatically cleared when vectoring to the TMR0 interrupt vector.

## 11.2 Using Timer0 with External Clock

When the external clock input is used for Timer0, it is synchronized with the internal phase clocks. Figure 11-3 shows the synchronization of the external clock. This synchronization is done after the prescaler. The output of the prescaler (PSOUT) is sampled twice in every instruction cycle to detect a rising or a falling edge. The timing requirements for the external clock are detailed in the electrical speciÞcation section for the desired device.

### 11.2.1 DELAY FROM EXTERNAL CLOCK EDGE

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time TMR0 is actually incremented. Figure 11-3 shows that this delay is between 3TOSC and 7TOSC. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4TOSC (±121 ns @ 33 MHz).

FIGURE 11-2: TIMER0 MODULE BLOCK DIAGRAM

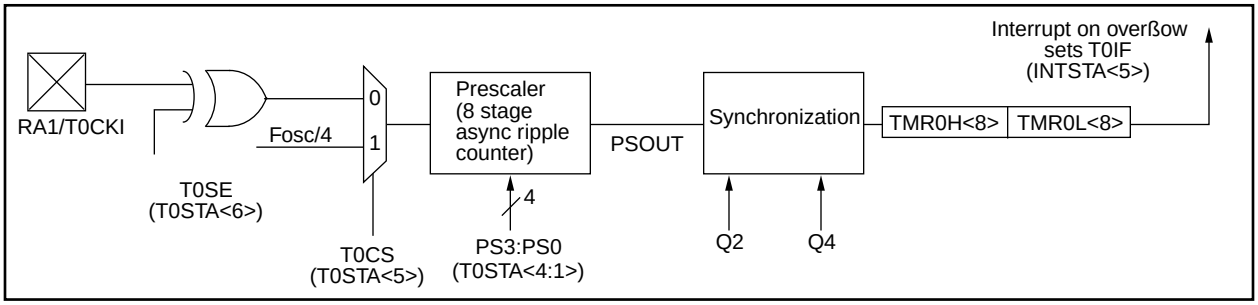
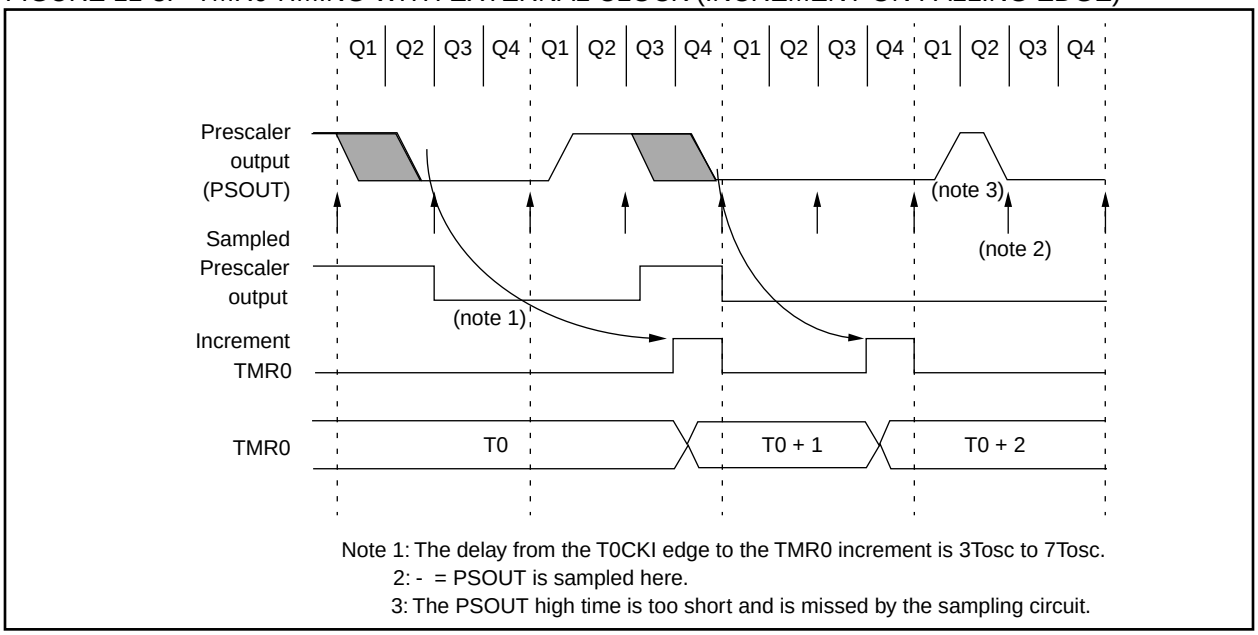



FIGURE 11-3: TMR0 TIMING WITH EXTERNAL CLOCK (INCREMENT ON FALLING EDGE)




Note 1: The delay from the T0CKI edge to the TMR0 increment is 3Tosc to 7Tosc.
2: - = PSOUT is sampled here.
3: The PSOUT high time is too short and is missed by the sampling circuit.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## 11.3 Read/Write Consideration f or TMR0

Although TMR0 is a 16-bit timer/counter, only 8-bits at a time can be read or written during a single instruction cycle. Care must be taken during any read or write.

### 11.3.1 READING 16-BIT VALUE

The problem in reading the entire 16-bit value is that after reading the low (or high) byte, its value may change from FFh to 00h.

Example 11-1 shows a 16-bit read. To ensure a proper read, interrupts must be disabled during this routine.

EXAMPLE 11-1: 16-BIT READ

```
MOVPF   TMR0L, TMPLO    ;read low tmr0
MOVPF   TMR0H, TMPHI    ;read high tmr0
MOVFP   TMPLO, WREG     ;tmplo -> wreg
CPFSLT  TMR0L           ;tmr0l < wreg?
RETURN                  ;no then return
MOVPF   TMR0L, TMPLO    ;read low tmr0
MOVPF   TMR0H, TMPHI    ;read high tmr0
RETURN                  ;return
```

### 11.3.2 WRITING A 16-BIT VALUE TO TMR0

Since writing to either TMR0L or TMR0H will effectively inhibit increment of that half of the TMR0 in the next cycle (following write), but not inhibit increment of the other half, the user must write to TMR0L Þrst and TMR0H next in two consecutive instructions, as shown in Example 11-2. The interrupt must be disabled. Any write to either TMR0L or TMR0H clears the prescaler.

EXAMPLE 11-2: 16-BIT WRITE

```
BSF   CPUSTA, GLINTD ; Disable interrupt
MOVFP RAM_L, TMR0L   ;
MOVFP RAM_H, TMR0H   ;
BCF   CPUSTA, GLINTD ; Done, enable interrupt
```

## 11.4 Prescaler Assignments

Timer0 has an 8-bit prescaler. The prescaler assignment is fully under software control; i.e., it can be changed Òon the ßyÓ during program execution. When changing the prescaler assignment, clearing the prescaler is recommended before changing assignment. The value of the prescaler is Òunknown,Ó and assigning a value that is less then the present value makes it difÞcult to take this unknown time into account.

FIGURE 11-4: TMR0 TIMING: WRITE HIGH OR LOW BYTE

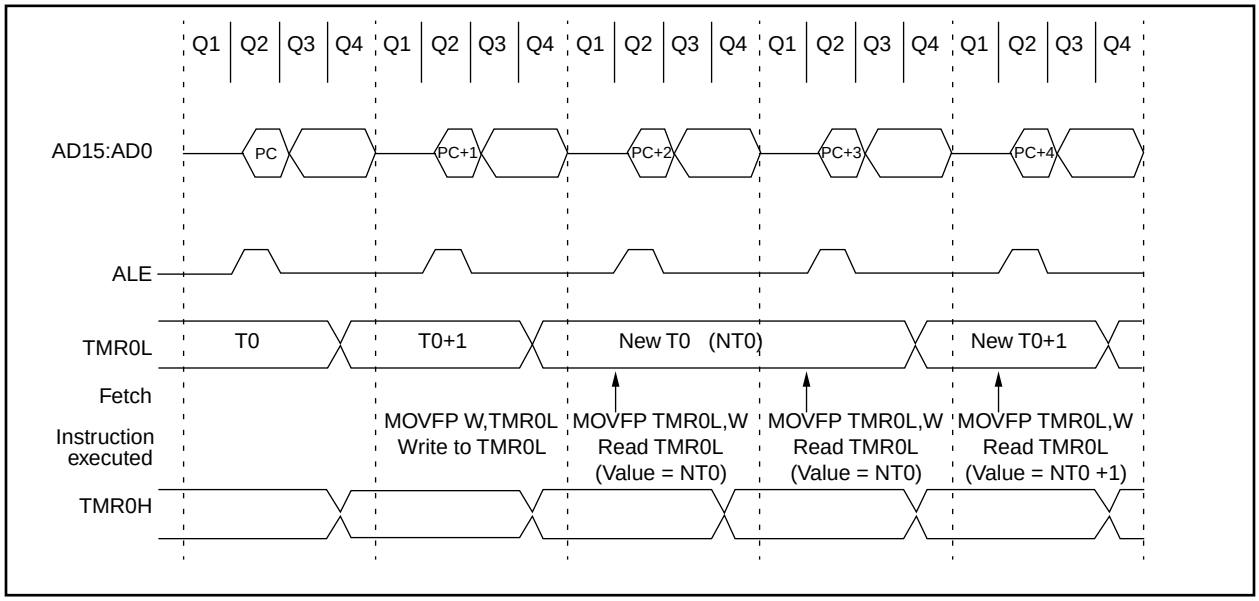
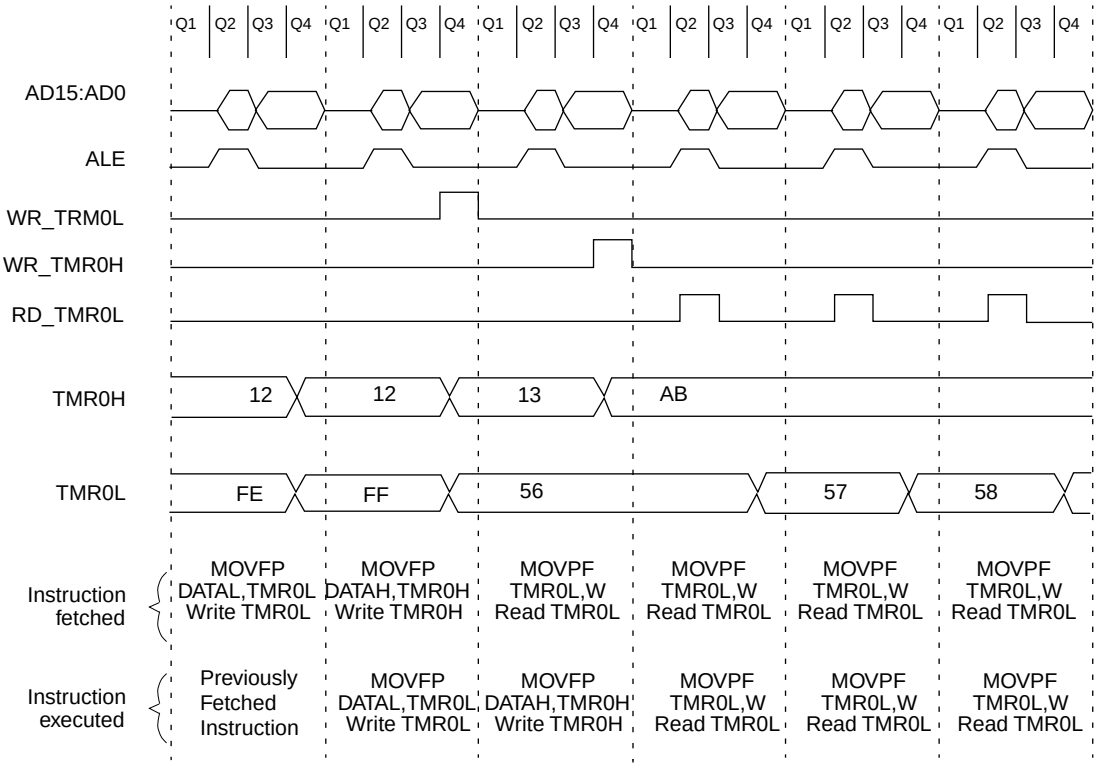


FIGURE 11-5: TMR0 READ/WRITE IN TIMER MODE




In this example, old TMR0 value is 12FEh, new value of AB56h is written.

TABLE 11-1: REGISTERS/BITS ASSOCIATED WITH TIMER0

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 05h, Unbanked | T0STA | INTEDG | T0SE | T0CS | PS3 | PS2 | PS1 | PS0 | Ñ | 0000 000- | 0000 000- |
| 06h, Unbanked | CPUSTA | Ñ | Ñ | STKAV | GLINTD | $\overline{TO}$ | $\overline{PD}$ | Ñ | Ñ | --11 11-- | --11 qq-- |
| 07h, Unbanked | INTSTA | PEIF | T0CKIF | T0IF | INTF | PEIE | T0CKIE | T0IE | INTE | 0000 0000 | 0000 0000 |
| 0Bh, Unbanked | TMR0L | TMR0 register; low byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Ch, Unbanked | TMR0H | TMR0 register; high byte | | | | | | | | xxxx xxxx | uuuu uuuu |

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', q - value depends on condition, Shaded cells are not used by Timer0.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.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## 12.0 TIMER1, TIMER2, TIMER3, PWMS AND CAPTURES

The PIC17C4X has a wealth of timers and time-based functions to ease the implementation of control applications. These time-base functions include two PWM outputs and two Capture inputs.

Timer1 and Timer2 are two 8-bit incrementing timers, each with a period register (PR1 and PR2 respectively) and separate overßow interrupt ßags. Timer1 and Timer2 can operate either as timers (increment on internal Fosc/4 clock) or as counters (increment on falling edge of external clock on pin RB4/TCLK12). They are also software conÞgurable to operate as a single 16-bit timer. These timers are also used as the time-base for the PWM (pulse width modulation) module.

Timer3 is a 16-bit timer/counter consisting of the TMR3H and TMR3L registers. This timer has four other associated registers. Two registers are used as a 16-bit period register or a 16-bit Capture1 register (PR3H/CA1H:PR3L/CA1L). The other two registers are strictly the Capture2 registers (CA2H:CA2L). Timer3 is the time-base for the two 16-bit captures.

TMR3 can be software conÞgured to increment from the internal system clock or from an external signal on the RB5/TCLK3 pin.

Figure 12-1 and Figure 12-2 are the control registers for the operation of Timer1, Timer2, and Timer3, as well as PWM1, PWM2, Capture1, and Capture2.

FIGURE 12-1: TCON1 REGISTER (ADDRESS: 16h, BANK 3)

| R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 |
|---|---|---|---|---|---|---|---|
| CA2ED1 | CA2ED0 | CA1ED1 | CA1ED0 | T16 | TMR3CS | TMR2CS | TMR1CS |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7-6: CA2ED1:CA2ED0: Capture2 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 5-4: CA1ED1:CA1ED0: Capture1 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 3: T16: Timer1:Timer2 Mode Select bit
1 = Timer1 and Timer2 form a 16-bit timer
0 = Timer1 and Timer2 are two 8-bit timers

bit 2: TMR3CS: Timer3 Clock Source Select bit
1 = TMR3 increments off the falling edge of the RB5/TCLK3 pin
0 = TMR3 increments off the internal clock

bit 1: TMR2CS: Timer2 Clock Source Select bit
1 = TMR2 increments off the falling edge of the RB4/TCLK12 pin
0 = TMR2 increments off the internal clock

bit 0: TMR1CS: Timer1 Clock Source Select bit
1 = TMR1 increments off the falling edge of the RB4/TCLK12 pin
0 = TMR1 increments off the internal clock



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FIGURE 12-2: TCON2 REGISTER (ADDRESS: 17h, BANK 3)

| R - 0 | R - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 |
|---|---|---|---|---|---|---|---|
| CA2OVF | CA1OVF | PWM2ON | PWM1ON | CA1/$\overline{PR3}$ | TMR3ON | TMR2ON | TMR1ON |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7: CA2OVF: Capture2 Overßow Status bit
This bit indicates that the capture value had not been read from the capture register pair (CA2H:CA2L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overßow). Subsequent capture events will not update the capture register with the Timer3 value until the capture register has been read (both bytes).
1 = Overßow occurred on Capture2 register
0 = No overßow occurred on Capture2 register

bit 6: CA1OVF: Capture1 Overßow Status bit
This bit indicates that the capture value had not been read from the capture register pair (PR3H/CA2H:PR3L/CA2L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overßow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).
1 = Overßow occurred on Capture1 register
0 = No overßow occurred on Capture1 register

bit 5: PWM2ON: PWM2 On bit
1 = PWM2 is enabled (The RB3/PWM2 pin ignores the state of the DDRB<3> bit)
0 = PWM2 is disabled (The RB3/PWM2 pin uses the state of the DDRB<3> bit for data direction)

bit 4: PWM1ON: PWM1 On bit
1 = PWM1 is enabled (The RB2/PWM1 pin ignores the state of the DDRB<2> bit)
0 = PWM1 is disabled (The RB2/PWM1 pin uses the state of the DDRB<2> bit for data direction)

bit 3: CA1/$\overline{PR3}$: CA1/$\overline{PR3}$ Register Mode Select bit
1 = Enables Capture1 (PR3H/CA1H:PR3L/CA1L is the Capture1 register. Timer3 runs without a period register)
0 = Enables the Period register (PR3H/CA1H:PR3L/CA1L is the Period register for Timer3)

bit 2: TMR3ON: Timer3 On bit
1 = Starts Timer3
0 = Stops Timer3

bit 1: TMR2ON: Timer2 On bit
This bit controls the incrementing of the Timer2 register. When Timer2:Timer1 form the 16-bit timer (T16 is set), TMR2ON must be set. This allows the MSB of the timer to increment.
1 = Starts Timer2 (Must be enabled if the T16 bit (TCON1<3>) is set)
0 = Stops Timer2

bit 0: TMR1ON: Timer1 On bit
When T16 is set (in 16-bit Timer Mode)
1 = Starts 16-bit Timer2:Timer1
0 = Stops 16-bit Timer2:Timer1

When T16 is clear (in 8-bit Timer Mode)
1 = Starts 8-bit Timer1
0 = Stops 8-bit Timer1


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## 12.1 Timer1 an d Timer2

### 12.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently conÞgured to increment from the internal instruction cycle clock or from an external clock source on the RB4/TCLK12 pin. The timer clock source is conÞgured by the TMRxCS bit (x = 1 for Timer1 or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (Fosc/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt ßag is set when the timer is reset. TMR1 and TMR2 have individual interrupt ßag bits. The TMR1 interrupt ßag bit is latched into TMR1IF, and the TMR2 interrupt ßag bit is latched into TMR2IF.

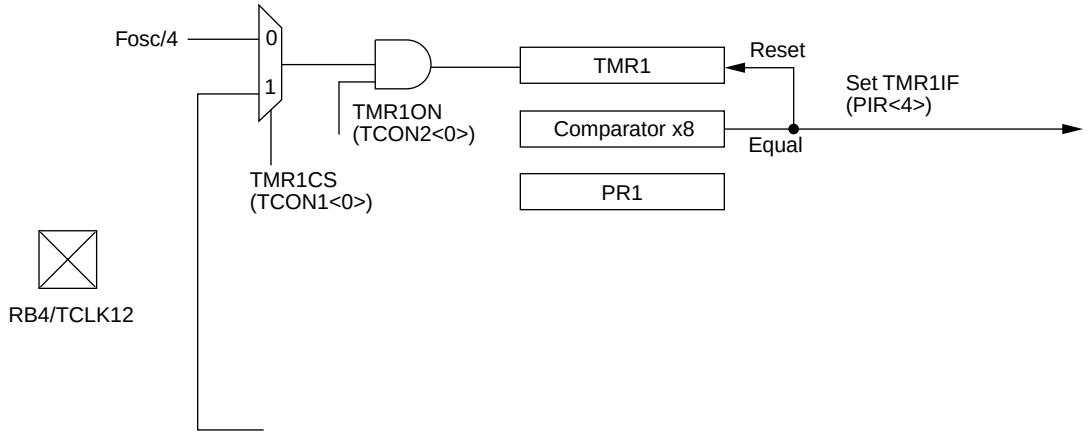
Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled by setting this bit and disabled by clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be enabled (PEIE is set) and global interrupts must be enabled (GLINTD is cleared).

The timers can be turned on and off under software control. When the Timerx On control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt ßag to be set.

#### 12.1.1.1 EXTERNAL CLOCK INPUT FOR TIMER1 OR TIMER2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical SpeciÞcation section.

FIGURE 12-3: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE



| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 18-17: $I_{OL}$ vs. $V_{OL}$, $V_{DD}$ = 5V

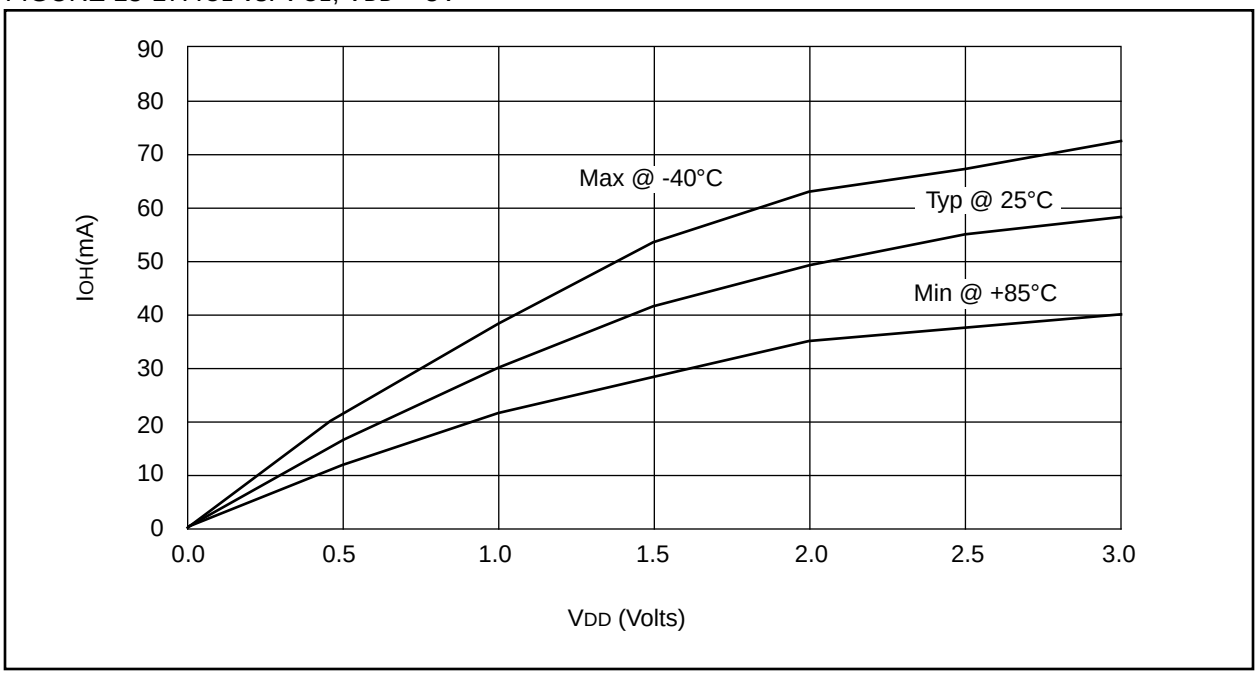
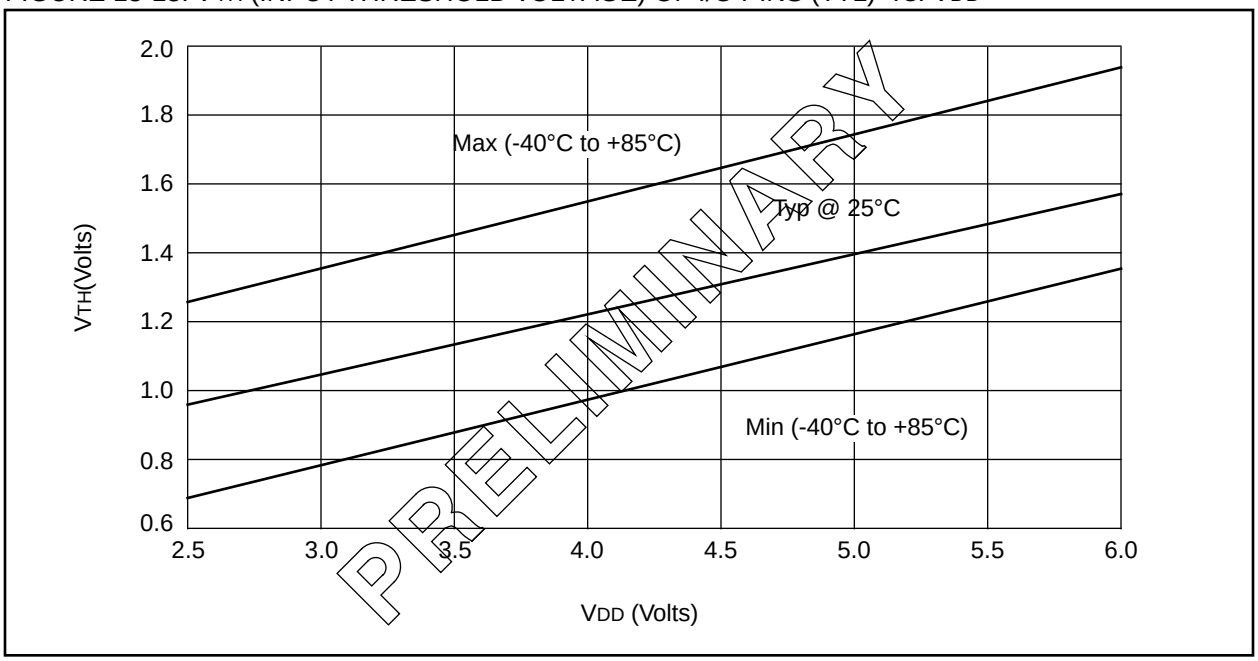



FIGURE 18-18: $V_{TH}$ (INPUT THRESHOLD VOLTAGE) OF I/O PINS (TTL) vs. $V_{DD}$

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|---|---|---|---|---|---|---|

FIGURE 18-19: $V_{TH}$, $V_{IL}$ of I/O PINS (SCHMITT TRIGGER) vs. $V_{DD}$

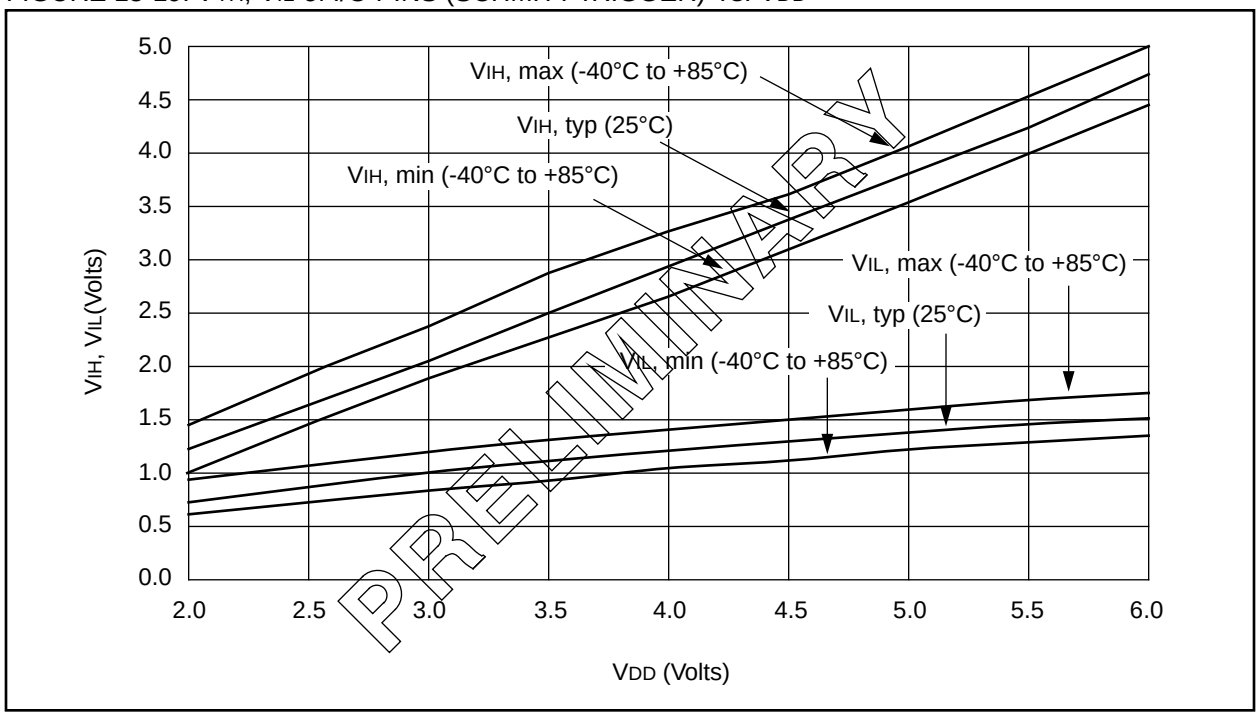
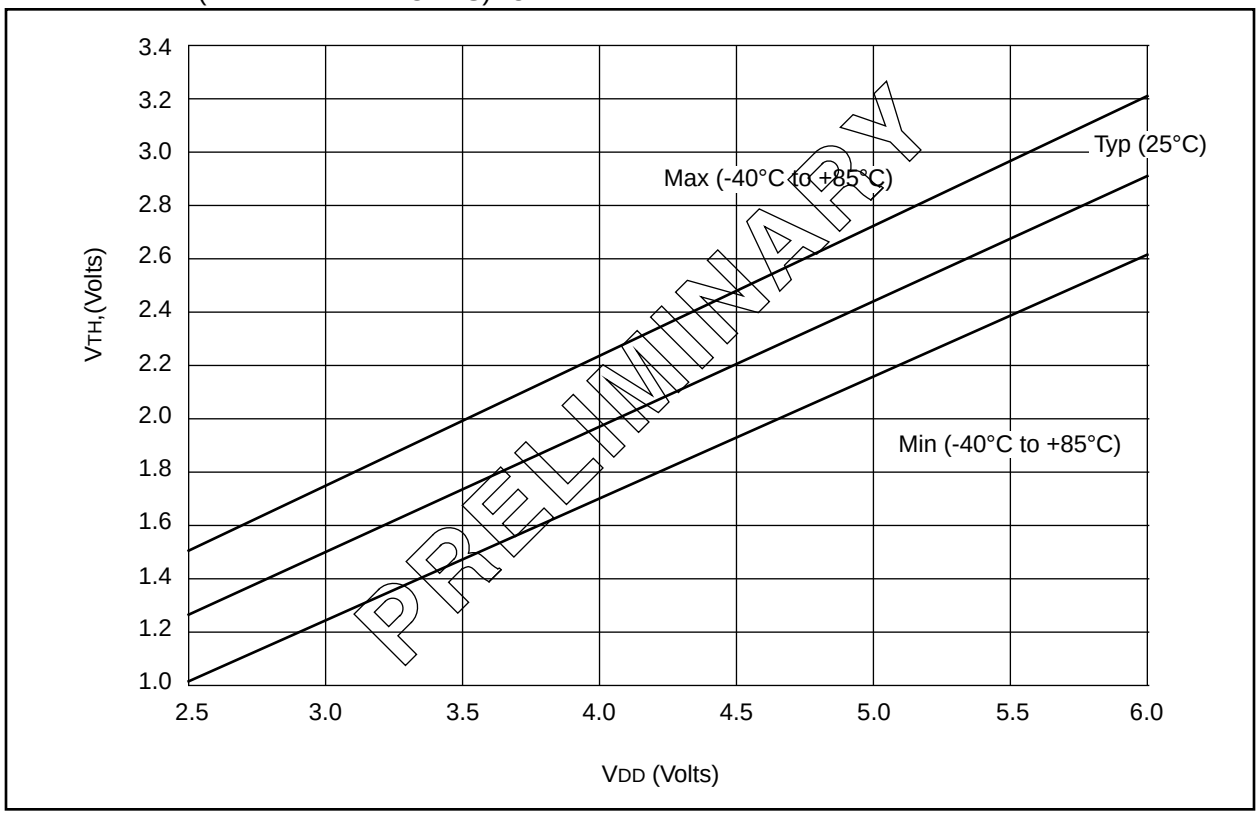



FIGURE 18-20: $V_{TH}$ (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LF MODES) vs. $V_{DD}$



NOTES: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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 19.0 PIC17CR42/42A/43/R43/44 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ambient temperature under bias ..... -55 to +125ûC

Storage temperature ..... -65ûC to +150ûC

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ (Note 2) ..... -0.6V to +14V

Voltage on RA2 and RA3 with respect to $V_{SS}$ ..... -0.6V to +14V

Voltage on all other pins with respect to $V_{SS}$ ..... -0.6V to $V_{DD}$ + 0.6V

Total power dissipation (Note 1) ..... 1.0W

Maximum current out of $V_{SS}$ pin(s) - total ..... 250 mA

Maximum current into $V_{DD}$ pin(s) - total ..... 200 mA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... 20 mA±

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... 20 mA±

Maximum output current sunk by any I/O pin (except RA2 and RA3) ..... 35 mA

Maximum output current sunk by RA2 or RA3 pins ..... 60 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA and PORTB (combined) ..... 150 mA

Maximum current sourced by PORTA and PORTB (combined) ..... 100 mA

Maximum current sunk by PORTC, PORTD and PORTE (combined) ..... 150 mA

Maximum current sourced by PORTC, PORTD and PORTE (combined) ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100W should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to $V_{SS}$.

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

| OSC | PIC17LCR42-08<br>PIC17LC42A-08<br>PIC17LC43-08<br>PIC17LCR43-08<br>PIC17LC44-08 | PIC17CR42-16<br>PIC17C42A-16<br>PIC17C43-16<br>PIC17CR43-16<br>PIC17C44-16 | PIC17CR42-25<br>PIC17C42A-25<br>PIC17C43-25<br>PIC17CR43-25<br>PIC17C44-25 | PIC17CR42-33<br>PIC17C42A-33<br>PIC17C43-33<br>PIC17CR43-33<br>PIC17C44-33 | JW Devices<br>(Ceramic Windowed Devices) |
|---|---|---|---|---|---|
| RC | VDD: 2.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. |
| XT | VDD: 2.5V to 6.0V<br>IDD: 12 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 8 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 24 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 16 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 25 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. |
| EC | VDD: 2.5V to 6.0V<br>IDD: 12 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 8 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 24 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 16 MHz Max | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 25 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. |
| LF | VDD: 2.5V to 6.0V<br>IDD: 150 mA max. at 32 kHz<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 mA typ. at 32 kHz<br>IPD: < 1 mA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 mA typ. at 32 kHz<br>IPD: < 1 mA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 mA typ. at 32 kHz<br>IPD: < 1 mA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 150 mA max. at 32 kHz<br>IPD: 5 mA max. at 5.5V WDT disabled<br>Freq: 2 MHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.



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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

19.1 DC CHARACTERISTICS: PIC17CR42/42A/43/R43/44-16 (Commercial, Industrial)
PIC17CR42/42A/43/R43/44-25 (Commercial, Industrial)
PIC17CR42/42A/43/R43/44-33 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature<br>-40ûC £ TA £ +85ûC for industrial and<br>0ûC £ TA £ +70ûC for commercial | | | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
| D001 | VDD | Supply Voltage | 4.5 | Ð | 6.0 | V | |
| D002 | VDR | RAM Data Retention Voltage (Note 1) | 1.5 * | Ð | Ð | V | Device in SLEEP mode |
| D003 | VPOR | VDD start voltage to ensure internal Power-on Reset signal | Ð | VSS | Ð | V | See section on Power-on Reset for details |
| D004 | SVDD | VDD rise rate to ensure internal Power-on Reset signal | 0.060 * | Ð | Ð | mV/ms | See section on Power-on Reset for details |
| D010 | IDD | Supply Current (Note 2) | Ð | 3 | 6 | mA | FOSC = 4 MHz (Note 4) |
| D011 | | | Ð | 6 | 12 * | mA | FOSC = 8 MHz |
| D012 | | | Ð | 11 | 24 * | mA | FOSC = 16 MHz |
| D013 | | | Ð | 19 | 38 | mA | FOSC = 25 MHz |
| D015 | | | Ð | 25 | 50 | mA | FOSC = 33 MHz |
| D014 | | | Ð | 95 | 150 | mA | FOSC = 32 kHz, WDT enabled (EC osc conÞguration) |
| D020 | IPD | Power-down Current (Note 3) | Ð | 10 | 40 | mA | VDD = 5.5V, WDT enabled |
| D021 | | | Ð | < 1 | 5 | mA | VDD = 5.5V, WDT disabled |

* These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as speciÞed.
Current consumed from the oscillator and I/OÕs driving external capacitive or resistive loads needs to be considered.
For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 · R).
For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL · VDD) · f
CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.
The capacitive currents are most signiÞcant when the device is conÞgured for external execution (includes extended microcontroller mode).

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc conÞguration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 19.2 DC CHARACTERISTICS: PIC17LC42A/43/LC44 (Commercial, Industrial) PIC17LCR42/43 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature<br>-40ûC £ TA £ +85ûC for industrial and<br>0ûC £ TA £ +70ûC for commercial | | | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
| D001 | VDD | Supply Voltage | 2.5 | Ð | 6.0 | V | |
| D002 | VDR | RAM Data Retention Voltage (Note 1) | 1.5 * | Ð | Ð | V | Device in SLEEP mode |
| D003 | VPOR | VDD start voltage to ensure internal Power-on Reset signal | Ð | VSS | Ð | V | See section on Power-on Reset for details |
| D004 | SVDD | VDD rise rate to ensure internal Power-on Reset signal | 0.060 * | Ð | Ð | mV/ms | See section on Power-on Reset for details |
| D010 | IDD | Supply Current (Note 2) | Ð | 3 | 6 | mA | FOSC = 4 MHz (Note 4) |
| D011 | | | Ð | 6 | 12 * | mA | FOSC = 8 MHz |
| D014 | | | Ð | 95 | 150 | mA | FOSC = 32 kHz, WDT disabled (EC osc conÞguration) |
| D020 | IPD | Power-down Current (Note 3) | Ð | 10 | 40 | mA | VDD = 5.5V, WDT enabled |
| D021 | | | Ð | < 1 | 5 | mA | VDD = 5.5V, WDT disabled |

* These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as speciÞed.
Current consumed from the oscillator and I/OÕs driving external capacitive or resistive loads needs to be considered.
For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 · R).
For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL · VDD) · f
CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.
The capacitive currents are most signiÞcant when the device is conÞgured for external execution (includes extended microcontroller mode).

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc conÞguration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

19.3 DC CHARACTERISTICS: PIC17CR42/42A/43/R43/44-16 (Commercial, Industrial)
PIC17CR42/42A/43/R43/44-25 (Commercial, Industrial)
PIC17CR42/42A/43/R43/44-33 (Commercial, Industrial)
PIC17LCR42/42A/43/R43/44-08 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature<br>-40ûC £ TA £ +85ûC for industrial and<br>0ûC £ TA £ +70ûC for commercial<br>Operating voltage VDD range as described in Section 19.1 | | | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
| | VIL | Input Low Voltage<br>I/O ports | | | | | |
| D030 | | with TTL buffer | VSS | Ð | 0.8 | V | 4.5V £ VDD £ 5.5V |
| | | | VSS | Ð | 0.2VDD | V | 2.5V £ VDD £ 4.5V |
| D031 | | with Schmitt Trigger buffer | VSS | Ð | 0.2VDD | V | |
| D032 | | MCLR, OSC1 (in EC and RC mode) | Vss | Ð | 0.2VDD | V | Note1 |
| D033 | | OSC1 (in XT, and LF mode) | Ð | 0.5VDD | Ð | V | |
| | VIH | Input High Voltage<br>I/O ports | | | | | |
| D040 | | with TTL buffer | 2.0 | Ð | VDD | V | 4.5V £ VDD £ 5.5V |
| | | | 1 + 0.2VDD | Ð | VDD | V | 2.5V £ VDD £ 4.5V |
| D041 | | with Schmitt Trigger buffer | 0.8VDD | Ð | VDD | V | |
| D042 | | MCLR | 0.8VDD | Ð | VDD | V | Note1 |
| D043 | | OSC1 (XT, and LF mode) | Ð | 0.5VDD | Ð | V | |
| D050 | VHYS | Hysteresis of Schmitt Trigger inputs | 0.15VDD * | Ð | Ð | V | |
| | | Input Leakage Current (Notes 2, 3) | | | | | |
| D060 | IIL | I/O ports (except RA2, RA3) | Ð | Ð | ±1 | mA | Vss £ VPIN £ VDD, I/O Pin at hi-impedance PORTB weak pull-ups disabled |
| D061 | | MCLR | Ð | Ð | ±2 | mA | VPIN = Vss or VPIN = VDD |
| D062 | | RA2, RA3 | | | ±2 | mA | Vss £ VRA2, VRA3 £ 12V |
| D063 | | OSC1, TEST (EC, RC modes) | Ð | Ð | ±1 | mA | Vss £ VPIN £ VDD |
| D063B | | OSC1, TEST (XT, LF modes) | Ð | Ð | VPIN | mA | RF ³ 1 MW, see Figure 14.2 |
| D064 | | MCLR | Ð | Ð | 10 | mA | VMCLR = VPP = 12V (when not programming) |
| D070 | IPURB | PORTB weak pull-up current | 60 | 200 | 400 | mA | VPIN = VSS, RBPU = 0<br>4.5V £ VDD £ 6.0V |

* These parameters are characterized but not tested.
Data in ÒTypÓ column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.
à These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator conÞguration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.
2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The speciÞed levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
3: Negative current is deÞned as coming out of the pin.
4: These speciÞcations are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming speciÞcations can be found in: PIC17CXX Programming SpeciÞcations (Literature number DS30139).
5: The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.
6: For TTL buffers, the better of the two speciÞcations may be used.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature
-40ûC £ TA £ +85ûC for industrial and
0ûC £ TA £ +70ûC for commercial
Operating voltage VDD range as described in Section 19.1

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | Output Low Voltage | | | | | |
| D080 | VOL | I/O ports (except RA2 and RA3) | | | | | IOL = VDD/1.250 mA |
| | | | Ð | Ð | 0.1VDD | V | 4.5V £ VDD £ 6.0V |
| | | | Ð | Ð | 0.1VDD * | V | VDD = 2.5V |
| D081 | | with TTL buffer | Ð | Ð | 0.4 | V | IOL = 6 mA, VDD = 4.5V Note 6 |
| D082 | | RA2 and RA3 | Ð | Ð | 3.0 | V | IOL = 60.0 mA, VDD = 6.0V |
| D083 | | OSC2/CLKOUT | Ð | Ð | 0.4 | V | IOL = 1 mA, VDD = 4.5V |
| D084 | | (RC and EC osc modes) | Ð | Ð | 0.1VDD * | V | IOL = VDD/5 mA (PIC17LC43/LC44 only) |
| | | Output High Voltage (Note 3) | | | | | |
| D090 | VOH | I/O ports (except RA2 and RA3) | | | | | IOH = -VDD/2.500 mA |
| | | | 0.9VDD | Ð | Ð | V | 4.5V £ VDD £ 6.0V |
| | | | 0.9VDD * | Ð | Ð | V | VDD = 2.5V |
| D091 | | with TTL buffer | 2.4 | Ð | Ð | V | IOH = -6.0 mA, VDD=4.5V Note 6 |
| D092 | | RA2 and RA3 | Ð | Ð | 12 | V | Pulled-up to externally applied voltage |
| D093 | | OSC2/CLKOUT | 2.4 | Ð | Ð | V | IOH = -5 mA, VDD = 4.5V |
| D094 | | (RC and EC osc modes) | 0.9VDD * | Ð | Ð | V | IOH = -VDD/5 mA (PIC17LC43/LC44 only) |
| | | Capacitive Loading Specs on Output Pins | | | | | |
| D100 | COSC2 | OSC2/CLKOUT pin | Ð | Ð | 25 | pF | In EC or RC osc modes when OSC2 pin is outputting CLKOUT. external clock is used to drive OSC1. |
| D101 | CIO | All I/O pins and OSC2 (in RC mode) | Ð | Ð | 50 | pF | |
| D102 | CAD | System Interface Bus (PORTC, PORTD and PORTE) | Ð | Ð | 50 | pF | In Microprocessor or Extended Microcontroller mode |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

à These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator conÞguration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The speciÞed levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is deÞned as coming out of the pin.

4: These speciÞcations are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming speciÞcations can be found in: PIC17CXX Programming SpeciÞcations (Literature number DS30139).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two speciÞcations may be used.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature<br>-40ûC £ TA £ +40ûC<br>Operating voltage VDD range as described in Section 19.1 | | | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
| | | Internal Program Memory Programming Specs (Note 4) | | | | | |
| D110 | VPP | Voltage on MCLR/VPP pin | 12.75 | Ð | 13.25 | V | Note 5 |
| D111 | VDDP | Supply voltage during programming | 4.75 | 5.0 | 5.25 | V | |
| D112 | IPP | Current into MCLR/VPP pin | Ð | 25 à | 50 à | mA | |
| D113 | IDDP | Supply current during programming | Ð | Ð | 30 à | mA | |
| D114 | TPROG | Programming pulse width | 10 | 100 | 1000 | ms | Terminated via internal/ external interrupt or a reset |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

à These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator conÞguration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The speciÞed levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is deÞned as coming out of the pin.

4: These speciÞcations are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming speciÞcations can be found in: PIC17CXX Programming SpeciÞcations (Literature number DS30139).

5: The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two speciÞcations may be used.

Note: When using the Table Write for internal programming, the device temperature must be less than 40ûC.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 19.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST ($I^2C$ specifications only)
4. Ts ($I^2C$ specifications only)

| T | | | |
|---|---|---|---|
| F | Frequency | T | Time |

Lowercase symbols (pp) and their meanings:

| pp | | | |
|---|---|---|---|
| ad | Address/Data | ost | Oscillator Start-Up Timer |
| al | ALE | pwrt | Power-Up Timer |
| cc | Capture1 and Capture2 | rb | PORTB |
| ck | CLKOUT or clock | rd | $\overline{RD}$ |
| dt | Data in | rw | $\overline{RD}$ or $\overline{WR}$ |
| in | INT pin | t0 | T0CKI |
| io | I/O port | t123 | TCLK12 and TCLK3 |
| mc | $\overline{MCLR}$ | wdt | Watchdog Timer |
| oe | $\overline{OE}$ | wr | $\overline{WR}$ |
| os | OSC1 | | |

Uppercase symbols and their meanings:

| S | | | |
|---|---|---|---|
| D | Driven | L | Low |
| E | Edge | P | Period |
| F | Fall | R | Rise |
| H | High | V | Valid |
| I | Invalid (Hi-impedance) | Z | Hi-impedance |


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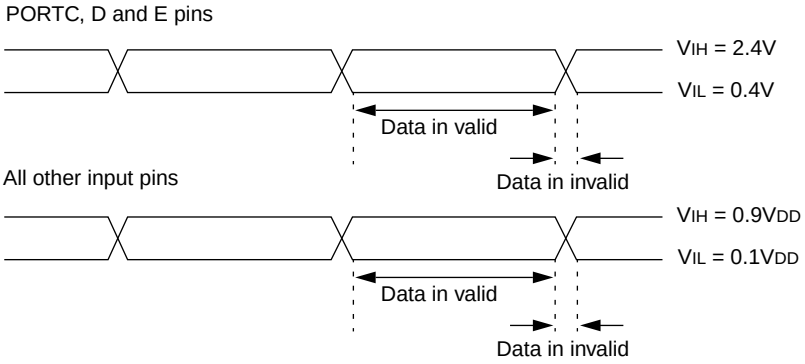
| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

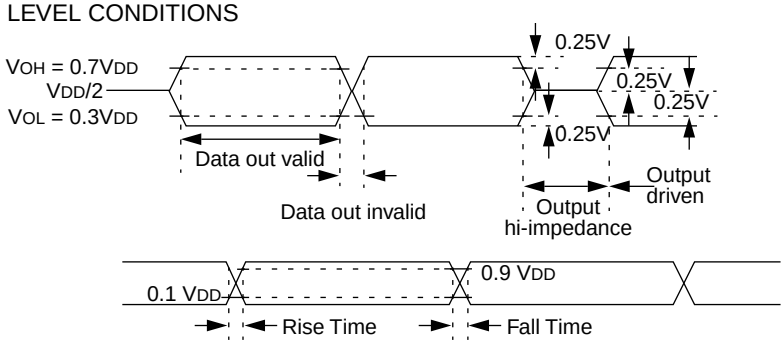
FIGURE 19-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the Þgures below.

INPUT LEVEL CONDITIONS

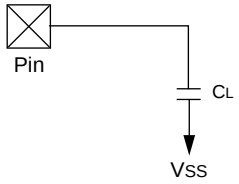



OUTPUT LEVEL CONDITIONS




LOAD CONDITIONS

Load Condition 1




50 pF £ CL

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 19.5 Timing Dia grams and SpeciÞ cations

FIGURE 19-2: EXTERNAL CLOCK TIMING

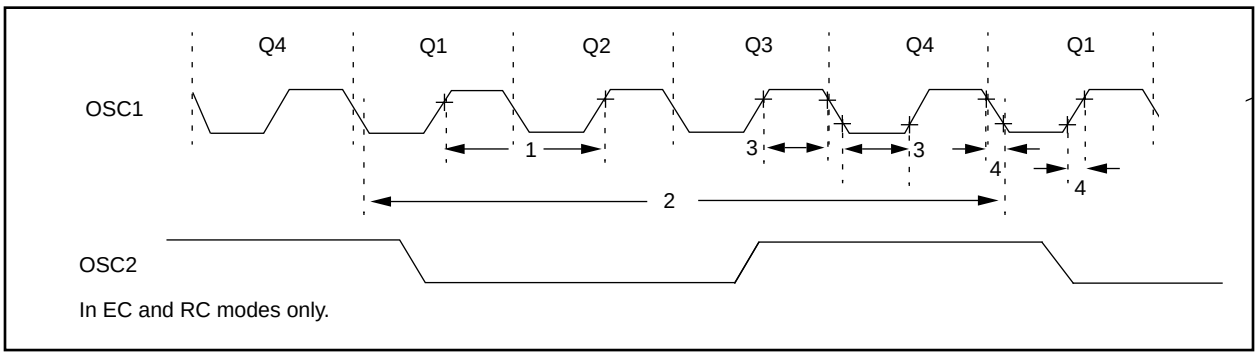



TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS

| Param No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Fosc | External CLKIN Frequency (Note 1) | DC | Ñ | 8 | MHz | EC osc mode - 08 devices (8 MHz devices) |
| | | | DC | Ñ | 16 | MHz | - 16 devices (16 MHz devices) |
| | | | DC | Ñ | 25 | MHz | - 25 devices (25 MHz devices) |
| | | | DC | Ñ | 33 | MHz | - 33 devices (33 MHz devices) |
| | | Oscillator Frequency (Note 1) | DC | Ñ | 4 | MHz | RC osc mode |
| | | | 1 | Ñ | 8 | MHz | XT osc mode - 08 devices (8 MHz devices) |
| | | | 1 | Ñ | 16 | MHz | - 16 devices (16 MHz devices) |
| | | | 1 | Ñ | 25 | MHz | - 25 devices (25 MHz devices) |
| | | | 1 | Ñ | 33 | MHz | - 33 devices (33 MHz devices) |
| | | | DC | Ñ | 2 | MHz | LF osc mode |
| 1 | Tosc | External CLKIN Period (Note 1) | 125 | Ñ | Ñ | ns | EC osc mode - 08 devices (8 MHz devices) |
| | | | 62.5 | Ñ | Ñ | ns | - 16 devices (16 MHz devices) |
| | | | 40 | Ñ | Ñ | ns | - 25 devices (25 MHz devices) |
| | | | 30.3 | Ñ | Ñ | ns | - 33 devices (33 MHz devices) |
| | | Oscillator Period (Note 1) | 250 | Ñ | Ñ | ns | RC osc mode |
| | | | 125 | Ñ | 1,000 | ns | XT osc mode - 08 devices (8 MHz devices) |
| | | | 62.5 | Ñ | 1,000 | ns | - 16 devices (16 MHz devices) |
| | | | 40 | Ñ | 1,000 | ns | - 25 devices (25 MHz devices) |
| | | | 30.3 | Ñ | 1,000 | ns | - 33 devices (33 MHz devices) |
| | | | 500 | Ñ | Ñ | ns | LF osc mode |
| 2 | TCY | Instruction Cycle Time (Note 1) | 121.2 | 4/Fosc | DC | ns | |
| 3 | TosL, TosH | Clock in (OSC1) high or low time | 10 à | Ñ | Ñ | ns | EC oscillator |
| 4 | TosR, TosF | Clock in (OSC1) rise or fall time | Ñ | Ñ | 5 à | ns | EC oscillator |

Data in ÒTypÓ column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

à These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All speciÞed values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these speciÞed limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at Òmin.Ó values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the Òmax.Ó cycle time limit is ÒDCÓ (no clock) for all devices.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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-3: CLKOUT AND I/O TIMING

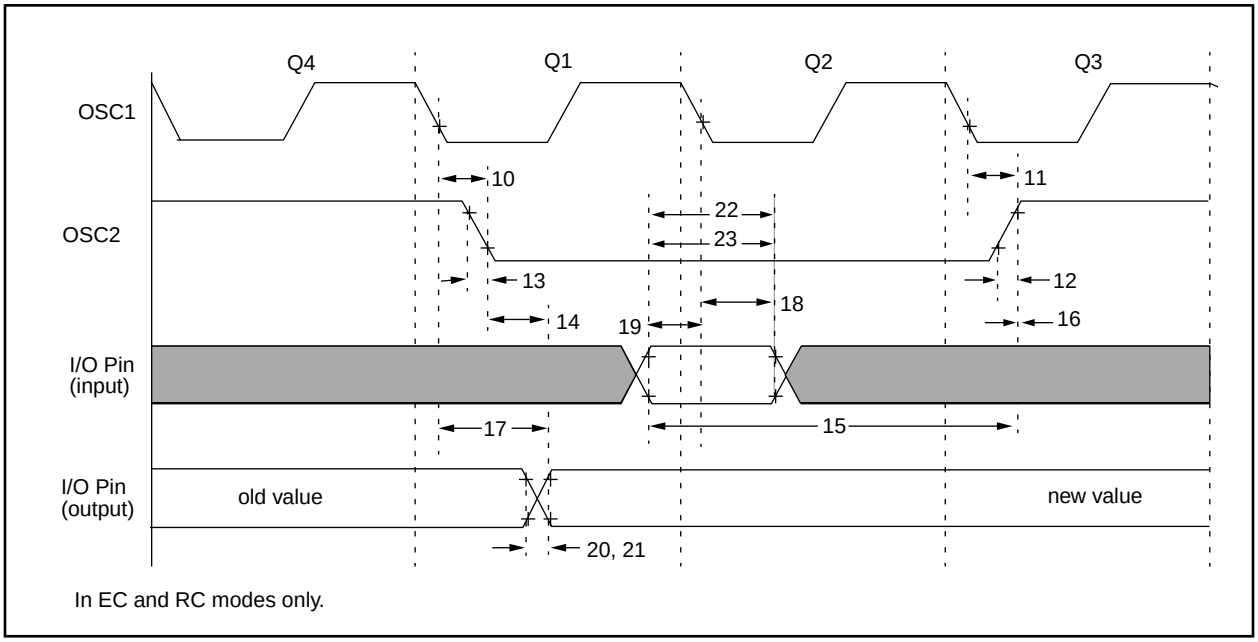


TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS

| Parameter No. | Sym | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10 | TosH2ckL | OSC1¯ to CLKOUT¯ | | Ñ | 15 à | 30 à | ns | Note 1 |
| 11 | TosH2ckH | OSC1¯ to CLKOUT- | | Ñ | 15 à | 30 à | ns | Note 1 |
| 12 | TckR | CLKOUT rise time | | Ñ | 5 à | 15 à | ns | Note 1 |
| 13 | TckF | CLKOUT fall time | | Ñ | 5 à | 15 à | ns | Note 1 |
| 14 | TckH2ioV | CLKOUT - to Port out valid | PIC17CR42/42A/43/ R43/44 | Ñ | Ñ | 0.5T CY + 20 à | ns | Note 1 |
| | | | PIC17LCR42/42A/43/ R43/44 | Ñ | Ñ | 0.5T CY + 50 à | ns | Note 1 |
| 15 | TioV2ckH | Port in valid before CLKOUT- | PIC17CR42/42A/43/ R43/44 | 0.25TCY + 25 à | Ñ | Ñ | ns | Note 1 |
| | | | PIC17LCR42/42A/43/ R43/44 | 0.25TCY + 50 à | Ñ | Ñ | ns | Note 1 |
| 16 | TckH2ioI | Port in hold after CLKOUT- | | 0 à | Ñ | Ñ | ns | Note 1 |
| 17 | TosH2ioV | OSC1¯ (Q1 cycle) to Port out valid | | Ñ | Ñ | 100 à | ns | |
| 18 | TosH2ioI | OSC1¯ (Q2 cycle) to Port input invalid (I/O in hold time) | | 0 à | Ñ | Ñ | ns | |
| 19 | TioV2osH | Port input valid to OSC1¯ (I/O in setup time) | | 30 à | Ñ | Ñ | ns | |
| 20 | TioR | Port output rise time | | Ñ | 10 à | 35 à | ns | |
| 21 | TioF | Port output fall time | | Ñ | 10 à | 35 à | ns | |
| 22 | TinHL | INT pin high or low time | | 25 * | Ñ | Ñ | ns | |
| 23 | TrbHL | RB7:RB0 change INT high or low time | | 25 * | Ñ | Ñ | ns | |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

à These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where CLKOUT output is 4 x TOSC.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

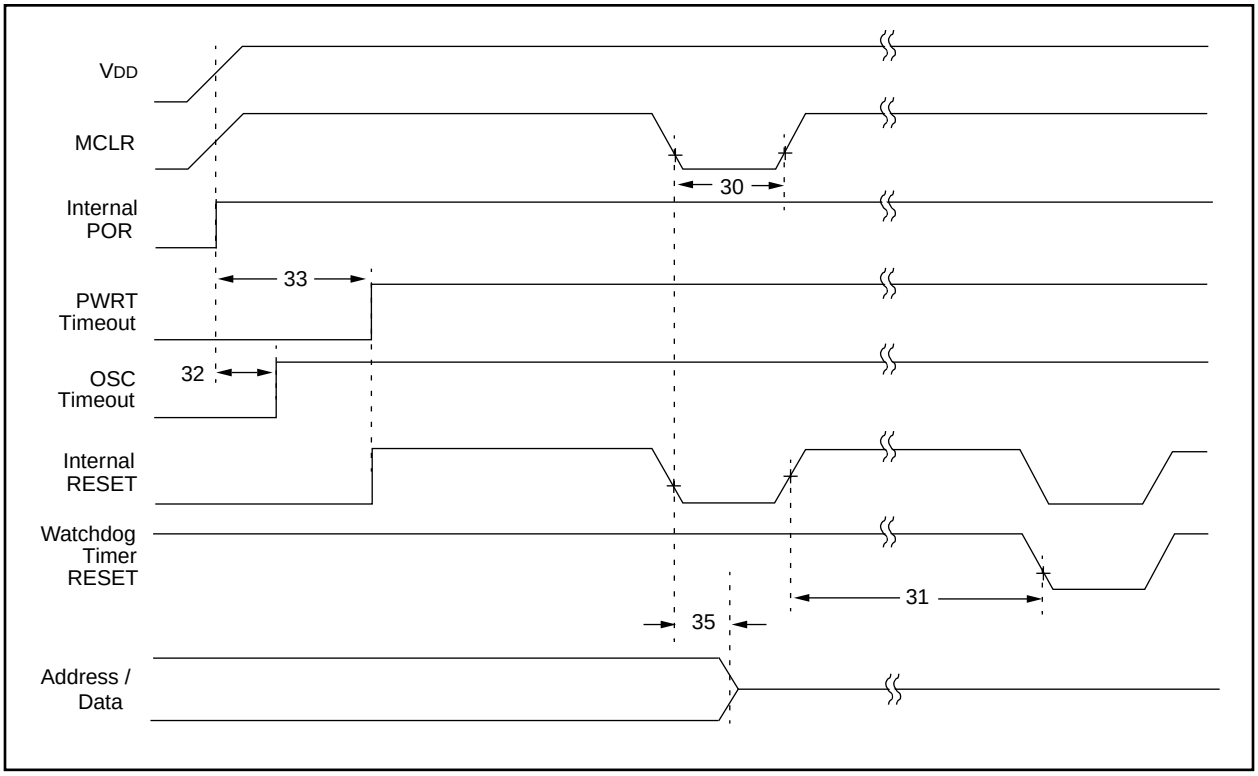


TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

| Parameter No. | Sym | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 30 | TmcL | $\overline{MCLR}$ Pulse Width (low) | | 100 * | Ñ | Ñ | ns | VDD = 5V |
| 31 | Twdt | Watchdog Timer Time-out Period (Prescale = 1) | | 5 * | 12 | 25 * | ms | VDD = 5V |
| 32 | Tost | Oscillation Start-up Timer Period | | Ñ | 1024T OSC¤ | Ñ | ms | T OSC = OSC1 period |
| 33 | Tpwrt | Power-up Timer Period | | 40 * | 96 | 200 * | ms | VDD = 5V |
| 35 | TmcL2adl | $\overline{MCLR}$ to System Interface bus (AD15:AD0>) invalid | PIC17CR42/42A/43/R43/44 | Ñ | Ñ | 100 * | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | Ñ | Ñ | 120 * | ns | |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

à These parameters are for design guidance only and are not tested, nor characterized.

¤ This speciÞcation ensured by design.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-5: TIMER0 CLOCK TIMINGS

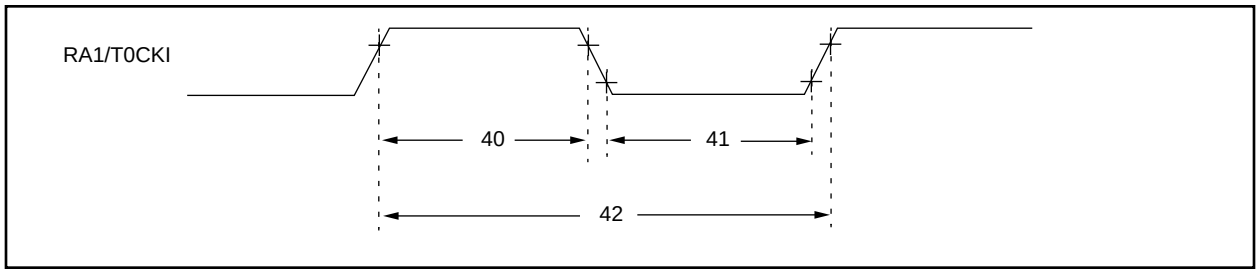


TABLE 19-5: TIMER0 CLOCK REQUIREMENTS

| Parameter No. | Sym | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | 0.5TCY + 20 ¤ | Ñ | Ñ | ns | |
| | | | With Prescaler | 10* | Ñ | Ñ | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | 0.5TCY + 20 ¤ | Ñ | Ñ | ns | |
| | | | With Prescaler | 10* | Ñ | Ñ | ns | |
| 42 | Tt0P | T0CKI Period | | Greater of: 20 ns or Tcy + 40 ¤ / N | Ñ | Ñ | ns | N = prescale value (1, 2, 4, ..., 256) |

* These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

¤ This speciÞcation ensured by design.

FIGURE 19-6: TIMER1, TIMER2, AND TIMER3 CLOCK TIMINGS

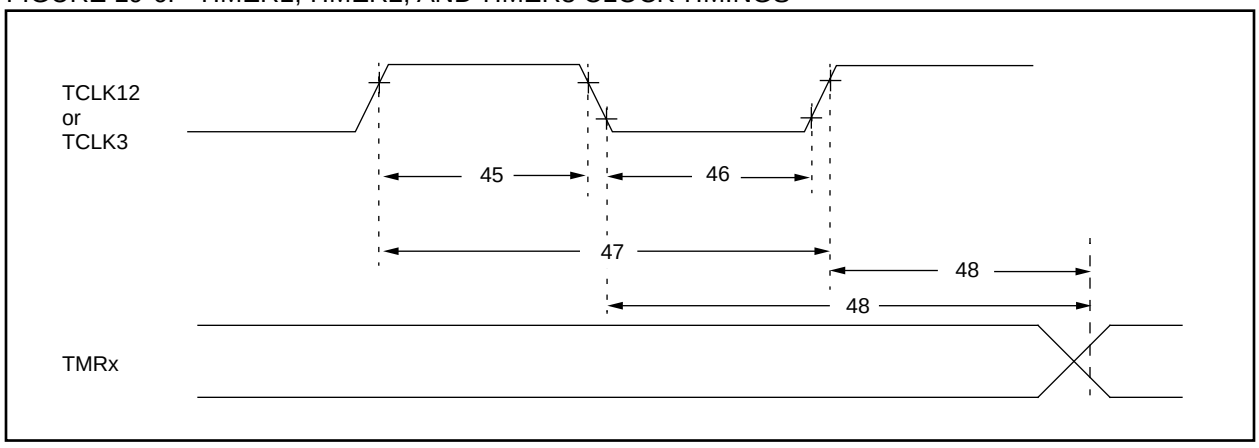


TABLE 19-6: TIMER1, TIMER2, AND TIMER3 CLOCK REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 45 | Tt123H | TCLK12 and TCLK3 high time | 0.5TCY + 20 ¤ | Ñ | Ñ | ns | |
| 46 | Tt123L | TCLK12 and TCLK3 low time | 0.5TCY + 20 ¤ | Ñ | Ñ | ns | |
| 47 | Tt123P | TCLK12 and TCLK3 input period | TCY + 40 ¤ / N | Ñ | Ñ | ns | N = prescale value (1, 2, 4, 8) |
| 48 | TckE2tmrI | Delay from selected External Clock Edge to Timer increment | 2TOSC ¤ | | 6Tosc ¤ | | |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ûC unless otherwise stated. These parameters are for design guidance only and are not tested.

¤ This speciÞcation ensured by design.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-7: CAPTURE TIMINGS

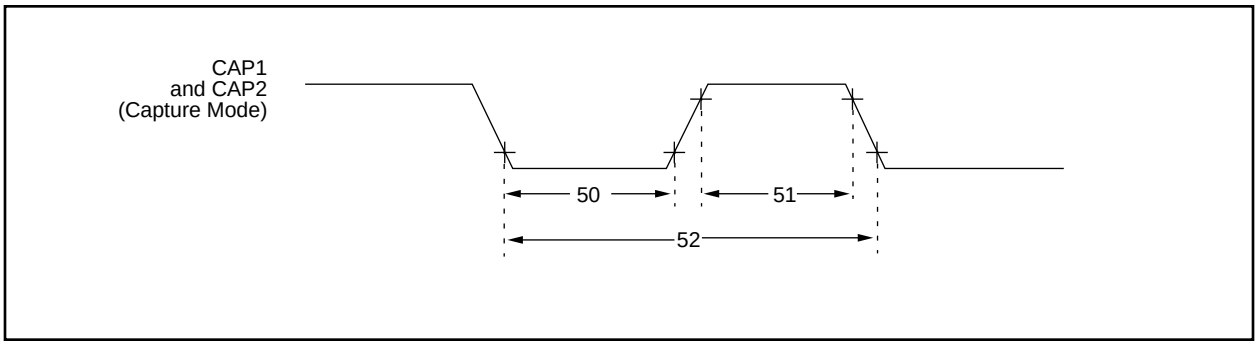


TABLE 19-7: CAPTURE REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 50 | TccL | Capture1 and Capture2 input low time | 10 * | Ñ | Ñ | ns | |
| 51 | TccH | Capture1 and Capture2 input high time | 10 * | Ñ | Ñ | ns | |
| 52 | TccP | Capture1 and Capture2 input period | $\frac{2T_{CY}}{N}$ ¤ | Ñ | Ñ | ns | N = prescale value (4 or 16) |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

¤ This speciÞcation ensured by design.

FIGURE 19-8: PWM TIMINGS

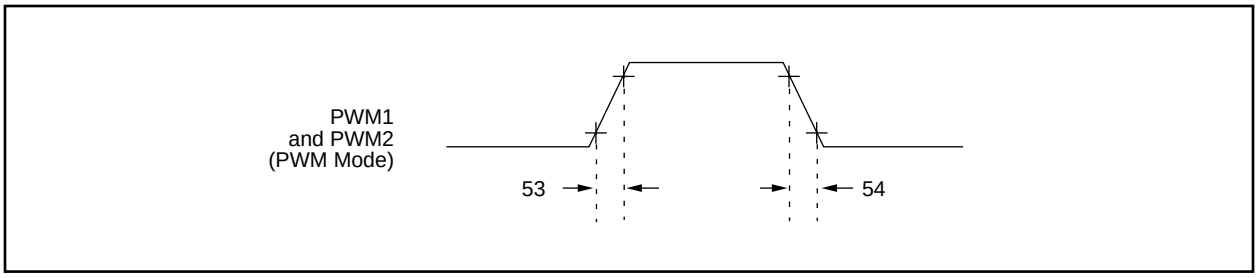


TABLE 19-8: PWM REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 53 | TccR | PWM1 and PWM2 output rise time | Ñ | 10 * | 35 *¤ | ns | |
| 54 | TccF | PWM1 and PWM2 output fall time | Ñ | 10 * | 35 *¤ | ns | |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

¤ This speciÞcation ensured by design.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-9: USART MODULE: SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

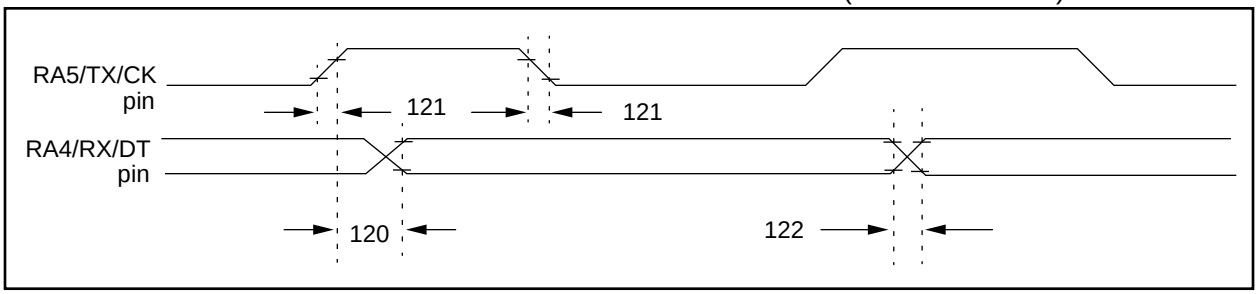


TABLE 19-9: SYNCHRONOUS TRANSMISSION REQUIREMENTS

| Param No. | Sym | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 120 | TckH2dtV | SYNC XMIT (MASTER & SLAVE) Clock high to data out valid | PIC17CR42/42A/43/R43/44 | Ñ | Ñ | 50 | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | Ñ | Ñ | 75 | ns | |
| 121 | TckRF | Clock out rise time and fall time (Master Mode) | PIC17CR42/42A/43/R43/44 | Ñ | Ñ | 25 | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | Ñ | Ñ | 40 | ns | |
| 122 | TdtRF | Data out rise time and fall time | PIC17CR42/42A/43/R43/44 | Ñ | Ñ | 25 | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | Ñ | Ñ | 40 | ns | |

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-10: USART MODULE: SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

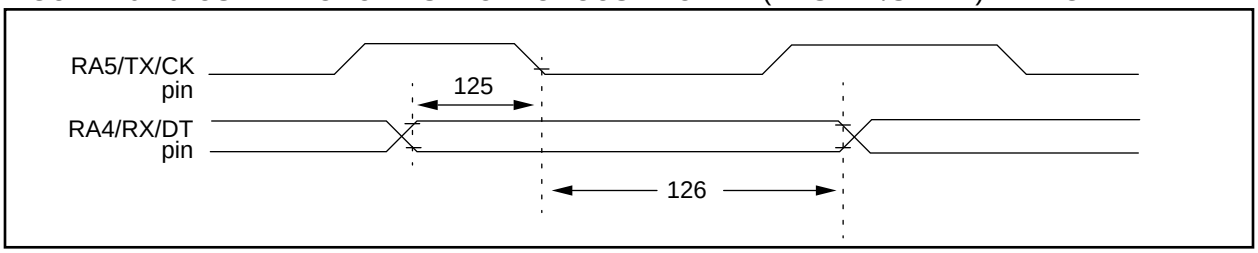


TABLE 19-10: SYNCHRONOUS RECEIVE REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 125 | TdtV2ckL | SYNC RCV (MASTER & SLAVE) Data hold before CK¯ (DT hold time) | 15 | Ñ | Ñ | ns | |
| 126 | TckL2dtl | Data hold after CK¯ (DT hold time) | 15 | Ñ | Ñ | ns | |

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-11: MEMORY INTERFACE WRITE TIMING (NOT SUPPORTED IN PIC17LC4X DEVICES)

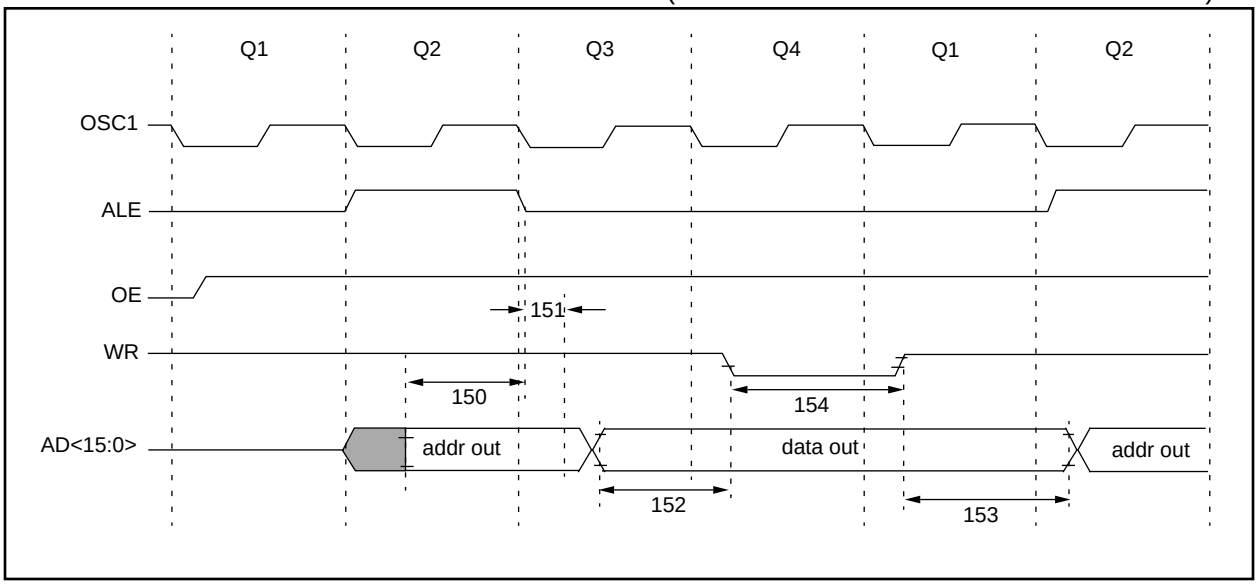


TABLE 19-11: MEMORY INTERFACE WRITE REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 150 | TadV2alL | AD<15:0> (address) valid to ALE¯ (address setup time) | 0.25Tcy - 10 | Ñ | Ñ | ns | |
| 151 | TalL2adI | ALE¯ to address out invalid (address hold time) | 0 | Ñ | Ñ | ns | |
| 152 | TadV2wrL | Data out valid to $\overline{WR}$¯ (data setup time) | 0.25Tcy - 40 | Ñ | Ñ | ns | |
| 153 | TwrH2adI | $\overline{WR}$- to data out invalid (data hold time) | Ñ | 0.25T CY ¤ | Ñ | ns | |
| 154 | TwrL | $\overline{WR}$ pulse width | Ñ | 0.25T CY ¤ | Ñ | ns | |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

¤ This speciÞcation ensured by design.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 19-12: MEMORY INTERFACE READ TIMING (NOT SUPPORTED IN PIC17LC4X DEVICES)

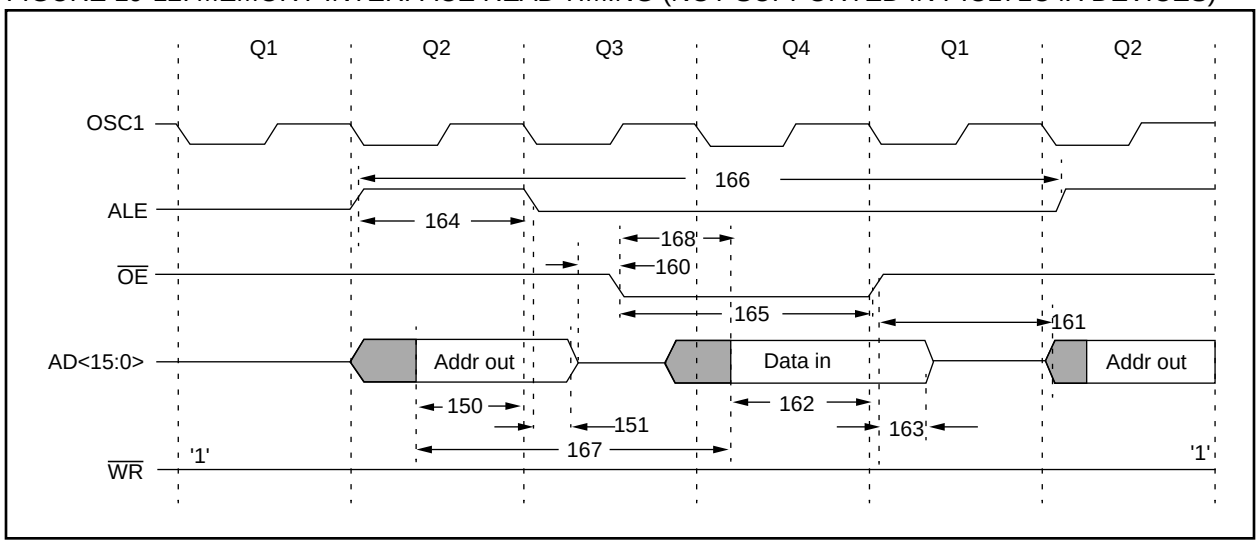


TABLE 19-12: MEMORY INTERFACE READ REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 150 | TadV2alL | AD15:AD0 (address) valid to ALE¯ (address setup time) | 0.25Tcy - 10 | Ñ | Ñ | ns | |
| 151 | TalL2adI | ALE¯ to address out invalid (address hold time) | 5* | Ñ | Ñ | ns | |
| 160 | TadZ2oeL | AD15:AD0 hi-impedance to OE¯ | 0* | Ñ | Ñ | ns | |
| 161 | ToeH2adD | OE- to AD15:AD0 driven | 0.25Tcy - 15 | Ñ | Ñ | ns | |
| 162 | TadV2oeH | Data in valid before OE- (data setup time) | 35 | Ñ | Ñ | ns | |
| 163 | ToeH2adI | OE- to data in invalid (data hold time) | 0 | Ñ | Ñ | ns | |
| 164 | TalH | ALE pulse width | Ñ | 0.25T CY ¤ | Ñ | ns | |
| 165 | ToeL | OE pulse width | 0.5Tcy - 35 ¤ | Ñ | Ñ | ns | |
| 166 | TalH2alH | ALE- to ALE- (cycle time) | Ñ | T CY ¤ | Ñ | ns | |
| 167 | Tacc | Address access time | Ñ | Ñ | 0.75T CY - 30 | ns | |
| 168 | Toe | Output enable access time (OE low to Data Valid) | Ñ | Ñ | 0.5T CY - 45 | ns | |

* These parameters are characterized but not tested.

Data in ÒTypÓ column is at 5V, 25ºC unless otherwise stated. These parameters are for design guidance only and are not tested.

¤ This speciÞcation ensured by design.

NOTES:


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 20.0 PIC17CR42/42A/43/R43/44 DC AND AC CHARACTERISTICS

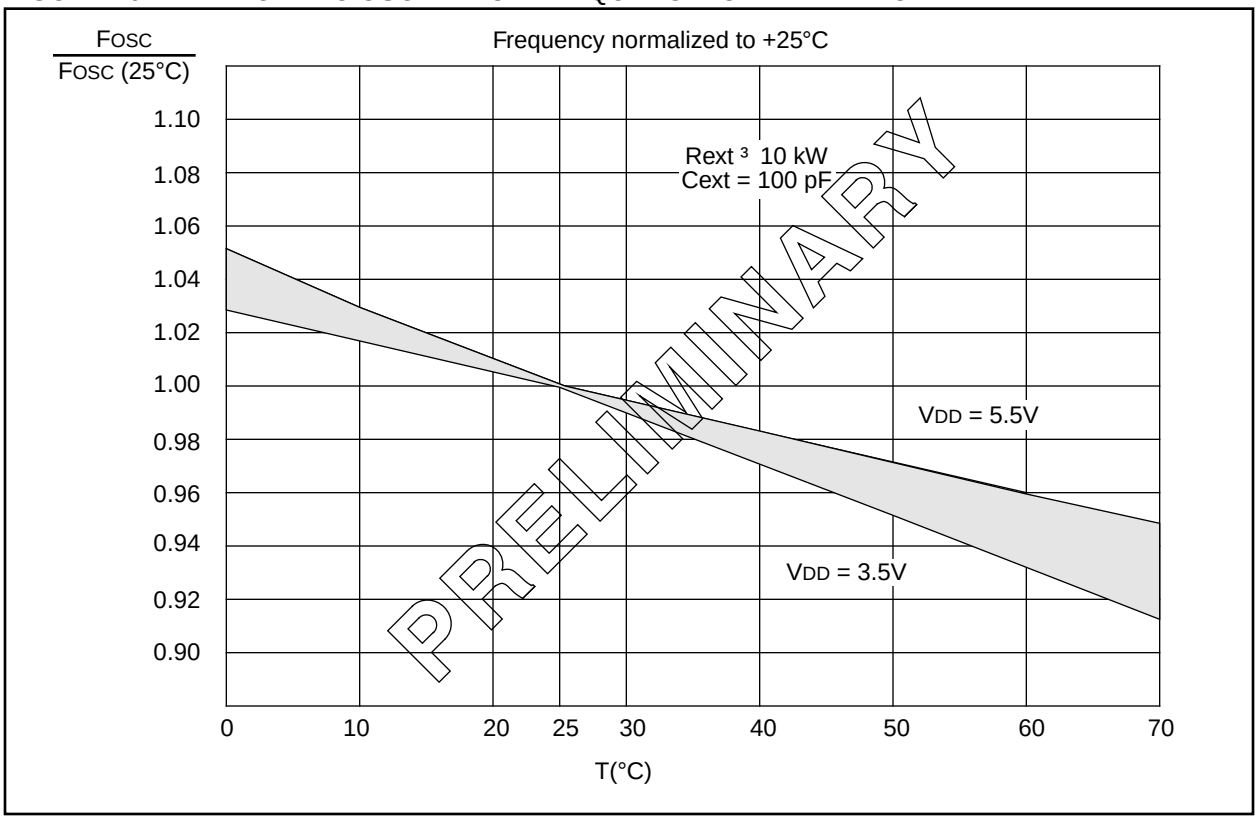
The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3s) and (mean - 3s) respectively where s is standard deviation.

TABLE 20-1: PIN CAPACITANCE PER PACKAGE TYPE

| Pin Name | Typical Capacitance (pF) | | | |
|---|---|---|---|---|
| | 40-pin DIP | 44-pin PLCC | 44-pin MQFP | 44-pin TQFP |
| All pins, except $\overline{MCLR}$, VDD, and VSS | 10 | 10 | 10 | 10 |
| $\overline{MCLR}$ pin | 20 | 20 | 20 | 20 |

FIGURE 20-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE






This document was created with FrameMaker 4.0.4

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-2: TYPICAL RC OSCILLATOR FREQUENCY vs. $V_{DD}$

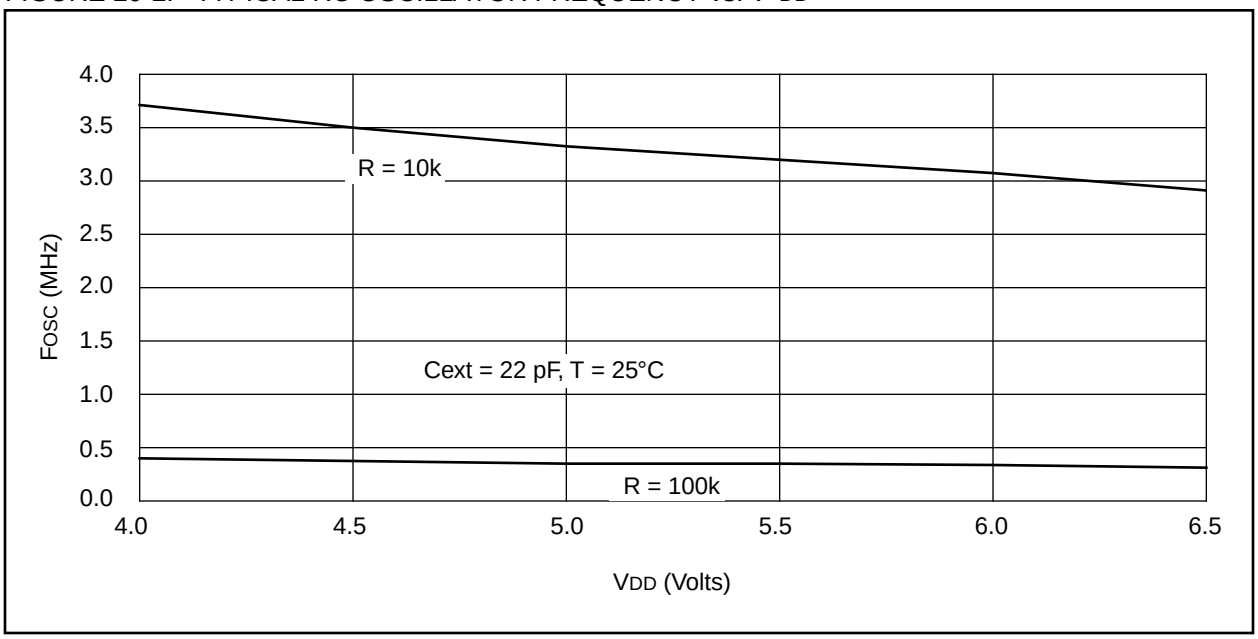
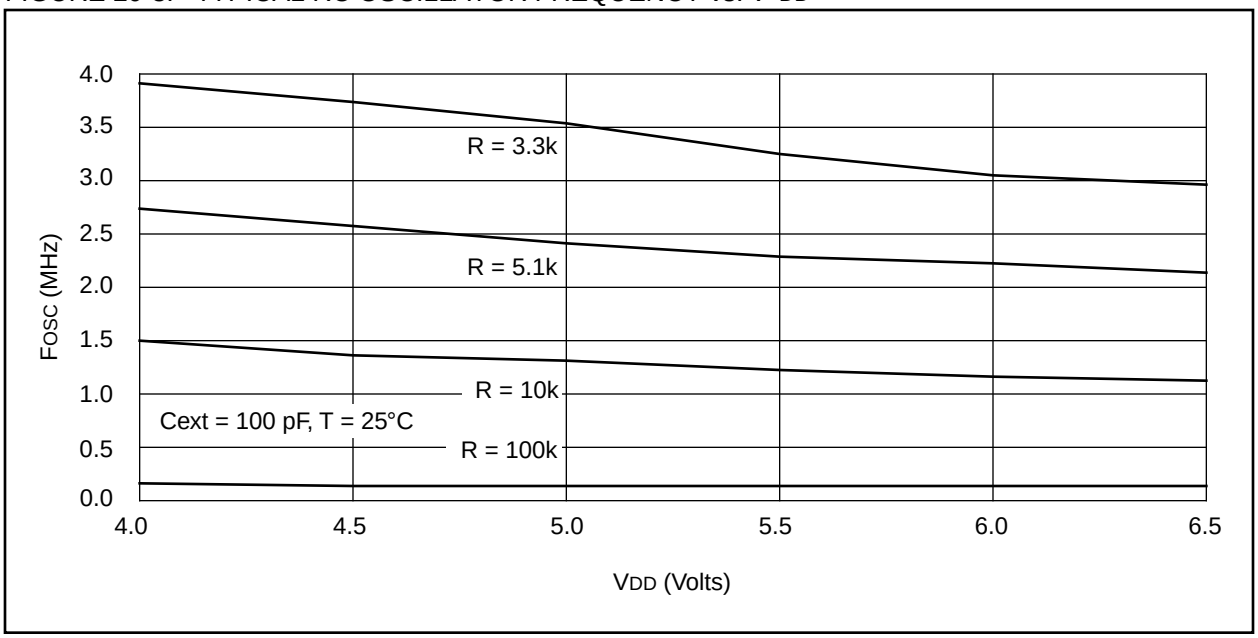



FIGURE 20-3: TYPICAL RC OSCILLATOR FREQUENCY vs. $V_{DD}$





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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-4: TYPICAL RC OSCILLATOR FREQUENCY vs. $V_{DD}$

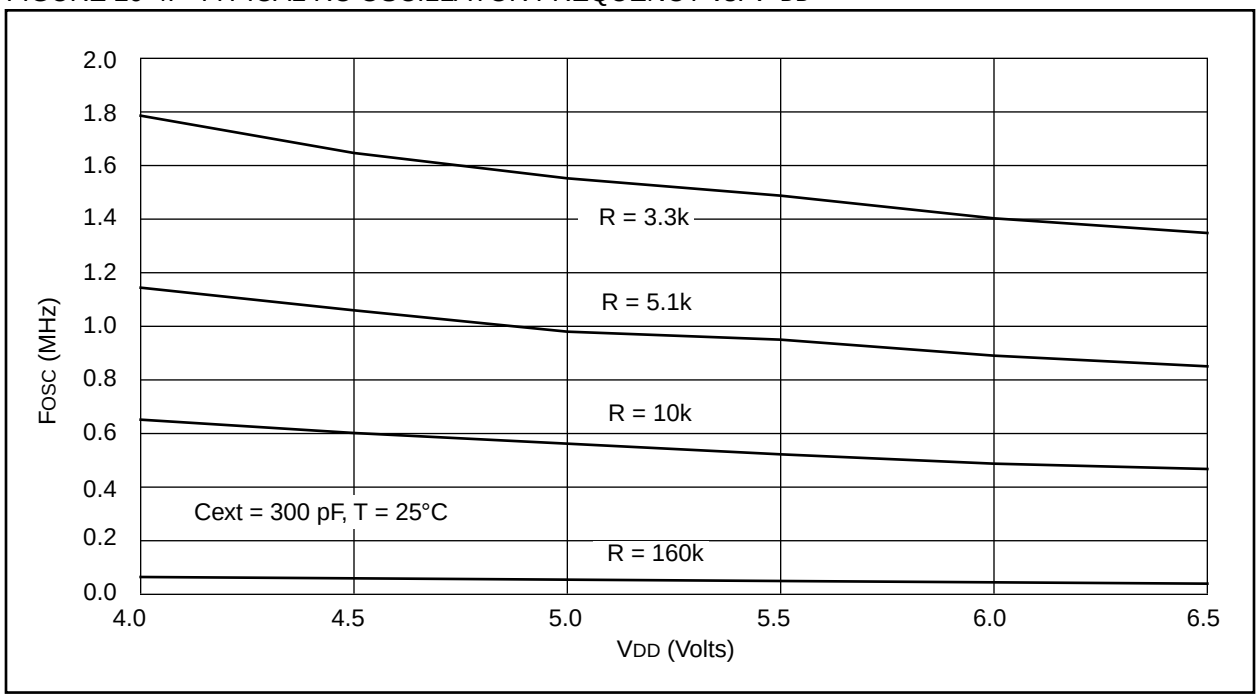



TABLE 20-2: RC OSCILLATOR FREQUENCIES

| Cext | Rext | Average Fosc @ 5V, 25°C | |
|---|---|---|---|
| 22 pF | 10k | 3.33 MHz | ± 12% |
| | 100k | 353 kHz | ± 13% |
| 100 pF | 3.3k | 3.54 MHz | ± 10% |
| | 5.1k | 2.43 MHz | ± 14% |
| | 10k | 1.30 MHz | ± 17% |
| | 100k | 129 kHz | ± 10% |
| 300 pF | 3.3k | 1.54 MHz | ± 14% |
| | 5.1k | 980 kHz | ± 12% |
| | 10k | 564 kHz | ± 16% |
| | 160k | 35 kHz | ± 18% |

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-5: TRANSCONDUCTANCE (gm) OF LF OSCILLATOR vs. $V_{DD}$

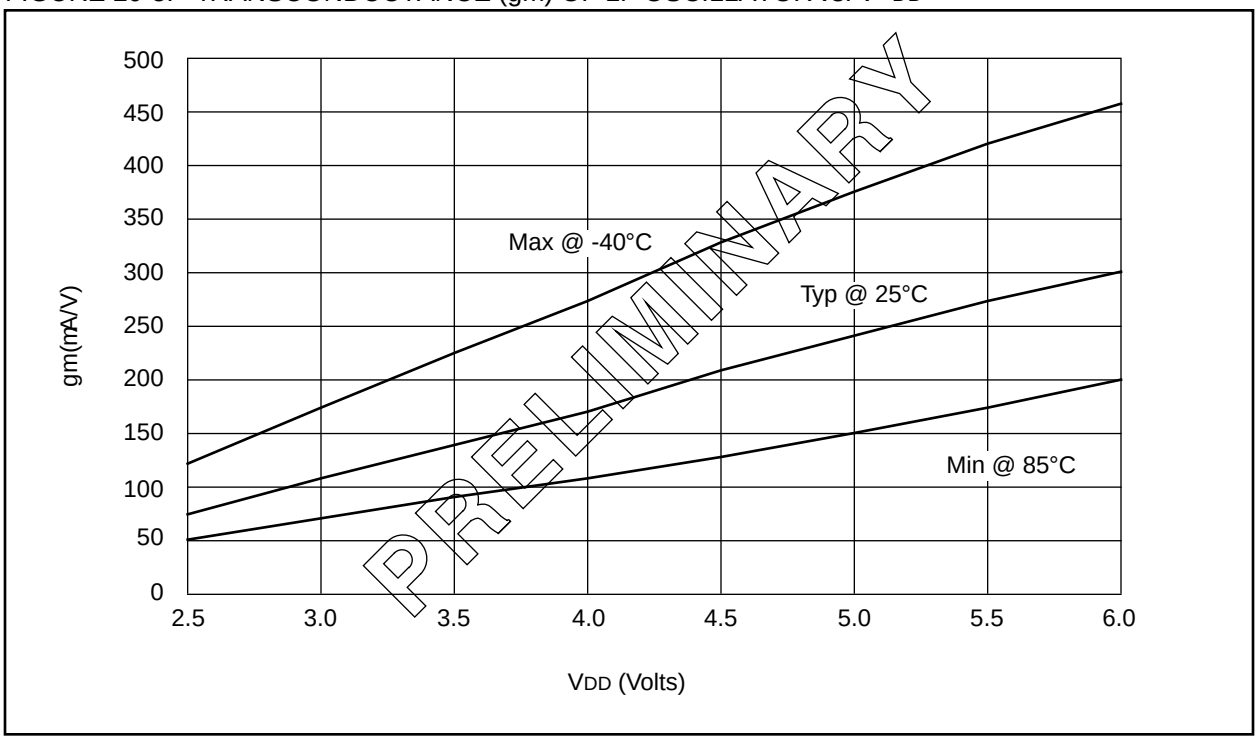
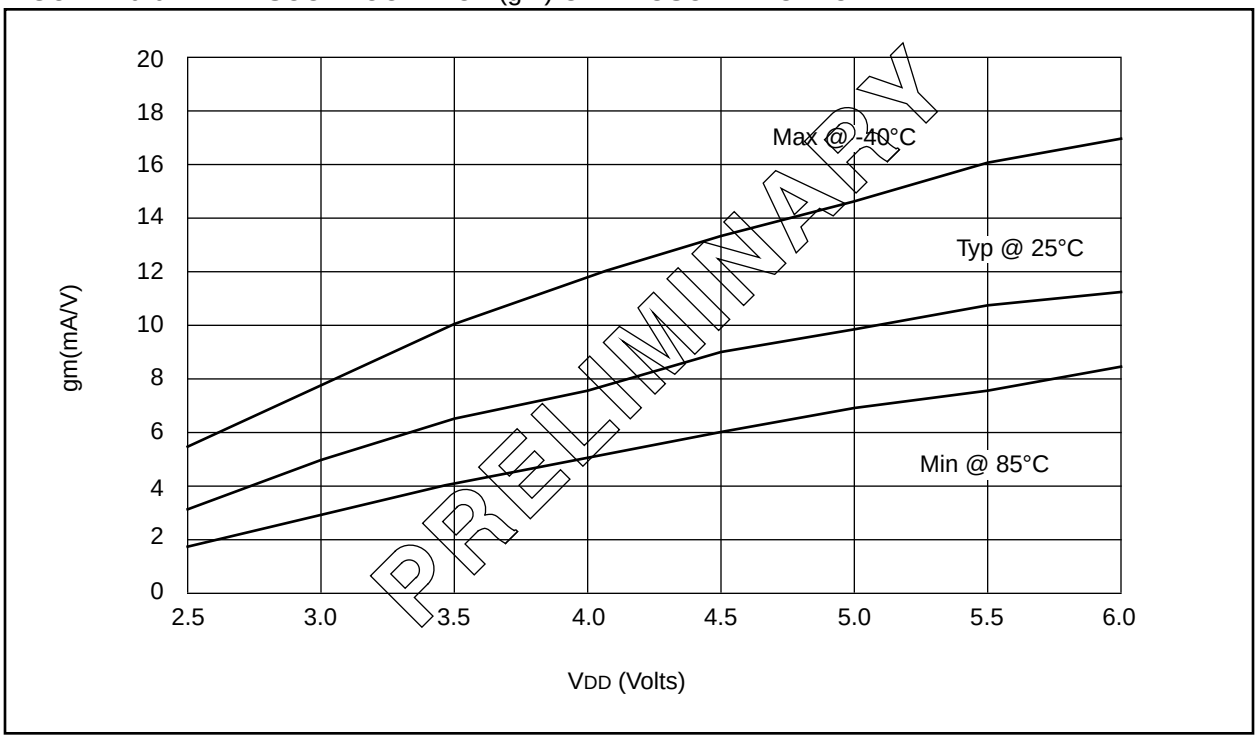



FIGURE 20-6: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. $V_{DD}$





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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-7: TYPICAL $I_{DD}$ vs. FREQUENCY (EXTERNAL CLOCK 25 °C)

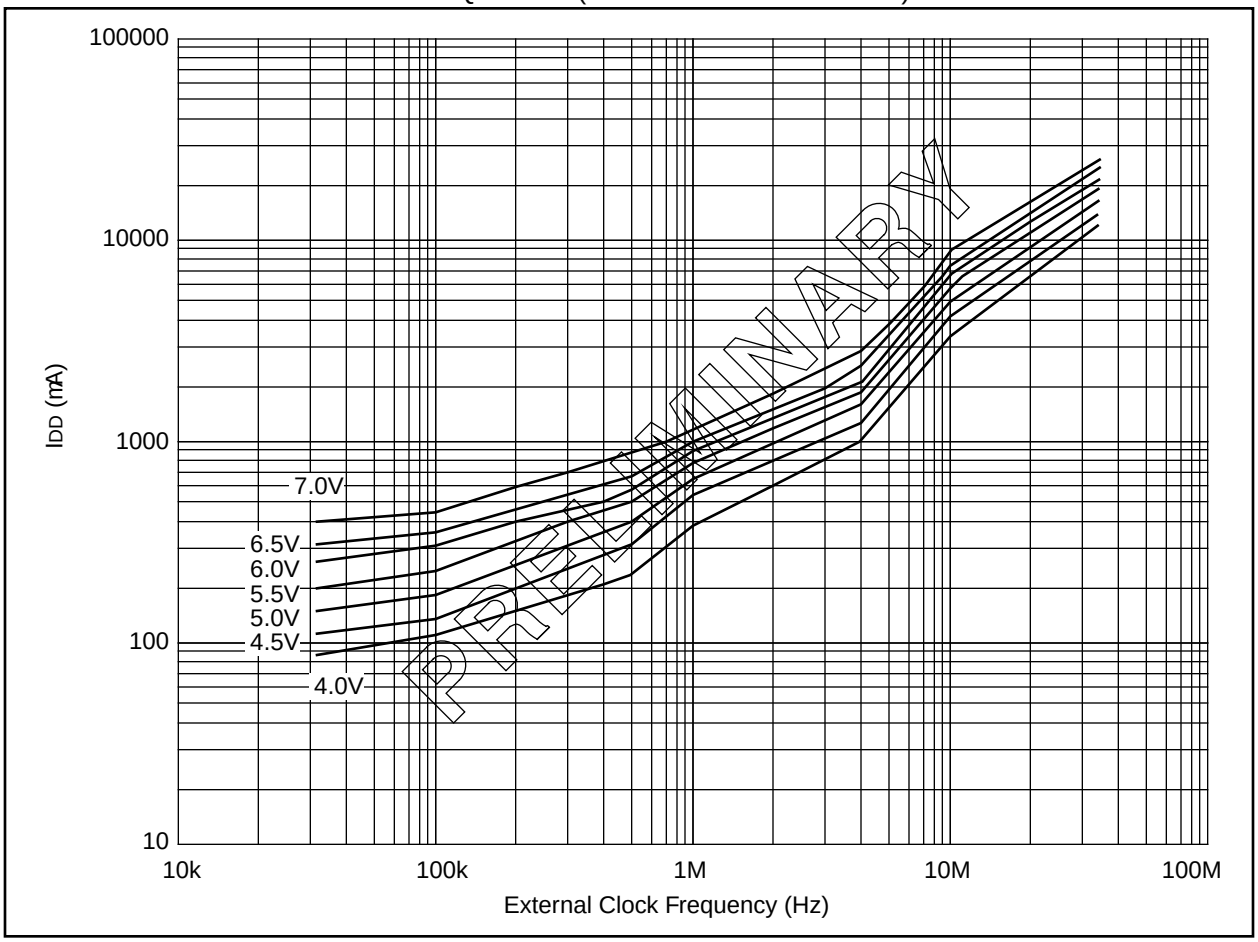
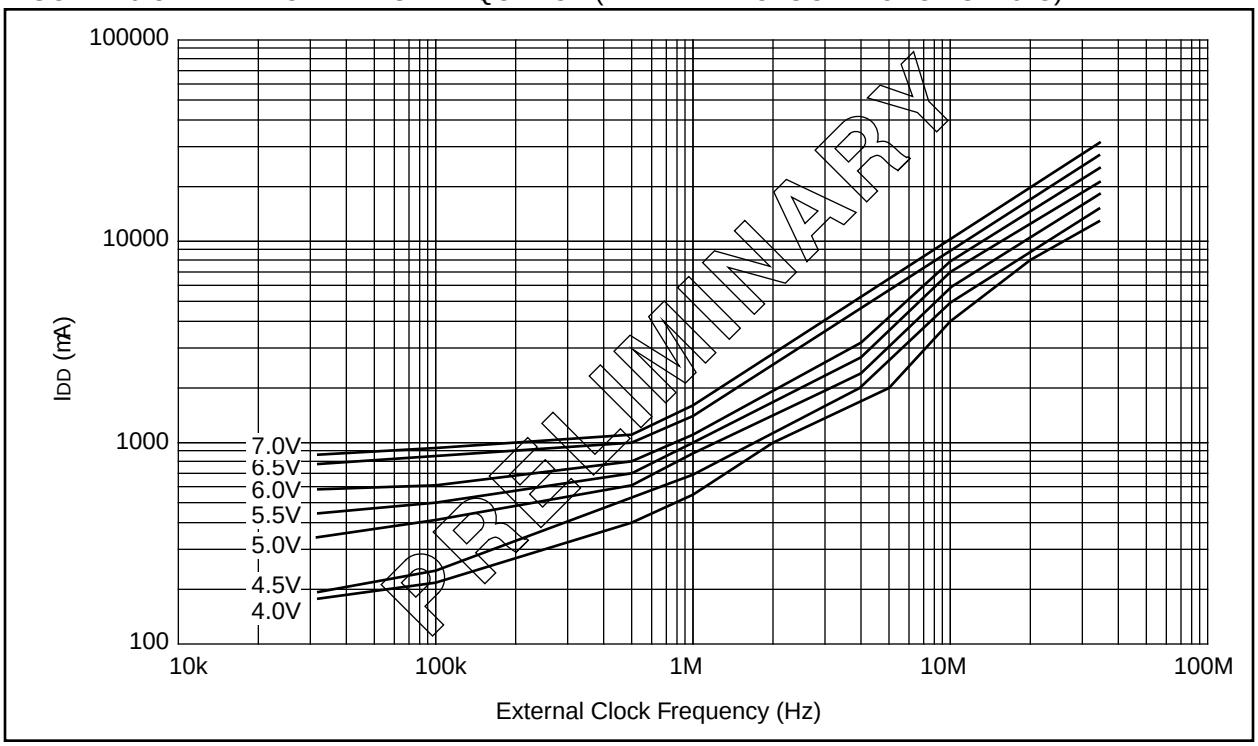



FIGURE 20-8: MAXIMUM $I_{DD}$ vs. FREQUENCY (EXTERNAL CLOCK 125 °C TO -40°C)



| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-9: TYPICAL $I_{PD}$ vs. $V_{DD}$ WATCHDOG DISABLED 25 °C

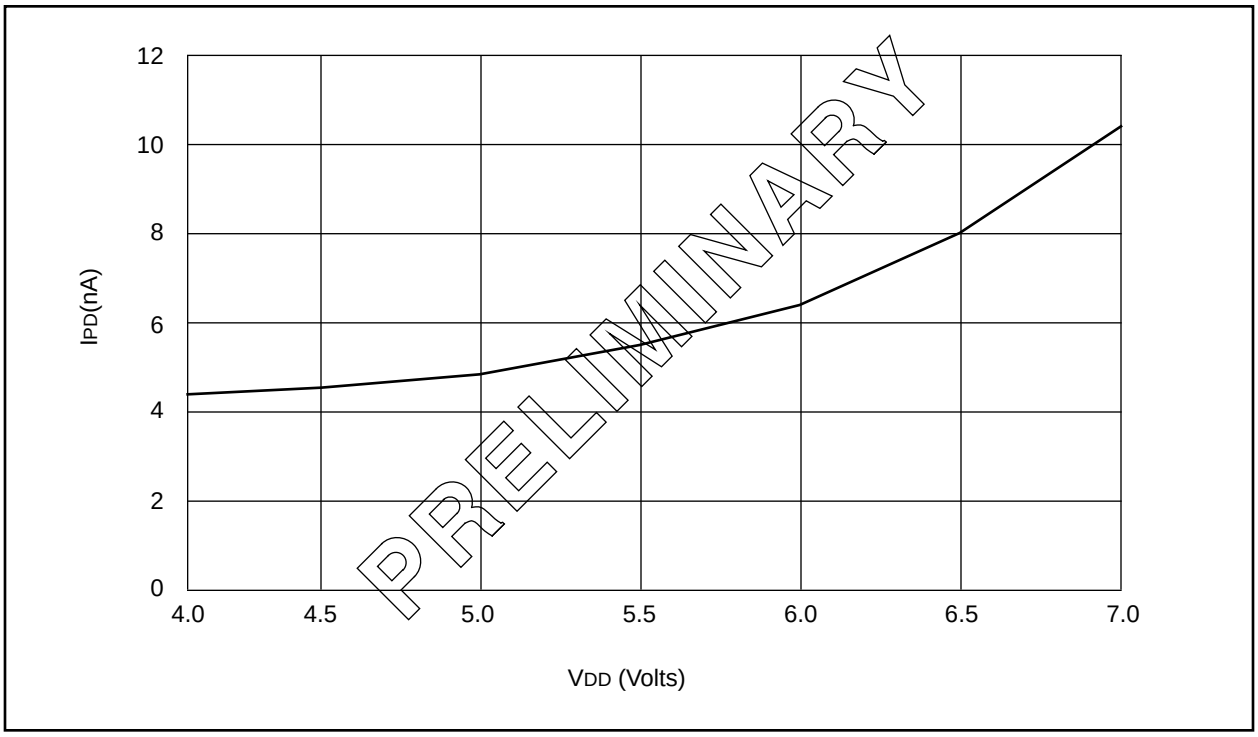
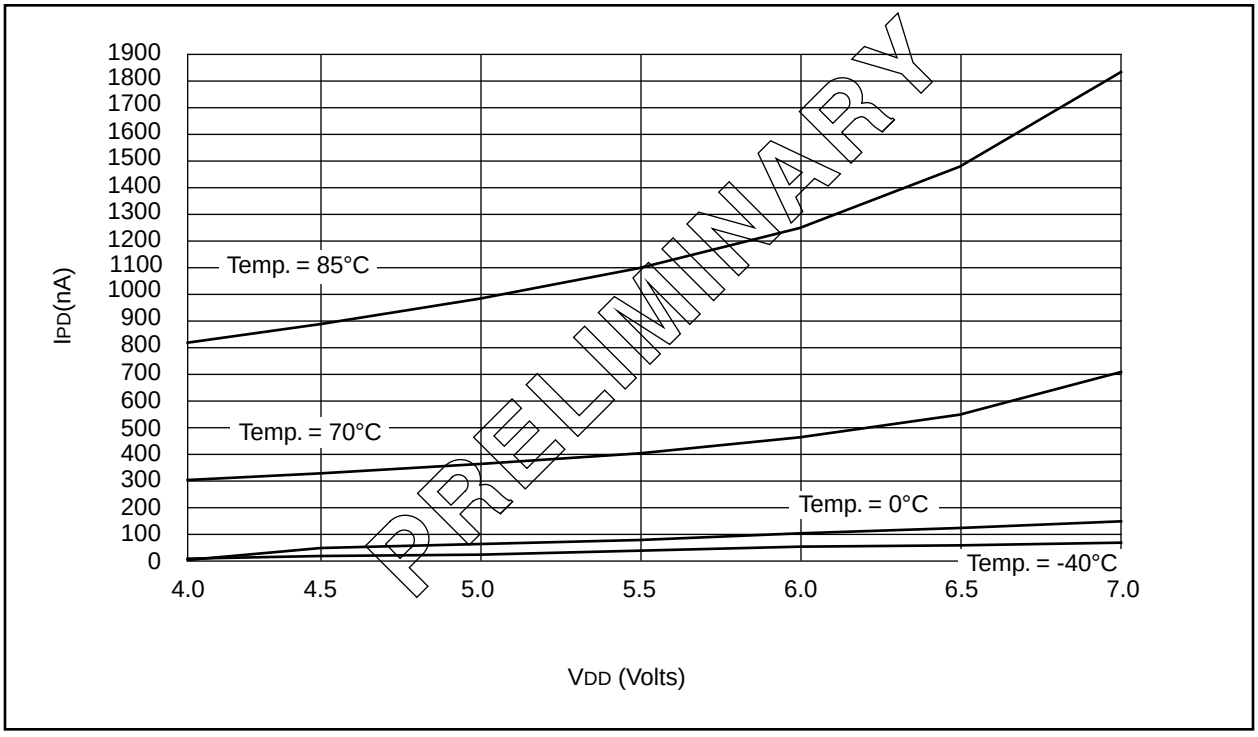



FIGURE 20-10: MAXIMUM $I_{PD}$ vs. $V_{DD}$ WATCHDOG DISABLED





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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-11: TYPICAL $I_{PD}$ vs. $V_{DD}$ WATCHDOG ENABLED 25 °C

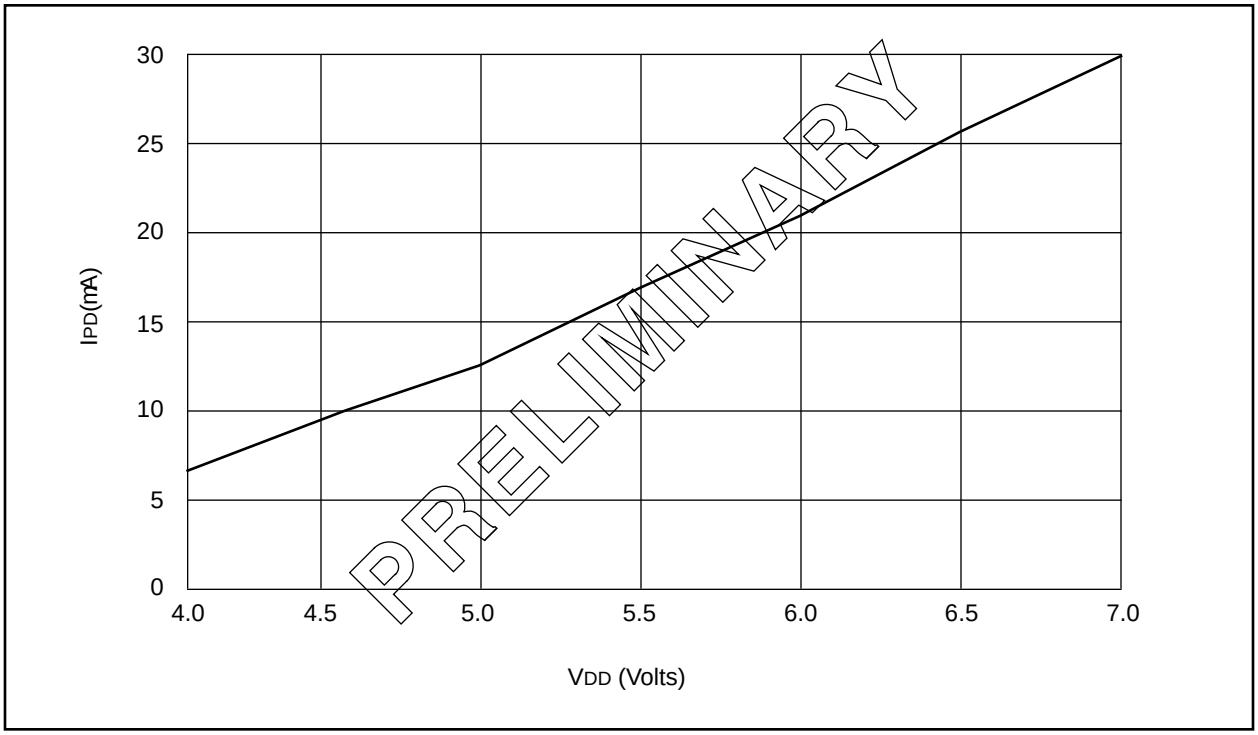
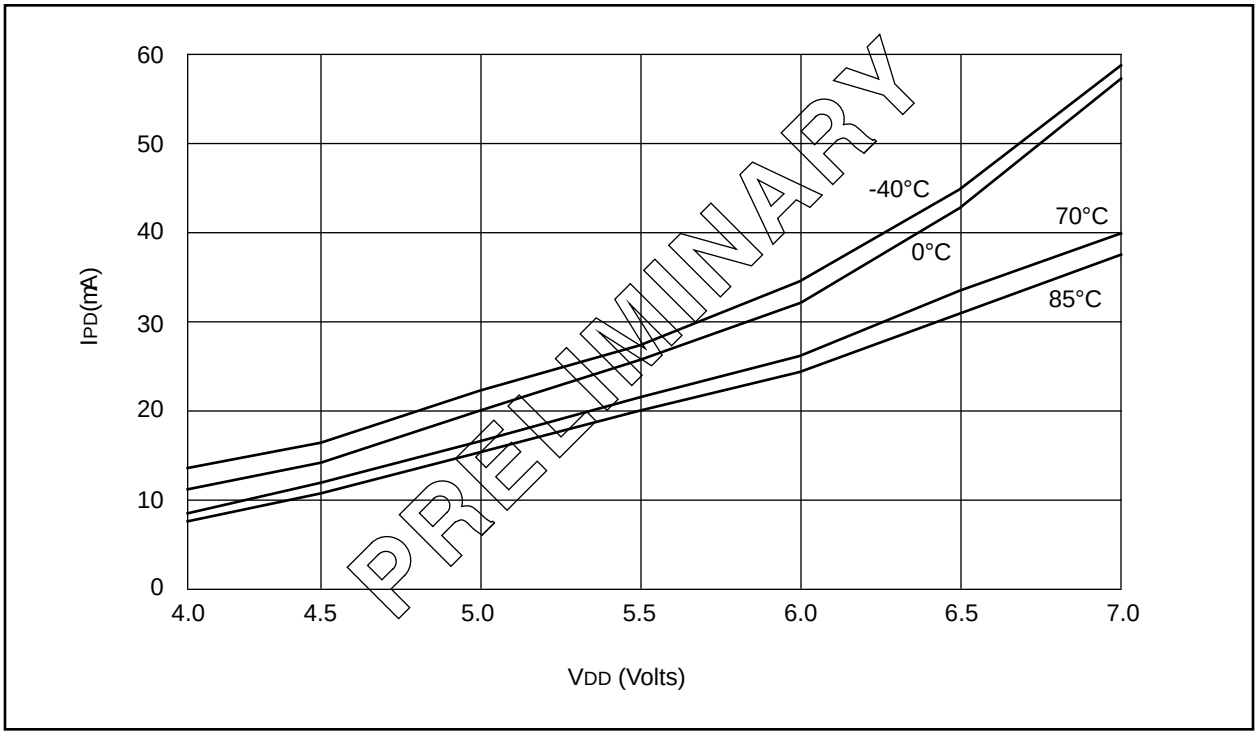



FIGURE 20-12: MAXIMUM $I_{PD}$ vs. $V_{DD}$ WATCHDOG ENABLED



| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-13: WDT TIMER TIME-OUT PERIOD vs. $V_{DD}$

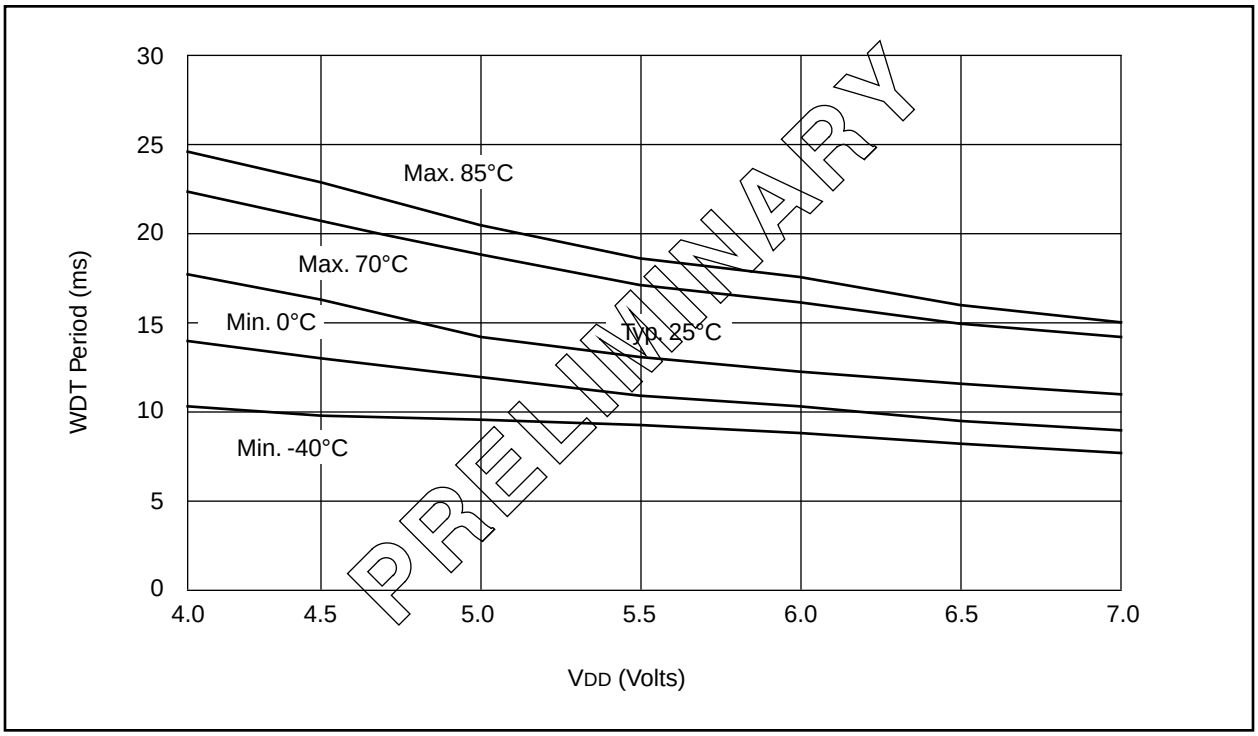
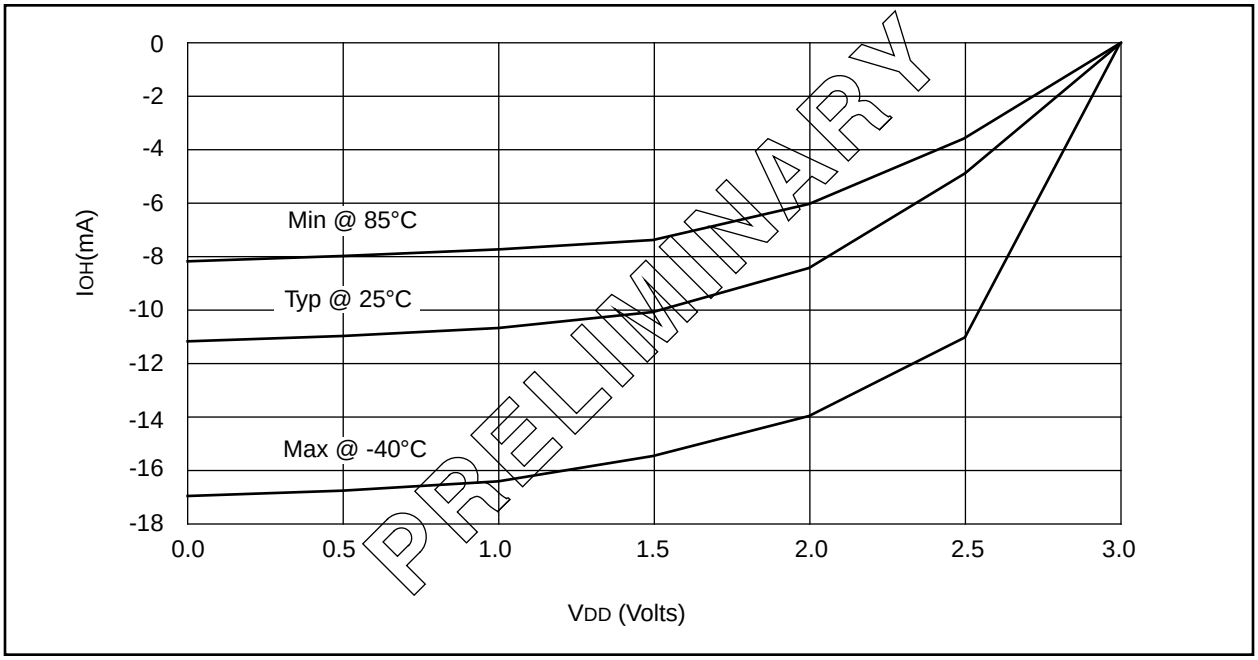



FIGURE 20-14: $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 3V





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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-15: $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 5V

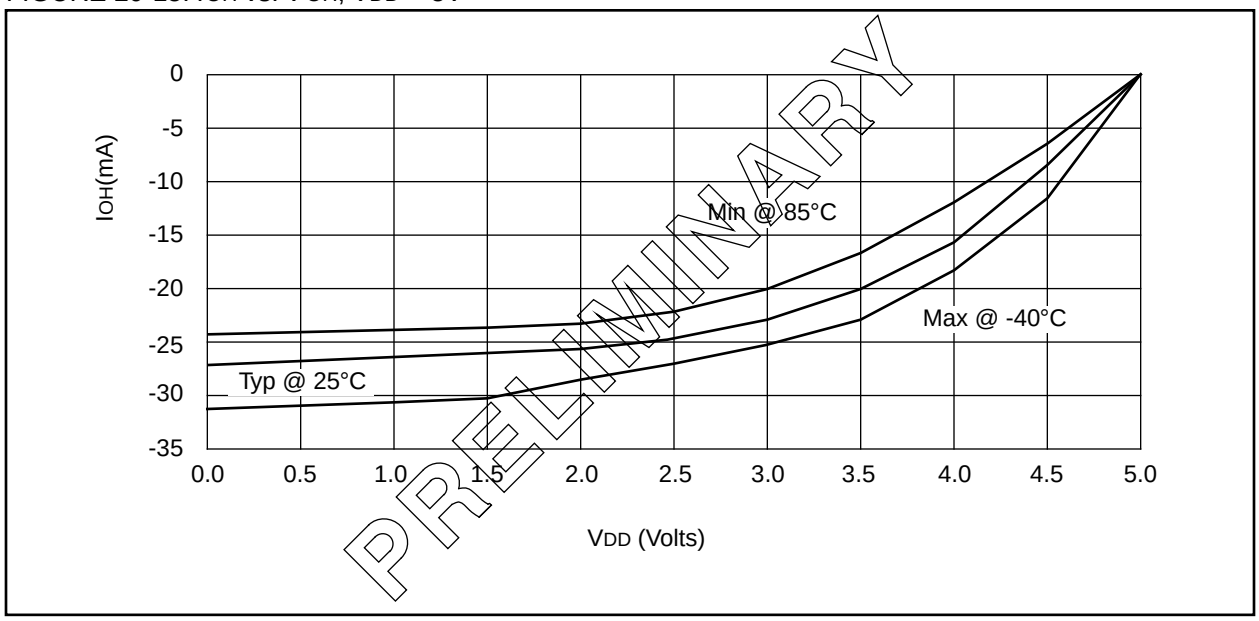
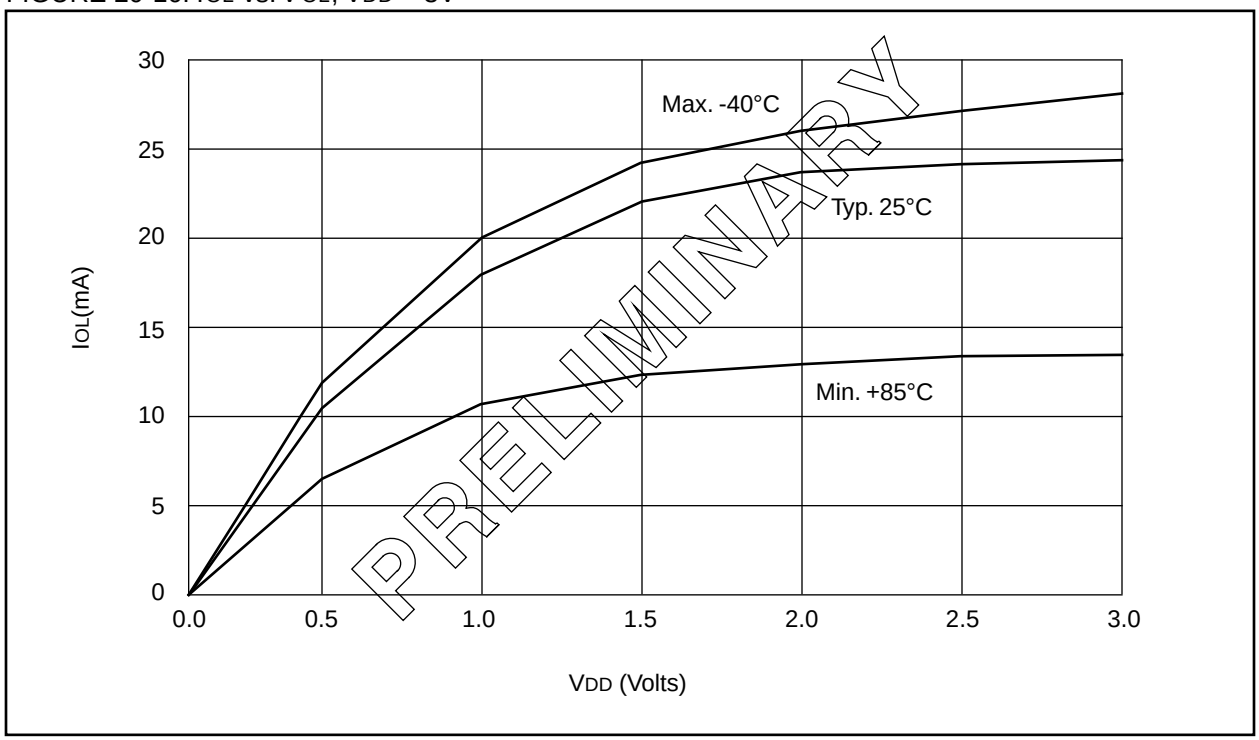



FIGURE 20-16: $I_{OL}$ vs. $V_{OL}$, $V_{DD}$ = 3V



| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-17: $I_{OL}$ vs. $V_{OL}$, $V_{DD}$ = 5V

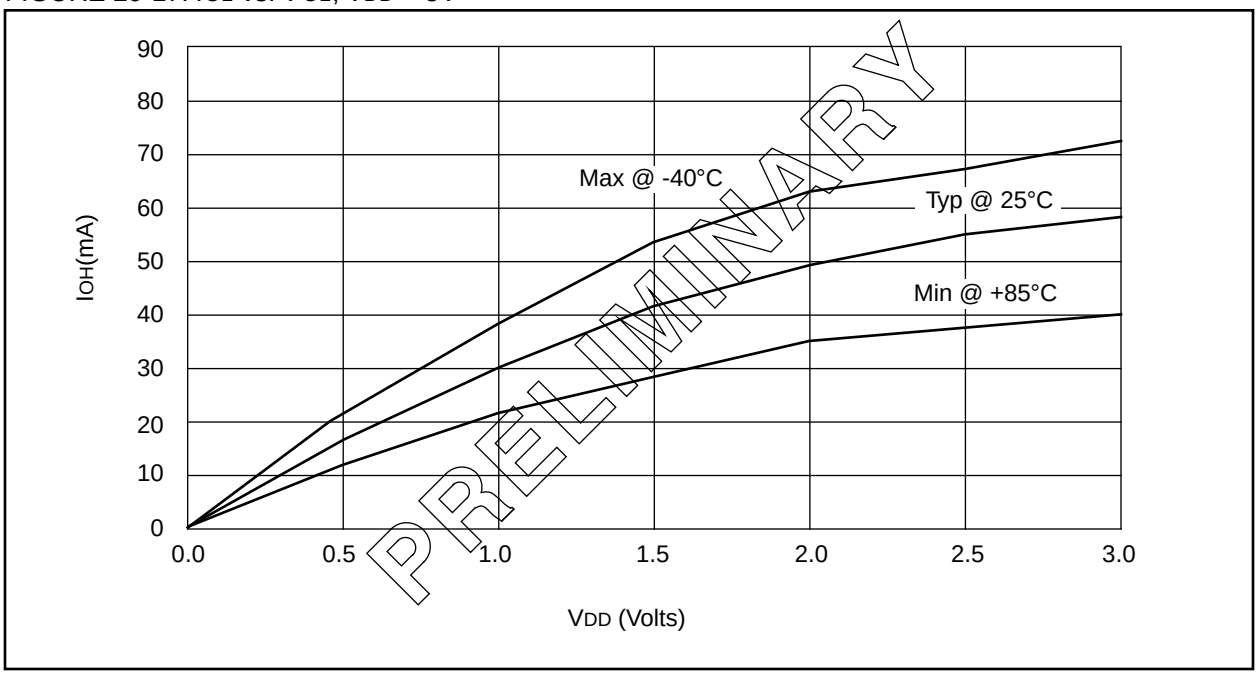
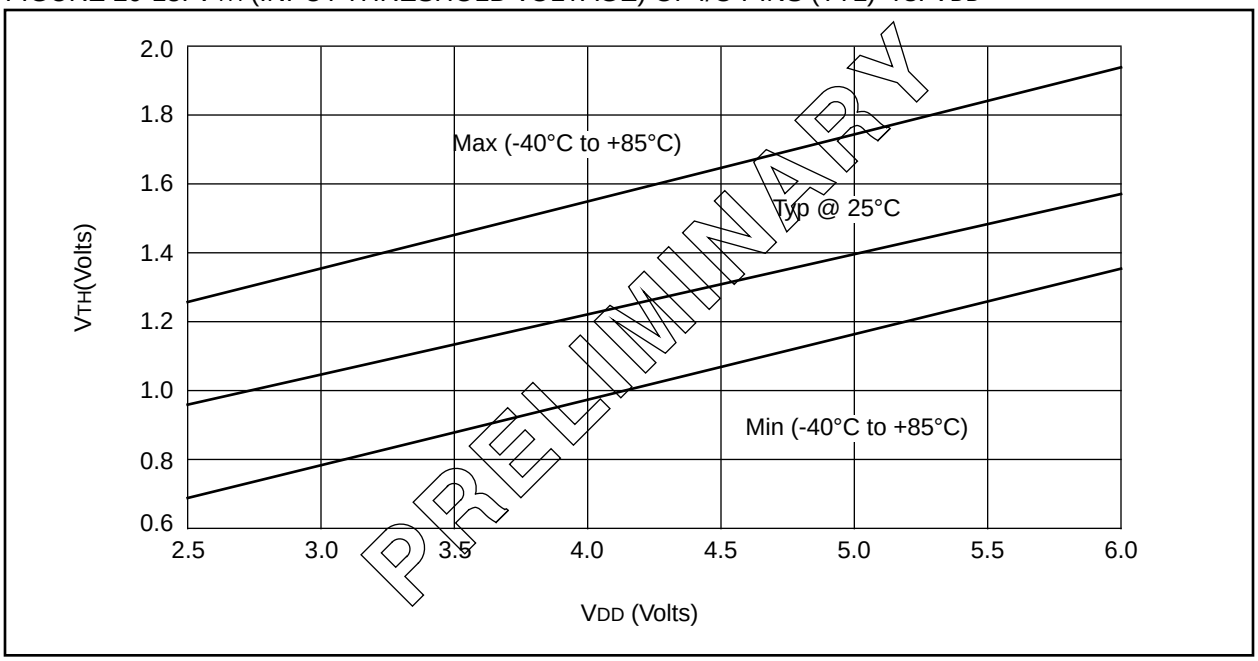



FIGURE 20-18: $V_{TH}$ (INPUT THRESHOLD VOLTAGE) OF I/O PINS (TTL) vs. $V_{DD}$





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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

FIGURE 20-19: $V_{TH}$, $V_{IL}$ of I/O PINS (SCHMITT TRIGGER) vs. $V_{DD}$

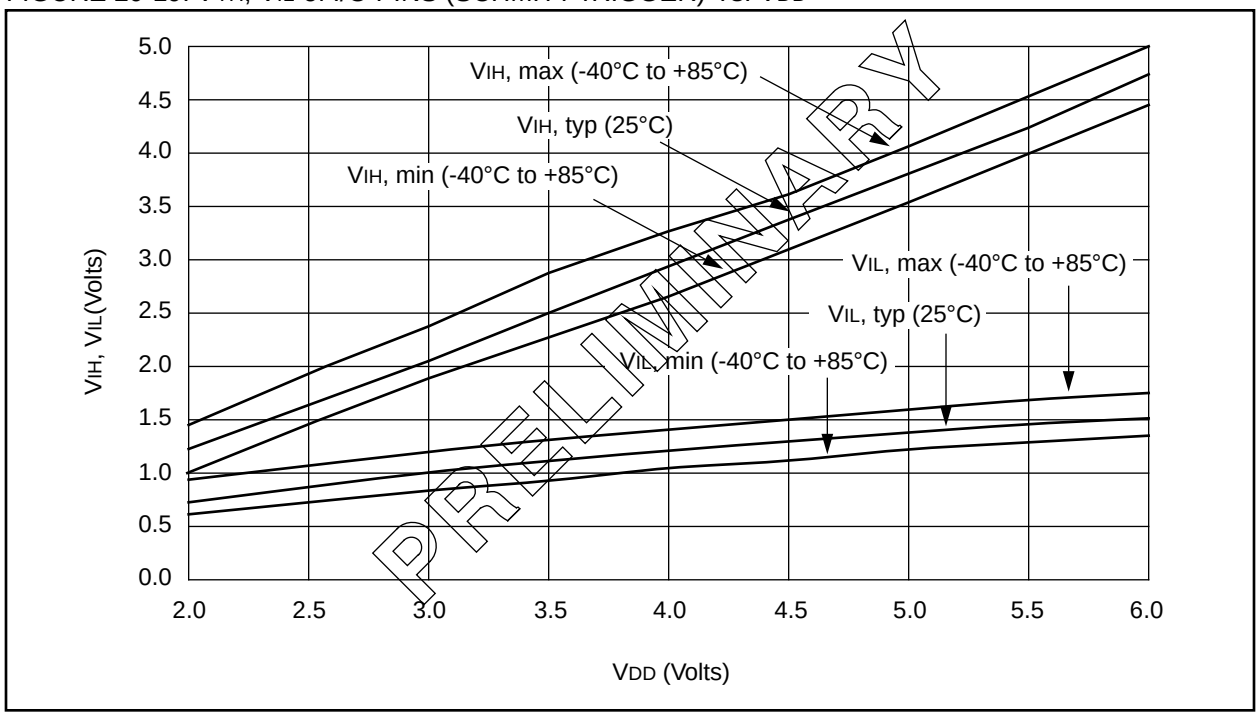
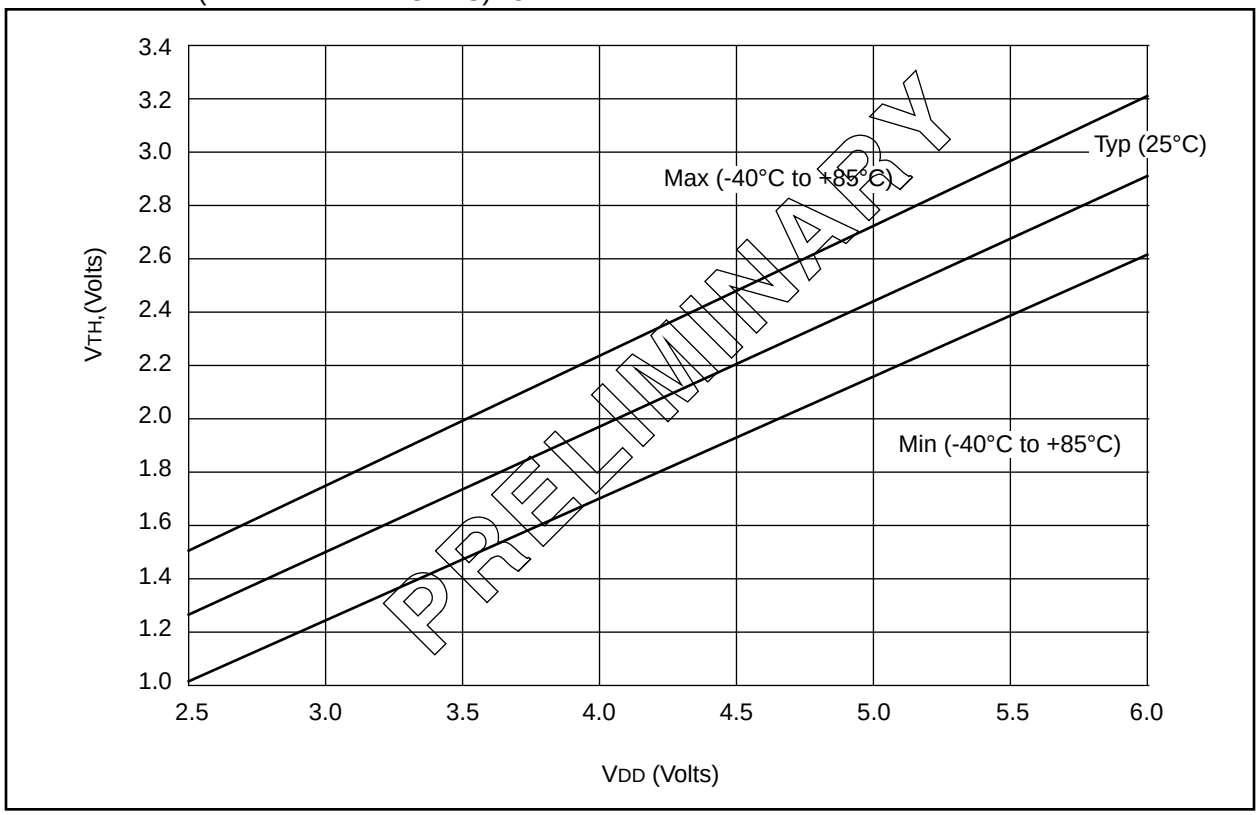



FIGURE 20-20: $V_{TH}$ (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LF MODES) vs. $V_{DD}$



NOTES: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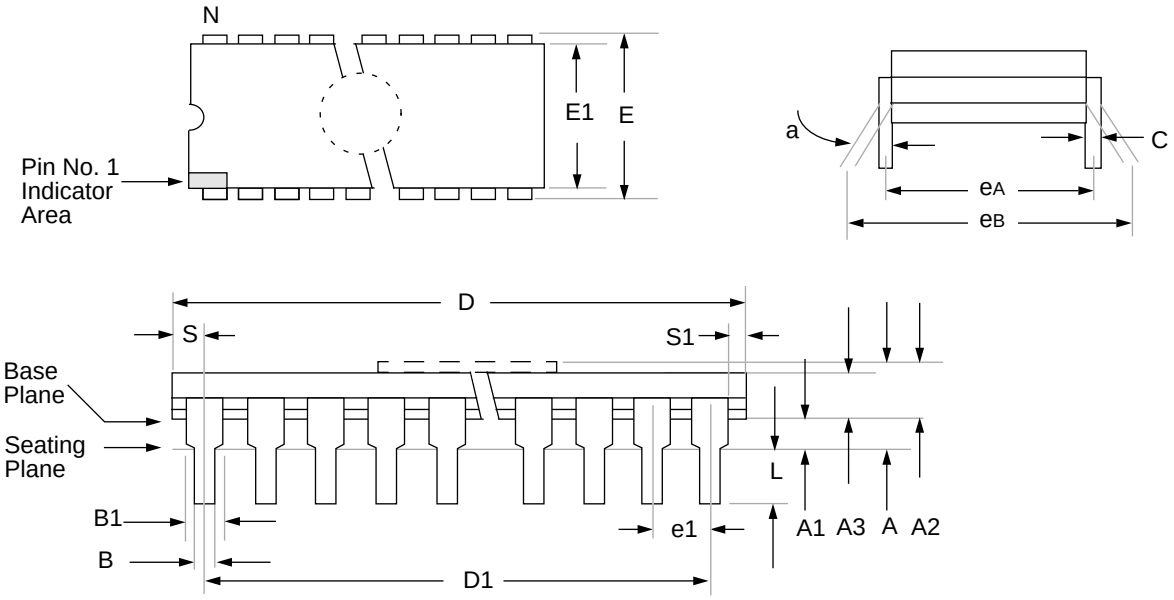
## 21.0 PACKAGING INFORMATION

### 21.1 40-Lead Ceramic CERDIP Dual In-line , and CERDIP Dual In-line with Window (600 mil)




| Package Group: Ceramic CERDIP Dual In-Line (CDP) | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| a | 0° | 10° | | 0° | 10° | |
| A | 4.318 | 5.715 | | 0.170 | 0.225 | |
| A1 | 0.381 | 1.778 | | 0.015 | 0.070 | |
| A2 | 3.810 | 4.699 | | 0.150 | 0.185 | |
| A3 | 3.810 | 4.445 | | 0.150 | 0.175 | |
| B | 0.355 | 0.585 | | 0.014 | 0.023 | |
| B1 | 1.270 | 1.651 | Typical | 0.050 | 0.065 | Typical |
| C | 0.203 | 0.381 | Typical | 0.008 | 0.015 | Typical |
| D | 51.435 | 52.705 | | 2.025 | 2.075 | |
| D1 | 48.260 | 48.260 | Reference | 1.900 | 1.900 | Reference |
| E | 15.240 | 15.875 | | 0.600 | 0.625 | |
| E1 | 12.954 | 15.240 | | 0.510 | 0.600 | |
| e1 | 2.540 | 2.540 | Reference | 0.100 | 0.100 | Reference |
| eA | 14.986 | 16.002 | Typical | 0.590 | 0.630 | Typical |
| eB | 15.240 | 18.034 | | 0.600 | 0.710 | |
| L | 3.175 | 3.810 | | 0.125 | 0.150 | |
| N | 40 | 40 | | 40 | 40 | |
| S | 1.016 | 2.286 | | 0.040 | 0.090 | |
| S1 | 0.381 | 1.778 | | 0.015 | 0.070 | |



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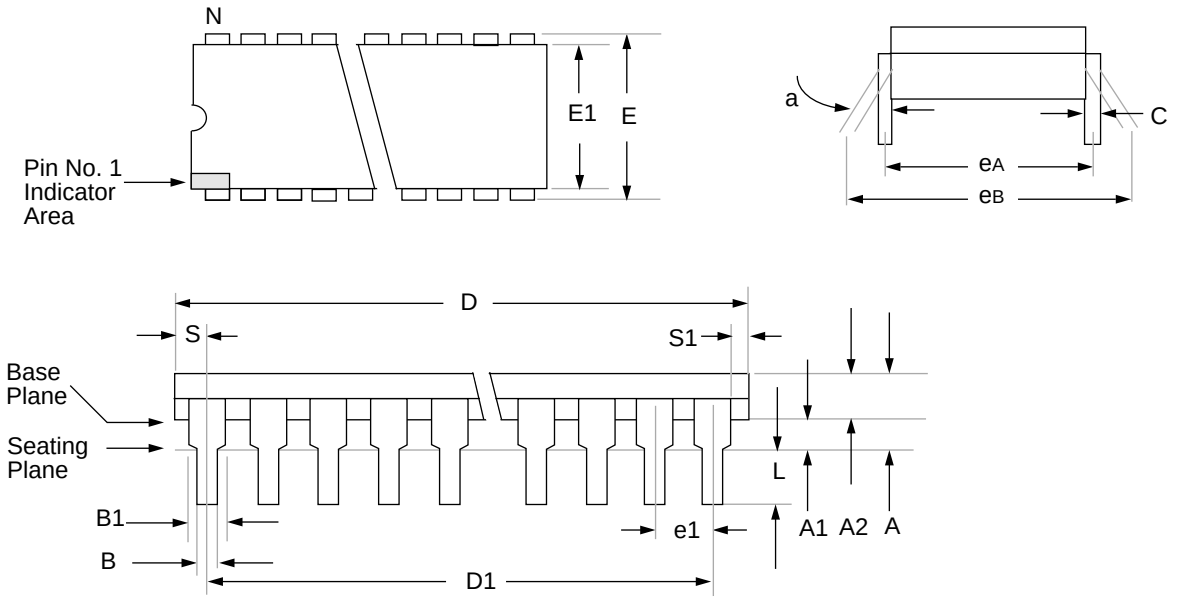
## 21.2 40-Lead Plastic Dual In-line (600 mil)




| Package Group: Plastic Dual In-Line (PLA) | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| a | 0° | 10° | | 0° | 10° | |
| A | Ð | 5.080 | | Ð | 0.200 | |
| A1 | 0.381 | Ð | | 0.015 | Ð | |
| A2 | 3.175 | 4.064 | | 0.125 | 0.160 | |
| B | 0.355 | 0.559 | | 0.014 | 0.022 | |
| B1 | 1.270 | 1.778 | Typical | 0.050 | 0.070 | Typical |
| C | 0.203 | 0.381 | Typical | 0.008 | 0.015 | Typical |
| D | 51.181 | 52.197 | | 2.015 | 2.055 | |
| D1 | 48.260 | 48.260 | Reference | 1.900 | 1.900 | Reference |
| E | 15.240 | 15.875 | | 0.600 | 0.625 | |
| E1 | 13.462 | 13.970 | | 0.530 | 0.550 | |
| e1 | 2.489 | 2.591 | Typical | 0.098 | 0.102 | Typical |
| eA | 15.240 | 15.240 | Reference | 0.600 | 0.600 | Reference |
| eB | 15.240 | 17.272 | | 0.600 | 0.680 | |
| L | 2.921 | 3.683 | | 0.115 | 0.145 | |
| N | 40 | 40 | | 40 | 40 | |
| S | 1.270 | Ð | | 0.050 | Ð | |
| S1 | 0.508 | Ð | | 0.020 | Ð | |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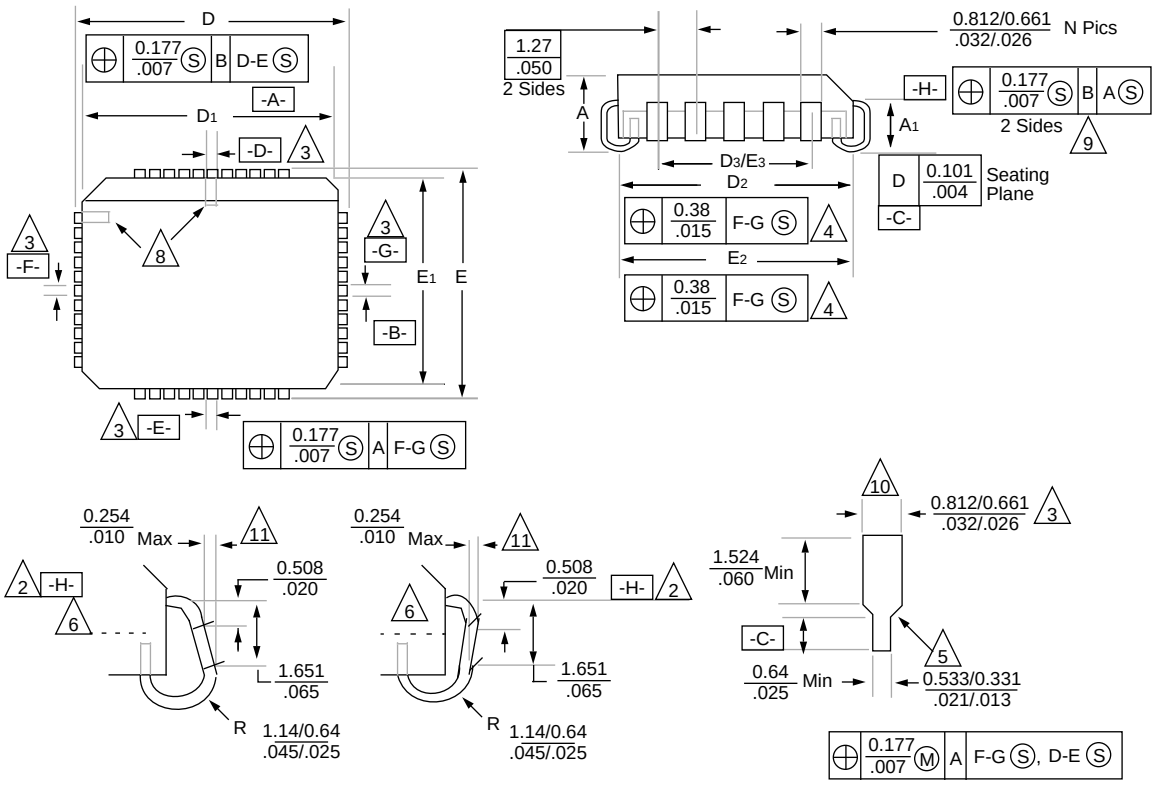
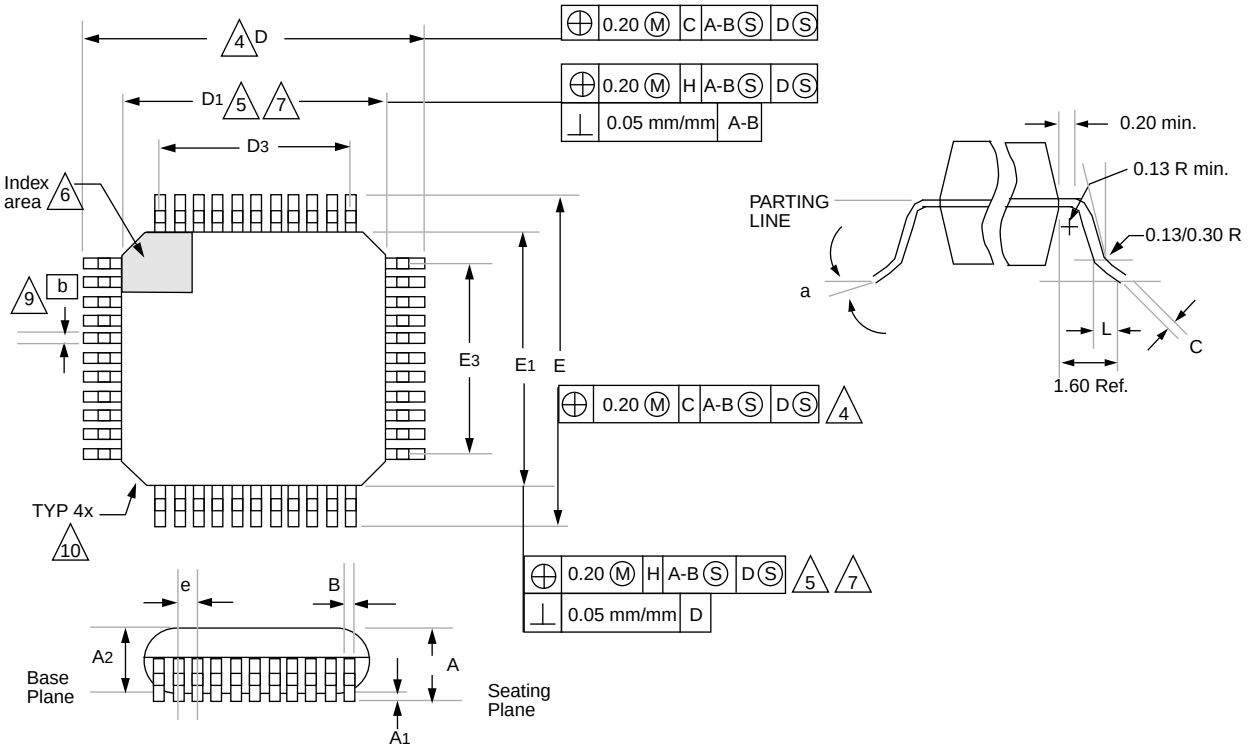
## 21.3 44-Lead Plastic Leaded Chip Carrier (Square)




| Package Group: Plastic Leaded Chip Carrier (PLCC) | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| A | 4.191 | 4.572 | | 0.165 | 0.180 | |
| A1 | 2.413 | 2.921 | | 0.095 | 0.115 | |
| D | 17.399 | 17.653 | | 0.685 | 0.695 | |
| D1 | 16.510 | 16.663 | | 0.650 | 0.656 | |
| D2 | 15.494 | 16.002 | | 0.610 | 0.630 | |
| D3 | 12.700 | 12.700 | Reference | 0.500 | 0.500 | Reference |
| E | 17.399 | 17.653 | | 0.685 | 0.695 | |
| E1 | 16.510 | 16.663 | | 0.650 | 0.656 | |
| E2 | 15.494 | 16.002 | | 0.610 | 0.630 | |
| E3 | 12.700 | 12.700 | Reference | 0.500 | 0.500 | Reference |
| N | 44 | 44 | | 44 | 44 | |
| CP | Ð | 0.102 | | Ð | 0.004 | |
| LT | 0.203 | 0.381 | | 0.008 | 0.015 | |

## 21.4 44-Lead Plastic Surface Mount (MQFP 10x10 mm Bod y 1.6/0.15 mm Lead Form)




| Package Group: Plastic MQFP | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| a | 0° | 7° | | 0° | 7° | |
| A | 2.000 | 2.350 | | 0.078 | 0.093 | |
| A1 | 0.050 | 0.250 | | 0.002 | 0.010 | |
| A2 | 1.950 | 2.100 | | 0.768 | 0.083 | |
| b | 0.300 | 0.450 | Typical | 0.011 | 0.018 | Typical |
| C | 0.150 | 0.180 | | 0.006 | 0.007 | |
| D | 12.950 | 13.450 | | 0.510 | 0.530 | |
| D1 | 9.900 | 10.100 | | 0.390 | 0.398 | |
| D3 | 8.000 | 8.000 | Reference | 0.315 | 0.315 | Reference |
| E | 12.950 | 13.450 | | 0.510 | 0.530 | |
| E1 | 9.900 | 10.100 | | 0.390 | 0.398 | |
| E3 | 8.000 | 8.000 | Reference | 0.315 | 0.315 | Reference |
| e | 0.800 | 0.800 | | 0.031 | 0.032 | |
| L | 0.730 | 1.030 | | 0.028 | 0.041 | |
| N | 44 | 44 | | 44 | 44 | |
| CP | 0.102 | Ð | | 0.004 | Ð | |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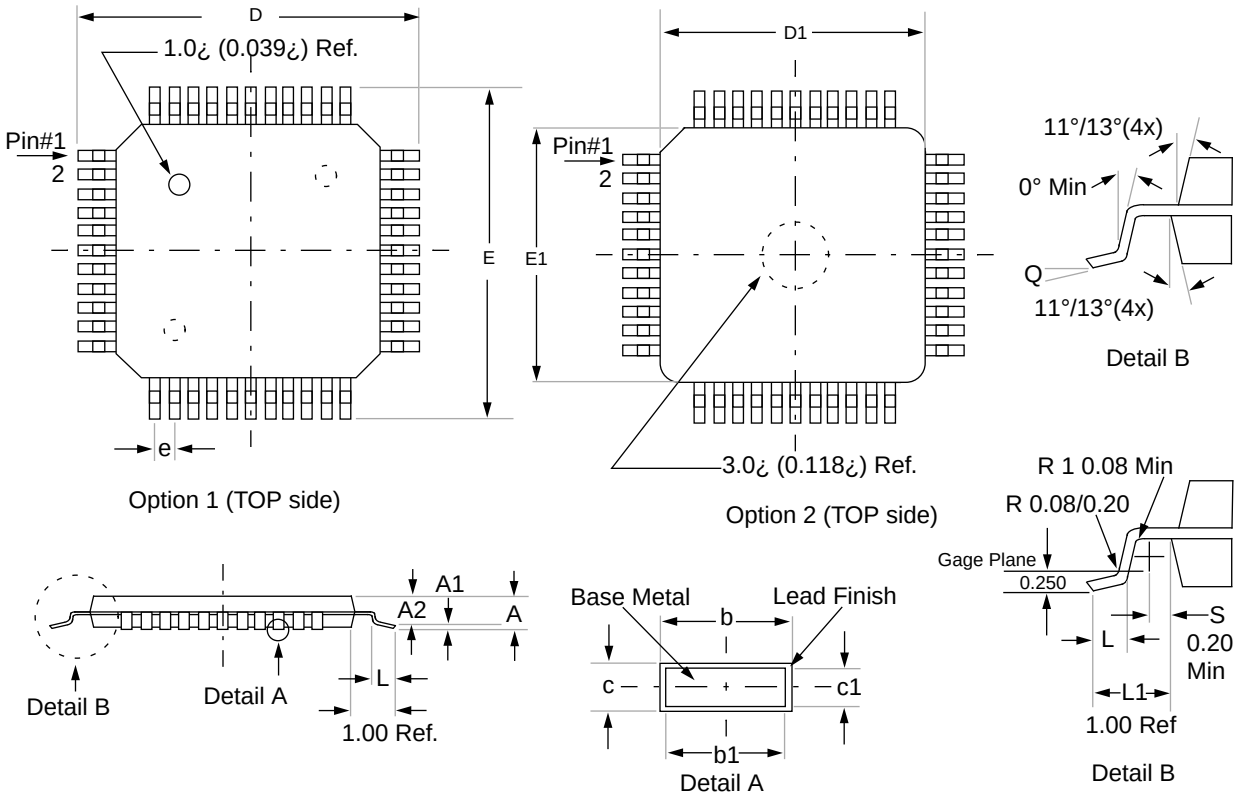
21.5 44-Lead Plastic Surface Mount (TQFP 10x10 mm Bod y 1.0/0.10 mm Lead Form)




| Package Group: Plastic TQFP | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| A | 1.00 | 1.20 | | 0.039 | 0.047 | |
| A1 | 0.05 | 0.15 | | 0.002 | 0.006 | |
| A2 | 0.95 | 1.05 | | 0.037 | 0.041 | |
| D | 11.75 | 12.25 | | 0.463 | 0.482 | |
| D1 | 9.90 | 10.10 | | 0.390 | 0.398 | |
| E | 11.75 | 12.25 | | 0.463 | 0.482 | |
| E1 | 9.90 | 10.10 | | 0.390 | 0.398 | |
| L | 0.45 | 0.75 | | 0.018 | 0.030 | |
| e | 0.80 BSC | | | 0.031 BSC | | |
| b | 0.30 | 0.45 | | 0.012 | 0.018 | |
| b1 | 0.30 | 0.40 | | 0.012 | 0.016 | |
| c | 0.09 | 0.20 | | 0.004 | 0.008 | |
| c1 | 0.09 | 0.16 | | 0.004 | 0.006 | |
| N | 44 | 44 | | 44 | 44 | |
| Q | 0° | 7° | | 0° | 7° | |

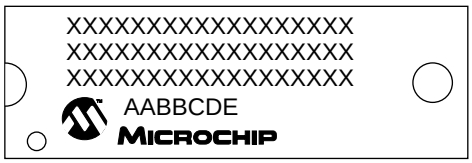
Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010Ó) per side. D1 and E1 dimensions including mold mismatch.

2: Dimension ÒbÓ does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003Ó)max.

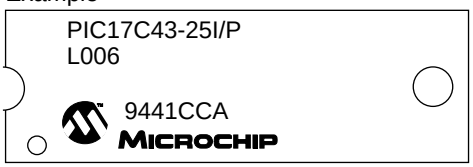
3: This outline conforms to JEDEC MS-026.

## 21.6 Package Marking Inf ormation

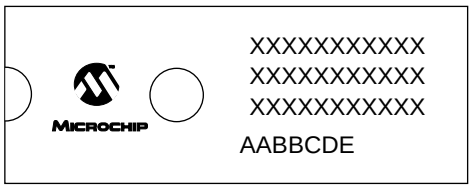
40-Lead PDIP/CERDIP



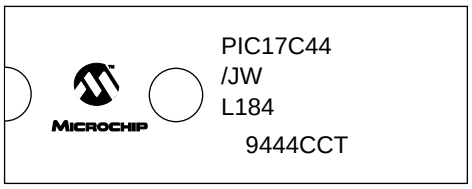

Example



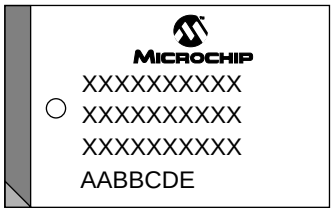

40 Lead CERDIP Windowed



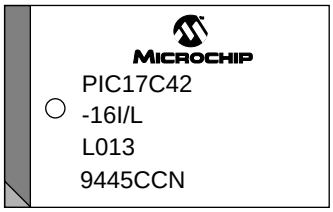

Example



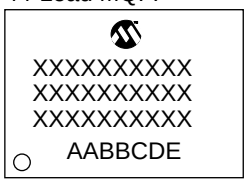

44-Lead PLCC




Example

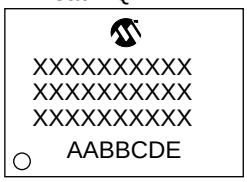



44-Lead MQFP




Example

44-Lead TQFP




Example

| | | |
|---|---|---|
| Legend: | MM...M | Microchip part number information |
| | XX...X | Customer speciÞc information* |
| | AA | Year code (last 2 digits of calendar year) |
| | BB | Week code (week of January 1 is week Ô01Õ) |
| | C | Facility code of the plant at which wafer is manufactured<br>C = Chandler, Arizona, U.S.A.,<br>S = Tempe, Arizona, U.S.A. |
| | D | Mask revision number |
| | E | Assembly code of the plant or country of origin in which part was assembled |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer speciÞc information. | |

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales OfÞce. For QTP devices, any special marking adders are included in QTP price.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## APPENDIX A: MODIFICATIONS

The following is the list of modiÞcations over the PIC16CXX microcontroller family:

1. Instruction word length is increased to 16-bit. This allows larger page sizes both in program memory (8 Kwords verses 2 Kwords) and register Þle (256 bytes versus 128 bytes).
2. Four modes of operation: microcontroller, protected microcontroller, extended microcontroller, and microprocessor.
3. 22 new instructions.
   The MOVF, TRIS and OPTION instructions have been removed.
4. 4 new instructions for transferring data between data memory and program memory. This can be used to Òself programÓ the EPROM program memory.
5. Single cycle data memory to data memory transfers possible (MOVPF and MOVFP instructions). These instructions do not affect the Working register (WREG).
6. W register (WREG) is now directly addressable.
7. A PC high latch register (PCLATH) is extended to 8-bits. The PCLATCH register is now both readable and writable.
8. Data memory paging is redeÞned slightly.
9. DDR registers replaces function of TRIS registers.
10. Multiple Interrupt vectors added. This can decrease the latency for servicing the interrupt.
11. Stack size is increased to 16 deep.
12. BSR register for data memory paging.
13. Wake up from SLEEP operates slightly differently.
14. The Oscillator Start-Up Timer (OST) and Power-Up Timer (PWRT) operate in parallel and not in series.
15. PORTB interrupt on change feature works on all eight port pins.
16. TMR0 is 16-bit plus 8-bit prescaler.
17. Second indirect addressing register added (FSR1 and FSR2). ConÞguration bits can select the FSR registers to auto-increment, auto-decrement, remain unchanged after an indirect address.
18. Hardware multiplier added (8 x 8 ® 16-bit) (PIC17C43 and PIC17C44 only).
19. Peripheral modules operate slightly differently.
20. Oscillator modes slightly redeÞned.
21. Control/Status bits and registers have been placed in different registers and the control bit for globally enabling interrupts has inverse polarity.
22. Addition of a test mode pin.
23. In-circuit serial programming is not implemented.

## APPENDIX B: COMPATIBILITY

To convert code written for PIC16CXX to PIC17CXX, the user should take the following steps:

1. Remove any TRIS and OPTION instructions, and implement the equivalent code.
2. Separate the interrupt service routine into its four vectors.
3. Replace:
   ```
   MOVF    REG1, W
   ```
   with:
   ```
   MOVFP   REG1, WREG
   ```
4. Replace:
   ```
   MOVF    REG1, W
   MOVWF   REG2
   ```
   with:
   ```
   MOVPF   REG1, REG2 ; Addr(REG1)<20h
   ```
   or
   ```
   MOVFP   REG1, REG2 ; Addr(REG2)<20h
   ```

   Note: If REG1 and REG2 are both at addresses greater then 20h, two instructions are required.
   ```
   MOVFP   REG1, WREG ;
   MOVPF   WREG, REG2 ;
   ```
5. Ensure that all bit names and register names are updated to new data memory map location.
6. Verify data memory banking.
7. Verify mode of operation for indirect addressing.
8. Verify peripheral routines for compatibility.
9. Weak pull-ups are enabled on reset.

To convert code from the PIC17C42 to all the other PIC17C4X devices, the user should take the following steps.

1. If the hardware multiply is to be used, ensure that any variables at address 18h and 19h are moved to another address.
2. Ensure that the upper nibble of the BSR was not written with a non-zero value. This may cause unexpected operation since the RAM bank is no longer 0.
3. The disabling of global interrupts has been enhanced so there is no additional testing of the GLINTD bit after a `BSF CPUSTA, GLINTD` instruction.



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## APPENDIX C: WHATÕS NEW

The structure of the document has been made consistent with other data sheets. This ensures that important topics are covered across all PIC16/17 families. Here is an overview of new features.

Added the following devices:

PIC17CR42

PIC17C42A

PIC17CR43

A 33 MHz option is now available.

## APPENDIX D: WHATÕS CHANGED

To make software more portable across the different PIC16/17 families, the name of several registers and control bits have been changed. This allows control bits that have the same function, to have the same name (regardless of processor family). Care must still be taken, since they may not be at the same special function register address. The following shows the register and bit names that have been changed:

| Old Name | New Name |
|---|---|
| TX8/9 | TX9 |
| RC8/9 | RX9 |
| RCD8 | RX9D |
| TXD8 | TX9D |

Instruction DECFSNZ corrected to DCFSNZ

Instruction INCFSNZ corrected to INFSNZ

Enhanced discussion on PWM to include equation for determining bits of PWM resolution.

Section 13.2.2 and 13.3.2 have had the description of updating the FERR and RX9 bits enhanced.

The location of conÞguration bit PM2 was changed (Figure 6-1 and Figure 14-1).

Enhanced description of the operation of the INTSTA register.

Added note to discussion of interrupt operation.

Tightened electrical spec D110.

Corrected steps for setting up USART Asynchronous Reception.


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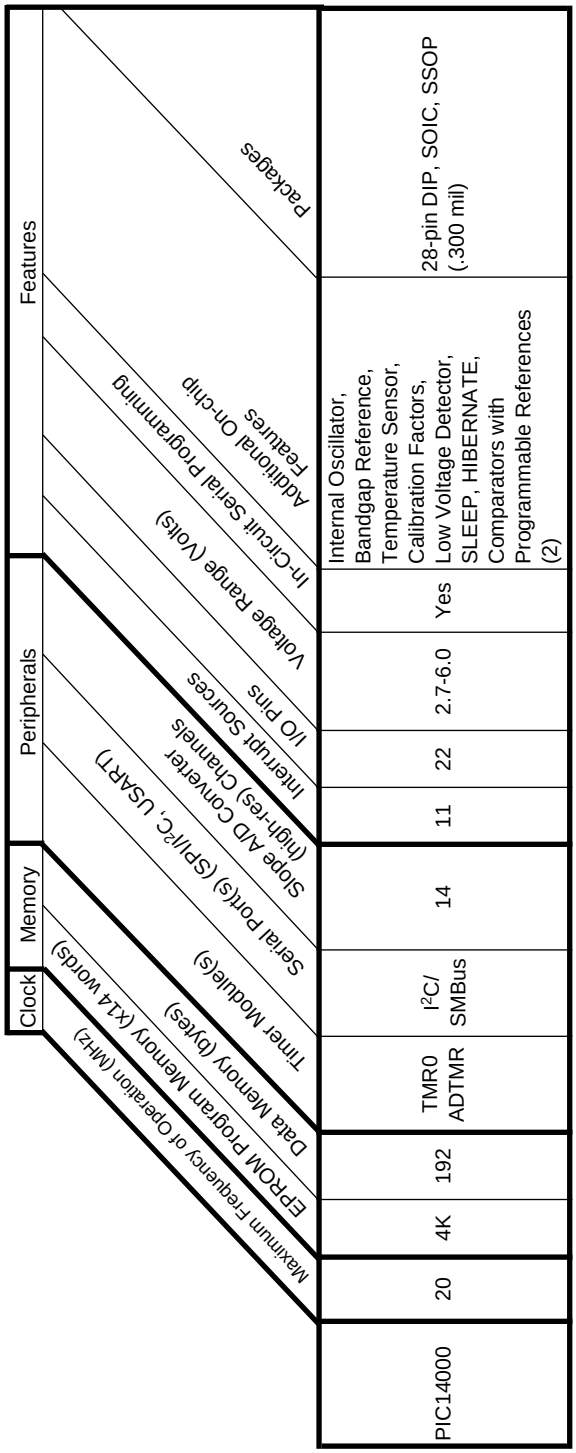
# APPENDIX E: PIC16/17 MICROCONTROLLERS

## E.1 PIC14000 Devices



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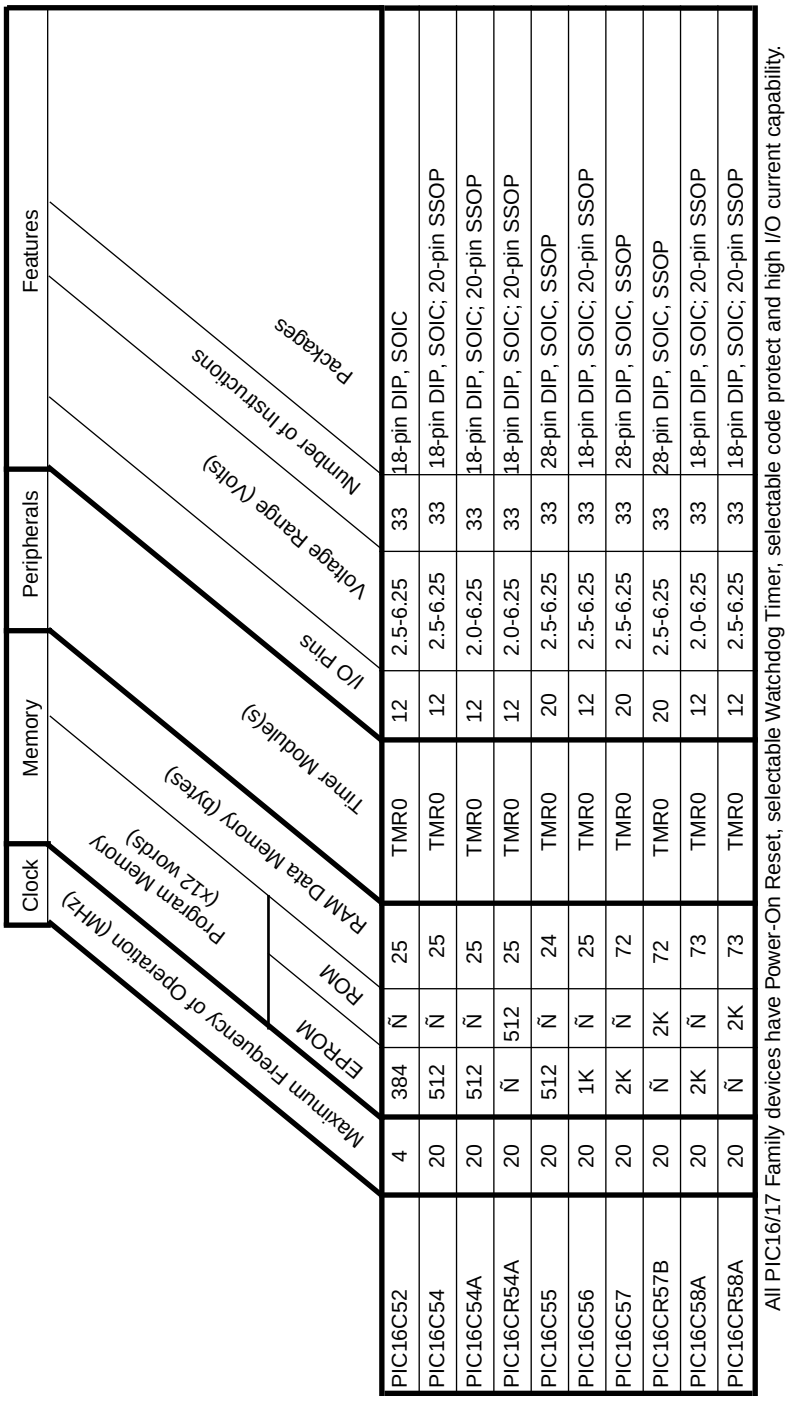
## E.2 PIC16C5X Family of Devices



| | Clock | Memory | | | | Peripherals | | Features | |
|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | Program Memory (x12 words) | EPROM | ROM | RAM Data Memory (bytes) | Timer Module(s) | I/O Pins | Voltage Range (Volts) | Number of Instructions | Packages |
| PIC16C52 | 4 | 384 | Ñ | 25 | | TMR0 | 12 | 2.5-6.25 | 33 | 18-pin DIP, SOIC |
| PIC16C54 | 20 | 512 | Ñ | 25 | | TMR0 | 12 | 2.5-6.25 | 33 | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C54A | 20 | 512 | Ñ | 25 | | TMR0 | 12 | 2.0-6.25 | 33 | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16CR54A | 20 | Ñ | 512 | 25 | | TMR0 | 12 | 2.0-6.25 | 33 | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C55 | 20 | 512 | Ñ | 24 | | TMR0 | 20 | 2.5-6.25 | 33 | 28-pin DIP, SOIC, SSOP |
| PIC16C56 | 20 | 1K | Ñ | 25 | | TMR0 | 12 | 2.5-6.25 | 33 | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C57 | 20 | 2K | Ñ | 72 | | TMR0 | 20 | 2.5-6.25 | 33 | 28-pin DIP, SOIC, SSOP |
| PIC16CR57B | 20 | Ñ | 2K | 72 | | TMR0 | 20 | 2.5-6.25 | 33 | 28-pin DIP, SOIC, SSOP |
| PIC16C58A | 20 | 2K | Ñ | 73 | | TMR0 | 12 | 2.0-6.25 | 33 | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16CR58A | 20 | Ñ | 2K | 73 | | TMR0 | 12 | 2.5-6.25 | 33 | 18-pin DIP, SOIC; 20-pin SSOP |

All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.



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## E.3 PIC16CXXX Family of Devices

| | Clock | Memory | | | Peripherals | | | | Features | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | EPROM | Program Memory (x14 words) | Data Memory (bytes) | Timer Module(s) | Comparator(s) | Internal Reference Voltage | Interrupt Sources | I/O Pins | Voltage Range (Volts) | Brown-out Reset | Packages |
| PIC16C554 | 20 | 512 | 80 | TMR0 | Ñ | Ñ | 3 | 13 | 2.5-6.0 | Ñ | Ñ | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C556 | 20 | 1K | 80 | TMR0 | Ñ | Ñ | 3 | 13 | 2.5-6.0 | Ñ | Ñ | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C558 | 20 | 2K | 128 | TMR0 | Ñ | Ñ | 3 | 13 | 2.5-6.0 | Ñ | Ñ | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C620 | 20 | 512 | 80 | TMR0 | 2 | Yes | 4 | 13 | 2.5-6.0 | Yes | Yes | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C621 | 20 | 1K | 80 | TMR0 | 2 | Yes | 4 | 13 | 2.5-6.0 | Yes | Yes | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C622 | 20 | 2K | 128 | TMR0 | 2 | Yes | 4 | 13 | 2.5-6.0 | Yes | Yes | 18-pin DIP, SOIC; 20-pin SSOP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16C6XXX Family devices use serial programming with clock pin RB6 and data pin RB7.

## E.4 PIC16C6X Family of Devices

| | Clock | Memory | | | | Peripherals | | | | | | Features | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | Program Memory (X14 words) | EPROM | ROM | Data Memory (bytes) | Timer Module(s) | Capture/Compare/PWM Module(s) | Serial Port(s) (SPI/I²C, USART) | Parallel Slave Port | Interrupt Sources | I/O Pins | Voltage Range (Volts) | In-Circuit Serial Programming | Brown-out Reset | Packages |
| PIC16C62 | 20 | 2K | Ñ | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Ñ | 7 | 22 | 3.0-6.0 | Yes | Ñ | | 28-pin SDIP, SOIC, SSOP |
| PIC16C62A(1) | 20 | 2K | Ñ | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Ñ | 7 | 22 | 2.5-6.0 | Yes | Yes | | 28-pin SDIP, SOIC, SSOP |
| PIC16CR62(1) | 20 | Ñ | 2K | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Ñ | 7 | 22 | 2.5-6.0 | Yes | Yes | | 28-pin SDIP, SOIC, SSOP |
| PIC16C63 | 20 | 4K | Ñ | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Ñ | 10 | 22 | 2.5-6.0 | Yes | Yes | | 28-pin SDIP, SOIC |
| PIC16CR63(1) | 20 | Ñ | 4K | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Ñ | 10 | 22 | 2.5-6.0 | Yes | Yes | | 28-pin SDIP, SOIC |
| PIC16C64 | 20 | 2K | Ñ | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Yes | 8 | 33 | 3.0-6.0 | Yes | Ñ | | 40-pin DIP; 44-pin PLCC, MQFP |
| PIC16C64A(1) | 20 | 2K | Ñ | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Yes | 8 | 33 | 2.5-6.0 | Yes | Yes | | 40-pin DIP; 44-pin PLCC, MQFP, TQFP |
| PIC16CR64(1) | 20 | Ñ | 2K | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Yes | 8 | 33 | 2.5-6.0 | Yes | Yes | | 40-pin DIP; 44-pin PLCC, MQFP, TQFP |
| PIC16C65 | 20 | 4K | Ñ | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Yes | 11 | 33 | 3.0-6.0 | Yes | Ñ | | 40-pin DIP; 44-pin PLCC, MQFP |
| PIC16C65A(1) | 20 | 4K | Ñ | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Yes | 11 | 33 | 2.5-6.0 | Yes | Yes | | 40-pin DIP; 44-pin PLCC, MQFP, TQFP |
| PIC16CR65(1) | 20 | Ñ | 4K | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Yes | 11 | 33 | 2.5-6.0 | Yes | Yes | | 40-pin DIP; 44-pin PLCC, MQFP, TQFP |

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.
All PIC16C6X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.


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## E.5 PIC16C7X Family of Devices

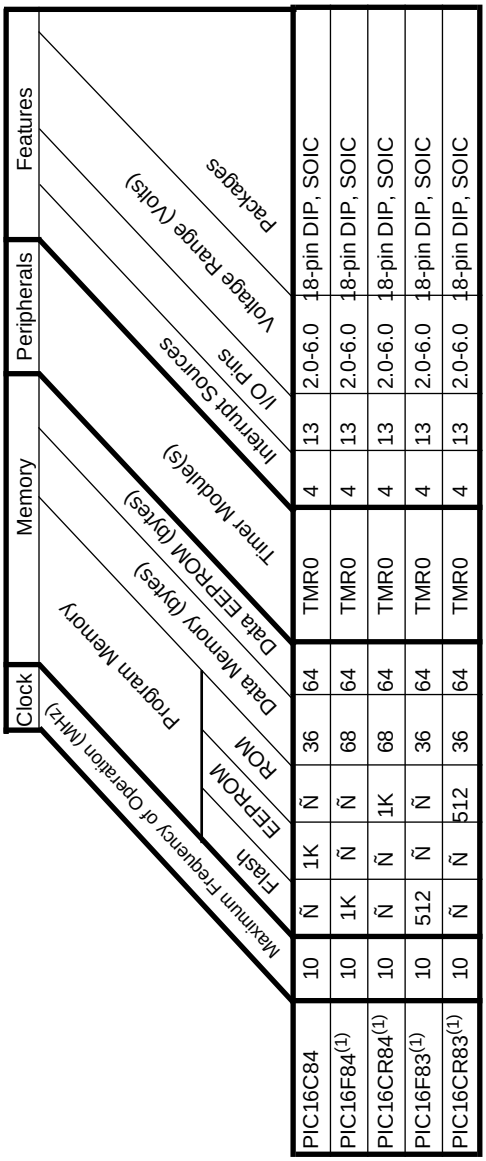
| | Clock | Memory | | Peripherals | | | | | | Features | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | EPROM Program Memory (x14 words) | Data Memory (bytes) | Timer Module(s) | Capture/Compare/PWM Module(s) | Serial Port(s) (SPI/I²C, USART) | Parallel Slave Port | A/D Converter (8-bit) Channels | Interrupt Sources | I/O Pins | Voltage Range (Volts) | In-Circuit Serial Programming | Brown-out Reset | Packages |
| PIC16C710 | 20 | 512 | 36 | TMR0 | Ñ | Ñ | Ñ | 4 | 4 | 13 | 3.0-6.0 | Yes | Yes | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C71 | 20 | 1K | 36 | TMR0 | Ñ | Ñ | Ñ | 4 | 4 | 13 | 3.0-6.0 | Yes | Ñ | 18-pin DIP, SOIC |
| PIC16C711 | 20 | 1K | 68 | TMR0 | Ñ | Ñ | Ñ | 4 | 4 | 13 | 3.0-6.0 | Yes | Yes | 18-pin DIP, SOIC; 20-pin SSOP |
| PIC16C72 | 20 | 2K | 128 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Ñ | 5 | 8 | 22 | 2.5-6.0 | Yes | Yes | 28-pin SDIP, SOIC, SSOP |
| PIC16C73 | 20 | 4K | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Ñ | 5 | 11 | 22 | 3.0-6.0 | Yes | Ñ | 28-pin SDIP, SOIC |
| PIC16C73A(1) | 20 | 4K | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Ñ | 5 | 11 | 22 | 2.5-6.0 | Yes | Yes | 28-pin SDIP, SOIC |
| PIC16C74 | 20 | 4K | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Yes | 8 | 12 | 33 | 3.0-6.0 | Yes | Ñ | 40-pin DIP; 44-pin PLCC, MQFP |
| PIC16C74A(1) | 20 | 4K | 192 | TMR0, TMR1, TMR2 | 2 | SPI/I²C, USART | Yes | 8 | 12 | 33 | 2.5-6.0 | Yes | Yes | 40-pin DIP; 44-pin PLCC, MQFP, TQFP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C7X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

## E.6 PIC16C8X Family of Devices



| | Clock | Memory | | | | Peripherals | | Features | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | Program Memory | Flash | EEPROM | ROM | Data Memory (bytes) | Data EEPROM (bytes) | Timer Module(s) | Interrupt Sources | I/O Pins | Voltage Range (Volts) | Packages |
| PIC16C84 | 10 | Ñ | 1K | Ñ | 36 | 64 | 64 | TMR0 | 4 | 13 | 2.0-6.0 | 18-pin DIP, SOIC |
| PIC16F84(1) | 10 | 1K | Ñ | Ñ | 68 | 64 | 64 | TMR0 | 4 | 13 | 2.0-6.0 | 18-pin DIP, SOIC |
| PIC16CR84(1) | 10 | Ñ | Ñ | 1K | 68 | 64 | 64 | TMR0 | 4 | 13 | 2.0-6.0 | 18-pin DIP, SOIC |
| PIC16F83(1) | 10 | 512 | Ñ | Ñ | 36 | 64 | 64 | TMR0 | 4 | 13 | 2.0-6.0 | 18-pin DIP, SOIC |
| PIC16CR83(1) | 10 | Ñ | Ñ | 512 | 36 | 64 | 64 | TMR0 | 4 | 13 | 2.0-6.0 | 18-pin DIP, SOIC |

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C8X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.



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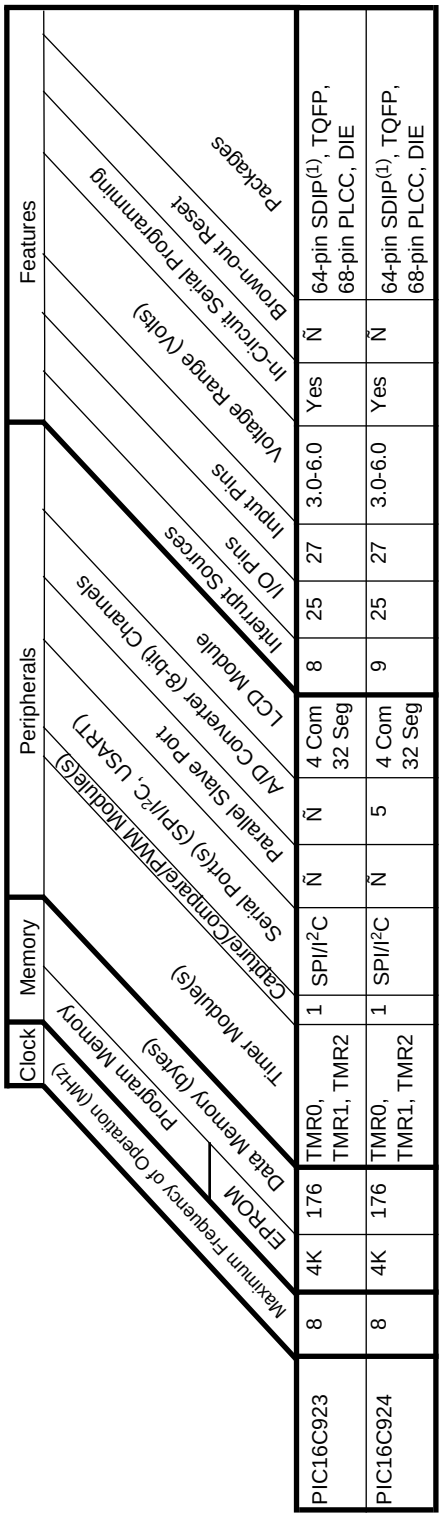
## E.7 PIC16C9XX Family Of Devices



| | Clock | | Memory | | | Peripherals | | | | | | Features | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | | Program Memory (words) | EPROM | Data Memory (bytes) | Timer Module(s) | Capture/Compare/PWM Module(s) | Serial Port(s) (SPI/I²C, USART) | Parallel Slave Port | A/D Converter (8-bit) Channels | LCD Module | Interrupt Sources | I/O Pins | Input Pins | Voltage Range (Volts) | In-Circuit Serial Programming | Brown-out Reset | Packages |
| PIC16C923 | 8 | | 4K | 176 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Ñ | Ñ | 4 Com 32 Seg | 8 | 25 | 27 | 3.0-6.0 | Yes | Ñ | | 64-pin SDIP(1), TQFP, 68-pin PLCC, DIE |
| PIC16C924 | 8 | | 4K | 176 | TMR0, TMR1, TMR2 | 1 | SPI/I²C | Ñ | Ñ | 4 Com 32 Seg | 9 | 25 | 27 | 3.0-6.0 | Yes | Ñ | | 64-pin SDIP(1), TQFP, 68-pin PLCC, DIE |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16CXX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip representative for availability of this package.

## E.8 PIC17CXX Family of Devices

| | Clock | Memory | | | | | Peripherals | | | | | Features | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | EPROM | ROM | Program Memory (Words) | RAM Data Memory (bytes) | Timer Module(s) | Captures PWMs | Serial Port(s) (USART) | Hardware Multiply | External Interrupts | Interrupt Sources | I/O Pins | Voltage Range (Volts) | Number of Instructions | Packages |
| PIC17C42 | 25 | 2K | Ñ | 232 | | TMR0,TMR1, TMR2,TMR3 | 2 2 | Yes | Ñ | Yes | 11 | 33 | 4.5-5.5 | 55 | 40-pin DIP; 44-pin PLCC, MQFP |
| PIC17C42A | 25 | 2K | Ñ | 232 | | TMR0,TMR1, TMR2,TMR3 | 2 2 | Yes | Yes | Yes | 11 | 33 | 2.5-6.0 | 58 | 40-pin DIP; 44-pin PLCC, TQFP, MQFP |
| PIC17CR42 | 25 | Ñ | 2K | 232 | | TMR0,TMR1, TMR2,TMR3 | 2 2 | Yes | Yes | Yes | 11 | 33 | 2.5-6.0 | 58 | 40-pin DIP; 44-pin PLCC, TQFP, MQFP |
| PIC17C43 | 25 | 4K | Ñ | 454 | | TMR0,TMR1, TMR2,TMR3 | 2 2 | Yes | Yes | Yes | 11 | 33 | 2.5-6.0 | 58 | 40-pin DIP; 44-pin PLCC, TQFP, MQFP |
| PIC17CR43 | 25 | Ñ | 4K | 454 | | TMR0,TMR1, TMR2,TMR3 | 2 2 | Yes | Yes | Yes | 11 | 33 | 2.5-6.0 | 58 | 40-pin DIP; 44-pin PLCC, TQFP, MQFP |
| PIC17C44 | 25 | 8K | | 454 | | TMR0,TMR1, TMR2,TMR3 | 2 2 | Yes | Yes | Yes | 11 | 33 | 2.5-6.0 | 58 | 40-pin DIP; 44-pin PLCC, TQFP, MQFP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.



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## PIN COMPATIBILITY

Devices that have the same package type and VDD, VSS and $\overline{MCLR}$ pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only requires minor software modiÞcation to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

TABLE E-1: PIN COMPATIBLE DEVICES

| Pin Compatible Devices | Package |
|---|---|
| PIC12C508, PIC12C509 | 8-pin |
| PIC16C54, PIC16C54A,<br>PIC16CR54A,<br>PIC16C56,<br>PIC16C58A, PIC16CR58A,<br>PIC16C61,<br>PIC16C554, PIC16C556, PIC16C558<br>PIC16C620, PIC16C621, PIC16C622,<br>PIC16C710, PIC16C71, PIC16C711,<br>PIC16F83, PIC16CR83,<br>PIC16C84, PIC16F84A, PIC16CR84 | 18-pin<br>20-pin |
| PIC16C55,<br>PIC16C57, PIC16CR57B | 28-pin |
| PIC16C62, PIC16CR62, PIC16C62A, PIC16C63,<br>PIC16C72, PIC16C73, PIC16C73A | 28-pin |
| PIC16C64, PIC16CR64, PIC16C64A,<br>PIC16C65, PIC16C65A,<br>PIC16C74, PIC16C74A | 40-pin |
| PIC17C42, PIC17CR42, PIC17C42A,<br>PIC17C43, PIC17CR43, PIC17C44 | 40-pin |
| PIC16C923, PIC16C924 | 64/68-pin |

NOTES:


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## APPENDIX F: ERRATA FOR PIC17C42 SILICON

The PIC17C42 devices that you have received have the following anomalies. At present there is no intention for future revisions to the present PIC17C42 silicon. If these cause issues for the application, it is recommended that you select the PIC17C42A device.

| Note: | New designs should use the PIC17C42A. |
|---|---|

1. When the Oscillator Start-Up Timer (OST) is enabled (in LF or XT oscillator modes), any interrupt that wakes the processor may cause a WDT reset. This occurs when the WDT is greater than or equal to 50% time-out period when the SLEEP instruction is executed. This will not occur in either the EC or RC oscillator modes.

   Work-arounds

a) Always ensure that the CLRWDT instruction is executed before the WDT increments past 50% of the WDT period. This will keep the ÒfalseÓ WDT reset from occurring.
b) When using the WDT as a normal timer (WDT disabled), ensure that the WDT is less than or equal to 50% time-out period when the SLEEP instruction is executed. This can be done by monitoring the $\overline{TO}$ bit for changing state from set to clear. Example 1 shows putting the PIC17C42 to sleep.

EXAMPLE F-1: PIC17C42 TO SLEEP

```
      BTFSS   CPUSTA, TO  ; TO = 0?
      CLRWDT              ; YES, WDT = 0
LOOP  BTFSC   CPUSTA, TO  ; WDT rollover?
      GOTO    LOOP        ; NO, Wait
      SLEEP               ; YES, goto Sleep
```

2. When the clock source of Timer1 or Timer2 is selected to external clock, the overßow interrupt ßag will be set twice, once when the timer equals the period, and again when the timer value is reset to 0h. If the latency to clear TMRxIF is greater than the time to the next clock pulse, no problems will be noticed. If the latency is less than the time to the next timer clock pulse, the interrupt will be serviced twice.

   Work-arounds

a) Ensure that the timer has rolled over to 0h before clearing the ßag bit.
b) Clear the timer in software. Clearing the timer in software causes the period to be one count less than expected.

Design considerations

The device must not be operated outside of the speciÞed voltage range. An external reset circuit must be used to ensure the device is in reset when a brown-out occurs or the $V_{DD}$ rise time is too long. Failure to ensure that the device is in reset when device voltage is out of speciÞcation may cause the device to lock-up and ignore the $\overline{MCLR}$ pin.



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| | | |
|---|---|---|
| Pattern: | QTP, SQTP, ROM Code (factory speciÞed) or Special Requirements. Blank for OTP and Windowed devices | |
| Package: | P | = PDIP |
| | JW | = Windowed CERDIP |
| | P | = PDIP (600 mil) |
| | PQ | = MQFP |
| | PT | = TQFP |
| | L | = PLCC |
| Temperature Range: | Ð | = 0ûC to +70ûC |
| | I | = Ð40ûC to +85ûC |
| Frequency Range: | 08 | = 8 MHz |
| | 16 | = 16 MHz |
| | 25 | = 25 Mhz |
| | 33 | = 33 Mhz |
| Device: | PIC17C44 | : Standard Vdd range |
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Examples

a) PIC17C42 Ð 16/P Commercial Temp., PDIP package, 16 MHZ, normal VDD limits

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01/18/02

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