# N-Channel 20-V (D-S) MOSFETs

## PRODUCT SUMMARY

| | $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) | $Q_g$ (Typ.) |
|---|---|---|---|---|
| Channel-1 | 20 | 0.0086 at $V_{GS}$ = 10 V | 16[a] | 9.5 nC |
| | | 0.0108 at $V_{GS}$ = 4.5 V | 16[a] | |
| Channel-2 | 20 | 0.0058 at $V_{GS}$ = 10 V | 16[a] | 27 nC |
| | | 0.0066 at $V_{GS}$ = 4.5 V | 16[a] | |

## FEATURES

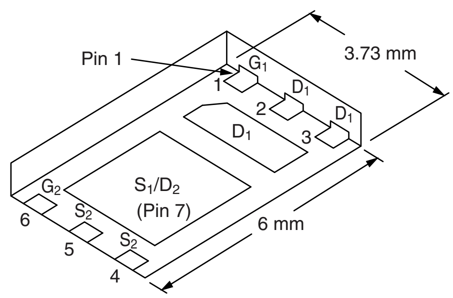
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- 100 % $R_g$ Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE

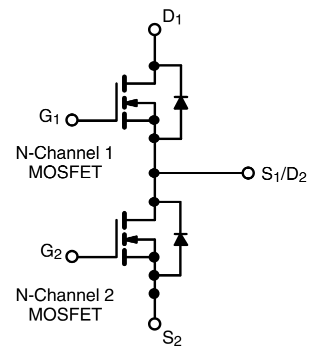
## APPLICATIONS

- Notebook System Power
- POL

**PowerPAIR® 6 x 3.7**




**Ordering Information:**
SiZ700DT-T1-GE3 (Lead (Pb)-free and Halogen-free)




## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted)

| Parameter | | Symbol | Channel-1 | Channel-2 | Unit |
|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 20 | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 16 | | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 16[a] | 16[a] | A |
| | $T_C$ = 70 °C | | 16[a] | 16[a] | |
| | $T_A$ = 25 °C | | 13.1[b, c] | 17.3[b, c] | |
| | $T_A$ = 70 °C | | 10.5[b, c] | 13.9[b, c] | |
| Pulsed Drain Current | | $I_{DM}$ | 60 | 60 | |
| Source Drain Current Diode Current | $T_C$ = 25 °C | $I_S$ | 14.7 | 16[a] | |
| | $T_A$ = 25 °C | | 1.96[b, c] | 2.3[b, c] | |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 2.36 | 2.8 | W |
| | $T_C$ = 70 °C | | 1.5 | 1.78 | |
| | $T_A$ = 25 °C | | 1.4[b, c] | 1.47[b, c] | |
| | $T_A$ = 70 °C | | 0.9[b, c] | 0.94[b, c] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | | °C |
| Soldering Recommendations (Peak Temperature)[d, e] | | | 260 | | |

## THERMAL RESISTANCE RATINGS

| Parameter | | Symbol | Channel-1 Typ. | Channel-1 Max. | Channel-2 Typ. | Channel-2 Max. | Unit |
|---|---|---|---|---|---|---|---|
| Maximum Junction-to-Ambient[b, f] | t ≤ 10 s | $R_{thJA}$ | 39 | 53 | 33 | 45 | °C/W |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 5.7 | 7.1 | 3.7 | 4.6 | |

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 90 °C/W for channel-1 and 85 °C/W for channel-2.

| SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | Ch-1 | 20 | | | V |
| | | $V_{GS}$ = 0 V, $I_D$ = 250 µA | Ch-2 | 20 | | | |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 µA | Ch-1 | | 21 | | mV/°C |
| | | $I_D$ = 250 µA | Ch-2 | | 21 | | |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | $I_D$ = 250 µA | Ch-1 | | - 5.8 | | |
| | | $I_D$ = 250 µA | Ch-2 | | - 5.8 | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 µA | Ch-1 | 0.8 | | 2.2 | V |
| | | $V_{DS} = V_{GS}$, $I_D$ = 250 µA | Ch-2 | 0.8 | | 2.2 | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 16 V | Ch-1 | | | ± 100 | nA |
| | | | Ch-2 | | | ± 100 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | Ch-1 | | | 1 | µA |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | Ch-2 | | | 1 | |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | Ch-1 | | | 10 | |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | Ch-2 | | | 10 | |
| On-State Drain Current[b] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | Ch-1 | 30 | | | A |
| | | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | Ch-2 | 30 | | | |
| Drain-Source On-State Resistance[b] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 15 A | Ch-1 | | 0.007 | 0.0086 | Ω |
| | | $V_{GS}$ = 10 V, $I_D$ = 20 A | Ch-2 | | 0.0047 | 0.0058 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 10 A | Ch-1 | | 0.0088 | 0.0108 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 15 A | Ch-2 | | 0.0054 | 0.0066 | |
| Forward Transconductance[b] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 15 A | Ch-1 | | 60 | | S |
| | | $V_{DS}$ = 10 V, $I_D$ = 20 A | Ch-2 | | 100 | | |
| **Dynamic[a]** | | | | | | | |
| Input Capacitance | $C_{iss}$ | Channel-1<br>$V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz<br>Channel-2<br>$V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | Ch-1 | | 1300 | | pF |
| | | | Ch-2 | | 3860 | | |
| Output Capacitance | $C_{oss}$ | | Ch-1 | | 290 | | |
| | | | Ch-2 | | 760 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | Ch-1 | | 132 | | |
| | | | Ch-2 | | 350 | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $I_D$ = 15 A | Ch-1 | | 20 | 35 | nC |
| | | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $I_D$ = 20 A | Ch-2 | | 55 | 85 | |
| | | Channel-1<br>$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 15 A<br>Channel-2<br>$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 20 A | Ch-1 | | 9.5 | 15 | |
| | | | Ch-2 | | 27 | 45 | |
| Gate-Source Charge | $Q_{gs}$ | | Ch-1 | | 3.2 | | |
| | | | Ch-2 | | 9.2 | | |
| Gate-Drain Charge | $Q_{gd}$ | | Ch-1 | | 2.4 | | |
| | | | Ch-2 | | 7.1 | | |
| Gate Resistance | $R_g$ | f = 1 MHz | Ch-1 | 0.3 | 1.3 | 2.6 | Ω |
| | | | Ch-2 | 0.2 | 1 | 2 | |

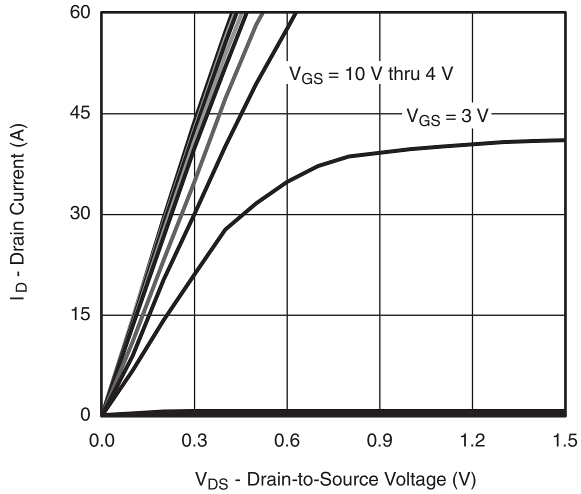
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Dynamic**[a] | | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | Channel-1<br>$V_{DD}$ = 10 V, $R_L$ = 10 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω<br><br>Channel-2<br>$V_{DD}$ = 10 V, $R_L$ = 10 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | Ch-1 | | 9 | 15 | ns |
| | | | Ch-2 | | 13 | 20 | |
| Rise Time | $t_r$ | | Ch-1 | | 8 | 15 | |
| | | | Ch-2 | | 8 | 15 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | Ch-1 | | 25 | 40 | |
| | | | Ch-2 | | 52 | 80 | |
| Fall Time | $t_f$ | | Ch-1 | | 8 | 15 | |
| | | | Ch-2 | | 15 | 25 | |
| Turn-On Delay Time | $t_{d(on)}$ | Channel-1<br>$V_{DD}$ = 10 V, $R_L$ = 10 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω<br><br>Channel-2<br>$V_{DD}$ = 10 V, $R_L$ = 10 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | Ch-1 | | 8 | 15 | |
| | | | Ch-2 | | 12 | 20 | |
| Rise Time | $t_r$ | | Ch-1 | | 9 | 15 | |
| | | | Ch-2 | | 8 | 15 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | Ch-1 | | 25 | 40 | |
| | | | Ch-2 | | 47 | 75 | |
| Fall Time | $t_f$ | | Ch-1 | | 8 | 15 | |
| | | | Ch-2 | | 10 | 15 | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | Ch-1 | | | 14.7 | A |
| | | | Ch-2 | | | 16 | |
| Pulse Diode Forward Current[a] | $I_{SM}$ | | Ch-1 | | | 60 | |
| | | | Ch-2 | | | 60 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 2 A, $V_{GS}$ = 0 V | Ch-1 | | 0.8 | 1.2 | V |
| | | $I_S$ = 2.3 A, $V_{GS}$ = 0 V | Ch-2 | | 0.8 | 1.2 | |
| Body Diode Reverse Recovery Time | $t_{rr}$ | Channel-1<br>$I_F$ = 2 A, dI/dt = 100 A/µs, $T_J$ = 25 °C<br><br>Channel-2<br>$I_F$ = 2.3 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | Ch-1 | | 25 | 50 | ns |
| | | | Ch-2 | | 40 | 80 | |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | Ch-1 | | 13 | 25 | nC |
| | | | Ch-2 | | 31 | 60 | |
| Reverse Recovery Fall Time | $t_a$ | | Ch-1 | | 12 | | ns |
| | | | Ch-2 | | 21 | | |
| Reverse Recovery Rise Time | $t_b$ | | Ch-1 | | 13 | | |
| | | | Ch-2 | | 19 | | |

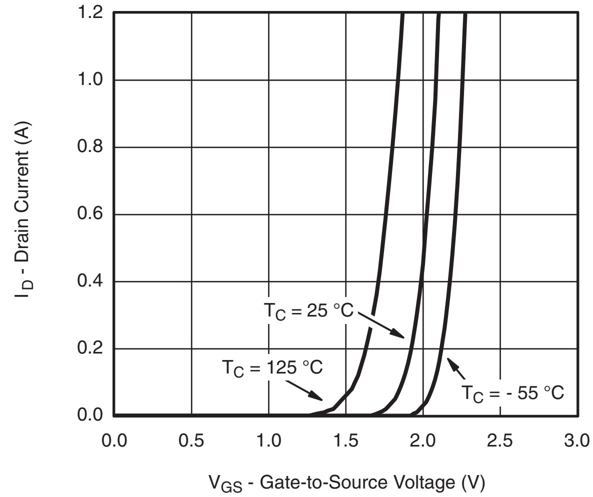
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

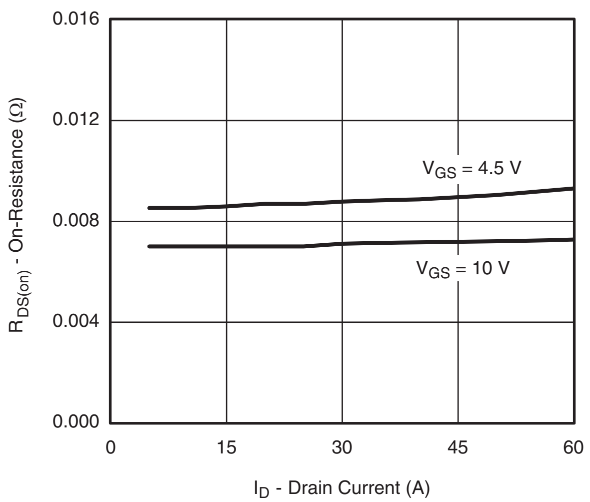
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



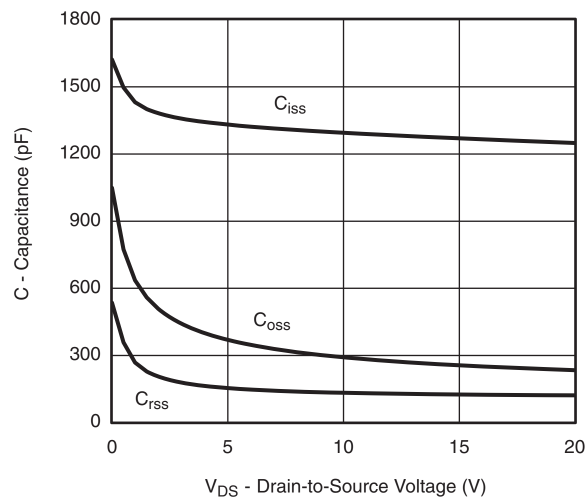

**Output Characteristics**



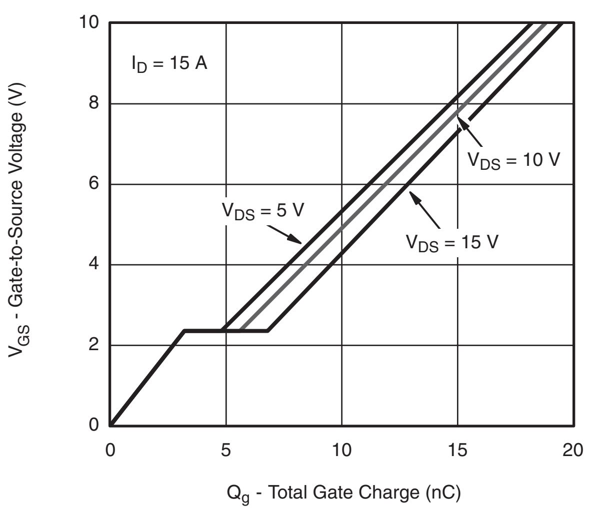

**Transfer Characteristics**



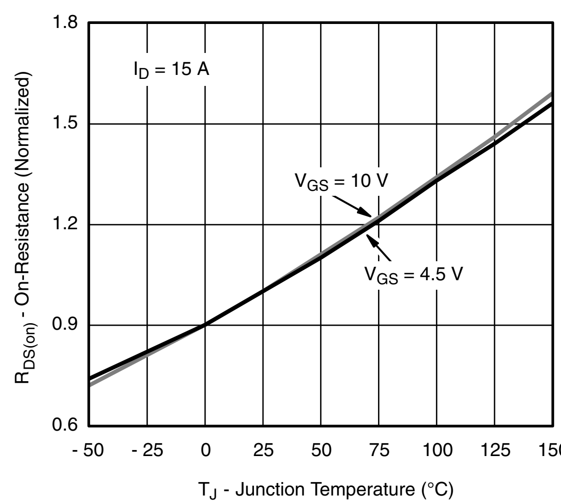

**On-Resistance vs. Drain Current**




**Capacitance**

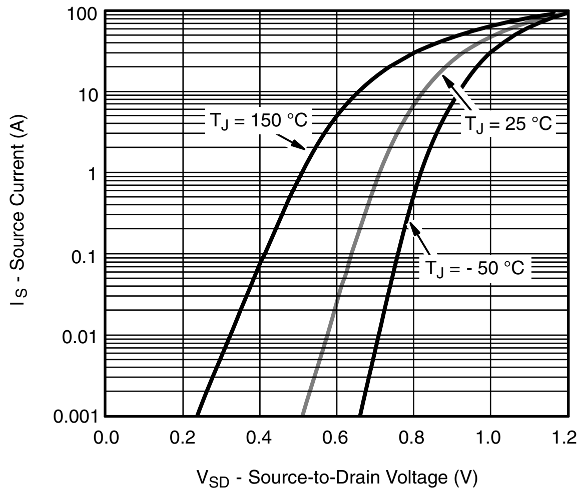



**Gate Charge**

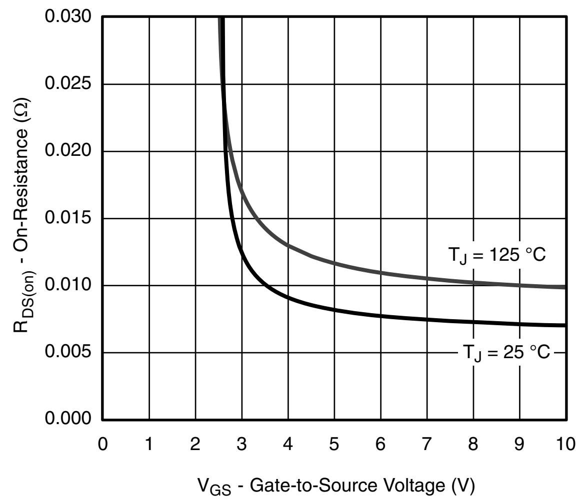



**On-Resistance vs. Junction Temperature**

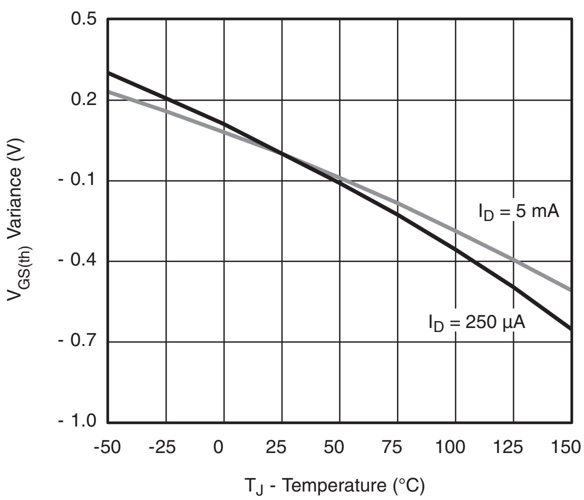
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



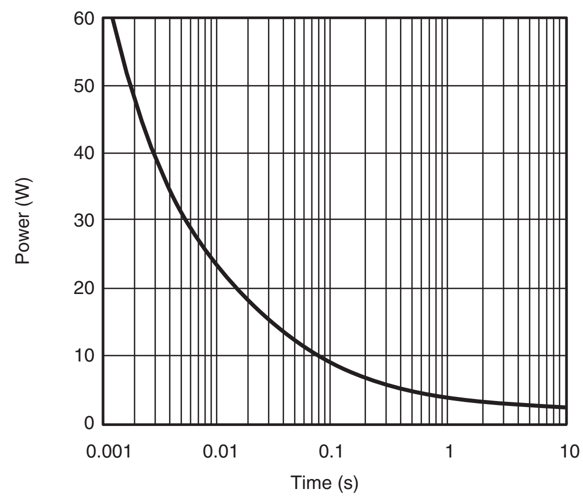

**Source-Drain Diode Forward Voltage**



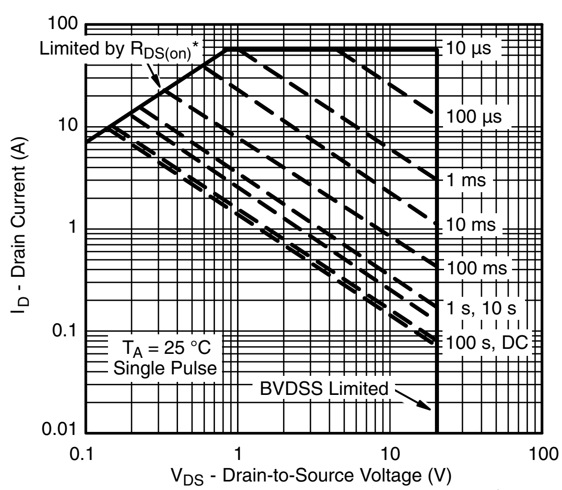

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**



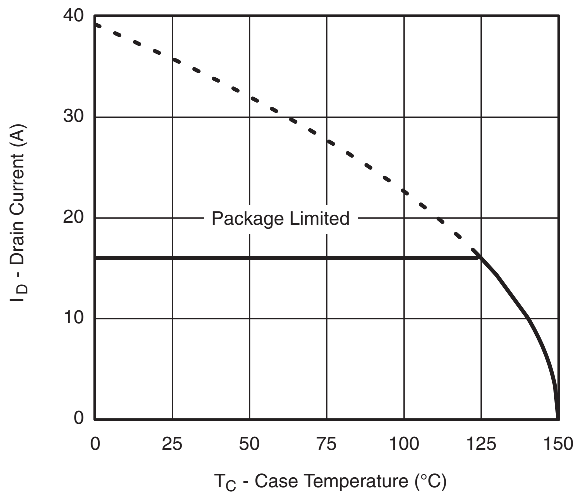

**Single Pulse Power**



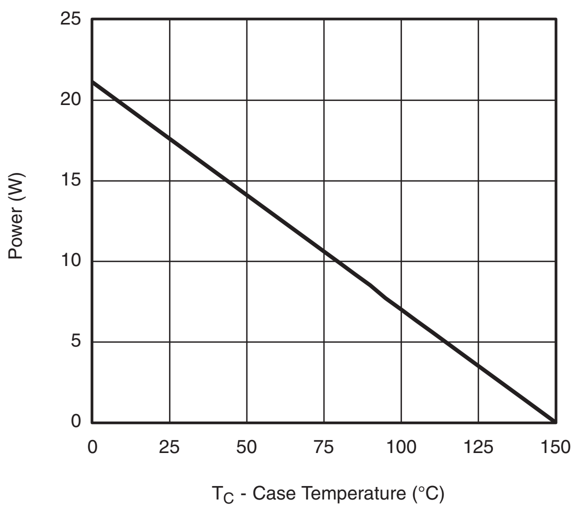

* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area, Junction-to-Ambient**

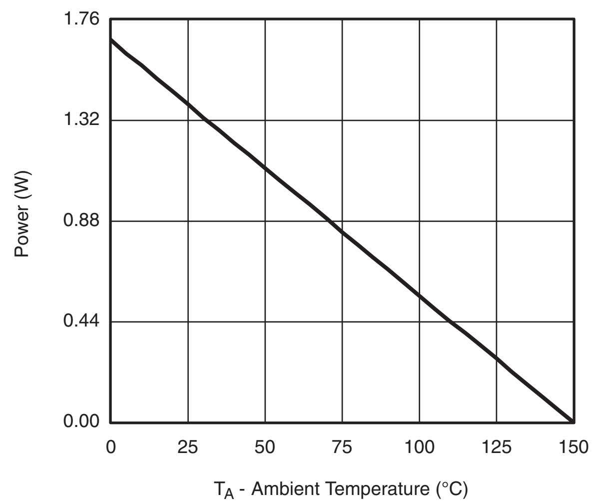
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




**Current Derating***



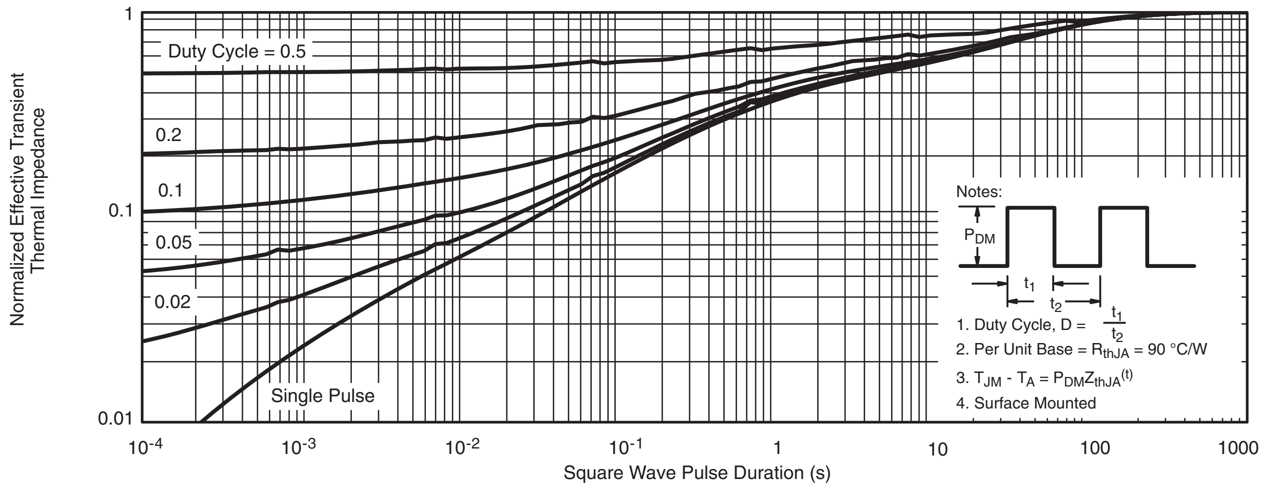

**Power, Junction-to-Case**



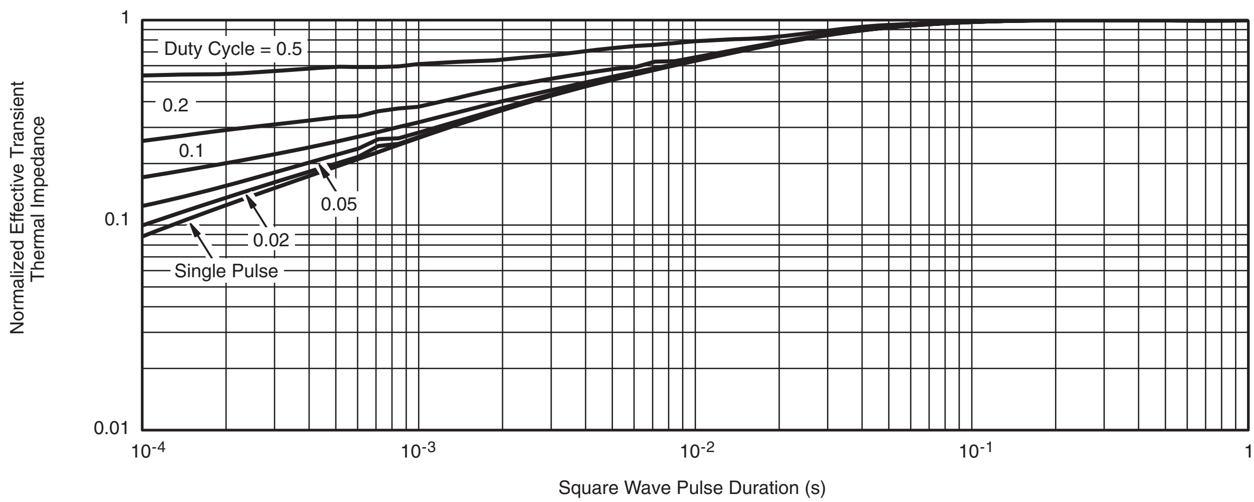

**Power, Junction-to-Ambient**

* The power dissipation $P_D$ is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

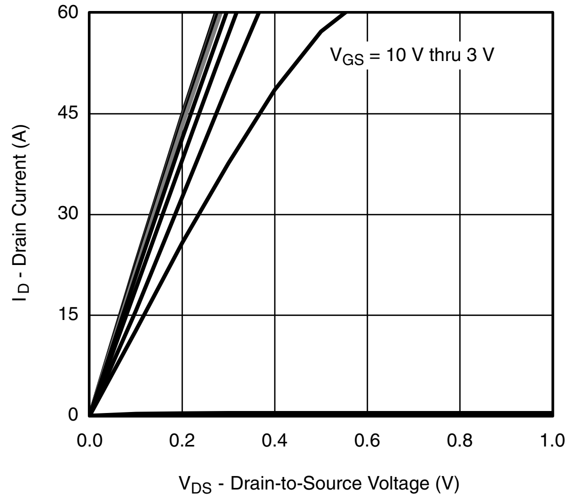



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

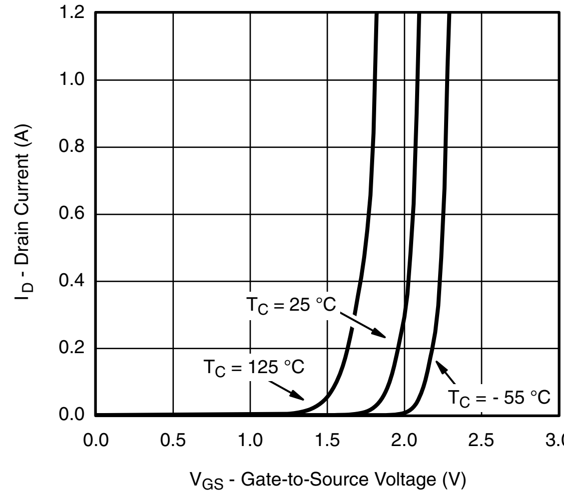



**Normalized Thermal Transient Impedance, Junction-to-Case**

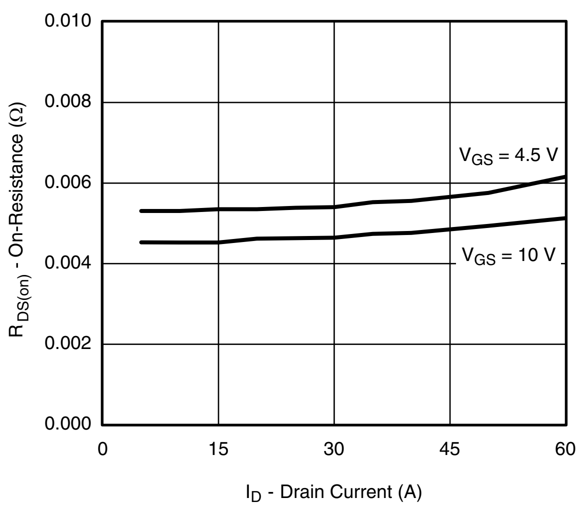
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



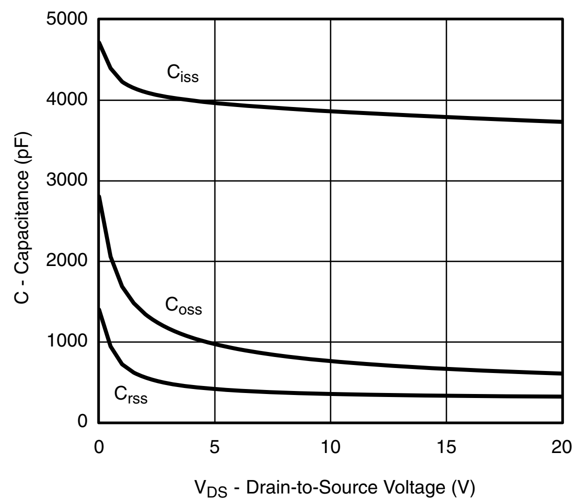

**Output Characteristics**



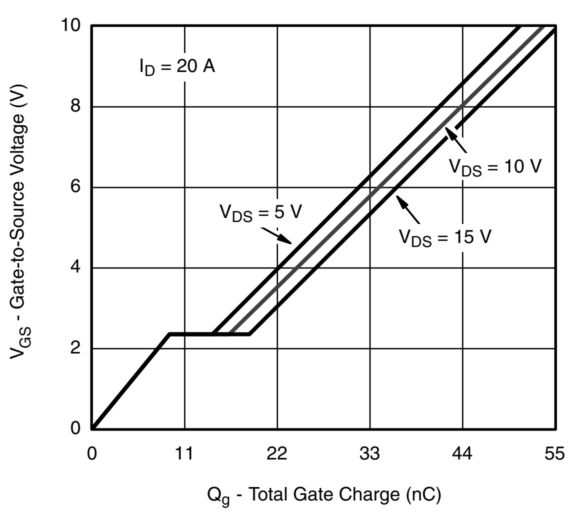

**Transfer Characteristics**



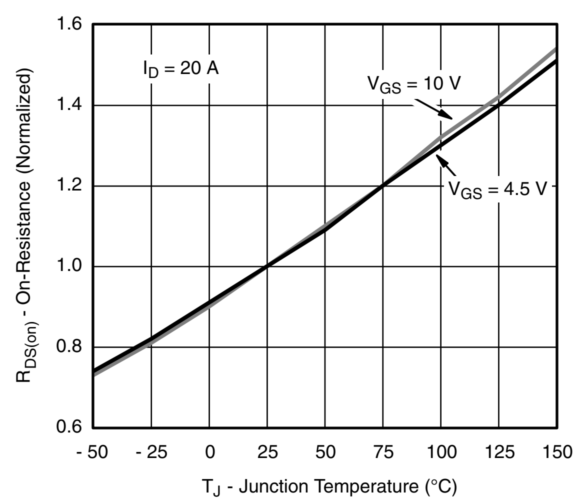

**On-Resistance vs. Drain Current**




**Capacitance**

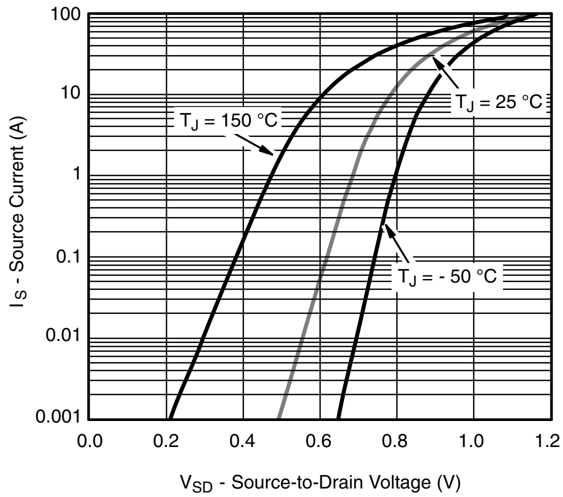



**Gate Charge**

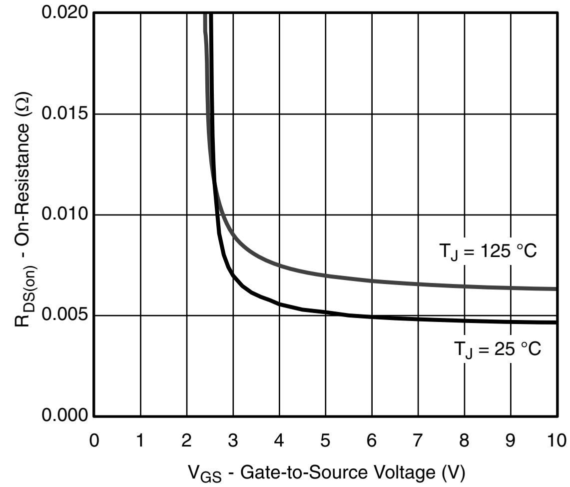



**On-Resistance vs. Junction Temperature**

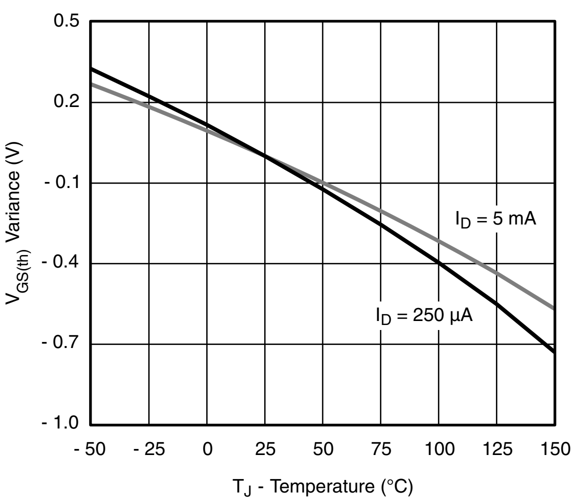
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



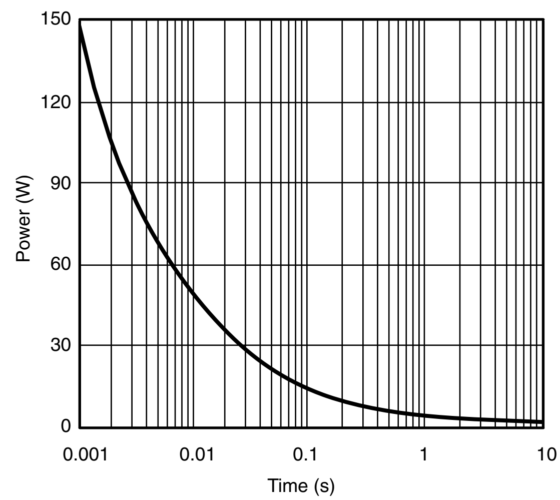

**Source-Drain Diode Forward Voltage**



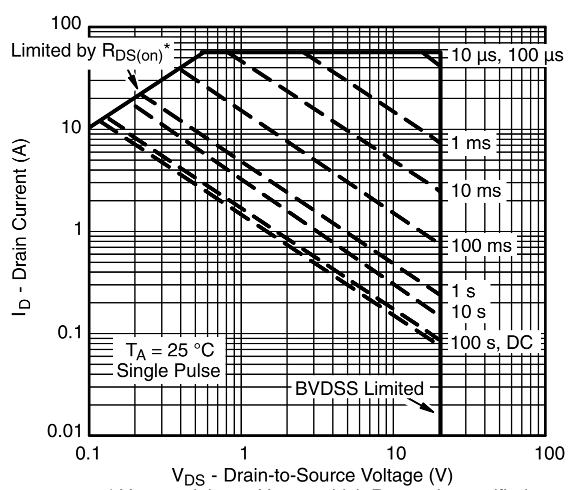

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**



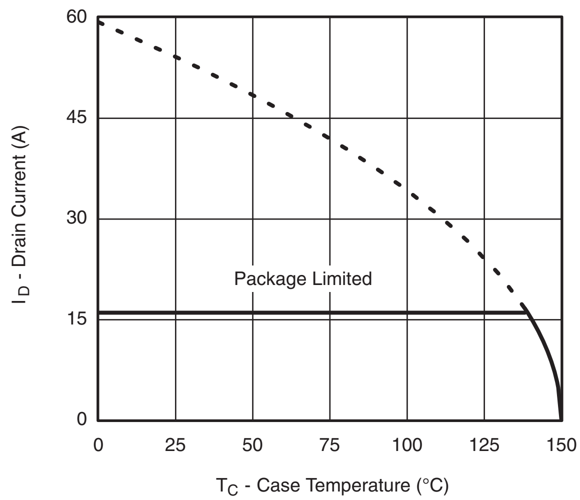

**Single Pulse Power**



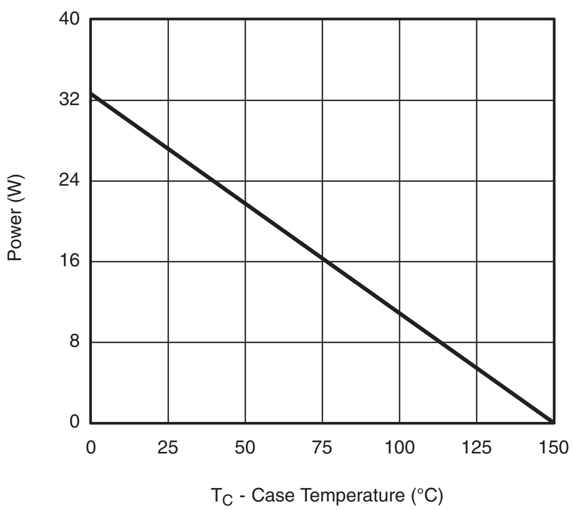

* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area, Junction-to-Ambient**

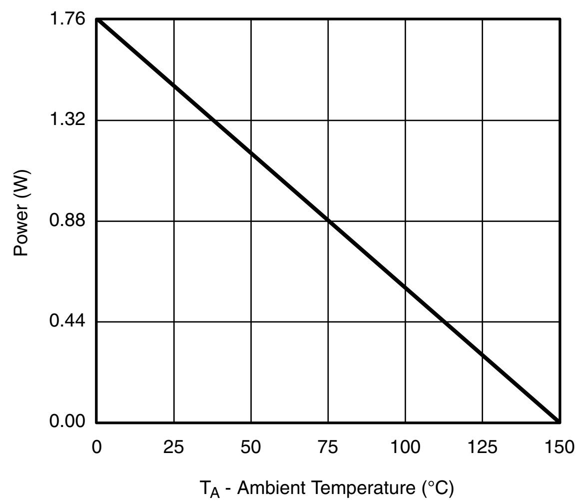
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating***



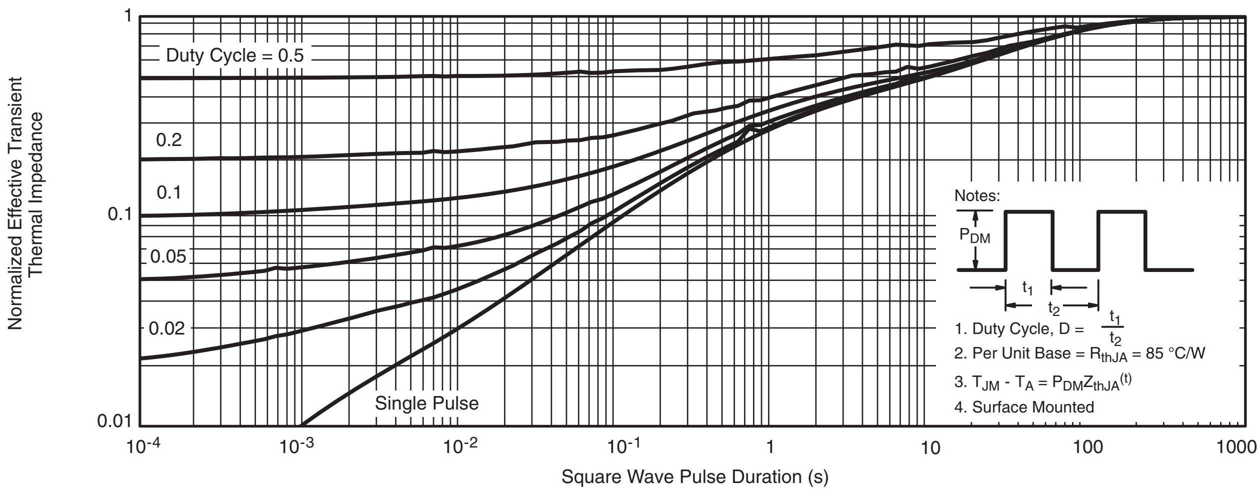

**Power, Junction-to-Case**



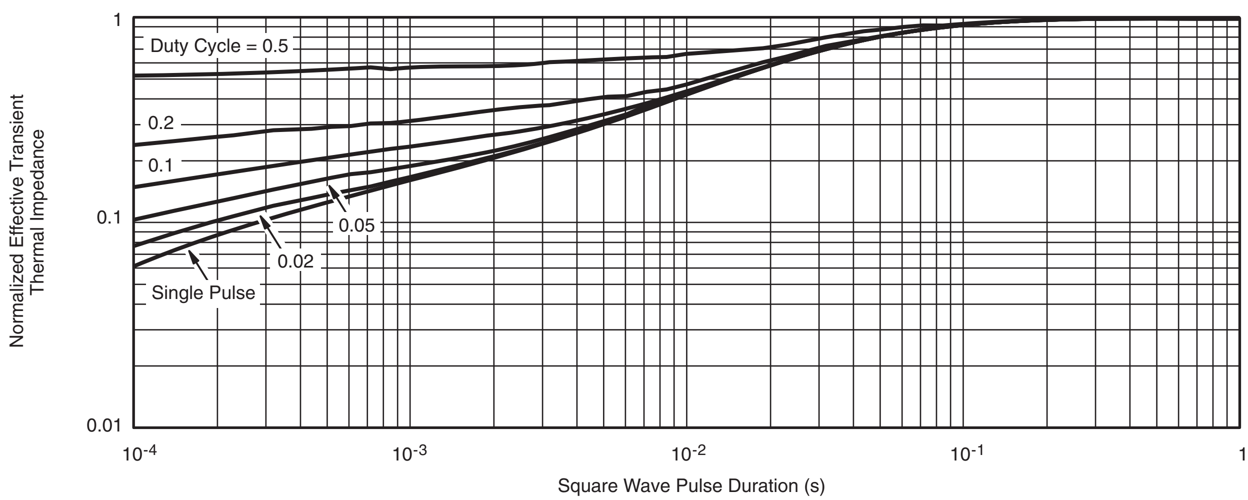

**Power, Junction-to-Ambient**

* The power dissipation $P_D$ is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



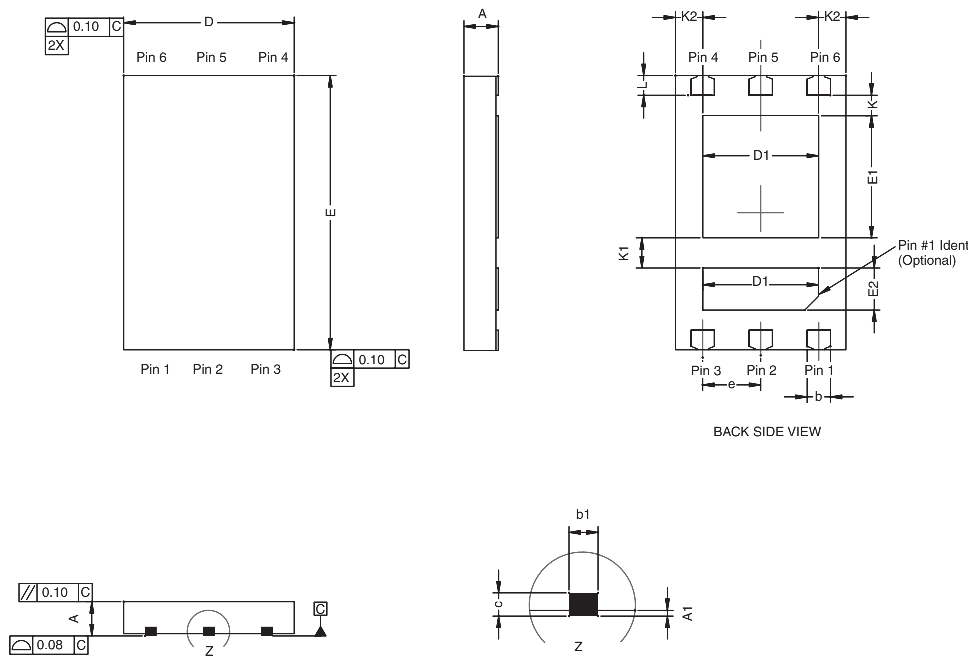

**Normalized Thermal Transient Impedance, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Case**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69090.*

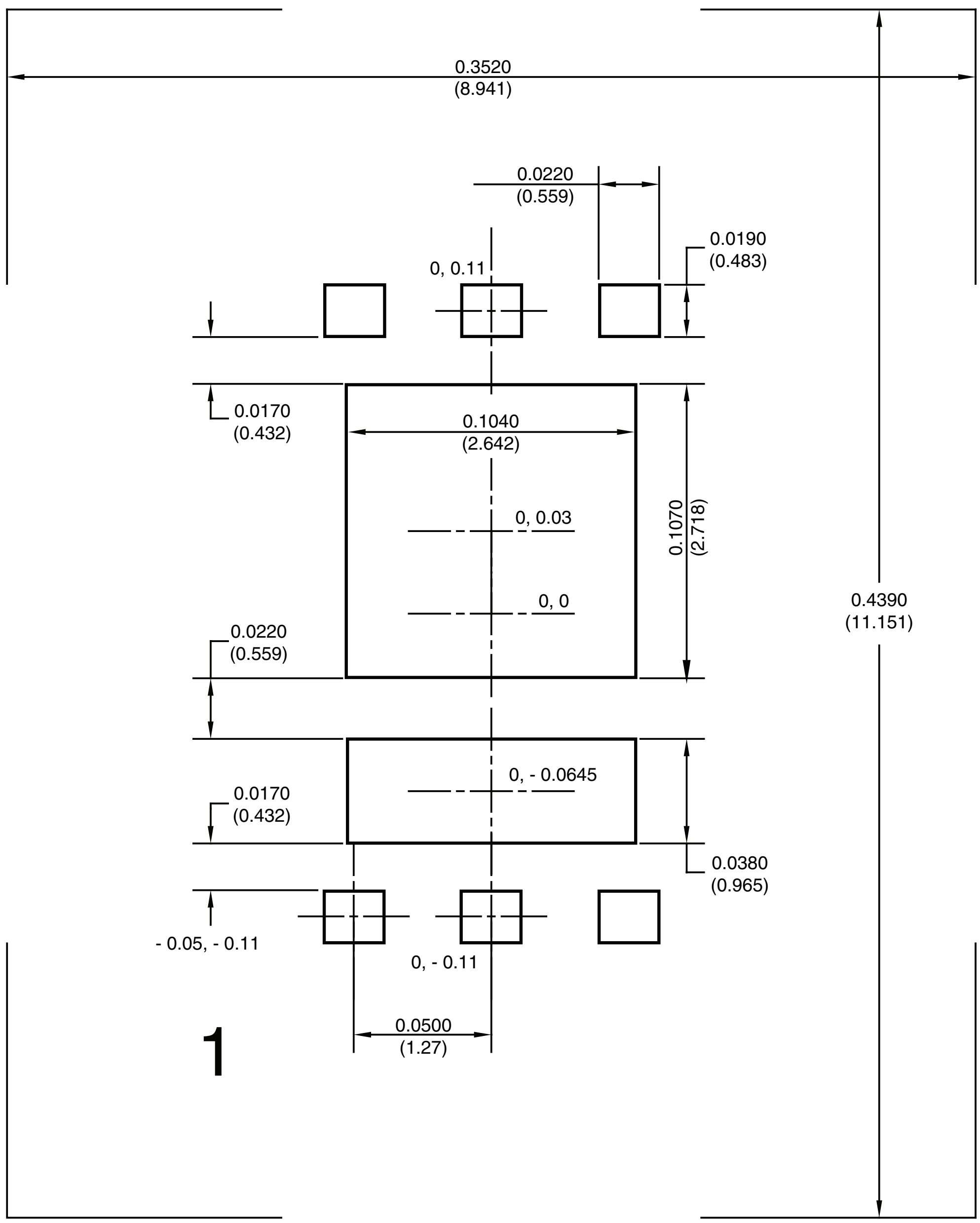
## PowerPAIR™ 6 x 3.7 CASE OUTLINE




| DIM. | MILLIMETERS MIN. | MILLIMETERS NOM. | MILLIMETERS MAX. | INCHES MIN. | INCHES NOM. | INCHES MAX. |
|---|---|---|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.032 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| b | 0.46 | 0.51 | 0.56 | 0.018 | 0.020 | 0.022 |
| b1 | 0.20 | 0.25 | 0.38 | 0.008 | 0.010 | 0.015 |
| C | 0.18 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| D | 3.65 | 3.73 | 3.81 | 0.144 | 0.147 | 0.150 |
| D1 | 2.41 | 2.53 | 2.65 | 0.095 | 0.100 | 0.104 |
| E | 5.92 | 6.00 | 6.08 | 0.233 | 0.236 | 0.239 |
| E1 | 2.62 | 2.67 | 2.72 | 0.103 | 0.105 | 0.107 |
| E2 | 0.87 | 0.92 | 0.97 | 0.034 | 0.036 | 0.038 |
| e | 1.27 BSC | | | 0.05 BSC | | |
| K | 0.45 TYP. | | | 0.018 TYP. | | |
| K1 | 0.66 TYP. | | | 0.026 TYP. | | |
| K2 | 0.60 TYP. | | | 0.024 TYP. | | |
| L | 0.38 | 0.43 | 0.48 | 0.015 | 0.017 | 0.019 |

ECN: S-82772-Rev. B, 17-Nov-08
DWG: 5979

**RECOMMENDED PAD FOR PowerPAIR™ 6 x 3.7**




Recommended PAD for PowerPAIR 6 x 3.7
Dimensions in inches (mm)
Keep-out 0.3520 (8.94) x 0.4390 (11.151)

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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