Complementary Low-Threshold MOSFET Pair

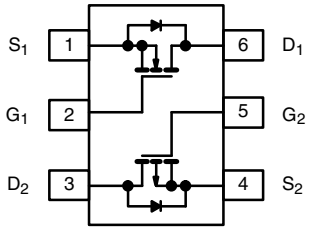
PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.385 at V_{GS} = 4.5 V	0.70
		0.630 at V_{GS} = 2.5 V	0.54
P-Channel	- 8	0.600 at V_{GS} = - 4.5 V	- 0.60
		0.850 at V_{GS} = - 2.5 V	- 0.50
		1.200 at V_{GS} = - 1.8 V	- 0.42

FEATURES

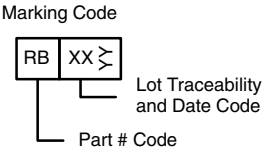
- TrenchFET® Power MOSFET
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

SOT-363
SC-70 (6-LEADS)



Top View



Ordering Information: Si1555DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)							
Parameter		Symbol	N-Channel		P-Channel		Unit
			5 s	Steady State	5 s	Steady State	
Drain-Source Voltage		V_{DS}	20		- 8		V
Gate-Source Voltage		V_{GS}	± 12		± 8		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	± 0.70	± 0.66	- 0.60	- 0.57	A
	T_A = 85 °C		± 0.50	± 0.48	- 0.43	- 0.41	
Pulsed Drain Current		I_{DM}	± 1				
Continuous Source Current (Diode Conduction)[a]		I_S	0.25	0.23	- 0.25	- 0.23	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	0.30	0.27	0.30	0.27	W
	T_A = 85 °C		0.16	0.14	0.16	0.14	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	360	415	°C/W
	Steady State		400	460	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	300	350	

Note:
a. Surface mounted on 1" x 1" FR4 board.

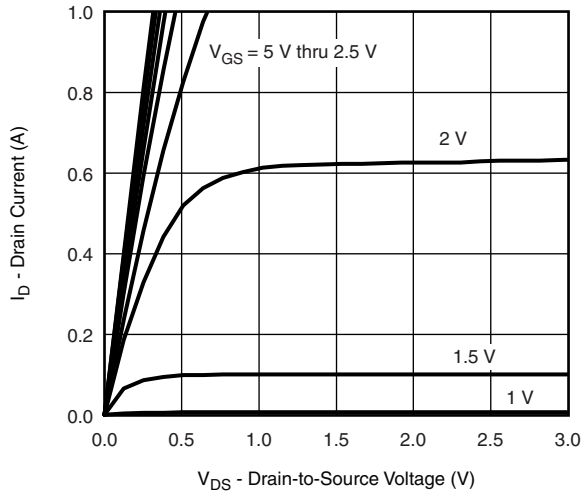
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.6		1.4	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	- 0.45		- 1	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	N-Ch			± 100	nA
		V_{DS} = 0 V, V_{GS} = ± 8 V	P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 8 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 85 °C	N-Ch			5	
		V_{DS} = - 8 V, V_{GS} = 0 V, T_J = 85 °C	P-Ch			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	N-Ch	1			A
		$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	P-Ch	- 1			
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.66 A	N-Ch		0.320	0.385	Ω
		V_{GS} = - 4.5 V, I_D = - 0.57 A	P-Ch		0.510	0.600	
		V_{GS} = 2.5 V, I_D = 0.40 A	N-Ch		0.560	0.630	
		V_{GS} = - 2.5 V, I_D = - 0.48 A	P-Ch		0.720	0.850	
		V_{GS} = - 1.8 V, I_D = - 0.20 A	P-Ch		1.000	1.200	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 0.66 A	N-Ch		1.5		S
		V_{DS} = - 4 V, I_D = - 0.57 A	P-Ch		1.2		
Diode Forward Voltage[a]	V_{SD}	I_S = 0.23 A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = - 0.23 A, V_{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 0.66 A P-Channel V_{DS} = - 4 V, V_{GS} = - 4.5 V, I_D = - 0.57 A	N-Ch		0.8	1.2	nC
			P-Ch		1.5	2.3	
Gate-Source Charge	Q_{gs}		N-Ch		0.06		
			P-Ch		0.17		
Gate-Drain Charge	Q_{gd}		N-Ch		0.30		
			P-Ch		0.16		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 20 Ω $I_D \cong$ 0.5 A, V_{GEN} = 4.5 V, R_g = 6 Ω P-Channel V_{DD} = - 4 V, R_L = 8 Ω $I_D \cong$ - 0.5 A, V_{GEN} = - 4.5 V, R_g = 6 Ω	N-Ch		10	20	ns
			P-Ch		6	12	
Rise Time	t_r		N-Ch		16	30	
			P-Ch		25	50	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		10	20	
			P-Ch		10	20	
Fall Time	t_f		N-Ch		10	20	
			P-Ch		10	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 0.23 A, dI/dt = 100 A/µs	N-Ch		20	40	
		I_F = - 0.23 A, dI/dt = 100 A/µs	P-Ch		20	40	

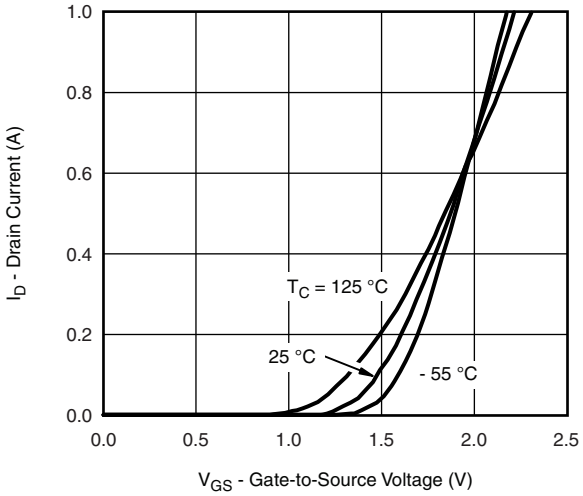
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

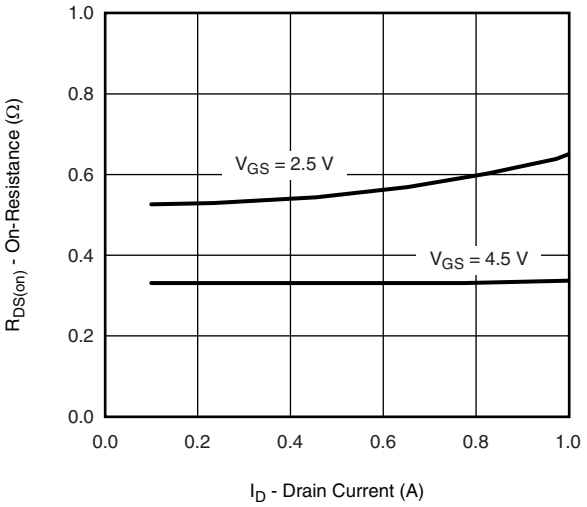
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



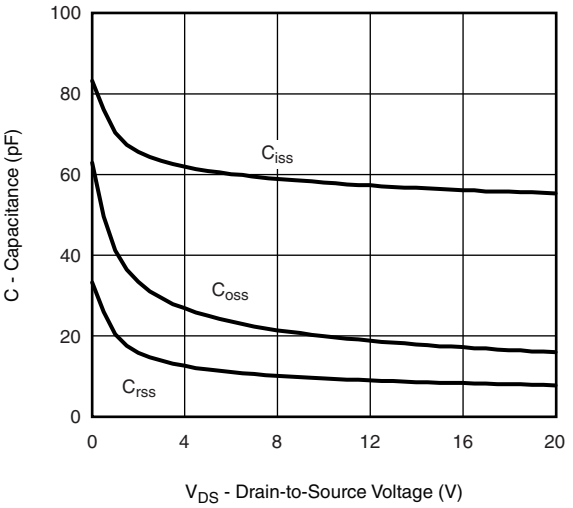
Output Characteristics



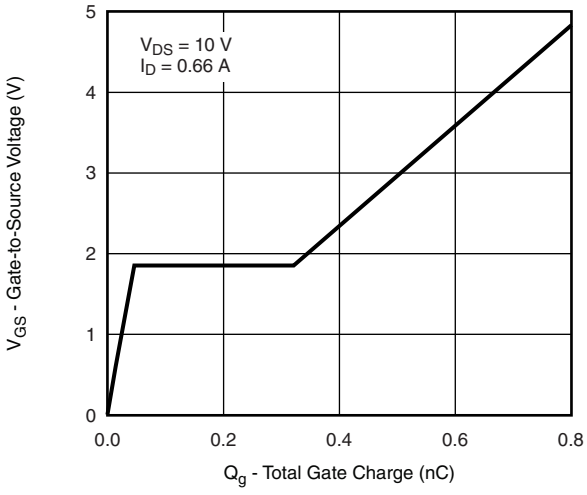
Transfer Characteristics



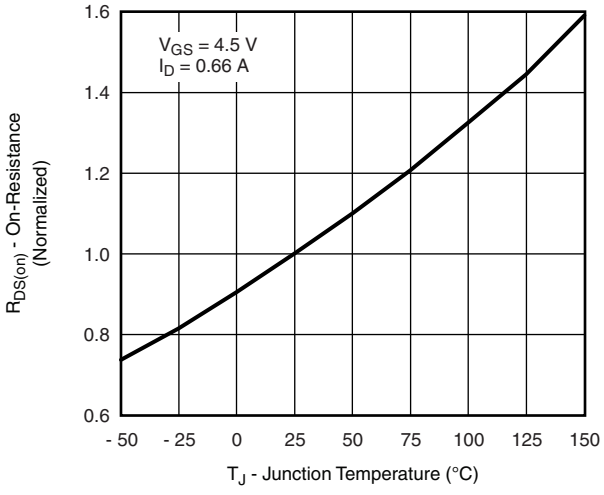
On-Resistance vs. Drain Current



Capacitance

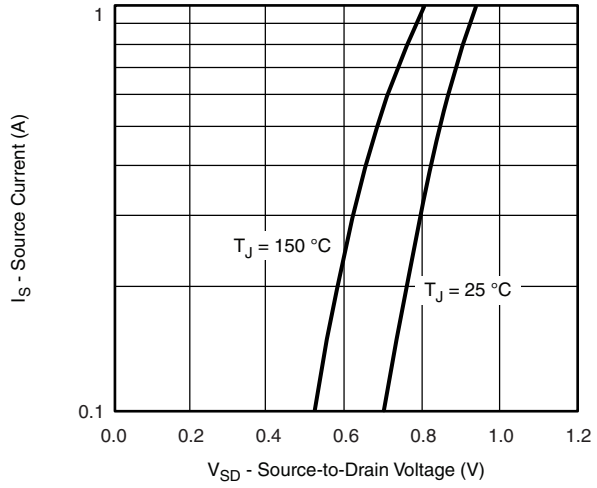


Gate Charge

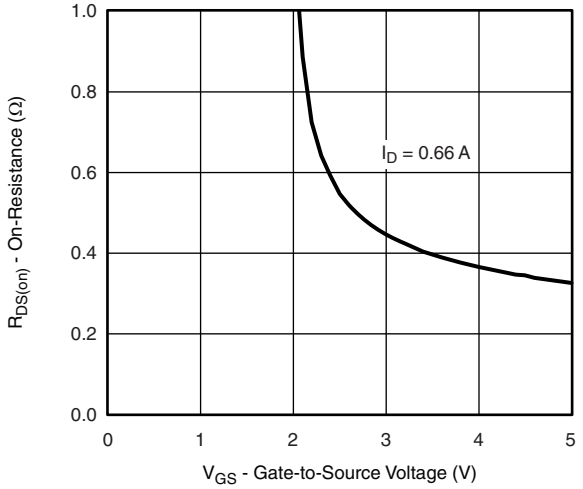


On-Resistance vs. Junction Temperature

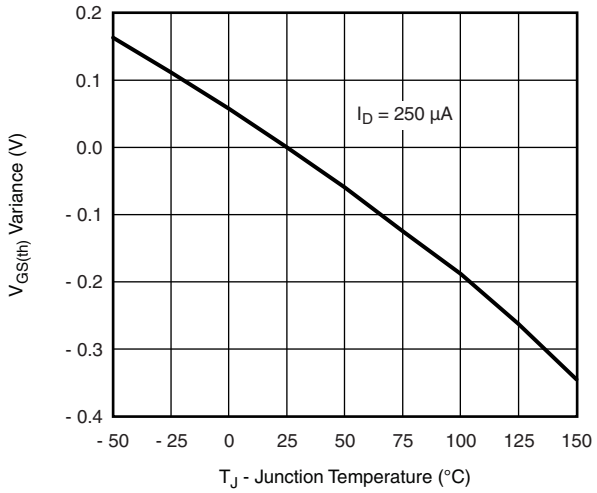
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



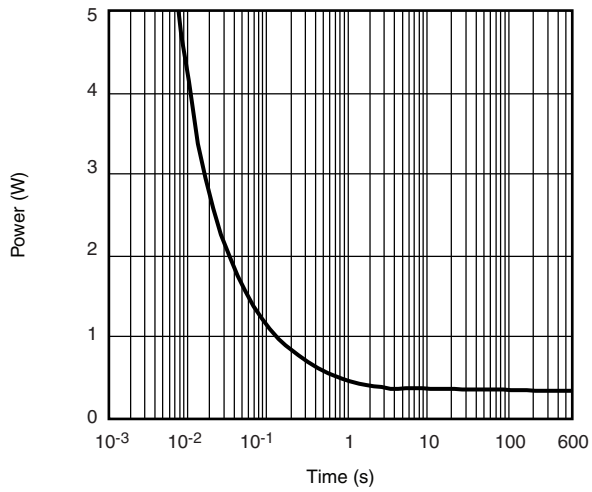
Source-Drain Diode Forward Voltage



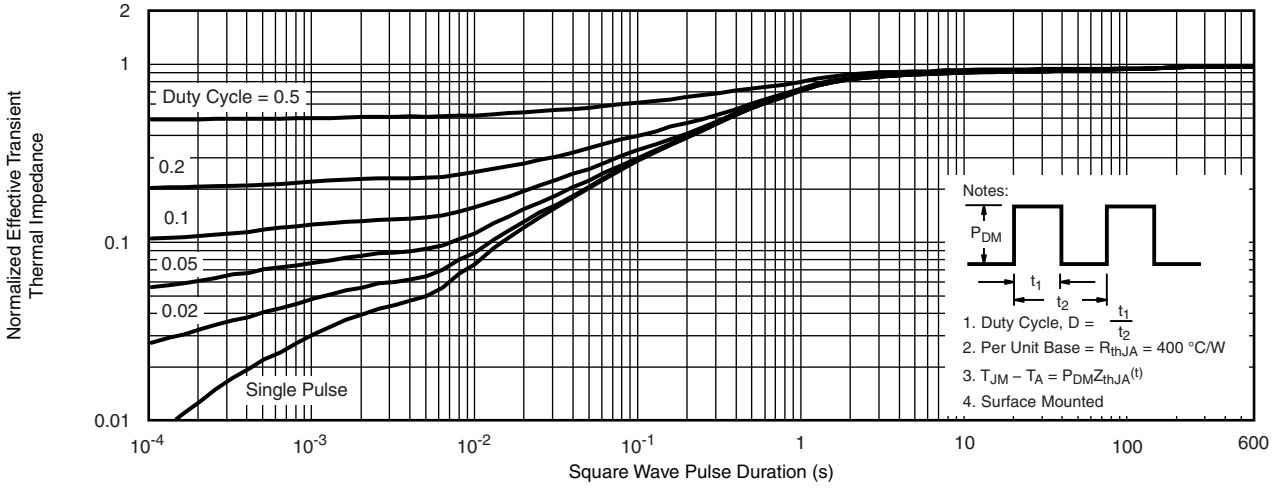
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



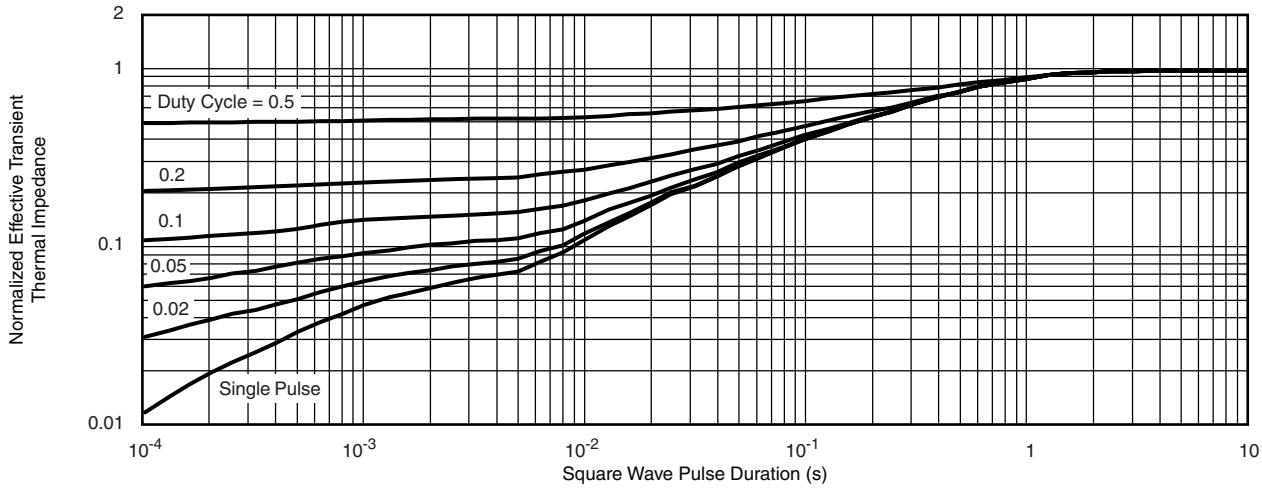
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

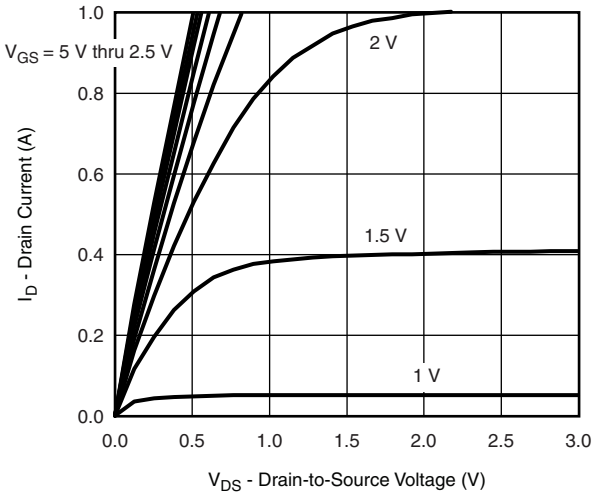
For technical questions, contact: pmostechsupport@vishay.com
Document Number: 71079
S13-0631-Rev. F, 25-Mar-13

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

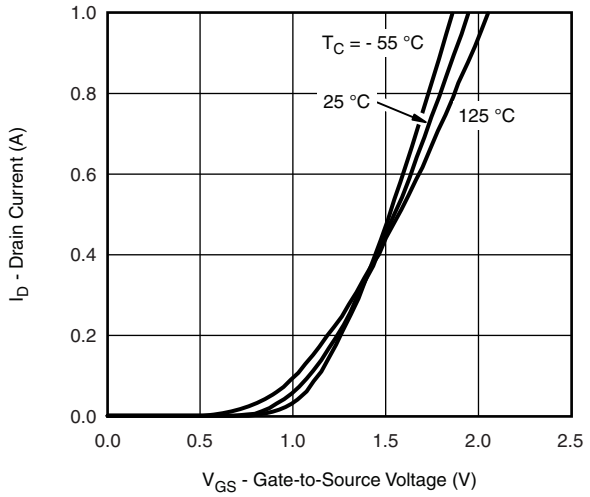


Normalized Thermal Transient Impedance, Junction-to-Foot

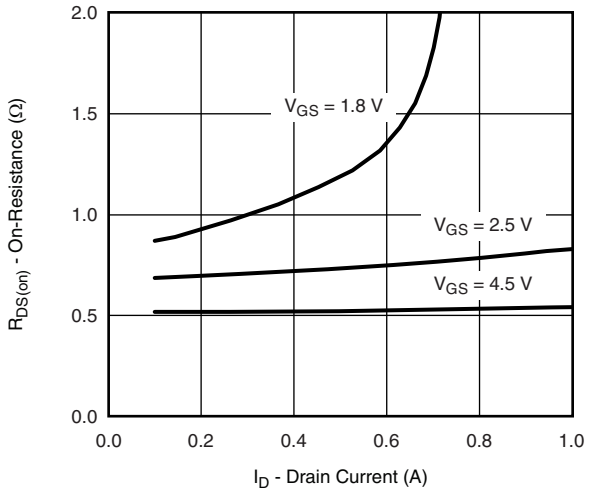
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



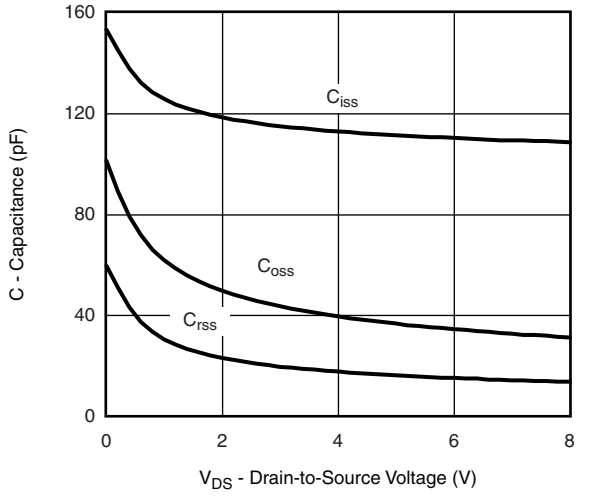
Output Characteristics



Transfer Characteristics

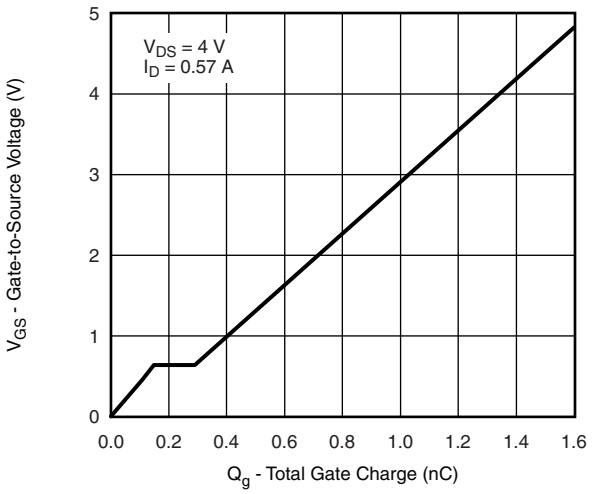


On-Resistance vs. Drain Current

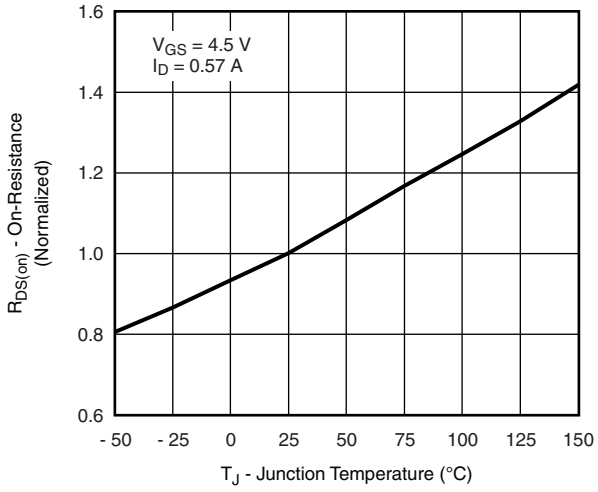


Capacitance

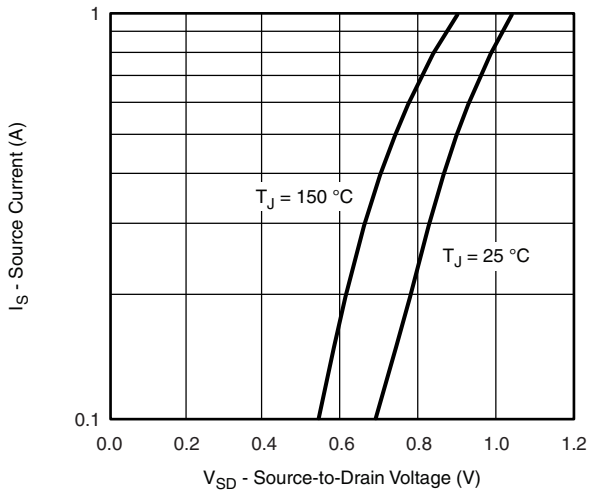
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



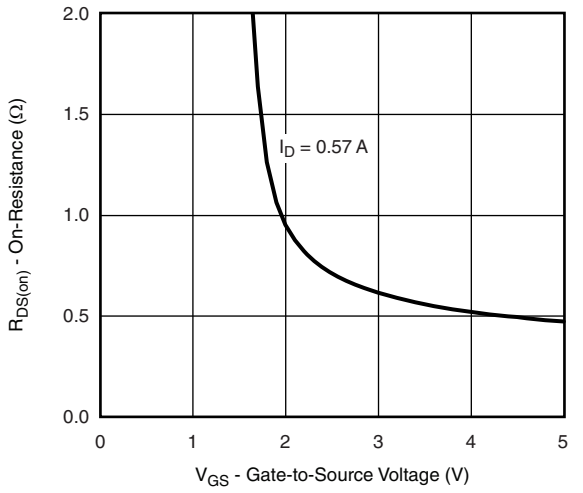
Gate Charge



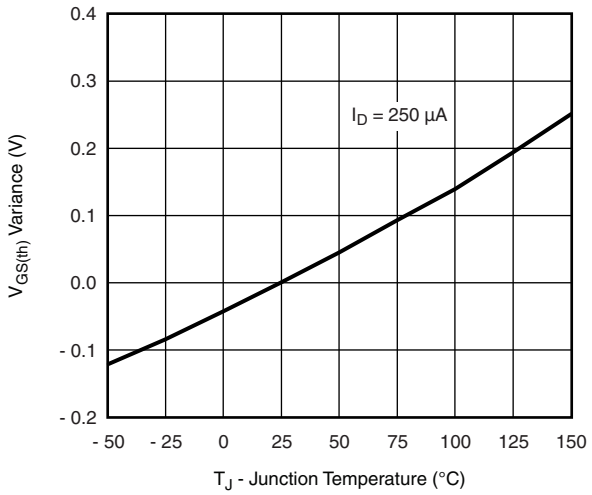
On-Resistance vs. Junction Temperature



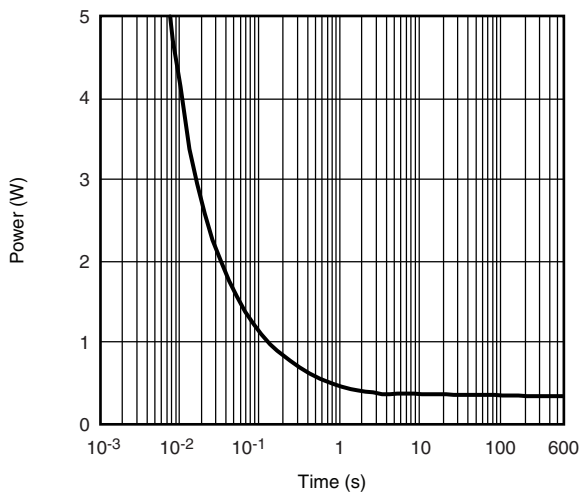
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



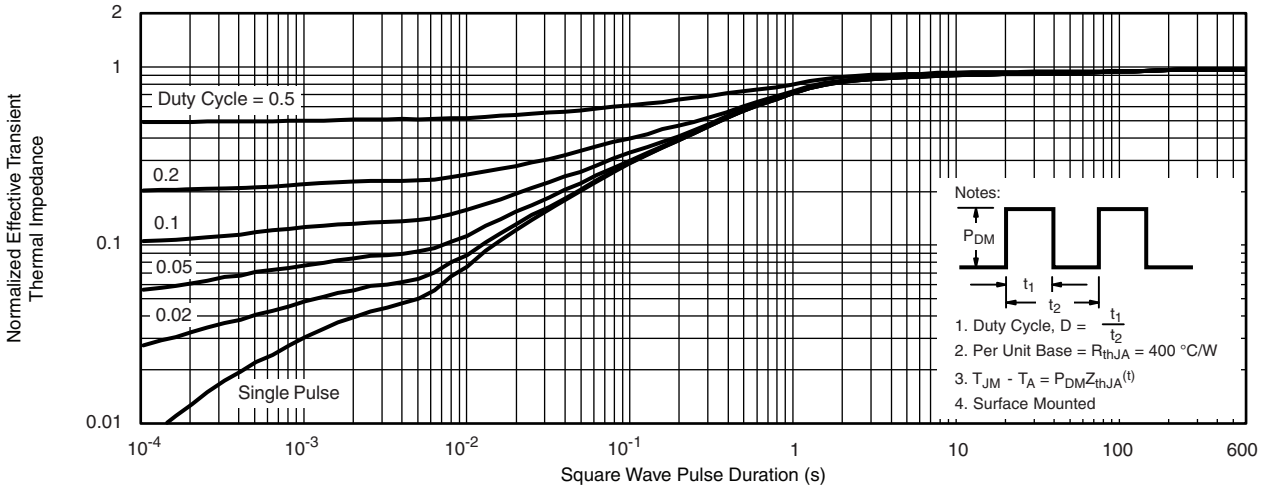
Threshold Voltage



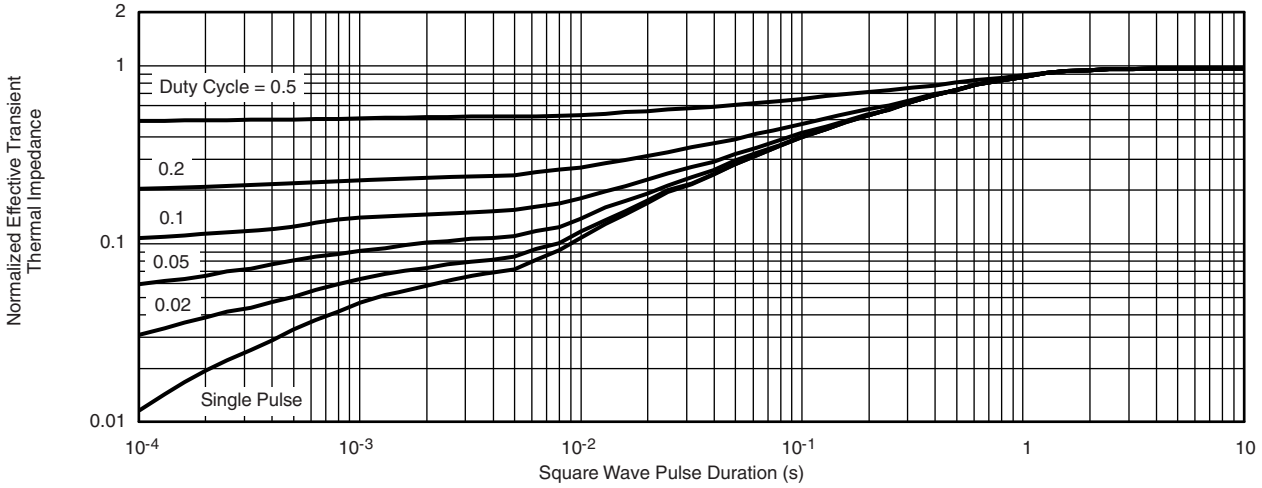
Single Pulse Power

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 71079
S13-0631-Rev. F, 25-Mar-13

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



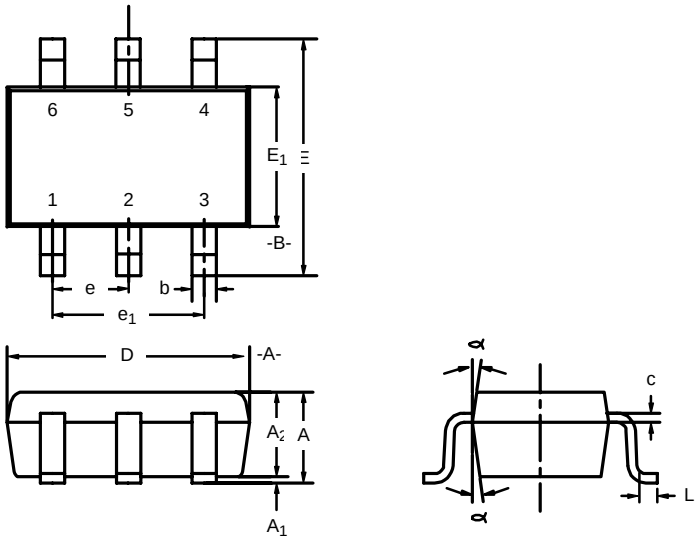
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71079.

SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.

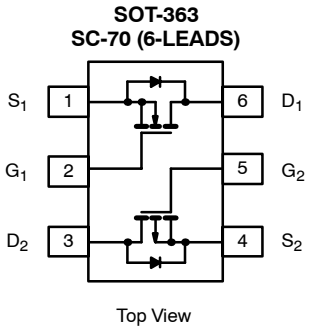


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The “foot” is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R\theta_{JA}$ for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

SC-70 (6-PIN)	
Room Ambient 25 °C	**Elevated Ambient 60 °C**
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150°C - 25°C}{400°C/W}$	$P_D = \frac{150°C - 60°C}{400°C/W}$
P_D = 312 mW	P_D = 225 mW

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

Testing

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of $R\theta_{JA}$ for the dual 6-pin SC-70 are as follows:

LITTLE FOOT SC-70 (6-PIN)	
1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518°C/W
2) Industry standard 1" square PCB with maximum copper both sides.	413°C/W

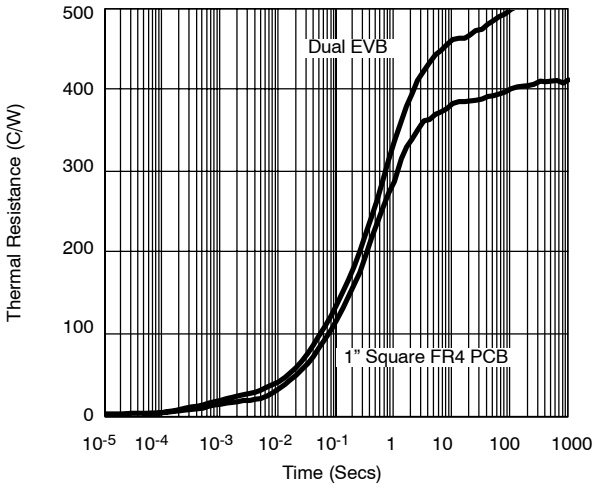


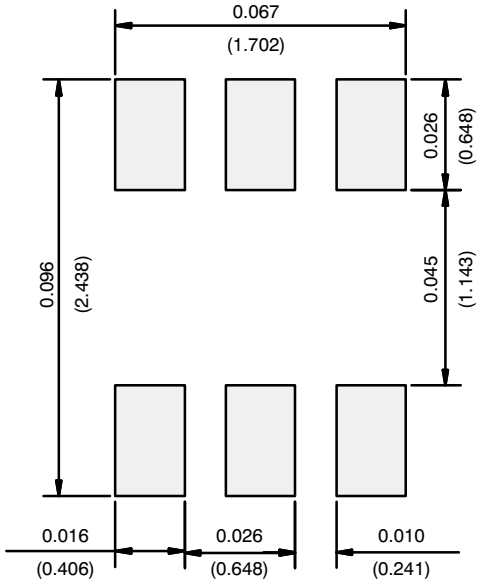
FIGURE 2. Comparison of Dual SC70-6 on EVB and 1" Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

ASSOCIATED DOCUMENT

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (http://www.vishay.com/doc?71334).

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.