

Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE
Available

PRODUCT SUMMARY		
V_{DS} (V)	-60	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.50
Q_g (Max.) (nC)	12	
Q_{gs} (nC)	3.8	
Q_{gd} (nC)	5.1	
Configuration	Single	

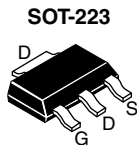
FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

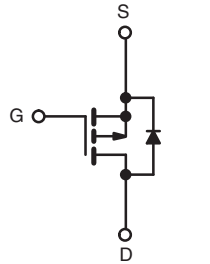
DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.



Marking code: FE



P-Channel MOSFET

ORDERING INFORMATION		
Package	SOT-223	SOT-223
Lead (Pb)-free and Halogen-free	SiHFL9014-GE3	SiHFL9014TR-GE3
Lead (Pb)-free	IRFL9014PbF	IRFL9014TRPbF ^a
	SiHFL9014-E3	SiHFL9014T-E3 ^a

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25$ °C	-1.8
		$T_C = 100$ °C	-1.1
Pulsed Drain Current ^a	I_{DM}	-14	A
Linear Derating Factor		0.025	
Linear Derating Factor (PCB Mount) ^e		0.017	
Single Pulse Avalanche Energy ^b	E_{AS}	140	mJ
Repetitive Avalanche Current ^a	I_{AR}	-1.8	A
Repetitive Avalanche Energy ^a	E_{AR}	0.31	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	3.1
		$T_A = 25$ °C	2.0
Maximum Power Dissipation (PCB Mount) ^e			W
Peak Diode Recovery dV/dt ^c	dV/dt	-4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s	300	

Notes

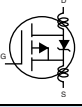

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = -25$ V, starting $T_J = 25$ °C, $L = 50$ mH, $R_g = 25$ Ω , $I_{AS} = -1.8$ A (see fig. 12).
 c. $I_{SD} \leq -6.7$ A, $di/dt \leq 90$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
 d. 1.6 mm from case.
 e. When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R _{thJA}	-	60	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

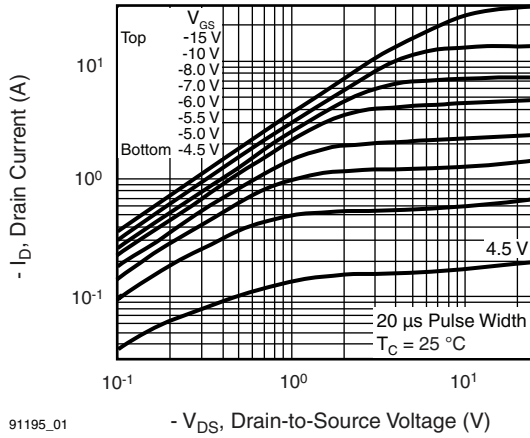
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		-60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	-0.059	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = -48 V, V _{GS} = 0 V, T _J = 125 °C		-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = 1.1 A ^b	-	-	0.50	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 25 V, I _D = 1.1 A ^b		1.3	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	270	-	pF
Output Capacitance	C _{oss}			-	170	-	
Reverse Transfer Capacitance	C _{rss}			-	31	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 6.7 A, V _{DS} = - 48 V, see fig. 6 and 13 ^b	-	-	12	nC
Gate-Source Charge	Q _{gs}			-	-	3.8	
Gate-Drain Charge	Q _{gd}			-	-	5.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 30 V, I _D = - 6.7 A, R _g = 24 Ω, R _D = 4.0 Ω, see fig. 10 ^b		-	11	-	ns
Rise Time	t _r			-	63	-	
Turn-Off Delay Time	t _{d(off)}			-	9.6	-	
Fall Time	t _f			-	31	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.8	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 14	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 1.8 A, V _{GS} = 0 V ^b		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 6.7 A, di/dt = 100 A/μs ^b		-	80	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.096	0.19	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

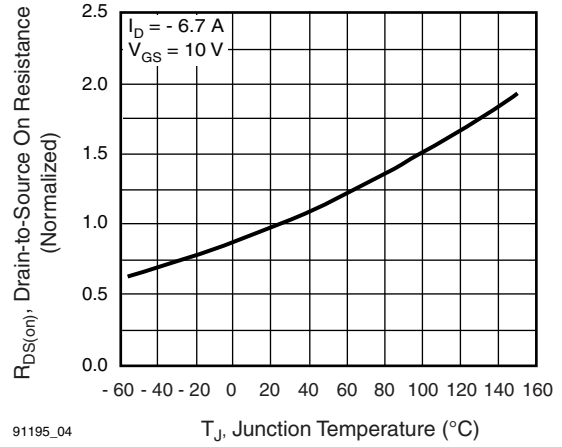


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



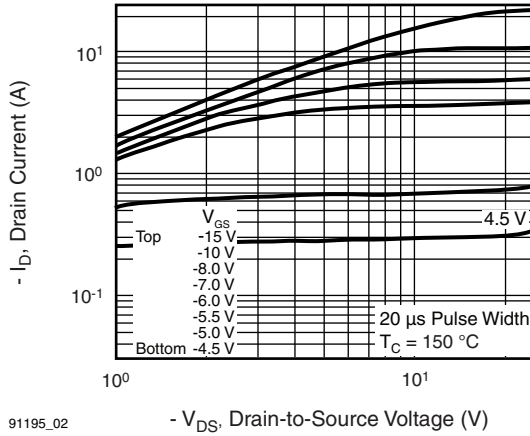
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Fig. 1 - Typical Output Characteristics, T_C = 25 °C



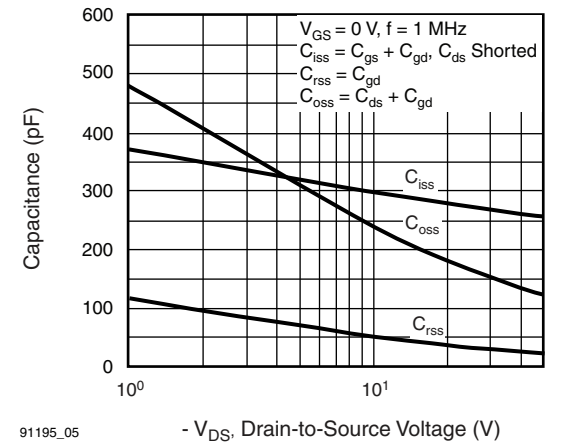
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Fig. 4 - Normalized On-Resistance vs. Temperature



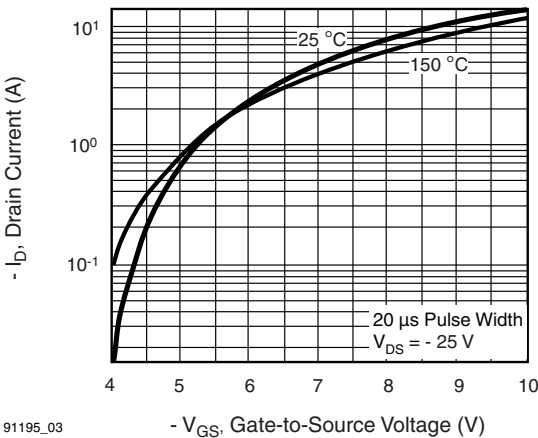
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Fig. 2 - Typical Output Characteristics, T_C = 150 °C



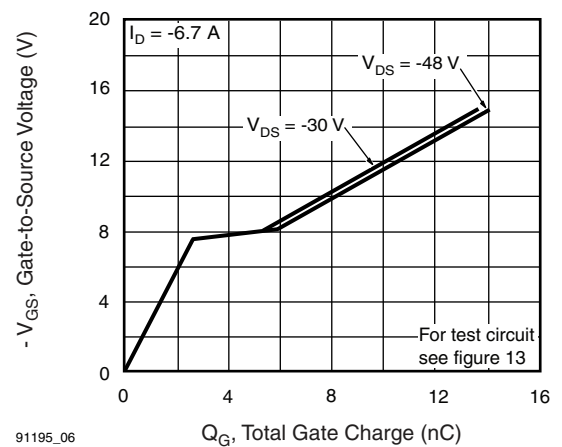
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



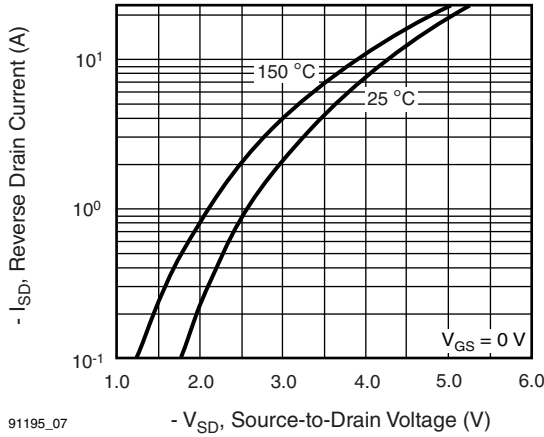
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Fig. 3 - Typical Transfer Characteristics



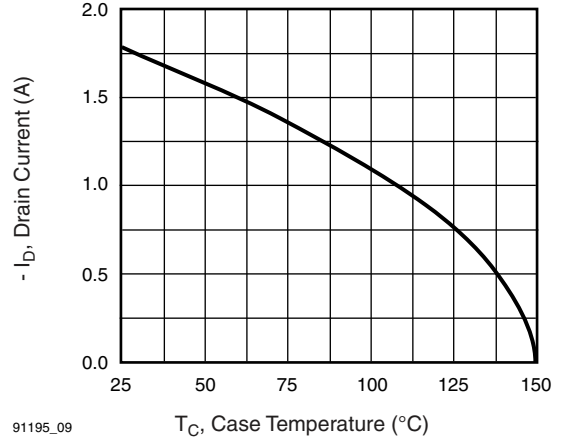
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



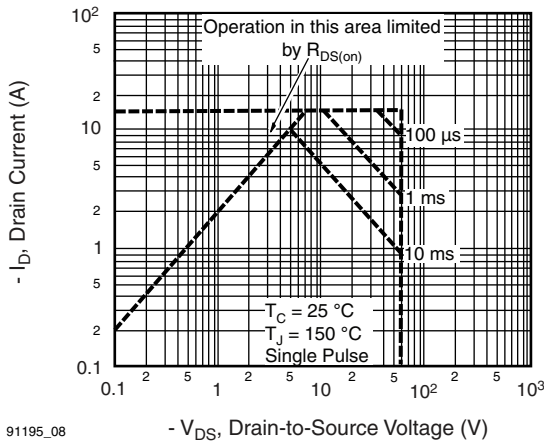
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

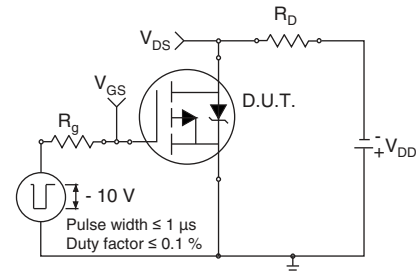


Fig. 10a - Switching Time Test Circuit

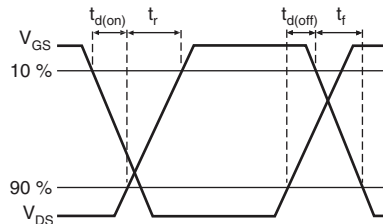
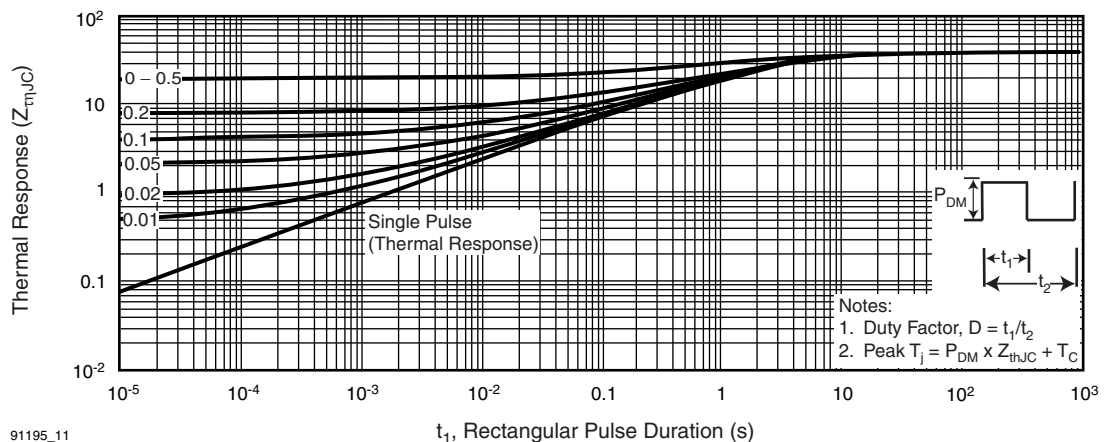


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

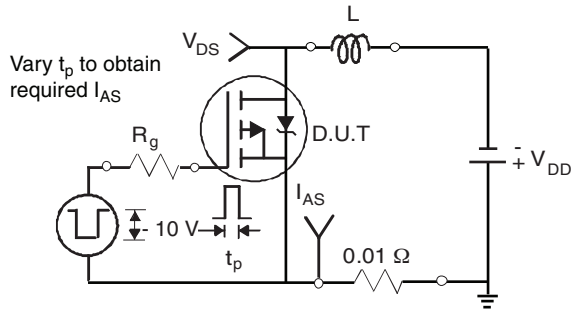


Fig. 12a - Unclamped Inductive Test Circuit

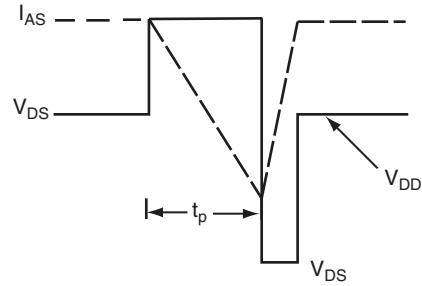


Fig. 12b - Unclamped Inductive Waveforms

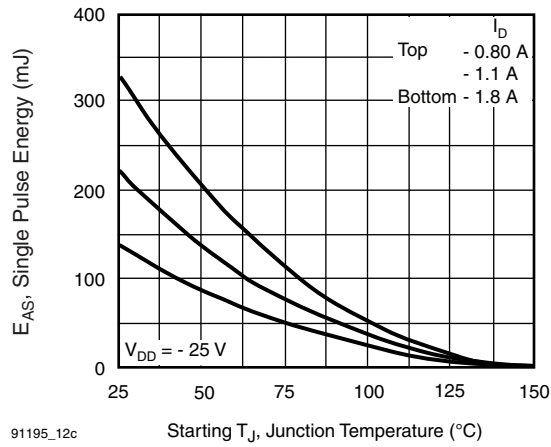


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

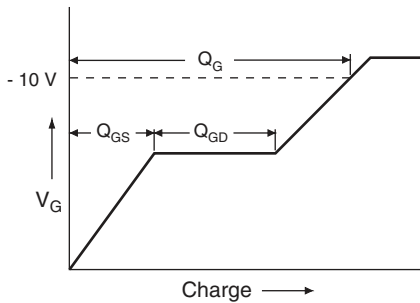


Fig. 13a - Basic Gate Charge Waveform

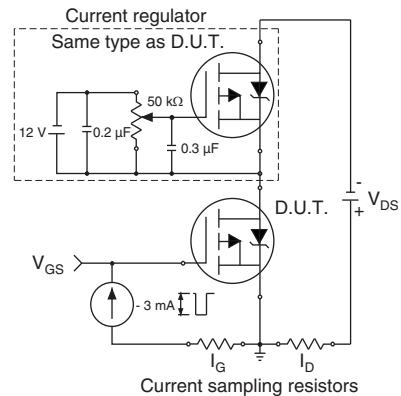
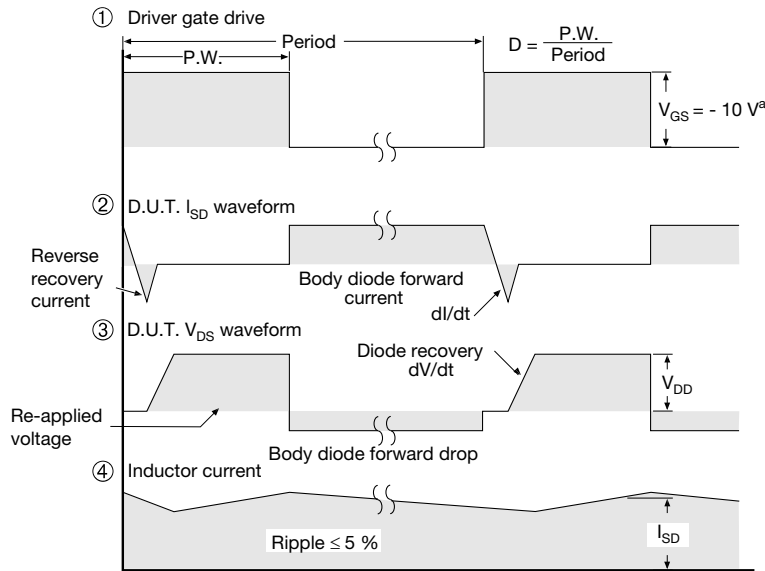


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

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SOT-223 (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08
DWG: 5969

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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