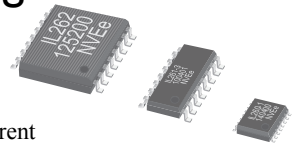
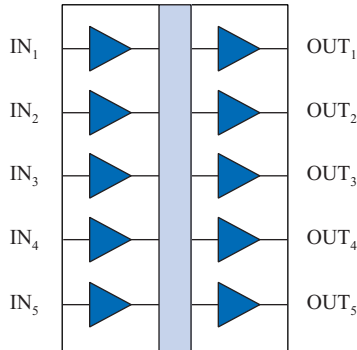


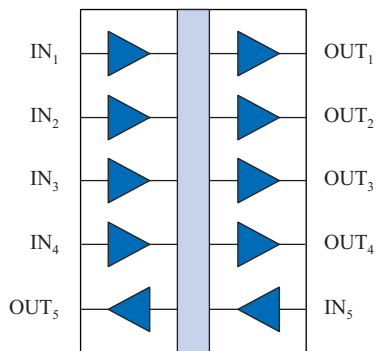
High Speed Five-Channel Digital Isolators



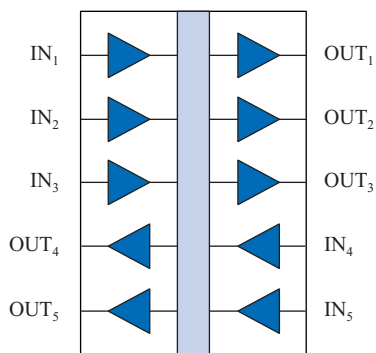
Functional Diagrams



IL260



IL261



IL262

Features

- High Speed: 110 Mbps
- 1.2 mA/channel typical quiescent current
- High isolation voltage: 5 kV_{RMS} per UL 1577 (V-Series)
- High working voltage: 1 kV_{RMS} per VDE 0884 (V-Series)
- 50 kV/μs typ.; 30 kV/μs min. common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- -40°C to +85°C operating temperature
- 44000 year barrier life
- Excellent magnetic immunity
- 2 ns typical pulse width distortion
- 100 ps pulse jitter
- 4 ns typical propagation delay skew
- 10 ns typical propagation delay
- 2 ns channel-to-channel skew
- VDE 0884 / IEC 60747-5-5 certified; UL 1577 recognized
- 0.15", 0.3", and True 8™ mm 16-pin SOIC; 16-pin QSOP packages

Applications

- ADCs and DACs
- Multiplexed data transmission
- Board-to-board communication
- Peripheral interfaces
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE's IL260-Series five-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop[®] spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. The unique fifth channel can be used to distribute isolated clocks or handshake signals to multiple delta-sigma A/D converters. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

Typical transient immunity of 50 kV/μs is unsurpassed. Performance is specified over the temperature range of -40°C to +85°C without derating.

The five-channel devices provide the highest channel density available. Parts are available in ultraminiature 16-pin QSOPs, as well as 0.15" and 0.3"-wide SOIC packages.

V-Series versions offer high isolation voltage of 5 kV_{RMS}.

Absolute Maximum Ratings⁽¹⁾

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	-55		150	°C	
Junction Temperature	T_J	-55		150	°C	
Ambient Operating Temperature	T_A	-40		85	°C	
Supply Voltage	V_{DD1}, V_{DD2}	-0.5		7	V	
Input Voltage	V_I	-0.5		$V_{DD} + 0.5$	V	
Output Voltage	V_O	-0.5		$V_{DD} + 0.5$	V	
Output Current Drive	I_O	-10		10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	-40		85	°C	
Junction Temperature	T_J	-40		110	°C	
Supply Voltage	V_{DD1}, V_{DD2}	3.0		5.5	V	3.3/5.0 V Operation
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	QSOP 0.15" SOIC 0.3" SOIC	4.03 4.03 8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.012	0.013		mm	
Leakage Current ⁽⁵⁾			0.2		μA _{RMS}	240 V _{RMS}
Barrier Resistance ⁽⁵⁾	R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance ⁽⁵⁾	C_{IO}		5		pF	f = 1 MHz
Comparative Tracking Index	CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	V_{IO}	1000 1500		V_{RMS} V_{DC}	At maximum operating temperature
Barrier Life			44000		Years	100°C, 1000 V _{RMS} , 60% CL activation energy

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC		60 60 60		°C/W	Soldered to double-sided board; free air
Junction–Case (Top) Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC		10 10 20		°C/W	
Power Dissipation	QSOP 0.15" SOIC 0.3" SOIC			675 700 800	mW	

Safety and Approvals

VDE 0884-10 (File Number 5016933-4880-0001; V-Series 5 kV-rated parts)

- Working voltage (V_{IORM}) 1000 V_{RMS} (1415 V_{PK}); basic insulation; pollution degree 2
- Transient overvoltage (V_{IOTM}) 6000 V_{PK}
- Surge voltage (V_{IOSM}) 10 kV_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

IEC 60747-5-5 (VDE 0884) (File Number 5016933-4880-0001; 2.5 kV-rated parts)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Transient overvoltage (V_{IOTM}) and surge voltage (V_{IOSM}) 4000 V_{PK}
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

VDE 0884-10 / IEC 60747-5-5 Safety-Limiting Values

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	$^{\circ}C$
Safety rating power (180 $^{\circ}C$)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	QSOP	300 V_{RMS}
-3	0.15" SOIC	300 V_{RMS}
None	0.3" SOIC (standard)	300 V_{RMS}
V	0.3" SOIC (high isolation voltage)	1000 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)

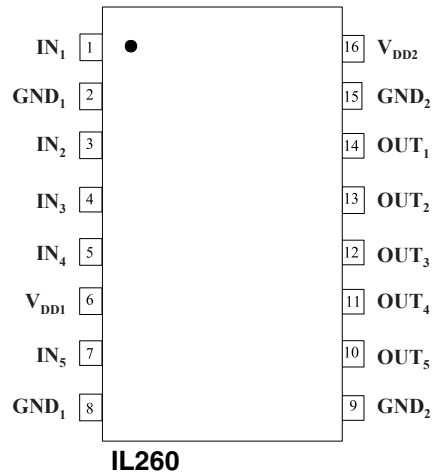
- 5 kV-rated V-Series parts tested at 6 kV_{RMS} (8480 V_{PK}) for 1 second; each lot sample tested at 5 kV_{RMS} (7060 V_{PK}) for 1 minute
- 2.5 kV-rated parts tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

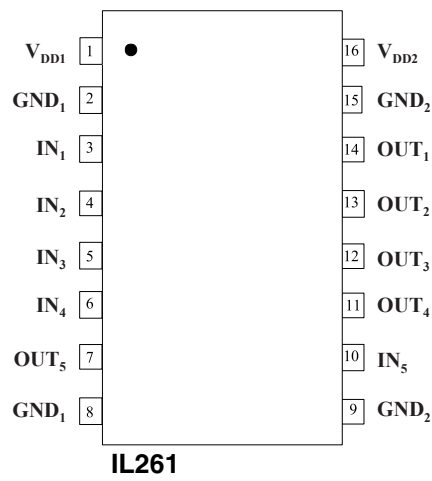
IL260 Pin Connections

1	IN ₁	Input 1
2	GND ₁	Ground*
3	IN ₂	Input 2
4	IN ₃	Input 3
5	IN ₄	Input 4
6	V _{DD1}	Supply Voltage 1
7	IN ₅	Input 5
8	GND ₁	Ground*
9	GND ₂	Ground*
10	OUT ₅	Output 5
11	OUT ₄	Output 4
12	OUT ₃	Output 3
13	OUT ₂	Output 2
14	OUT ₁	Output 1
15	GND ₂	Ground*
16	V _{DD2}	Supply Voltage 2



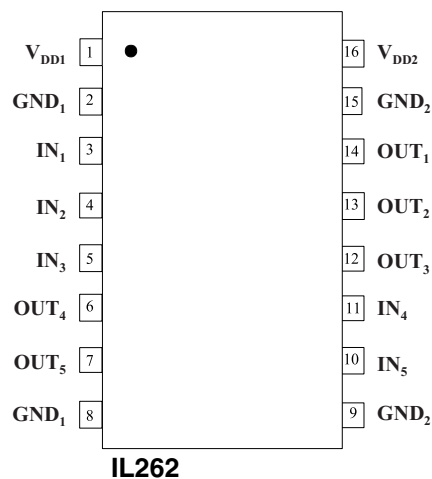
IL261 Pin Connections

1	V _{DD1}	Supply Voltage 1
2	GND ₁	Ground*
3	IN ₁	Input 1
4	IN ₂	Input 2
5	IN ₃	Input 3
6	IN ₄	Input 4
7	OUT ₅	Output 5
8	GND ₁	Ground*
9	GND ₂	Ground*
10	IN ₅	Input 5
11	OUT ₄	Output 4
12	OUT ₃	Output 3
13	OUT ₂	Output 2
14	OUT ₁	Output 1
15	GND ₂	Ground*
16	V _{DD2}	Supply Voltage 2



IL262 Pin Connections

1	V _{DD1}	Supply Voltage 1
2	GND ₁	Ground*
3	IN ₁	Input 1
4	IN ₂	Input 2
5	IN ₃	Input 3
6	OUT ₄	Output 4
7	OUT ₅	Output 5
8	GND ₁	Ground*
9	GND ₂	Ground*
10	IN ₅	Input 5
11	IN ₄	Input 4
12	OUT ₃	Output 3
13	OUT ₂	Output 2
14	OUT ₁	Output 1
15	GND ₂	Ground*
16	V _{DD2}	Supply Voltage 2



*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

3.3 Volt Electrical Specifications (T _{min} to T _{max})							
Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Current	IL260	I _{DD1}		300	400	μA	
	IL261			1.2	1.75	mA	
	IL262			2.4	3.5	mA	
Output Quiescent Current	IL260	I _{DD2}		6	8.75	mA	
	IL261			4.8	7	mA	
	IL262			4.8	7	mA	
Logic Input Current		I _i	-10		10	μA	
Logic High Output Voltage		V _{OH}	V _{DD} -0.1	V _{DD}		V	I _O = -20 μA, V _i =V _{IH}
			0.8 x V _{DD}	0.9 x V _{DD}			I _O = -4 mA, V _i =V _{IH}
Logic Low Output Voltage		V _{OL}		0	0.1	V	I _O = 20 μA, V _i =V _{IL}
				0.5	0.8		I _O = 4 mA, V _i =V _{IL}

Switching Specifications (V _{DD} = 3.3 V)							
Maximum Data Rate			100	110		Mbps	C _L = 15 pF
Minimum Pulse Width ⁽⁷⁾		PW	10			ns	50% Points, V _O
Propagation Delay Input to Output (High to Low)		t _{PHL}		12	18	ns	C _L = 15 pF
Propagation Delay Input to Output (Low to High)		t _{PLH}		12	18	ns	C _L = 15 pF
Pulse Width Distortion t _{PHL} -t _{PLH} ⁽²⁾		PWD		2	3	ns	C _L = 15 pF
Propagation Delay Skew ⁽³⁾		t _{PSK}		4	6	ns	C _L = 15 pF
Output Rise Time (10%-90%)		t _R		2	4	ns	C _L = 15 pF
Output Fall Time (10%-90%)		t _F		2	4	ns	C _L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low) ⁽⁴⁾		CM _H , CM _L	30	50		kV/μs	V _{CM} = 1500 V _{DC} t _{TRANSIENT} = 25 ns
Channel-to-Channel Skew				2	3	ns	C _L = 15 pF
Dynamic Power Consumption ⁽⁶⁾				140	240	μA/Mbps	per channel

Magnetic Field Immunity ⁽⁸⁾ (V _{DD2} = 3V, 3V < V _{DD1} < 5.5V)							
Power Frequency Magnetic Immunity		H _{PF}	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity		H _{PM}	1800	2000		A/m	t _b = 8μs
Damped Oscillatory Magnetic Field		H _{OSC}	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier ⁽⁹⁾		K _X		2.5			

5 Volt Electrical Specifications (T_{min} to T_{max})							
Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Current	IL260	I_{DD1}		350	500	μ A	
	IL261			1.8	2.5	mA	
	IL262			3.6	5	mA	
Output Quiescent Current	IL260	I_{DD2}		9	12.5	mA	
	IL261			7.2	10	mA	
	IL262			7.2	10	mA	
Logic Input Current		I_i	-10		10	μ A	
Logic High Output Voltage		V_{OH}	$V_{DD}-0.1$	V_{DD}		V	$I_O = -20 \mu A, V_i = V_{IH}$
			$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{ mA}, V_i = V_{IH}$
Logic Low Output Voltage		V_{OL}		0	0.1	V	$I_O = 20 \mu A, V_i = V_{iL}$
				0.5	0.8		$I_O = 4 \text{ mA}, V_i = V_{iL}$

Switching Specifications ($V_{DD} = 5 \text{ V}$)							
Maximum Data Rate			100	110		Mbps	$C_L = 15 \text{ pF}$
Minimum Pulse Width ⁽⁷⁾		PW	10			ns	50% Points, V_o
Propagation Delay Input to Output (High to Low)		t_{PHL}		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)		t_{PLH}		10	15	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $ ⁽²⁾		PWD		2	3	ns	$C_L = 15 \text{ pF}$
Pulse Jitter ⁽¹⁰⁾		t_j		100		ps	$C_L = 15 \text{ pF}$
Propagation Delay Skew ⁽³⁾		t_{PSK}		4	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10%–90%)		t_R		1	3	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10%–90%)		t_F		1	3	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High to Logic Low) ⁽⁴⁾		$ CM_H , CM_L $	30	50		kV/ μ s	$V_{CM} = 1500 \text{ V}_{DC}$ $t_{TRANSIENT} = 25 \text{ ns}$
Channel-to-Channel Skew				2	3	ns	$C_L = 15 \text{ pF}$
Dynamic Power Consumption ⁽⁶⁾				200	340	μ A/Mbps	per channel

Magnetic Field Immunity ⁽⁸⁾ ($V_{DD2} = 5\text{V}, 3\text{V} < V_{DD1} < 5.5\text{V}$)							
Power Frequency Magnetic Immunity		H_{PF}	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity		H_{PM}	4000	4500		A/m	$t_p = 8 \mu s$
Damped Oscillatory Magnetic Field		H_{OSC}	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier ⁽⁹⁾		K_X		2.5			

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_o > 0.8 V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_o < 0.8 \text{ V}$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 6).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Application Information

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. There are no internal clocks or carriers. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1

Residential, Commercial & Light Industrial
Methods EN55022, EN55014

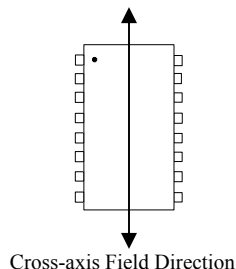
EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



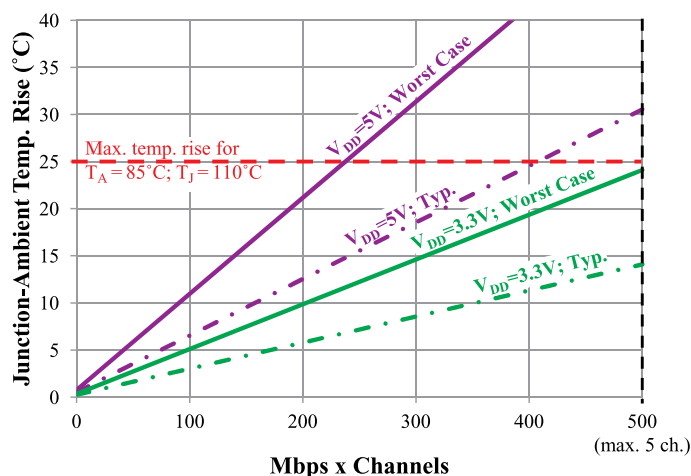
Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Thermal Management

IsoLoop Isolators are designed for low power dissipation and thermal performance, providing unmatched channel density for high-performance isolators. Nevertheless, package temperature rise should be considered when running multiple channels at high speed. Power consumption is higher at 5 volt operation than at 3.3 volts, and dynamic supply current is higher on the input side of the isolators than the output side, so thermal management is more important with five-volt input-side power supplies.

IL260/IL261/IL262 parts have a maximum junction temperature of 110°C. Based on the specifications contained in this datasheet, the derating curve at typical operating conditions is as follows:



Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both GND₁ and GND₂ are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V_{DD} pins.

Maintaining Creepage

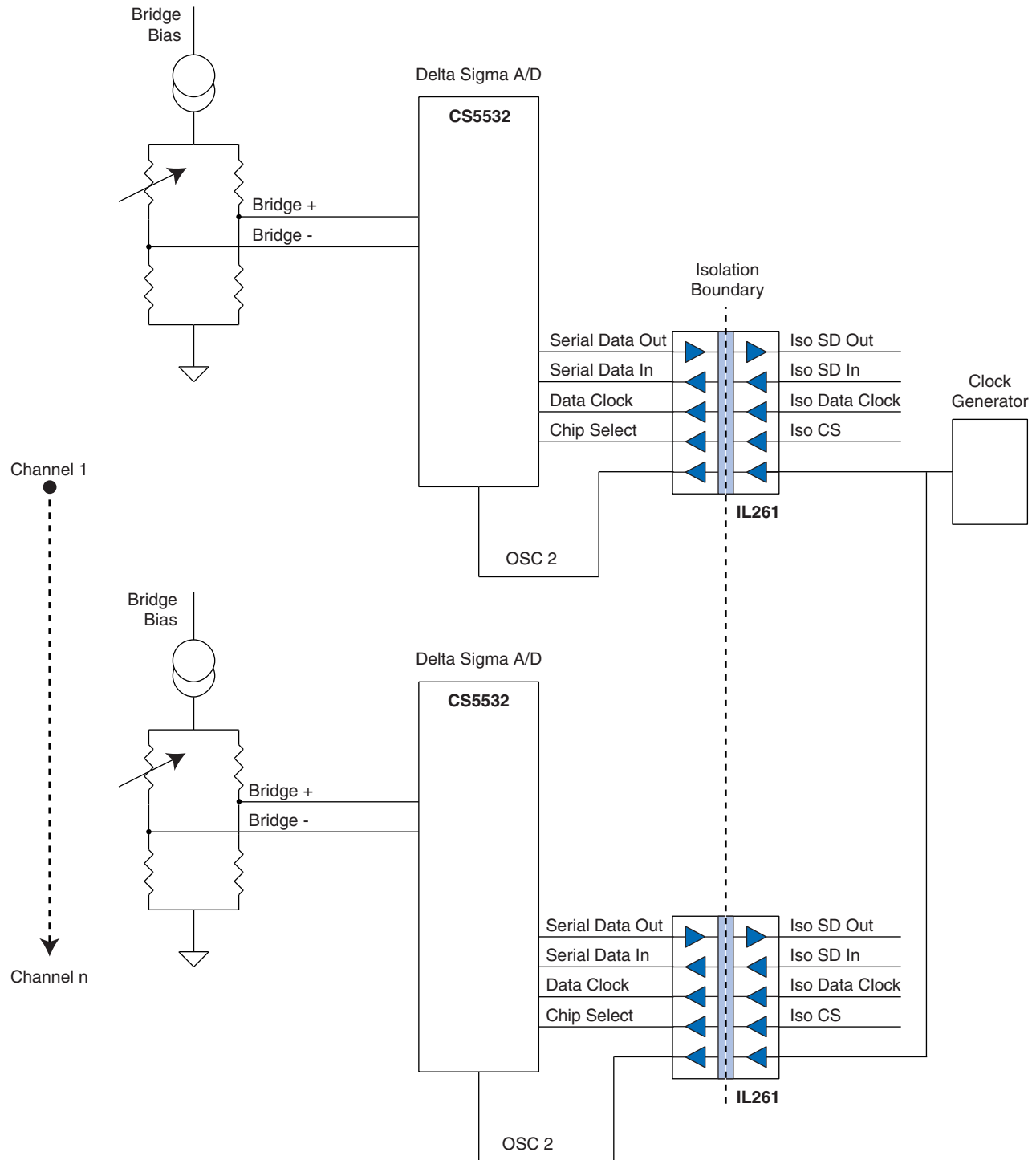
Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Application Diagram—Multi-Channel Delta-Sigma A/D Converter

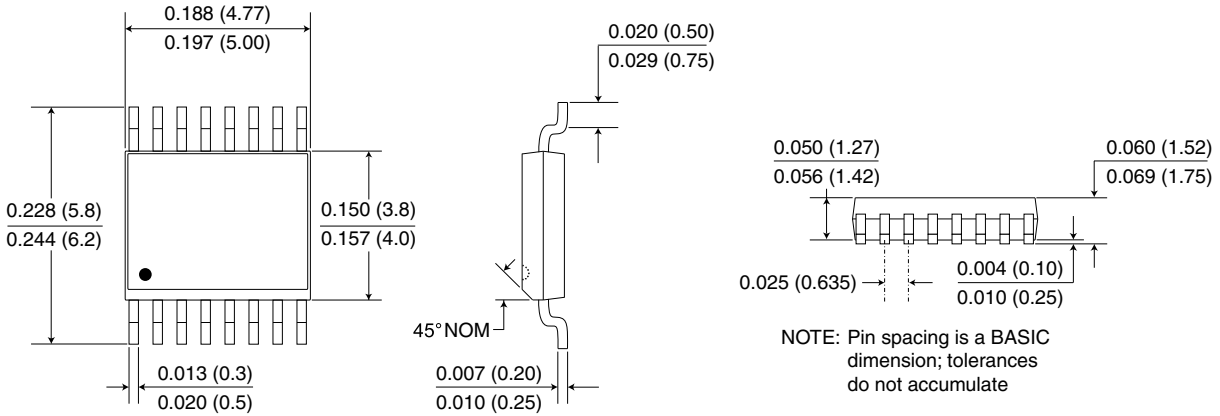
In a typical single-channel delta-sigma ADC, the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:



Package Drawings

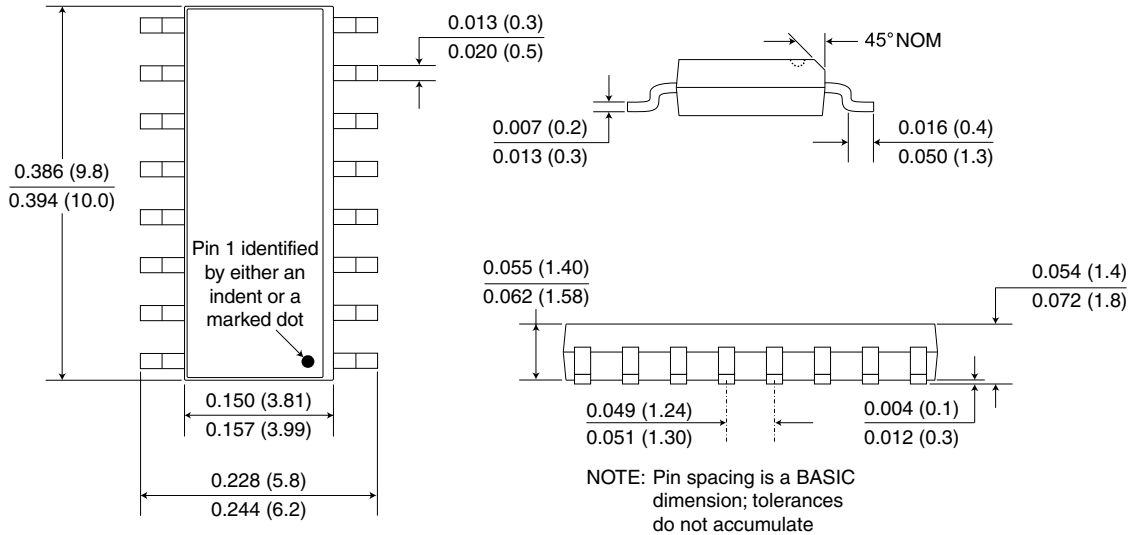
Ultraminiature 16-pin QSOP Package (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



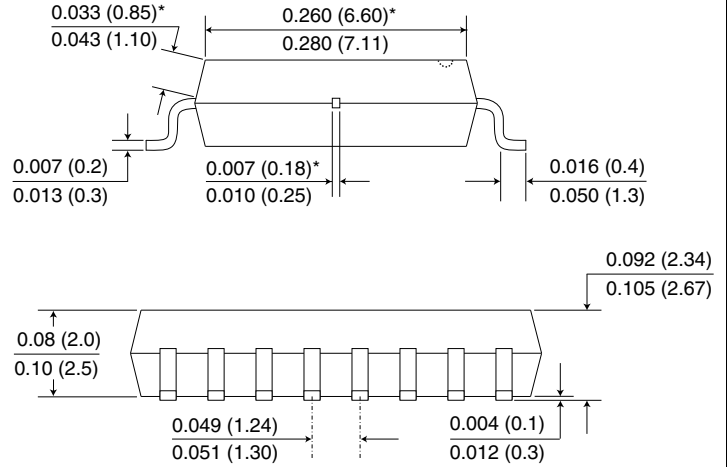
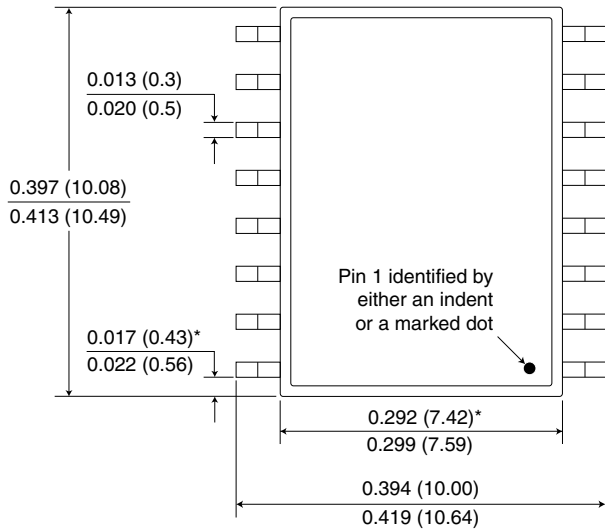
0.15" 16-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X



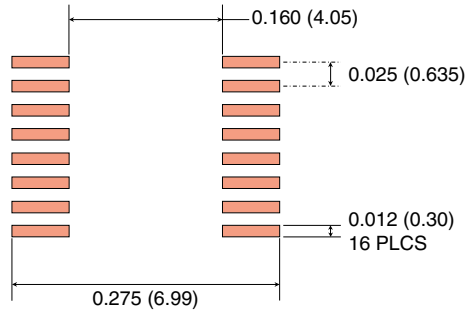
NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

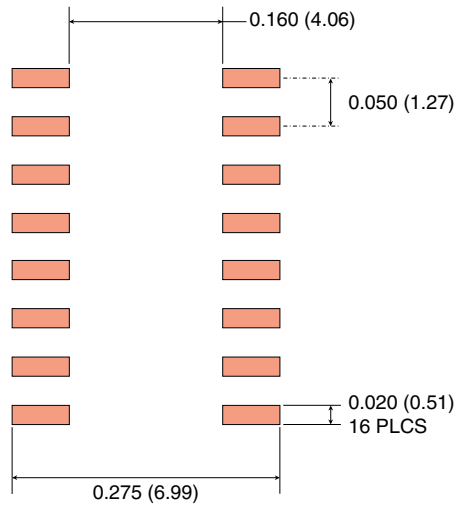
4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



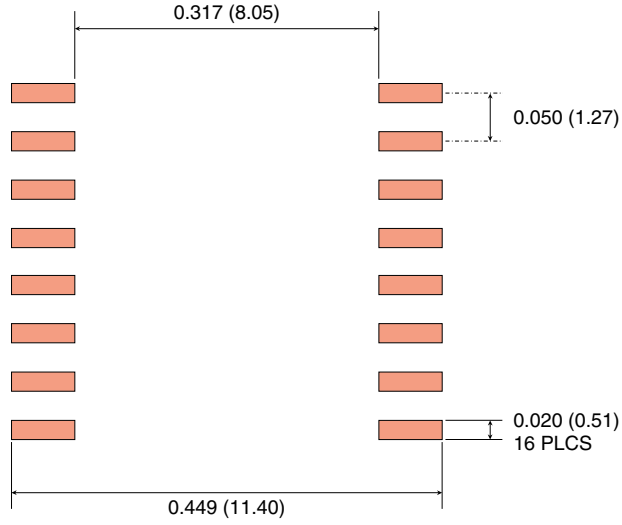
0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



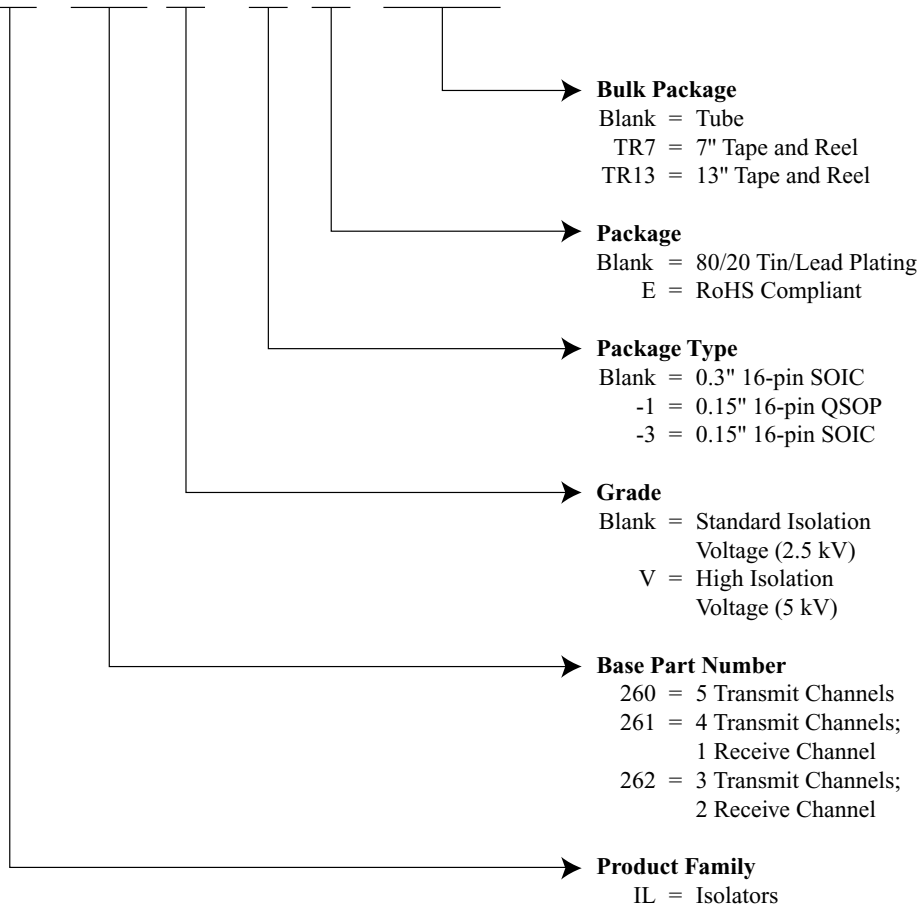
Available Parts

Available Parts	Transmit Channels	Receive Channels	Isolation Voltage (RMS)	Package
IL260-1E	5	0	2.5 kV	QSOP
IL260-3E	5	0	2.5 kV	Narrow SOIC
IL260E	5	0	2.5 kV	Wide SOIC
IL260VE	5	0	5 kV	Wide SOIC
IL261-1E	4	1	2.5 kV	QSOP
IL261-3E	4	1	2.5 kV	Narrow SOIC
IL261E	4	1	2.5 kV	Wide SOIC
IL261VE	4	1	5 kV	Wide SOIC
IL262-3E	3	2	2.5 kV	Narrow SOIC
IL262E	3	2	2.5 kV	Wide SOIC
IL262VE	3	2	5 kV	Wide SOIC

All part types are available on tape and reel.

Ordering Information

IL 260 V - 3 E TR13



Revision History

ISB-DS-001- IL260/1/2-S
September 2014

Changes

- Added V-Series 5 kV isolation voltage versions.
- More detailed “Available Parts” table.

ISB-DS-001-IL260/1/2-R

Changes

- Added QSOP packages (-1 suffix).
- Revised and added details to thermal characteristic specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).
- Added “Thermal Management” paragraph in Applications section.

ISB-DS-001-IL260/1/2-Q

Change

- IEC 60747-5-5 (VDE 0884) certification.

ISB-DS-001-IL260/1/2-P

Changes

- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

ISB-DS-001-IL260/1/2-O

Changes

- Increased transient immunity specifications based on additional data.
- Added VDE 0884 pending.
- Added high voltage endurance specifications.
- Increased magnetic immunity specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

ISB-DS-001-IL260/1/2-N

Changes

- Detailed isolation and barrier specifications.
- Cosmetic changes.

ISB-DS-001-IL260/1/2-M

Change

- Tightened typical output quiescent supply specs.

ISB-DS-001-IL260/1/2-L

Change

- Update terms and conditions.

ISB-DS-001-IL260/1/2-K

Change

- Added clarification of internal ground connections.

ISB-DS-001-IL260/1/2-J

Change

- Relaxed Vdd1 quiescent current specification to 500 μ A.

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September 2014