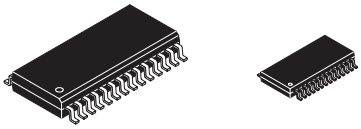


SLAS290C − OCTOBER 2001 − REVISED OCTOBER 2004

3-V, 10-Bit, 40-MSPS CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Analog Supply 3 V**
- **Digital Supply 3 V**
- **Configurable Input Functions:**
  - **Single Ended**
  - **Differential**
- **Differential Nonlinearity: ±0.45 LSB**
- **Signal-to-Noise: 60 dB Typ $f_{(IN)}$ at 4.8 MHz**
- **Spurious Free Dynamic Range: 72 dB**
- **Adjustable Internal Voltage Reference**
- **On-Chip Voltage Reference Generator**
- **Unsigned Binary Data Output**
- **Out-of-Range Indicator**
- **Power-Down Mode**

APPLICATIONS

- **Video/CCD Imaging**
- **Communications**
- **Set-Top Box**
- **Medical**

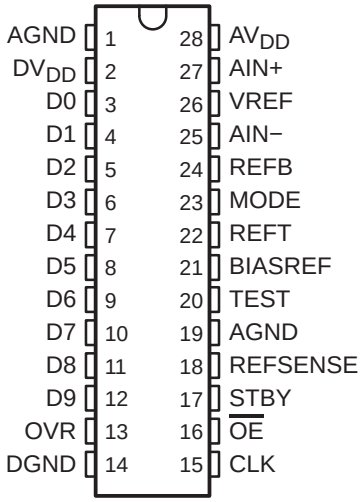
DESCRIPTION

The THS1040 is a CMOS, low power, 10-bit, 40-MSPS analog-to-digital converter (ADC) that operates from a single 3-V supply. The THS1040 has been designed to give circuit developers flexibility. The analog input to the THS1040 can be either single-ended or differential. The THS1040 provides a wide selection of voltage references to match the user's design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output indicates any out-of-range condition in THS1040's input signal.

The speed, resolution, and single-supply operation of the THS1040 are suited to applications in set-top-box (STB), video, multimedia, imaging, high-speed acquisition, and communications. The speed and resolution ideally suit charge-couple device (CCD) input systems such as color scanners, digital copiers, digital cameras, and camcorders. A wide input voltage range allows the THS1040 to be applied in both imaging and communications systems.

The THS1040C is characterized for operation from 0°C to 70°C, while the THS1040I is characterized for operation from −40°C to 85°C.

28-PIN TSSOP/SOIC PACKAGE
(TOP VIEW)

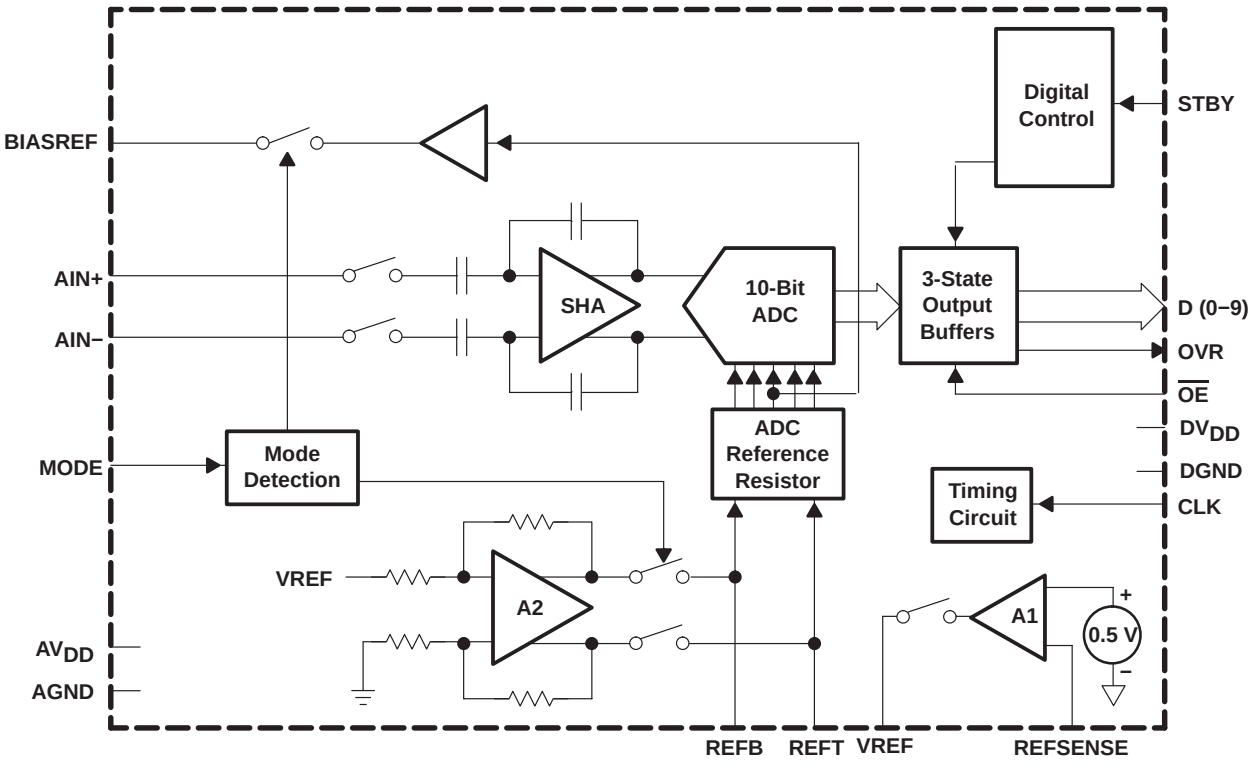


AVAILABLE OPTIONS

PRODUCT	PACKAGE LEAD	PACKAGE DESGIGNATOR†	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKINGS	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS1040C	TSSOP−28	PW	0°C to 70°C	TH1040	THS1040CPW	Tube, 50
					THS1040CPWR	Tube and Reel, 2000
THS1040I			−40°C to 85°C	TJ1040	THS1040IPW	Tube, 50
					THS1040IPWR	Tube and Reel, 2000
THS1040C	SOP−28	DW	0°C to 70°C	TH1040	THS1040CDW	Tube, 20
					THS1040CDWR	Tube and Reel, 1000
THS1040I			−40°C to 85°C	TJ1040	THS1040IDW	Tube, 20
					THS1040IDWR	Tube and Reel, 1000

† For the most current specification and package information, refer to the TI web site at *www.ti.com*.

functional block diagram



NOTE: A1 − Internal bandgap reference
A2 − Internal ADC reference generator

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1, 19	I	Analog ground
AIN+	27	I	Positive analog input
AIN−	25	I	Negative analog input
AV_{DD}	28	I	Analog supply
BIASREF	21	O	When the MODE pin is at AV_{DD}, a buffered $AV_{DD}/2$ is present at this pin that can be used by external input biasing circuits. The output is high impedance when MODE is AGND or $AV_{DD}/2$.
CLK	15	I	Clock input
DGND	14	I	Digital ground
DV_{DD}	2	I	Digital supply
D0	3	O	Digital data bit 0 (LSB)
D1	4		Digital data bit 1
D2	5		Digital data bit 2
D3	6		Digital data bit 3
D4	7		Digital data bit 4
D5	8		Digital data bit 5
D6	9		Digital data bit 6
D7	10		Digital data bit 7
D8	11		Digital data bit 8
D9	12		Digital data bit 9 (MSB)
MODE	23	I	Operating mode select (AGND, $AV_{DD}/2$, or AV_{DD})
$\overline{OE}$	16	I	High to 3-state the data bus, low to enable the data bus
OVR	13	O	Out-of-range indicator
REFB	24	I/O	Bottom ADC reference voltage
REFSENSE	18	I	VREF mode control
REFT	22	I/O	Top ADC reference voltage
STBY	17	I	Drive high to power-down the THS1040
TEST	20	I	Production test pin. Tie to DV_{DD} or DGND
VREF	26	I/O	Internal or external reference

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: AV_{DD} to AGND, DV_{DD} to DGND . . . . . −0.3 V to 4 V
AGND to DGND . . . . . −0.3 V to 0.3 V
AV_{DD} to DV_{DD} . . . . . −4 V to 4 V
MODE input voltage range, MODE to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Reference voltage input range, REFT, REFB, to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Analog input voltage range, AIN to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Reference input voltage range, VREF to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Reference output voltage range, VREF to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Clock input voltage range, CLK to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Digital input voltage range, digital input to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
Digital output voltage range, digital output to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
Operating junction temperature range, T_J . . . . . 0°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

over operating free-air temperature range T_A, (unless otherwise noted)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Power Supply						
Supply voltage	AV_{DD}, DV_{DD}		3	3	3.6	V
Analog and Reference Inputs						
VREF input voltage	$V_{I(VREF)}$	REFSENSE = AV_{DD}	0.5		1	V
REFT input voltage	$V_{I(REFT)}$	MODE = AGND	1.75		2	V
REFB input voltage	$V_{I(REFB)}$	MODE = AGND	1		1.25	V
Reference input voltage	$V_{I(REFT)} - V_{I(REFB)}$	MODE = AGND	0.5		1	V
Reference common mode voltage	$(V_{I(REFT)} + V_{I(REFB)})/2$	MODE = AGND	$(AV_{DD}/2) - 0.05$		$(AV_{DD}/2) + 0.05$	V
Analog input voltage differential (see Note 1)	$V_{I(AIN)}$	REFSENSE = AGND	−1		1	V
		REFSENSE = VREF	−0.5		0.5	V
Analog input capacitance, C_I					10	pF
Clock input (see Note 2)			0		AV_{DD}	V
Digital Outputs						
Maximum digital output load resistance	R_L		100			kΩ
Maximum digital output load capacitance	C_L				10	pF
Digital Inputs						
High-level input voltage, V_{IH}			2.4		DV_{DD}	V
Low-level input voltage, V_{IL}			DGND		0.8	V
Clock frequency (see Note 3)	t_c	$f_{(CLK)}$ = 5 MHz to 40 MHz	25		200	nS
Clock pulse duration	$t_{w(CKL)}$, $t_{w(CKH)}$	$f_{(CLK)}$ = 40 MHz	11.25	12.5	13.75	nS
Operating free-air temperature, T_A		THS1040C	0		70	°C
		THS1040I	−40		85	

NOTE 1: $V_{I(AIN)}$ is AIN+ − AIN− range, based on $V_{I(REFT)} - V_{I(REFB)}$ = 1 V. Varies proportional to the $V_{I(REFT)} - V_{I(REFB)}$ value. Input common mode voltage is recommended to be $AV_{DD}/2$.
NOTE 2: The clock pin is referenced to AV_{SS} and powered by AV_{DD}.
NOTE 3: Clock frequency can be extended to this range without degradation of performance.

electrical characteristics

over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 40 MSPS/50% duty cycle, MODE = AV_{DD} (internal reference), differential input range = 1 V_{PP} and 2 V_{PP}, $T_A = T_{min}$ to T_{max} (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV_{DD}	Supply voltage		3		3.6	V
DV_{DD}			3		3.6	
I_{CC}	Operating supply current	See Note 4		33	40	mA
P_D	Power dissipation	See Note 4		100	120	mW
$P_{D(STBY)}$	Standby power			75		µW
	Power up time for all references from standby, $t_{(PU)}$	10 µF bypass		770		µs
$t_{(WU)}$	Wake-up time	See Note 5		45		µs

REFT, REFB internal ADC reference voltages outputs (MODE = AV_{DD} or AV_{DD}/2) (See Note 6)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference voltage top, REFT	VREF = 0.5 V	AV_{DD} = 3 V		1.75		V
	VREF = 1 V			2		
Reference voltage bottom, REFB	VREF = 0.5 V	AV_{DD} = 3 V		1.25		V
	VREF = 1 V			1		
Input resistance between REFT and REFB			1.4	1.9	2.5	kΩ

VREF (on-chip voltage reference generator)

PARAMETER	MIN	TYP	MAX	UNIT
Internal 0.5-V reference voltage (REFSENSE = VREF)	0.45	0.5	0.55	V
Internal 1-V reference voltage (REFSENSE = AGND)	0.95	1	1.05	V
Reference input resistance (REFSENSE = AV_{DD}, MODE = AV_{DD}/2 or AV_{DD})	7	14	21	kΩ

dc accuracy

	PARAMETER	MIN	TYP	MAX	UNIT
	Resolution		10		Bits
INL	Integral nonlinearity (see definitions)	−1.5	±0.75	1.5	LSB
DNL	Differential nonlinearity (see definitions)	−0.9	±0.45	0.9	LSB
	Zero error (see definitions)	−1.5	0.7	1.5	%FSR
	Full-scale error (see definitions)	−3	2.2	3	%FSR
	Missing code	No missing code assured			

NOTE 4: Apply a −1 dBFS 10-KHz triangle wave at AIN+ and AIN− with an internal bandgap reference and ADC reference enabled, and BIASREF enabled at AV_{DD}/2. Any additional load at BIASREF or VREF may require additional current.

NOTE 5: Wake-up time is from the power-down state to accurate ADC samples being taken and is specified for MODE = AGND with external reference sources applied to the device at the time of release of power-down, and an applied 40-MHz clock. Circuits that need to power up are the bandgap, bias generator, ADC, and SHA.

NOTE 6: External reference values are listed in the *Recommended Operating Conditions Table*.

electrical characteristics

over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 40 MSPS/50% duty cycle, MODE = AV_{DD} (internal reference), differential input range = 1 V_{PP} and 2 V_{PP}, T_A = T_{min} to T_{max} (unless otherwise noted) (continued)

dynamic performance (ADC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f = 4.8 MHz, −0.5 dBFS	8.8	9.6		Bits
		f = 20 MHz, −0.5 dBFS		9.5		
SFDR	Spurious free dynamic range	f = 4.8 MHz, −0.5 dBFS	60.5	72		dB
		f = 20 MHz, −0.5 dBFS		70		
THD	Total harmonic distortion	f = 4.8 MHz, −0.5 dBFS		−72.5	−61.3	dB
		f = 20 MHz, −0.5 dBFS		−71.6		
SNR	Signal-to-noise ratio	f = 4.8 MHz, −0.5 dBFS	55.7	60		dB
		f = 20 MHz, −0.5 dBFS		57		
SINAD	Signal-to-noise and distortion	f = 4.8 MHz, −0.5 dBFS	55.6	59.7		dB
		f = 20 MHz, −0.5 dBFS		59.6		
BW	Full power bandwidth (−3 dB)			900		MHz

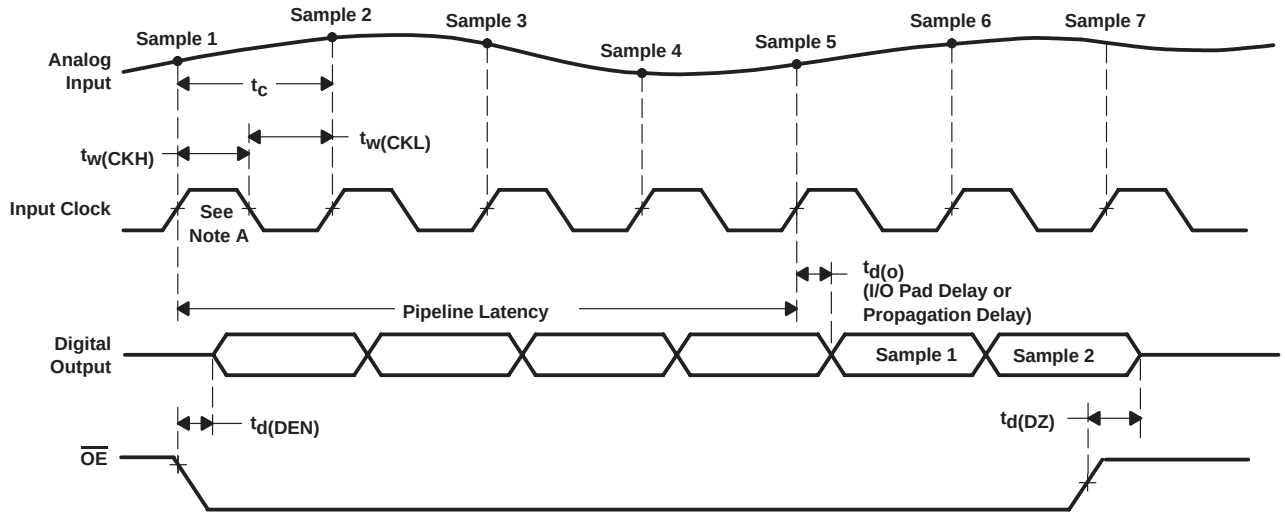
digital specifications

PARAMETER			MIN	NOM	MAX	UNIT
Digital Inputs						
V_{IH}	High-level input voltage	Clock input	0.8 × AV_{DD}			V
		All other inputs	0.8 × DV_{DD}			
V_{IL}	Low-level input voltage	Clock input			0.2 × AV_{DD}	V
		All other inputs			0.2 × DV_{DD}	
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				|−1|	µA
C_i	Input capacitance			5		pF
Digital Outputs						
V_{OH}	High-level output voltage	I_{load} = 50 µA	DV_{DD}−0.4			V
V_{OL}	Low-level output voltage	I_{load} = −50 µA			0.4	V
	High-impedance output current				±1	µA
	Rise/fall time	C_{load} = 15 pF		3.5		ns
Clock Input						
t_c	Clock cycle time		25		200	ns
$t_{w(CKH)}$	Pulse duration, clock high		11.25		110	ns
$t_{w(CKL)}$	Pulse duration, clock low		11.25		110	ns
	Clock duty cycle		45%	50%	55%	
$t_{d(o)}$	Clock to data valid, delay time			9.5	16	ns
	Pipeline latency			4		Cycles
$t_{d(AP)}$	Aperture delay time			0.1		ns
	Aperture uncertainty (jitter)			1		ps

timing

PARAMETER			MIN	TYP	MAX	UNIT
$t_{d(DZ)}$	Output disable to Hi-Z output, delay time		0		10	ns
$t_{d(DEN)}$	Output enable to output valid, delay time		0		10	ns
$V_{O(BIASREF)}$	Output voltage	MODE = AV_{DD}	(AV_{DD}/2) − 0.1		(AV_{DD}/2) + 0.1	V

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timing measurements are based on 50% of edge transition.

Figure 1. Digital Output Timing Diagram

TYPICAL CHARACTERISTICS

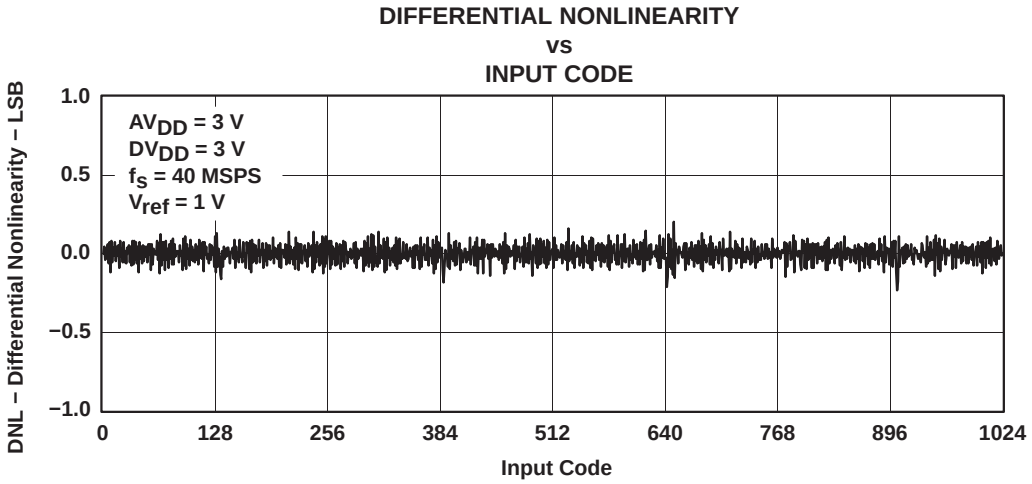


Figure 2

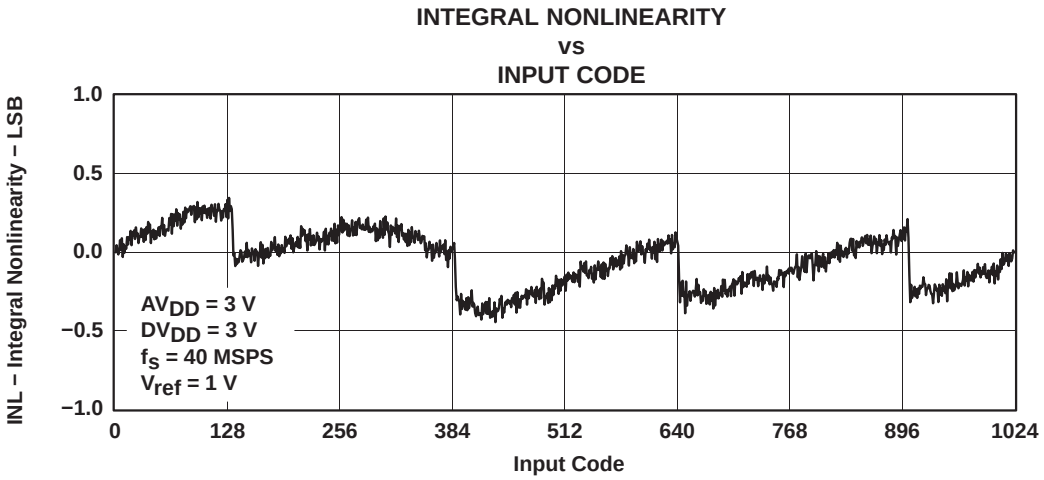


Figure 3

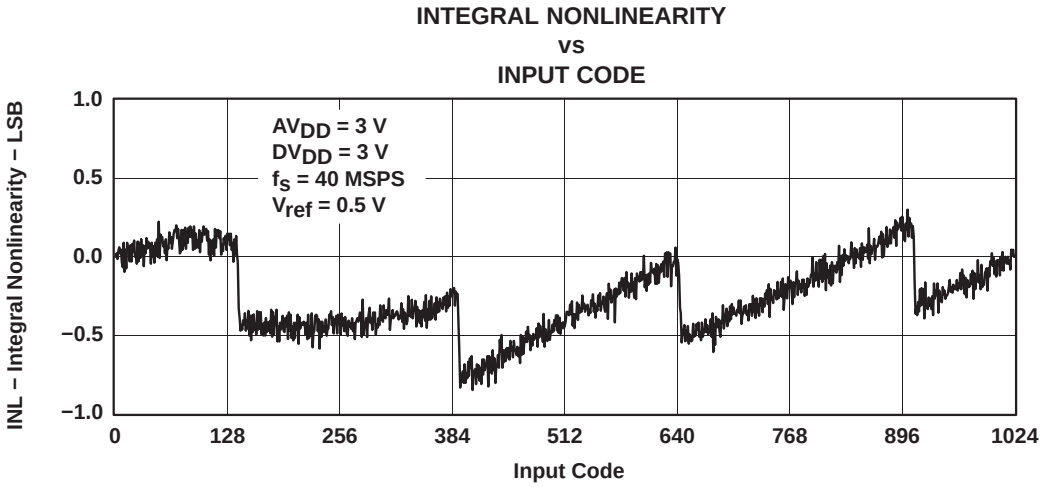


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

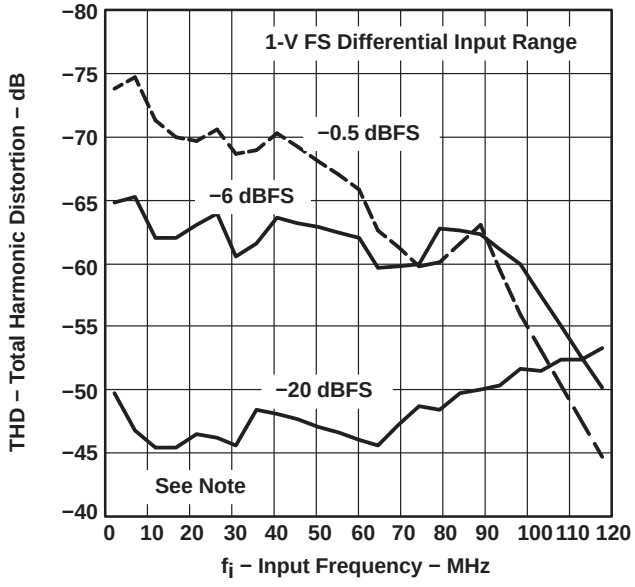


Figure 5

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

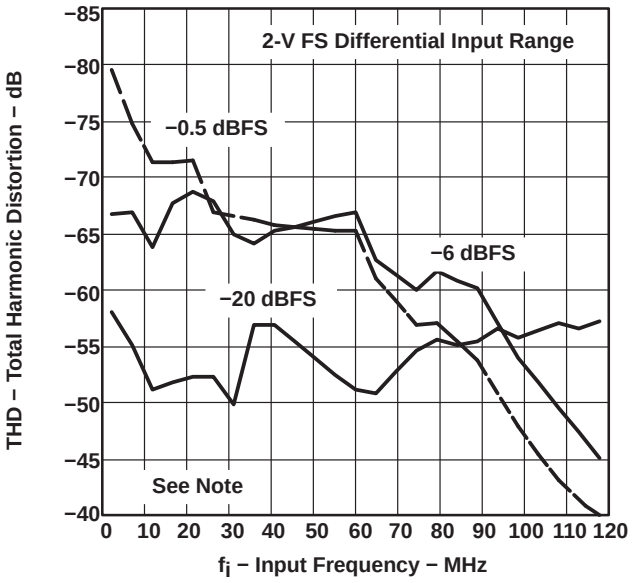


Figure 6

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

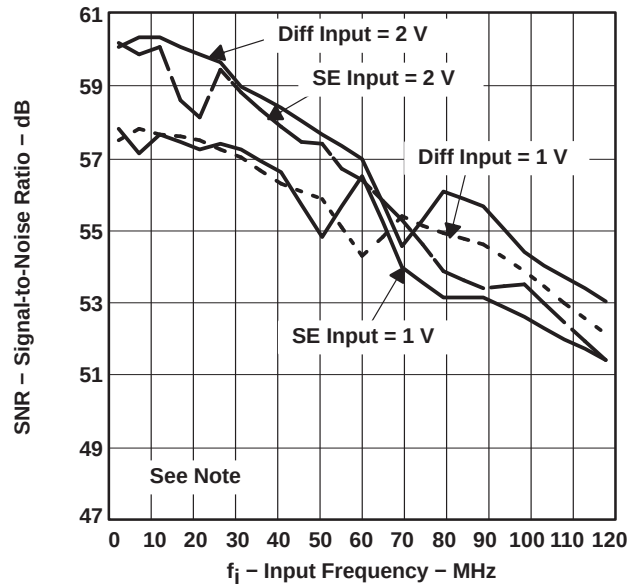


Figure 7

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

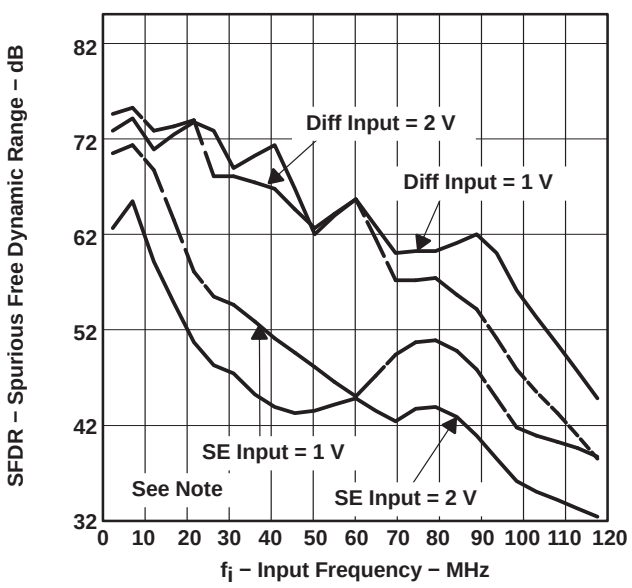


Figure 8

NOTE: AV_{DD} = DV_{DD} = 3 V, f_S = 40 MSPS, 20-pF capacitors AIN+ to AGND and AIN− to AGND,
Input series resistor = 25 Ω,
2-V Input: Ext Ref, REFT = 2 V, REFB = 1 V, −0.5 dBFS
1-V Input: Ext Ref, REFT = 1.75 V, REFB = 1.25 V, −0.5 dBFS

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE PLUS DISTORTION vs INPUT FREQUENCY

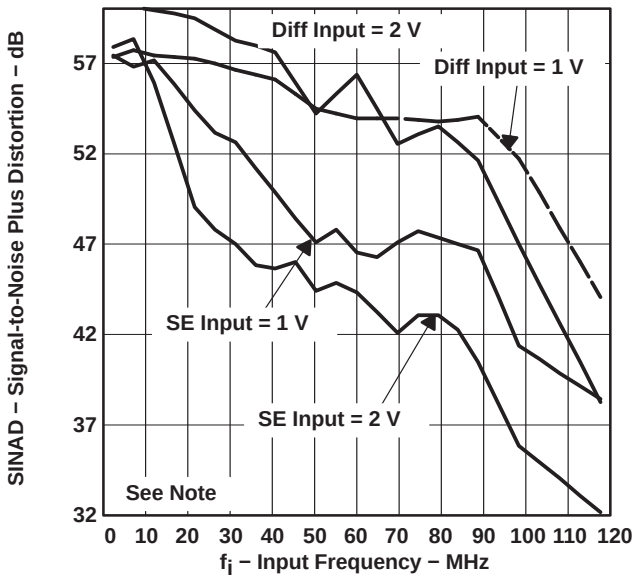


Figure 9

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

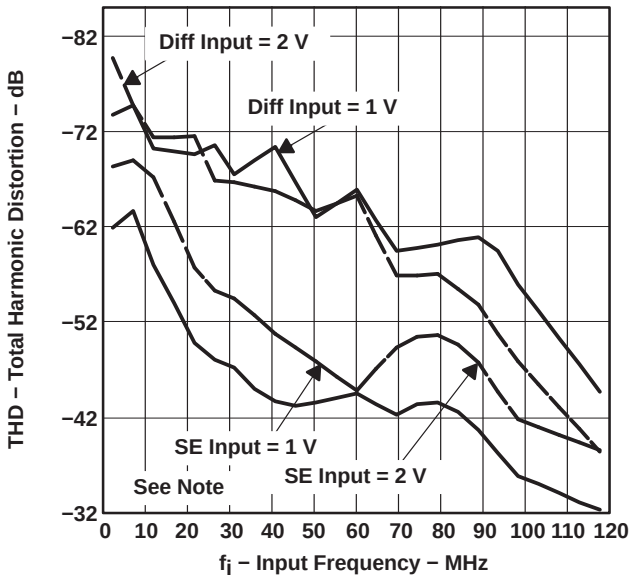


Figure 10

NOTE: AV_{DD} = DV_{DD} = 3 V, f_S = 40 MSPS, 20-pF capacitors AIN+ to AGND and AIN− to AGND,
Input series resistor = 25 Ω,
2-V Input: Ext Ref, REFT = 2 V, REFB = 1 V, −0.5 dBFS
1-V Input: Ext Ref, REFT = 1.75 V, REFB = 1.25 V, −0.5 dBFS

TOTAL HARMONIC DISTORTION vs SAMPLE RATE

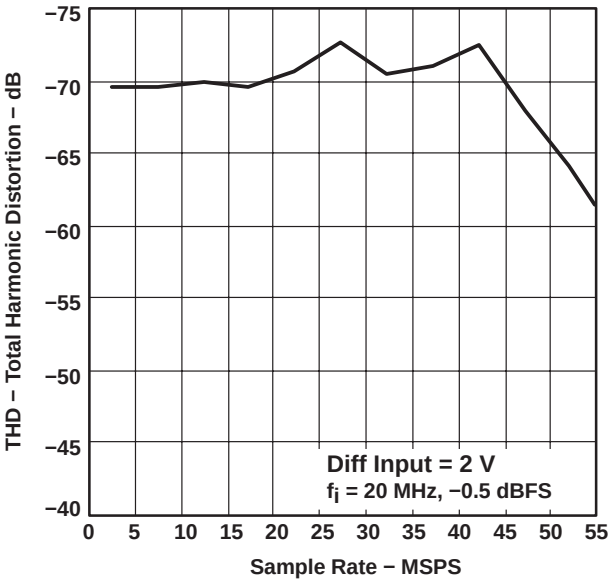


Figure 11

SIGNAL-TO-NOISE RATIO vs SAMPLE RATE

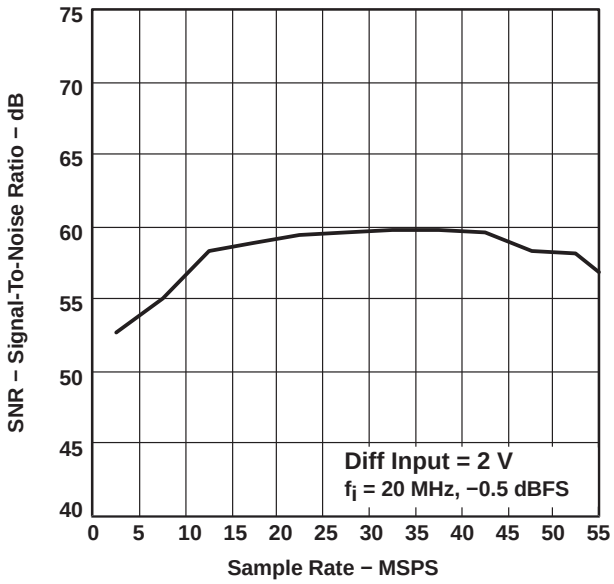


Figure 12

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs SAMPLE RATE

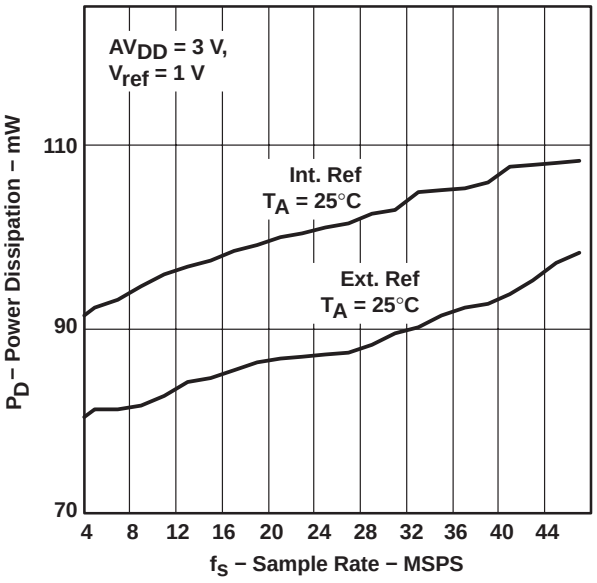


Figure 13

TOTAL CURRENT vs CLOCK FREQUENCY

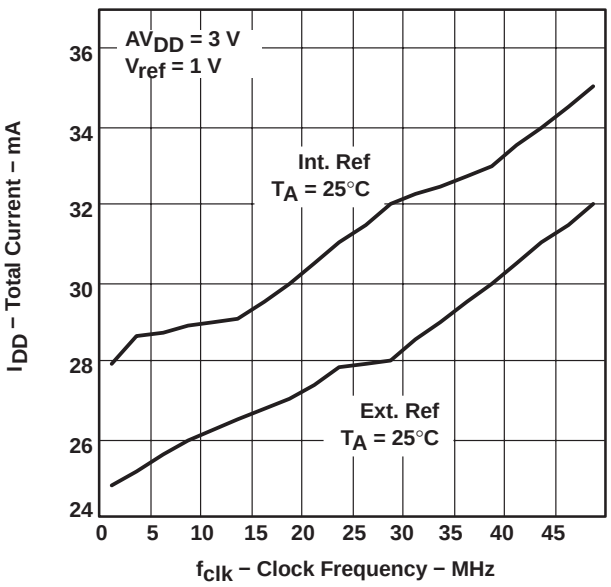


Figure 14

INPUT BANDWIDTH

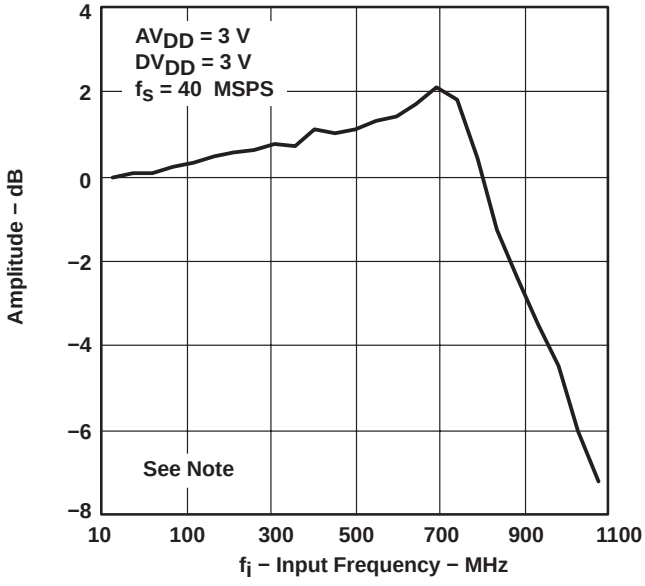


Figure 15

NOTE: No series resistors and no bypass capacitors at AIN+ and AIN− inputs.

TYPICAL CHARACTERISTICS

POWER-UP TIME FOR INTERNAL REFERENCE VOLTAGE FROM STANDBY

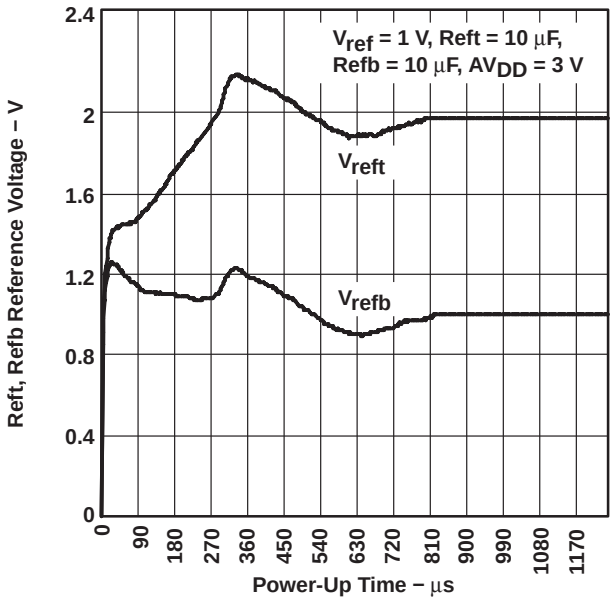


Figure 16

ADC CODES vs WAKE-UP SETTLING TIME

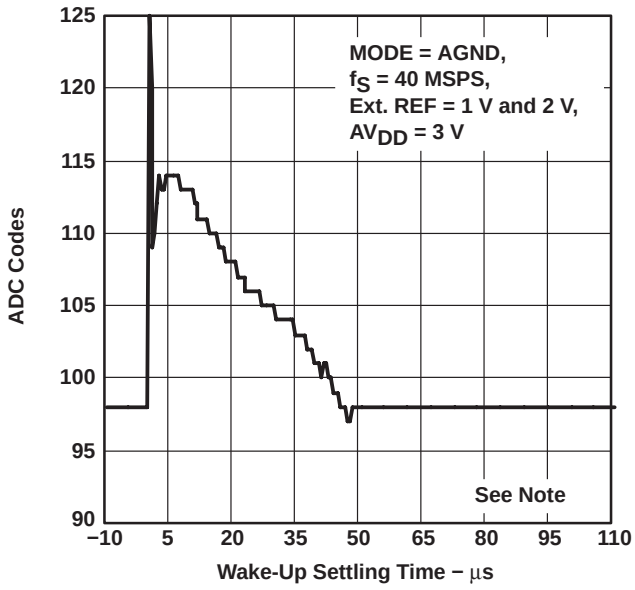


Figure 17

TYPICAL CHARACTERISTICS

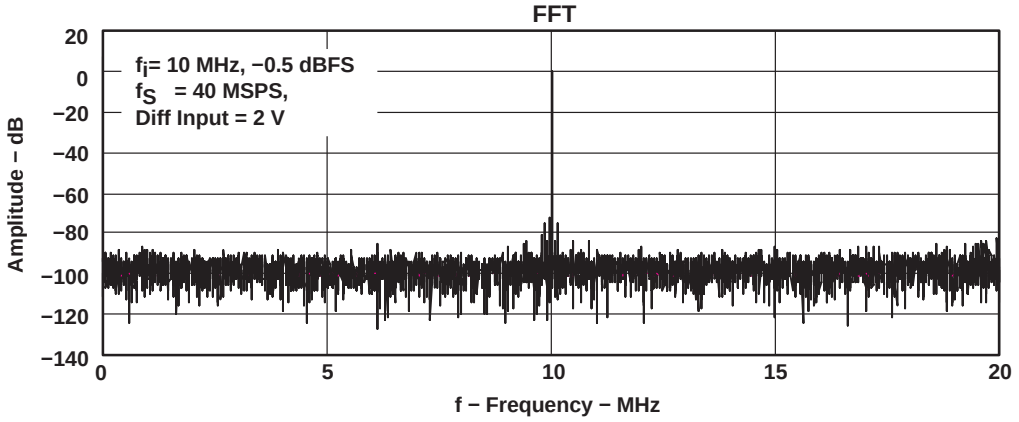


Figure 18

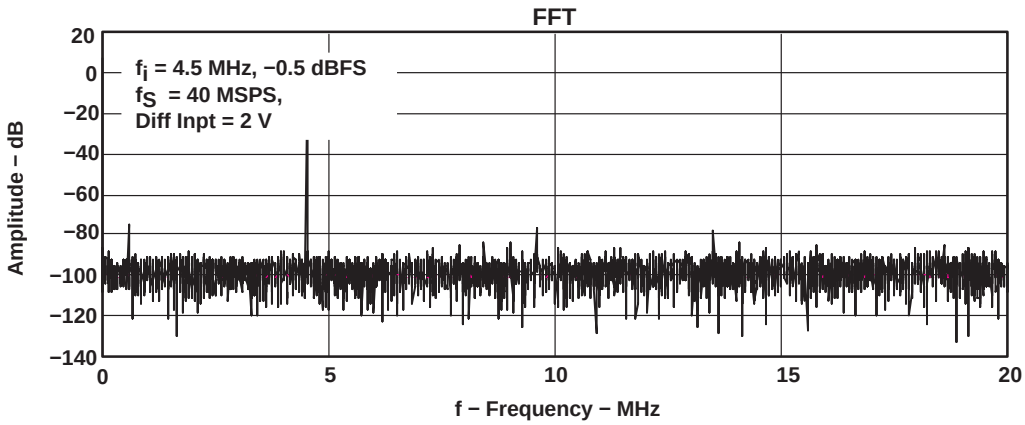


Figure 19

PRINCIPLES OF OPERATION

functional overview

See the functional block diagram. A single-ended, sample rate clock is required at pin CLK for device operation. Analog inputs AIN+ and AIN− are sampled on each rising edge of CLK in a switched capacitor sample and hold unit, the output of which feeds the ADC core, where analog-to-digital conversion is performed against the ADC reference voltages REFT and REFB.

Internal or external ADC reference voltage configurations are selected by connecting the MODE pin appropriately. When MODE = AGND, the user must provide external sources at pins REFB and REFT. When MODE = AV_{DD} or MODE = $AV_{DD}/2$, an internal ADC references generator (A2) is enabled which drives the REFT and REFB pins using the voltage at pin VREF as its input. The user can choose to drive VREF from the internal bandgap reference, or disable A1 and provide their own reference voltage at pin VREF.

On the fourth rising CLK edge following the edge that sampled AIN+ and AIN−, the conversion result is output via data pins D0 to D9. The output buffers can be disabled by pulling pin $\overline{OE}$ high.

The following sections explain further:

- How signals flow from AIN+ and AIN− to the ADC core, and how the reference voltages at REFT and REFB set the ADC input range and hence the input range at AIN+ and AIN−.
- How to set the ADC references REFT and REFB using external sources or the internal reference buffer (A2) to match the device input range to the input signal.
- How to set the output of the internal bandgap reference (A1) if required.

signal processing chain (sample and hold, ADC)

Figure 20 shows the signal flow through the sample and hold unit to the ADC core.

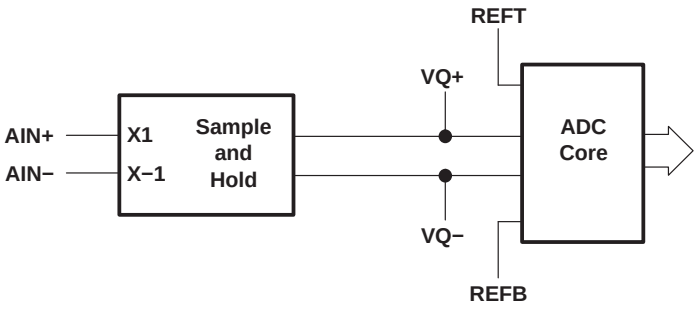


Figure 20. Analog Input Signal Flow

PRINCIPLES OF OPERATION

sample-and-hold

Differential input signal sources can be connected directly to the AIN+ and AIN− pins using either dc- or ac-coupling.

For single-ended sources, the signal can be dc- or ac-coupled to one of AIN+ or AIN−, and a suitable reference voltage (usually the midscale voltage, see *operating configuration examples*) must be applied to the other pin. Note that connecting the signal to AIN− results in it being inverted during sampling.

The sample and hold differential output voltage VQ = (VQ+) − (VQ−) is given by:

$$VQ = (AIN+) - (AIN-) \quad (1)$$

analog-to-digital converter

VQ is digitized by the ADC, using the voltages at pins REFT and REFB to set the ADC zero-scale (code 0) and full-scale (code 1023) input voltages.

$$VQ(ZS) = -(REFT - REFB) \quad (2)$$

$$VQ(FS) = (REFT - REFB) \quad (3)$$

Any inputs at AIN+ and AIN− that give VQ voltages less than VQ(ZS) or greater than VQ(FS) lie outside the ADC's conversion range and attempts to convert such voltages are signalled by driving pin OVR high when the conversion result is output. VQ voltages less than VQ(ZS) digitize to give ADC output code 0 and VQ voltages greater than VQ(FS) give ADC output code 1023.

complete system and system input range

Combining the above equations to find the input voltages [(AIN+) − (AIN−)] that correspond to the limits of the ADC's valid input range gives:

$$(REFB - REFT) \leq [(AIN+) - (AIN-)] \leq (REFT - REFB) \quad (4)$$

For both single-ended and differential inputs, the ADC can thus handle signals with a peak-to-peak input range [(AIN+) − (AIN−)] of:

$$[(AIN+) - (AIN-)] \text{ pk-pk input range} = 2 \times (REFT - REFB) \quad (5)$$

The REFT and REFB voltage difference and the gain sets the device input range. The next sections describe in detail the various methods available for setting voltages REFT and REFB to obtain the desired input span and device performance.

PRINCIPLES OF OPERATION

ADC reference generation

The THS1040 ADC references REFT and REFB can be driven from external (off-chip) sources or from the internal (on-chip) reference buffer A2. The voltage at the MODE pin determines the ADC references source.

Connecting MODE to AGND enables external ADC references mode. In this mode the internal buffer A2 is powered down and the user must provide the REFT and REFB voltages by connecting external sources directly to these pins. This mode is useful where several THS1040 devices must share common references for best matching of their ADC input ranges, or when the application requires better accuracy and temperature stability than the on-chip reference source can provide.

Connecting MODE to AV_{DD} or $AV_{DD}/2$ enables internal ADC references mode. In this mode the buffer A2 is powered up and drives the REFT and REFB pins. External reference sources should not be connected in this mode. Using internal ADC references mode when possible helps to reduce the component count and hence the system cost.

When MODE is connected to AV_{DD}, a buffered $AV_{DD}/2$ voltage is available at the BIASREF pin. This voltage can be used as a dc bias level for any ac-coupling networks connecting the input signal sources to the AIN+ and AIN− pins.

MODE PIN	REFERENCE SELECTION	BIASREF PIN FUNCTION
AGND	External	High impedance
$AV_{DD}/2$	Internal	High impedance
AV_{DD}	Internal	$AV_{DD}/2$ for AIN± bias

external reference mode (MODE = AGND)

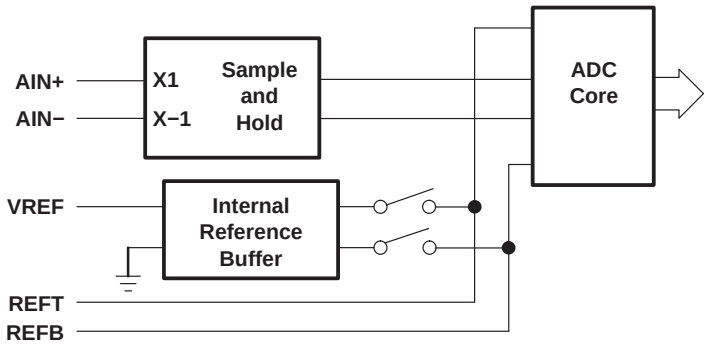


Figure 21. ADC Reference Generation, MODE = AGND

Connecting pin MODE to AGND powers down the internal references buffer A2 and disconnects its outputs from the REFT and REFB pins. The user must connect REFT and REFB to external sources to provide the ADC reference voltages required to match the THS1040 input range to their application requirements. The common-mode reference voltage must be $AV_{DD}/2$ for correct THS1040 operation:

$$\frac{(REFT + REFB)}{2} = \frac{AV_{DD}}{2} \quad (6)$$

PRINCIPLES OF OPERATION

internal reference mode (MODE = AV_{DD} or $AV_{DD}/2$)

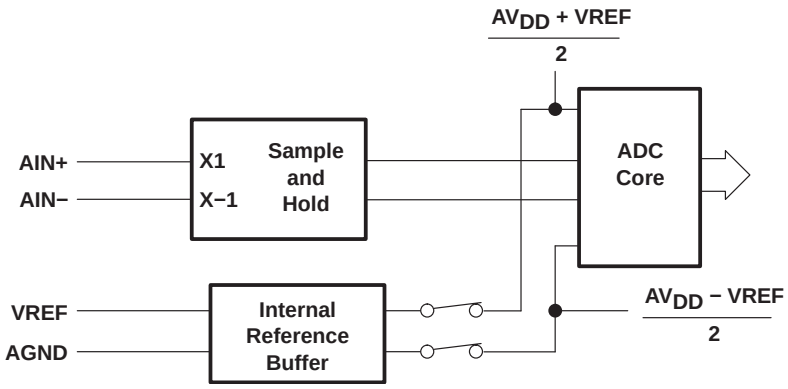


Figure 22. ADC Reference Generation, MODE = $AV_{DD}/2$

Connecting MODE to AV_{DD} or $AV_{DD}/2$ enables the internal ADC references buffer A2. The outputs of A2 are connected to the REFT and REFB pins and its inputs are connected to pins VREF and AGND. The resulting voltages at REFT and REFB are:

$$REFT = \frac{\left(AV_{DD} + VREF\right)}{2} \quad (7)$$

$$REFB = \frac{\left(AV_{DD} - VREF\right)}{2} \quad (8)$$

Depending on the connection of the REFSENSE pin, the voltage on VREF may be driven by an off-chip source or by the internal bandgap reference A1 (see *onboard reference generator*) to match the THS1040 input range to their application requirements.

When MODE = AV_{DD} the BIASREF pin provides a buffered, stabilized $AV_{DD}/2$ output voltage that can be used as a bias reference for ac coupling networks connecting the signal sources to the AIN+ or AIN− inputs. This removes the need for the user to provide a stabilized external bias reference.

PRINCIPLES OF OPERATION

internal reference mode (MODE = AV_{DD} or $AV_{DD}/2$) (continued)

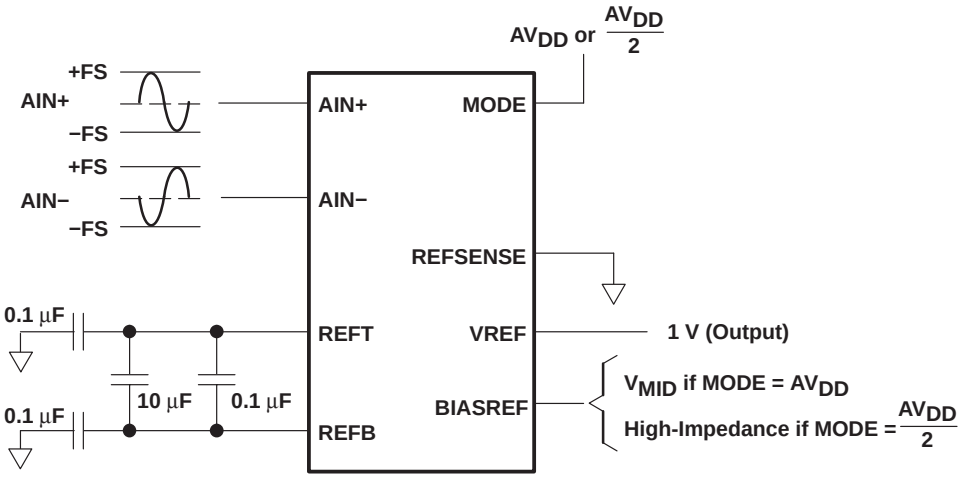


Figure 23. Internal Reference Mode, 1-V Reference Span

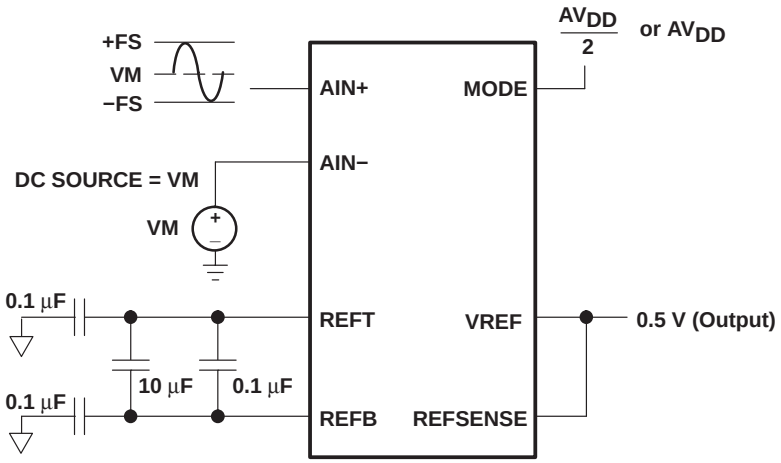


Figure 24. Internal Reference Mode, 0.5-V Reference Span, Single-Ended Input

PRINCIPLES OF OPERATION

onboard reference generator configuration

The internal bandgap reference A1 can provide a supply-voltage-independent and temperature-independent voltage on pin VREF.

External connections to REFSENSE control A1's output to the VREF pin as shown in Table 1.

Table 1. Effect of REFSENSE Connection on VREF Value

REFSENSE CONNECTION	A1 OUTPUT TO VREF	SEE:
VREF pin	0.5 V	Figure 25
AGND	1 V	Figure 26
External divider junction	$(1 + R_a/R_b)/2$ V	Figure 27
AV_{DD}	Open circuit	Figure 28

REFSENSE = AV_{DD} powers the internal bandgap reference A1 down, saving power when A1 is not required. If MODE is connected to AV_{DD} or $AV_{DD}/2$, then the voltage at VREF determines the ADC reference voltages:

$$REFT = \frac{AV_{DD}}{2} + \frac{VREF}{2} \quad (9)$$

$$REFB = \frac{AV_{DD}}{2} - \frac{VREF}{2} \quad (10)$$

$$REFT - REFB = VREF \quad (11)$$

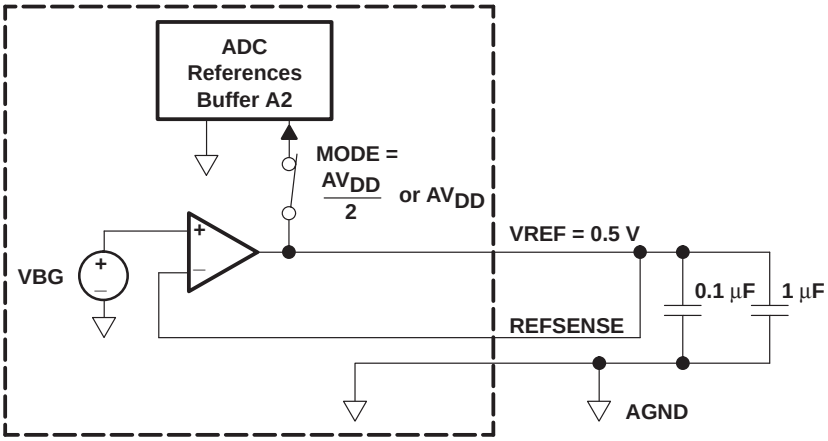


Figure 25. 0.5-V VREF Using the Internal Bandgap Reference A1

PRINCIPLES OF OPERATION

onboard reference generator configuration (continued)

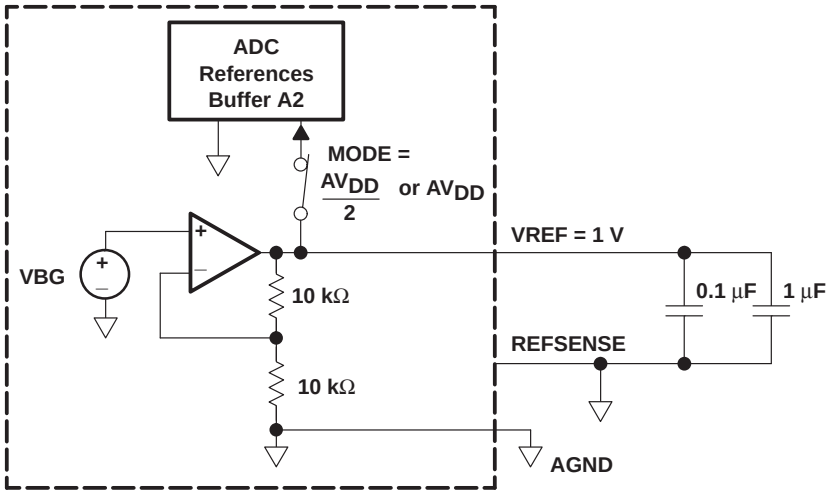


Figure 26. 1-V VREF Using the Internal Bandgap Reference A1

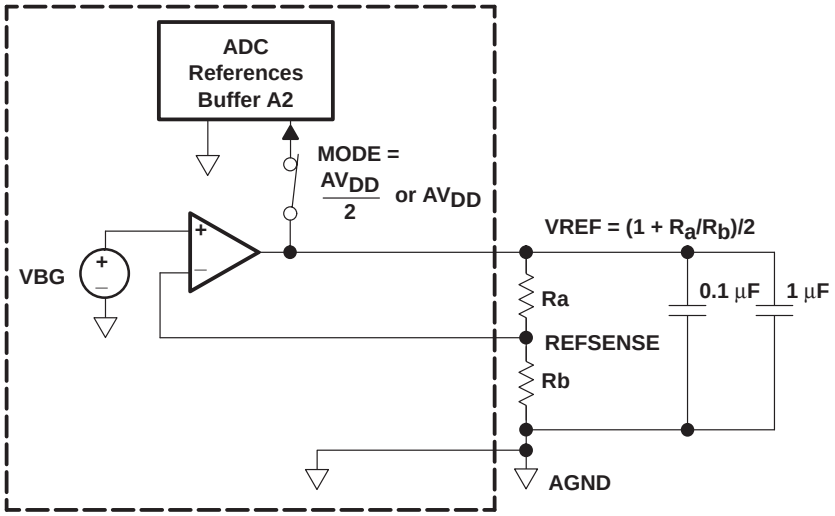


Figure 27. External Divider Mode

onboard reference generator configuration (continued)

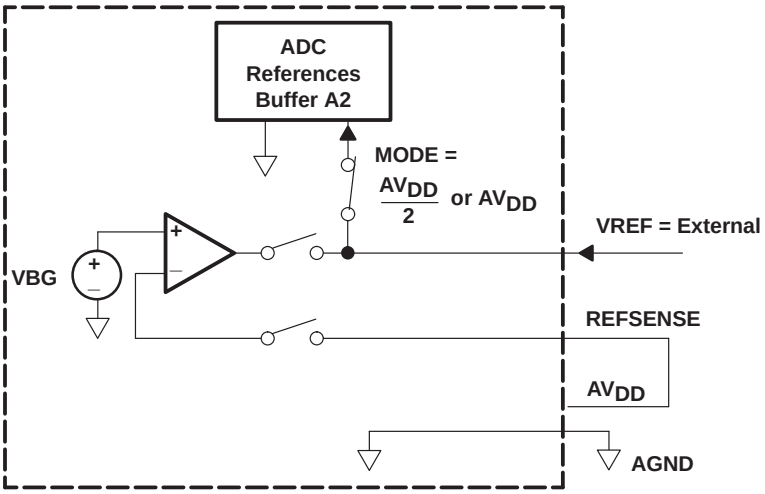


Figure 28. Drive VREF Mode

operating configuration examples

Figure 29 shows a configuration using the internal ADC references for digitizing a single-ended signal with span 0 V to 2 V. Tying REFSENSE to ground gives 1 V at pin VREF. Tying MODE to $AV_{DD}/2$ then sets the REFT and REFB voltages via the internal reference generator for a 2-V_{p-p} ADC input range. The VREF pin provides the 1-V mid-scale bias voltage required at AIN−. VREF should be well decoupled to AGND to prevent sample-and-hold switching at AIN− from corrupting the VREF voltage.

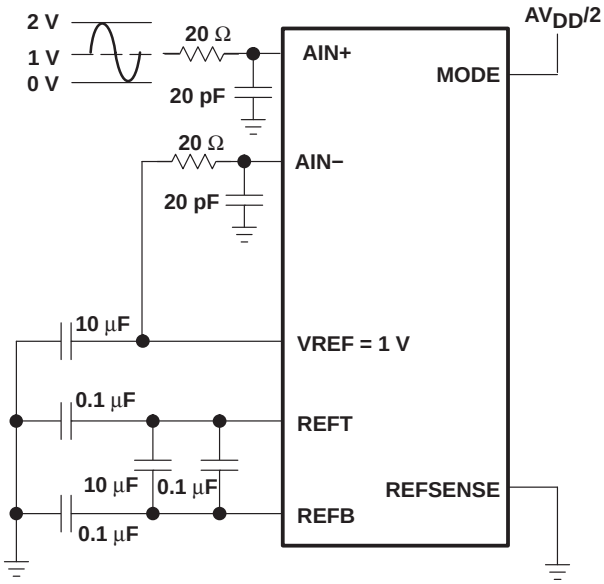


Figure 29. Operating Configuration: 2-V Single-Ended Input, Internal ADC References

PRINCIPLES OF OPERATION

operating configuration examples (continued)

Figure 30 shows a configuration using the internal ADC references for digitizing a dc-coupled differential input with 1.5-V_{p-p} span and 1.5-V common-mode voltage. External resistors are used to set the internal bandgap reference output at VREF to 0.75 V. Tying MODE to AV_{DD} then sets the REFT and REFB voltages via the internal reference generator for a 1.5-V_{p-p} ADC input range.

If a transformer is used to generate the differential ADC input from a single-ended signal, then the BIASREF pin provides a suitable bias voltage for the secondary windings center tap when MODE = AV_{DD}.

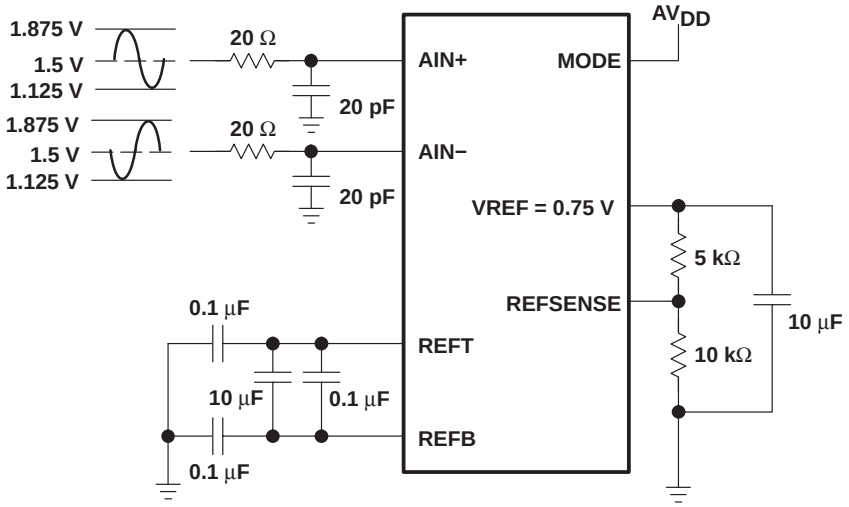


Figure 30. Operating Configuration: 1.5-V Differential Input, Internal ADC References

Figure 31 shows a configuration using the internal ADC references and an external VREF source for digitizing a dc-coupled single-ended input with span 0.5 V to 2 V. A 1.25-V external source provides the bias voltage for the AIN− pin and also, via a buffered potential divider, the 0.75 VREF voltage required to set the input range to 1.5 V_{p-p} MODE is tied to AV_{DD} to set internal ADC references configuration.

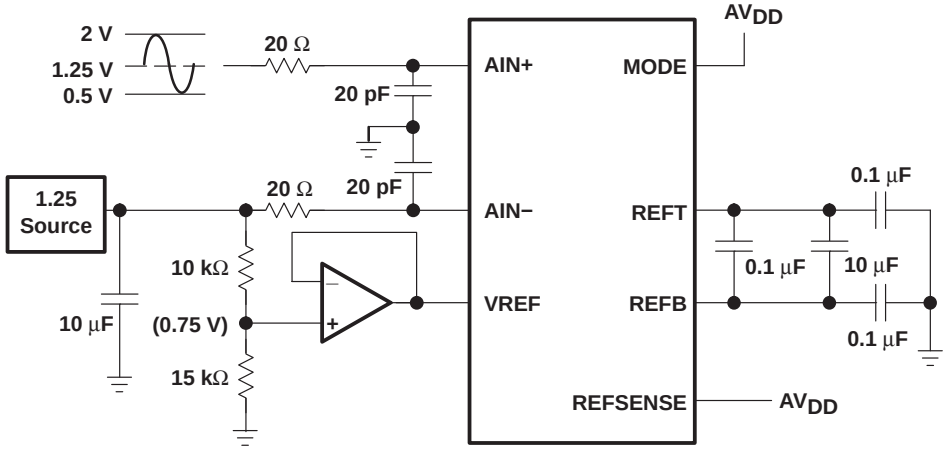


Figure 31. Operating Configuration: 1.5-V Single-Ended Input, External VREF Source

PRINCIPLES OF OPERATION

power management

In power-sensitive applications (such as battery-powered systems) where the THS1040 is not required to convert continuously, power can be saved between conversion intervals by placing the THS1040 into power-down mode. This is achieved by pulling the STBY pin high. In power-down mode, the device typically consumes less than 0.1 mW of power.

If the internal VREF generator (A1) is not required, it can be powered down by tying pin REFSENSE to AV_{DD}, saving approximately 1.2 mA of supply current.

If the BIASREF function is not required when using internal references then tying MODE to $AV_{DD}/2$ powers the BIASREF buffer down, saving approximately 1.2 mA.

digital I/O

While the $\overline{OE}$ pin is held low, ADC conversion results are output at pins D0 (LSB) to D9 (MSB). The ADC input over-range indicator is output at pin OVR. OVR is also disabled when $\overline{OE}$ is held high.

The only ADC output data format supported is unsigned binary (output codes 0 to 1023). Twos complement output (output codes −512 to 511) can be obtained by using an external inverter to invert the D9 output.

APPLICATION INFORMATION

driving the THS1040 analog inputs

driving the clock input

Obtaining good performance from the THS1040 requires care when driving the clock input.

Different sections of the sample-and-hold and ADC operate while the clock is low or high. The user should ensure that the clock duty cycle remains near 50% to ensure that all internal circuits have as much time as possible in which to operate.

The CLK pin should also be driven from a low jitter source for best dynamic performance. To maintain low jitter at the CLK input, any clock buffers external to the THS1040 should have fast rising edges. Use a fast logic family such as AC or ACT to drive the CLK pin, and consider powering any clock buffers separately from any other logic on the PCB to prevent digital supply noise appearing on the buffered clock edges as jitter.

As the CLK input threshold is nominally around $AV_{DD}/2$, any clock buffers need to have an appropriate supply voltage to drive above and below this level.

driving the sample and hold inputs

driving the AIN+ and AIN− pins

Figure 32 shows an equivalent circuit for the THS1040 AIN+ and AIN− pins. The load presented to the system at the AIN pins comprises the switched input sampling capacitor, C_{Sample}, and various stray capacitances, C_1 and C_2.

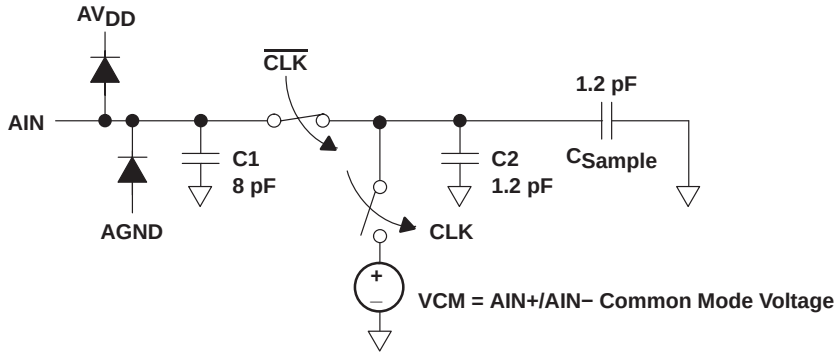


Figure 32. Equivalent Circuit for Analog Input Pins AIN+ and AIN−

The input current pulses required to charge C_{Sample} and C_2 can be time averaged and the switched capacitor circuit modelled as an equivalent resistor:

$$R_{IN2} = \frac{1}{C_S \times f_{CLK}} \quad (12)$$

where C_S is the sum of C_{Sample} and C_2. This model can be used to approximate the input loading versus source resistance for high impedance sources.

APPLICATION INFORMATION

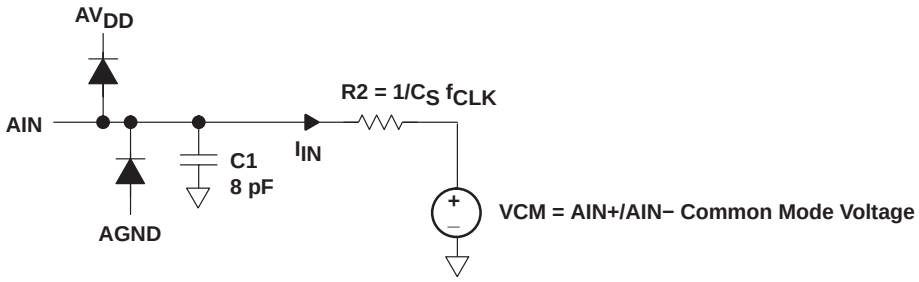


Figure 33. Equivalent Circuit for the AIN Switched Capacitor Input

AIN input damping

The charging current pulses into AIN+ and AIN− can make the signal sources jump or ring, especially if the sources are slightly inductive at high frequencies. Inserting a small series resistor of 20 Ω or less and a small capacitor to ground of 20 pF or less in the input path can damp source ringing (see Figure 34). The resistor and capacitor values can be made larger than 20 Ω and 20 pF if reduced input bandwidth and a slight gain error (due to potential division between the external resistors and the AIN equivalent resistors) are acceptable.

Note that the capacitors should be soldered to a clean analog ground with a common ground point to prevent any voltage drops in the ground plane appearing as a differential voltage at the ADC inputs.

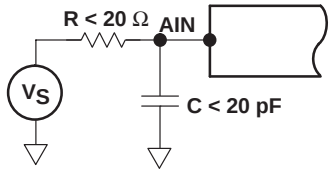


Figure 34. Damping Source Ringing Using a Small Resistor and Capacitor

driving the VREF pin

Figure 35 shows the equivalent load on the VREF pin when driving the ADC internal references buffer via this pin (MODE = AV_{DD}/2 or AV_{DD} and REFSENSE = AV_{DD}).

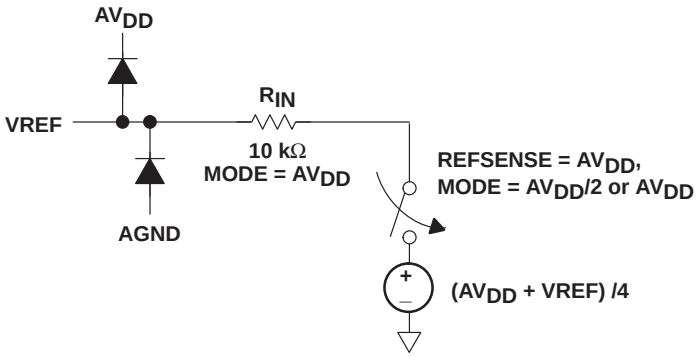


Figure 35. Equivalent Circuit of VREF

The nominal input current I_{REF} is given by:

$$I_{REF} = \frac{3\,V_{REF} - AV_{DD}}{4 \times R_{IN}} \quad (13)$$

APPLICATION INFORMATION

driving the VREF pin (continued)

Note that the maximum current may be up to 30% higher. The user should ensure that VREF is driven from a low noise, low drift source, well decoupled to analog ground and capable of driving the maximum I_{REF}.

driving REFT and REFB (external ADC references, MODE = AGND)

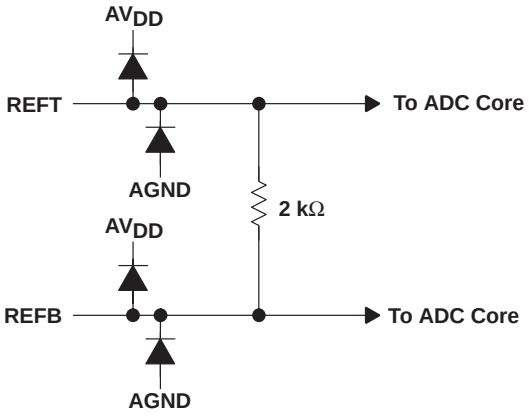


Figure 36. Equivalent Circuit of REFT and REFB Inputs

reference decoupling

VREF pin

When the on-chip reference generator is enabled, the VREF pin should be decoupled to the circuit board's analog ground plane close to the THS1040 AGND pin via a 1-µF capacitor and a 0.1-µF ceramic capacitor.

REFT and REFB pins

In any mode of operation, the REFT and REFB pins should be decoupled as shown in Figure 37. Use short board traces between the THS1040 and the capacitors to minimize parasitic inductance.

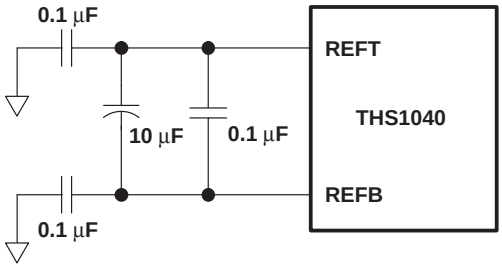


Figure 37. Recommended Decoupling for the ADC Reference Pins REFT and REFB

BIASREF pin

When using the on-chip BIASREF source, the BIASREF pin should be decoupled to the circuit board's analog ground plane close to the THS1040 AGND pin via a 1-µF capacitor and a 0.1-µF ceramic capacitor.

APPLICATION INFORMATION

supply decoupling

The analog (AV_{DD}, AGND) and digital (DV_{DD}, DGND) power supplies to the THS1040 must be separately decoupled for best performance. Each supply needs at least a 10-µF electrolytic or tantalum capacitor (as a charge reservoir) and a 100-nF ceramic type capacitor placed as close as possible to the respective pins (to suppress spikes and supply noise).

digital output loading and circuit board layout

The THS1040 outputs are capable of driving rail-to-rail with up to 10 pF of load per pin at 40-MHz clock frequency and 3-V digital supply. Minimizing the load on the outputs improves THS1040 signal-to-noise performance by reducing the switching noise coupling from the THS1040 output buffers to the internal analog circuits. The output load capacitance can be minimized by buffering the THS1040 digital outputs with a low input capacitance buffer placed as close to the output pins as physically possible, and by using the shortest possible tracks between the THS1040 and this buffer. Inserting small resistors in the range 100 Ω to 300 Ω between the THS1040 I/O outputs and their loads can help minimize the output-related noise in noise-critical applications.

Noise levels at the output buffers, which may affect the analog circuits within THS1040, increase with the digital supply voltage. Where possible, consider using the lowest DV_{DD} that the application can tolerate.

Use good layout practices when designing the application PCB to ensure that any off-chip return currents from the THS1040 digital outputs (and any other digital circuits on the PCB) do not return via the supplies to any sensitive analog circuits. The THS1040 should be soldered directly to the PCB for best performance. Socketing the device degrades performance by adding parasitic socket inductance and capacitance to all pins.

user tips for obtaining best performance from the THS1040

- Choose differential input mode for best distortion performance.
- Choose a 2-V ADC input span for best noise performance.
- Choose a 1-V ADC input span for best distortion performance.
- Drive the clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.
- Use a small RC filter (typically 20 Ω and 20 pF) between the signal source(s) the AIN+ (and AIN−) input(s) when the systems bandwidth requirements allow this.

APPLICATION INFORMATION

definitions

- Integral nonlinearity (INL)—Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.
- Differential nonlinearity (DNL)—An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level) ÷ (2^n – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.
- Zero-error—Zero-error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).
- Full-scale error—Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).
- Wake-up time—Wake-up time is from the power-down state to accurate ADC samples being taken and is specified for MODE = AGND with external reference sources applied to the device at the time of release of power-down, and an applied 40-MHz clock. Circuits that need to power up are the bandgap, bias generator, ADC, and SHA.
- Power-up time—Power-up time is from the power-down state to accurate ADC samples being taken and is specified for MODE = $AV_{DD}/2$ or AV_{DD} and an applied 40-MHz clock. Circuits that need to power up include VREF reference generation (A1), bias generator, ADC, the SHA, and the on-chip ADC reference generator (A2).
- Aperture delay—The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.
- Aperture uncertainty (Jitter)—The sample-to-sample variation in aperture delay.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS1040CDW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70		
THS1040CDWG4	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70		
THS1040CPW	OBSOLETE	TSSOP	PW	28		TBD	Call TI	Call TI	0 to 70	TH1040	
THS1040IDW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	-40 to 85	TJ1040	
THS1040IPW	OBSOLETE	TSSOP	PW	28		TBD	Call TI	Call TI	-40 to 85	TJ1040	
THS1040IPWR	OBSOLETE	TSSOP	PW	28		TBD	Call TI	Call TI	-40 to 85	TJ1040	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

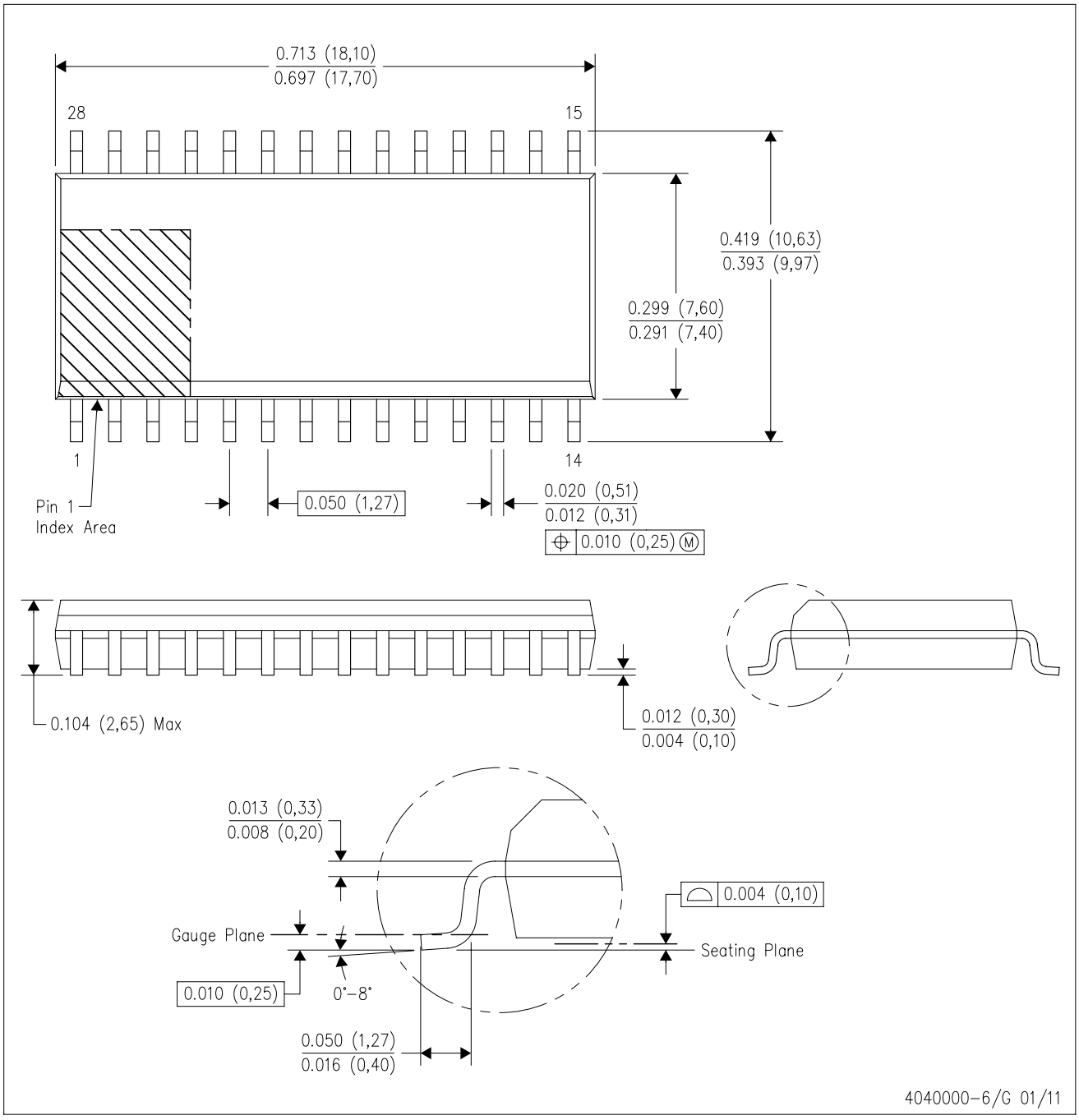
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

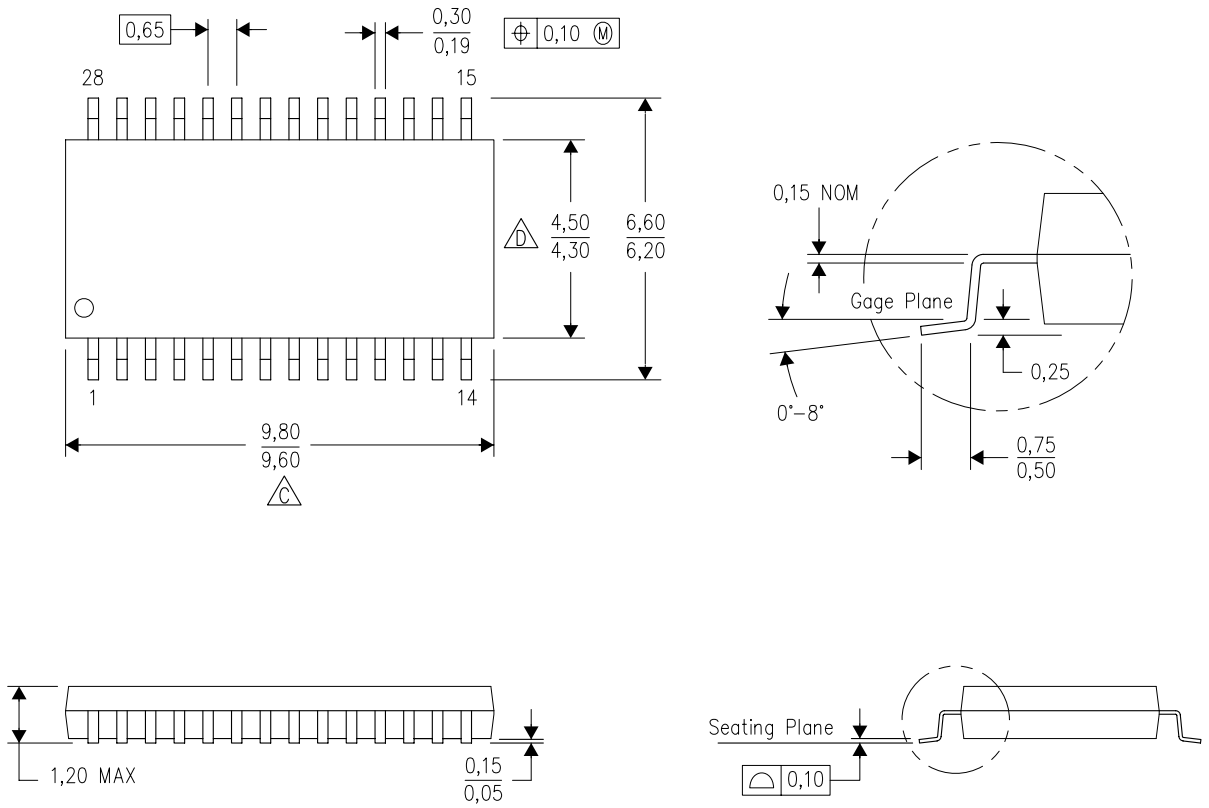
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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